

The convenience timer is a CMOS timer IC which operates with low current consumption, and is suitable for the time management of the relative time.

The S-35730 Series outputs the clock pulse.

4 types of clock pulse frequency can be selected from 1 Hz to 32.768 kHz depending on the SET0 pin and the SET1 pin settings.

**Caution** This product can be used in vehicle equipment and in-vehicle equipment. Before using the product in the purpose, contact to ABLIC Inc. is indispensable.

## ■ Features

- Clock pulse output function: Settable clock pulse frequency, with an output control pin
- Low current consumption: 0.7  $\mu$ A typ. (Quartz crystal:  $C_L = 6.0$  pF,  $V_{DD} = 3.0$  V, ENBL pin = "H",  $T_a = +25^\circ\text{C}$ , FOUT pin = Nch open-drain output)
- Wide range of operation voltage: 1.8 V to 5.5 V
- Built-in 32.768 kHz crystal oscillation circuit
- Operation temperature range:  $T_a = -40^\circ\text{C}$  to  $+125^\circ\text{C}$
- Lead-free (Sn 100%), halogen-free
- AEC-Q100 qualified\*1

\*1. Contact our sales office for details.

## ■ Applications

- Intermittent operation of various systems
- Regular status monitoring of various systems

## ■ Package

- TMSOP-8

■ Block Diagram

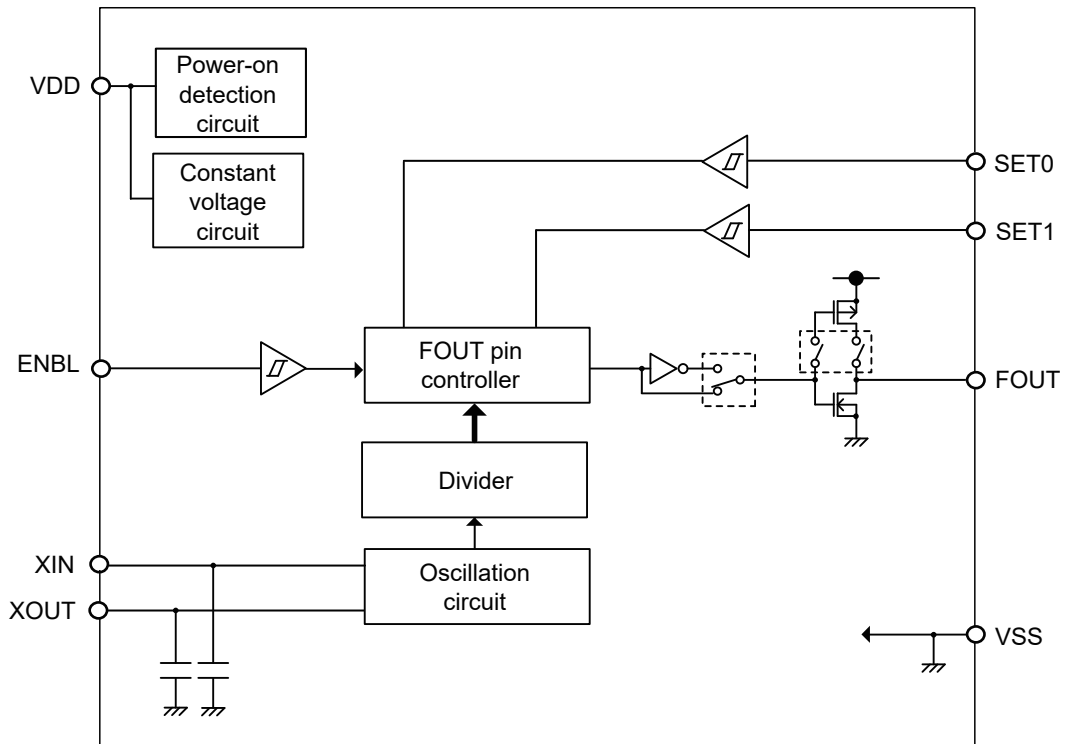


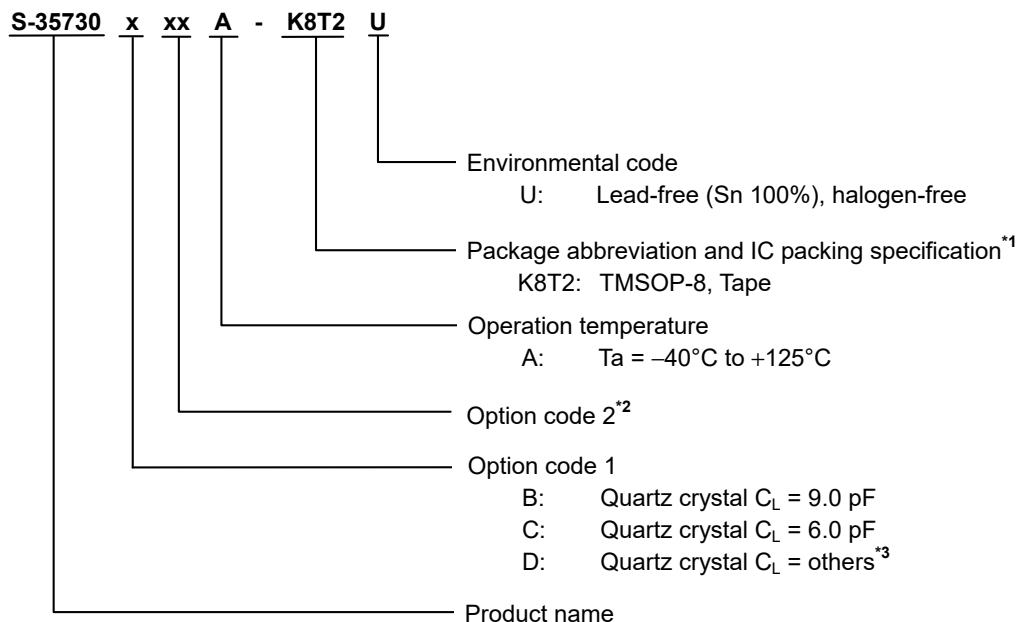
Figure 1

### ■ AEC-Q100 Qualified

This IC supports AEC-Q100 for operation temperature grade 1.  
 Contact our sales office for details of AEC-Q100 reliability specification.

### ■ Product Name Structure

#### 1. Product name



- \*1. Refer to the tape drawing.
- \*2. A sequence number added by the optional function that is user-selected.
- \*3. Contact our sales office for details.

#### 2. Package

**Table 1 Package Drawing Codes**

Package Name	Dimension	Tape	Reel
TMSOP-8	FM008-A-P-SD	FM008-A-C-SD	FM008-A-R-SD

#### 3. Product name list

**Table 2**

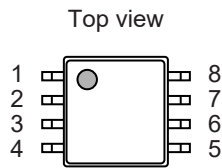
Product Name	FOUT Pin Output Form <sup>*1</sup>	SET0 Pin, SET1 Pin Settings <sup>*2</sup> (SET0, SET1)			
		0, 0	0, 1	1, 0	1, 1
S-35730C01A-K8T2U	CMOS output	32.768 kHz	32 Hz	1.024 kHz	1 Hz

- \*1. The pin of Nch open-drain output / CMOS output is selectable. Refer to "■ Pin Functions".
- \*2. Regarding the pin settings and clock pulse frequency combinations, refer to "■ FOUT Pin Clock Pulse Output".

**Remark** Please contact our sales office for products with specifications other than the above.

■ **Pin Configuration**

1. **TMSOP-8**



**Figure 2**

**Table 3 List of Pins**

Pin No.	Symbol	Description	I/O	Configuration
1	ENBL	Input pin for clock pulse output control	Input	CMOS input
2	XOUT	Connection pins for quartz crystal	-	-
3	XIN			
4	VSS	GND pin	-	-
5	FOUT	Output pin for clock pulse	Output	Nch open-drain output / CMOS output is selectable
6	SET0	Input pins for clock pulse frequency setting	Input	CMOS input
7	SET1			
8	VDD	Pin for positive power supply	-	-

## ■ Pin Functions

### 1. SET0, SET1 (Input for clock pulse frequency setting) pins

These pins input the clock pulse frequency setting signals.

4 types of clock pulse frequency can be selected depending on the pin settings. Regarding the combination, refer to "1. Options of clock pulse frequency" in "■ FOUT Pin Clock Pulse Output".

### 2. ENBL (Input for clock pulse output control) pin

This pin controls the clock pulse output from the FOUT pin. The clock pulse is output from the FOUT pin when the ENBL pin is "H". The FOUT pin is fixed when the ENBL pin is "L".

### 3. FOUT (Output for clock pulse) pin

This pin outputs the clock pulse. Regarding the operation of the clock pulse output, refer to "2. ENBL pin and clock pulse output of FOUT pin" in "■ FOUT Pin Clock Pulse Output".

Also, the FOUT pin output form of Nch open-drain output / CMOS output can be selected.

### 4. XIN, XOUT (Connection for quartz crystal) pins

Connect a quartz crystal between the XIN pin and the XOUT pin.

### 5. VDD (Positive power supply) pin

Connect this pin with a positive power supply. Regarding the values of voltage to be applied, refer to "■ Recommended Operation Conditions".

### 6. VSS pin

Connect this pin to GND.

■ Equivalent Circuits of Pins

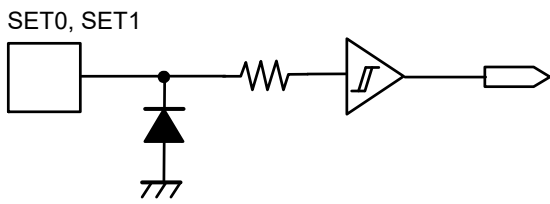


Figure 3 SET0 Pin, SET1 Pin

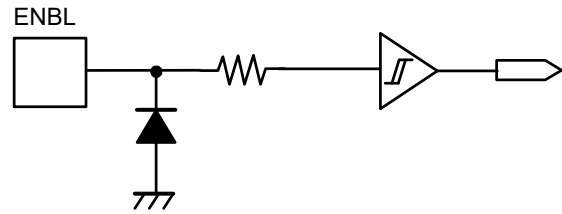


Figure 4 ENBL Pin

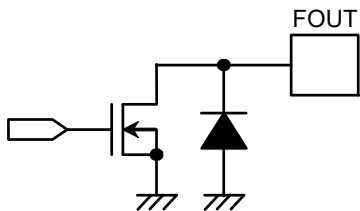


Figure 5 FOUT Pin (Nch Open-drain Output)

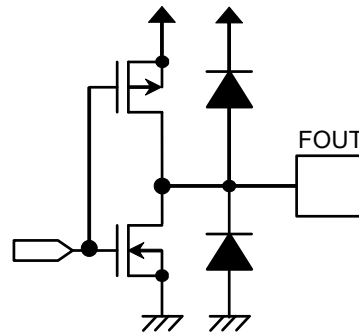


Figure 6 FOUT Pin (CMOS Output)

## ■ Absolute Maximum Ratings

Table 4

Item	Symbol	Applied Pin	Absolute Maximum Rating	Unit
Power supply voltage	V <sub>DD</sub>	–	V <sub>SS</sub> – 0.3 to V <sub>SS</sub> + 6.5	V
Input voltage	V <sub>IN</sub>	SET0, SET1, ENBL	V <sub>SS</sub> – 0.3 to V <sub>SS</sub> + 6.5	V
Output voltage	V <sub>OUT</sub>	FOUT*1	V <sub>SS</sub> – 0.3 to V <sub>SS</sub> + 6.5	V
		FOUT*2	V <sub>SS</sub> – 0.3 to V <sub>DD</sub> + 0.3 ≤ V <sub>SS</sub> + 6.5	V
Operation ambient temperature*3	T <sub>opr</sub>	–	–40 to +125	°C
Storage temperature	T <sub>stg</sub>	–	–55 to +150	°C

\*1. When an Nch open-drain output product is selected.

\*2. When a CMOS output product is selected.

\*3. Conditions with no condensation or frost. Condensation or frost causes short-circuiting between pins, resulting in a malfunction.

**Caution** The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

## ■ Recommended Operation Conditions

Table 5

(V<sub>SS</sub> = 0 V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Operation power supply voltage	V <sub>DD</sub>	Ta = –40°C to +125°C	1.8	–	5.5	V

## ■ Oscillation Characteristics

Table 6

(Ta = +25°C, V<sub>DD</sub> = 3.0 V, V<sub>SS</sub> = 0 V unless otherwise specified)

(Quartz crystal (NX3215SD, C<sub>L</sub> = 6.0 pF) manufactured by Nihon Dempa Kogyo Co., Ltd.)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	V <sub>STA</sub>	Within 10 seconds	1.8	–	5.5	V
Oscillation start time	t <sub>STA</sub>	–	–	–	1	s
IC-to-IC frequency deviation*1	δIC	–	–20	–	+20	ppm

\*1. Reference value

■ DC Electrical Characteristics

**Table 7**

(Ta = -40°C to +125°C, V<sub>SS</sub> = 0 V unless otherwise specified)  
 (Quartz crystal (NX3215SD, C<sub>L</sub> = 6.0 pF) manufactured by Nihon Dempa Kogyo Co., Ltd.)

Item	Symbol	Applied Pin	Condition	Min.	Typ.	Max.	Unit
Current consumption 1	I <sub>DD1</sub>	-	V <sub>DD</sub> = 3.0 V, Ta = -40°C to +85°C, ENBL pin = V <sub>SS</sub> , FOUT pin = no load	-	1.7	3.0	μA
			V <sub>DD</sub> = 3.0 V, Ta = +125°C, ENBL pin = V <sub>SS</sub> , FOUT pin = no load	-	2.7	4.5	μA
Current consumption 2	I <sub>DD2</sub>	-	V <sub>DD</sub> = 3.0 V, Ta = -40°C to +85°C, ENBL pin = V <sub>DD</sub> , FOUT pin output = 32.768 kHz, FOUT pin = no load*1	-	0.7	0.85	μA
			V <sub>DD</sub> = 3.0 V, Ta = +125°C, ENBL pin = V <sub>DD</sub> , FOUT pin output = 32.768 kHz, FOUT pin = no load*1	-	1.2	1.9	μA
			V <sub>DD</sub> = 3.0 V, Ta = -40°C to +85°C, ENBL pin = V <sub>DD</sub> , FOUT pin output = 32.768 kHz, FOUT pin = no load*2	-	4.0	6.0	μA
			V <sub>DD</sub> = 3.0 V, Ta = +125°C, ENBL pin = V <sub>DD</sub> , FOUT pin output = 32.768 kHz, FOUT pin = no load*2	-	4.5	7.0	μA
High level input leakage current	I <sub>IzH</sub>	SET0, SET1, ENBL	V <sub>IN</sub> = V <sub>DD</sub>	-0.5	-	0.5	μA
Low level input leakage current	I <sub>IzL</sub>	SET0, SET1, ENBL	V <sub>IN</sub> = V <sub>SS</sub>	-0.5	-	0.5	μA
High level output leakage current	I <sub>ozH</sub>	FOUT*2	V <sub>OUT</sub> = V <sub>DD</sub>	-0.5	-	0.5	μA
Low level output leakage current	I <sub>ozL</sub>	FOUT*2	V <sub>OUT</sub> = V <sub>SS</sub>	-0.5	-	0.5	μA
High level input voltage	V <sub>IH</sub>	SET0, SET1, ENBL	-	0.7 × V <sub>DD</sub>	-	V <sub>SS</sub> + 5.5	V
Low level input voltage	V <sub>IL</sub>	SET0, SET1, ENBL	-	V <sub>SS</sub> - 0.3	-	0.3 × V <sub>DD</sub>	V
High level output voltage*2	V <sub>OH</sub>	FOUT	I <sub>OH</sub> = -0.4 mA	0.8 × V <sub>DD</sub>	-	-	V
Low level output voltage	V <sub>OL</sub>	FOUT	I <sub>OL</sub> = 2.0 mA	-	-	0.4	V

\*1. When an Nch open-drain output product is selected.

\*2. When a CMOS output product is selected.

## ■ FOUT Pin Clock Pulse Output

### 1. Options of clock pulse frequency

4 types of FOUT pin clock pulse output can be selected as the option from the frequency of 1 Hz to 32.768 kHz. **Table 8** shows the pin settings and the list of options for the FOUT pin clock pulse frequency.

**Table 8 List of Options**

Pin Setting		Clock Pulse Frequency 1	Clock Pulse Frequency 2	Clock Pulse Frequency 3	Clock Pulse Frequency 4
SET0	SET1				
L	L	32.768 kHz	16.384 kHz	8.192 kHz	4.096 kHz
L	H	128 Hz	64 Hz	32 Hz	16 Hz
H	L	2.048 kHz	1.024 kHz	512 Hz	256 Hz
H	H	8 Hz	4 Hz	2 Hz	1 Hz

For example, when the pin setting is SET0 pin = "L" and SET1 pin = "L", 1 clock pulse frequency can be selected from "32.768 kHz", "16.384 kHz", "8.192 kHz" and "4.096 kHz". The others cannot be selected.

**Table 9** shows the example of the clock pulse frequency combination.

**Table 9 Example of Options**

Pin Setting		Clock Pulse Frequency
SET0	SET1	
L	L	32.768 kHz
L	H	32 Hz
H	L	1.024 kHz
H	H	1 Hz

### 2. ENBL pin and clock pulse output of FOUT pin

The FOUT pin outputs the clock pulse when the ENBL pin is "H". The FOUT pin is fixed to Nch open-drain output = "H" or CMOS output = "L" when the ENBL pin is "L". Since the input signal of the ENBL pin is not synchronized with the clock pulse output from the FOUT pin, the duty ratio may change when the "H" and "L" of the ENBL pin changes.

The example of the FOUT pin output timing is shown below.



**Figure 7 Example FOUT Pin Output Timing (Nch Open-drain Output)**



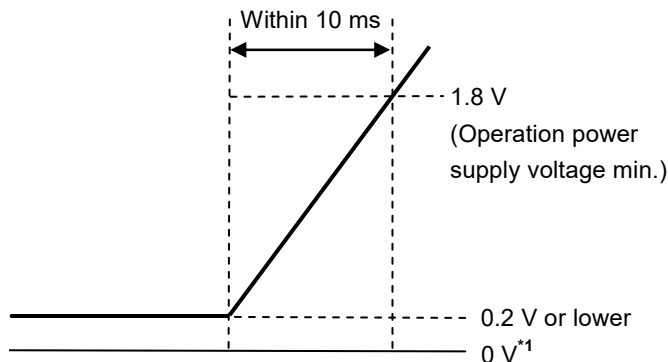
**Figure 8 Example of FOUT Pin Output Timing (CMOS Output)**

The SET0 pin and the SET1 pin input signals are not synchronized with the clock pulse output from the FOUT pin as well. Therefore, duty ratio may change if the SET0 pin and the SET1 pin settings are changed when the ENBL pin is "H".

Moreover, since the crystal oscillation circuit is unstable immediately after power-on, regardless of the status of the ENBL pin, the FOUT pin is fixed to Nch open-drain output = "H" or CMOS output = "L" for about 0.5 seconds after power-on.

### ■ Power-on Detection Circuit

In order for the power-on detection circuit to operate normally, raise the power supply voltage of the IC from 0.2 V or lower to that it reaches 1.8 V of the operation power supply voltage minimum value within 10 ms, as shown in **Figure 9**.



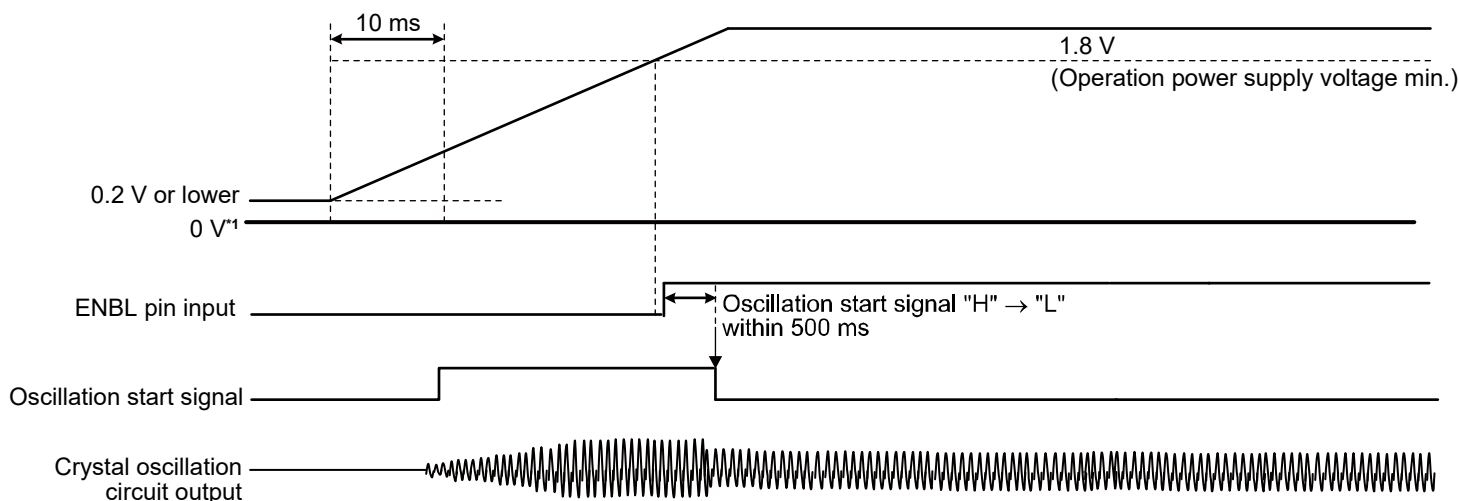
\*1. 0 V means that there is no potential difference between the VDD pin and the VSS pin of the S-35730 Series.

**Figure 9 How to Raise Power Supply Voltage**

If the power supply voltage of the S-35730 Series cannot be raised under the above conditions, the power-on detection circuit may not operate normally and an oscillation may not start. In such case, perform the operations shown in "1. When power supply voltage is raised at ENBL pin = "L" " and "2. When power supply voltage is raised at ENBL pin = "H" ".

#### 1. When power supply voltage is raised at ENBL pin = "L"

Set the ENBL pin to "L" until the power supply voltage reaches 1.8 V or higher. While the ENBL pin is set to "L", the oscillation start signal becomes "H", and the crystal oscillation circuit normally oscillates. If the ENBL pin is set to "H" after the power supply voltage reaches 1.8 V, the oscillation start signal becomes "L" within 500 ms, and the oscillation status is maintained.

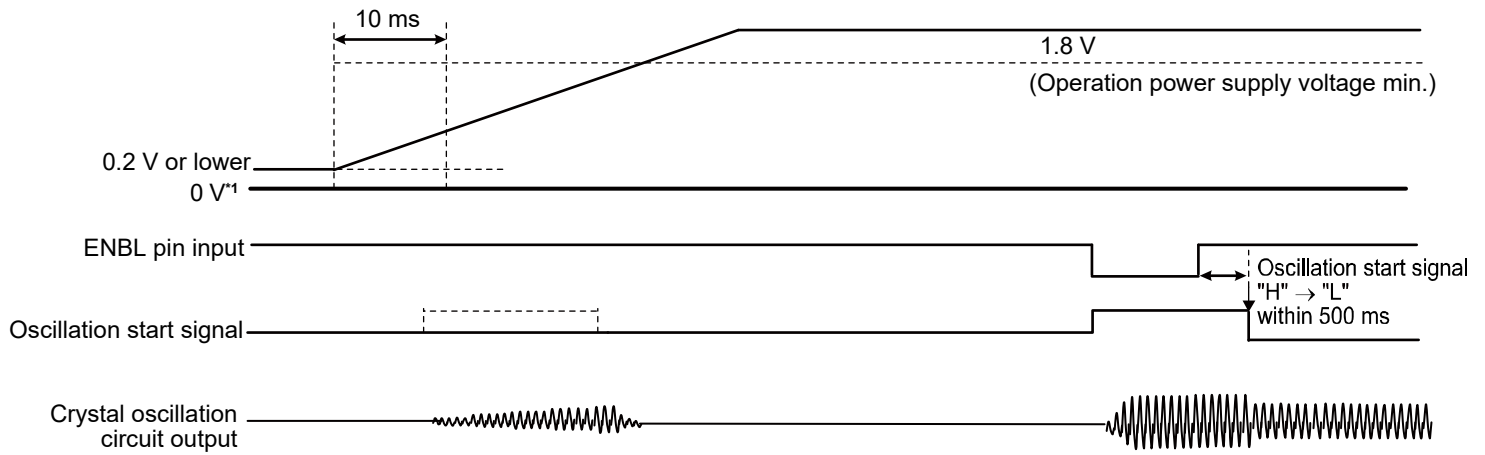


\*1. 0 V means that there is no potential difference between the VDD pin and the VSS pin of the S-35730 Series.

**Figure 10 When Power Supply Voltage is Raised at ENBL Pin = "L"**

**2. When power supply voltage is raised at ENBL pin = "H"**

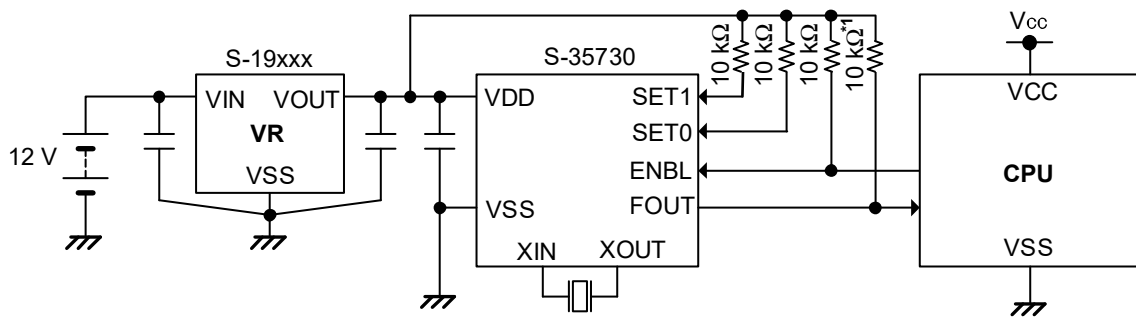
Set the ENBL pin to "L" after the power supply voltage reaches 1.8 V or higher. If the ENBL pin is set to "L" for 500 ms or longer, the oscillation start signal becomes "H", and the crystal oscillation circuit normally oscillates. After that, if the ENBL pin is set to "H", the oscillation start signal becomes "L" within 500 ms, and the oscillation status is maintained.



\*1. 0 V means that there is no potential difference between the VDD pin and the VSS pin of the S-35730 Series.

**Figure 11 When Power Supply Voltage is Raised at ENBL Pin = "H"**

■ Example of Application Circuit



\*1. This resistor is unnecessary when a CMOS output product is selected.

Figure 12

**Caution** The above connection diagram does not guarantee operation. Set the constants after performing sufficient evaluation using the actual application

### ■ Configuration of Crystal Oscillation Circuit

Since the S-35730 Series has built-in capacitors ( $C_g$  and  $C_d$ ), adjustment of oscillation frequency is unnecessary. However, the crystal oscillation circuit is sensitive to external noise and parasitic capacitance ( $C_P$ ), these effects may become a factor to worsen the clock accuracy. Therefore, the following steps are recommended for optimizing the configuration of the crystal oscillation circuit.

- Locate the bypass capacitor adjacent to the power supply pin of the S-35730 Series.
- Place the S-35730 Series and the quartz crystal as close to each other as possible, and shorten the wiring.
- Increase the insulation resistance between pins and the board wiring patterns of XIN and XOUT.
- Do not place any signal or power lines close to the crystal oscillation circuit.
- Locate the GND layer immediately below the crystal oscillation circuit.  
 (In the case of a multi-layer board, only the layer farthest from the oscillation circuit should be located as the GND layer. Do not locate a circuit pattern on the intermediate layers.)

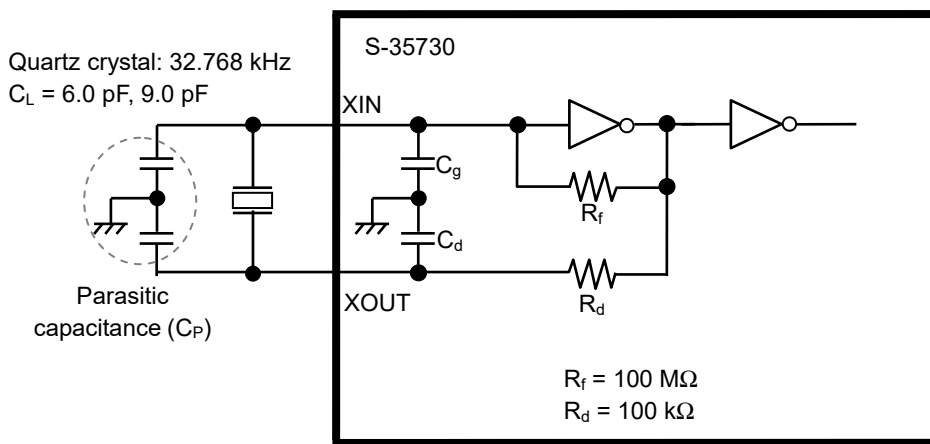


Figure 13 Configuration of Crystal Oscillation Circuit

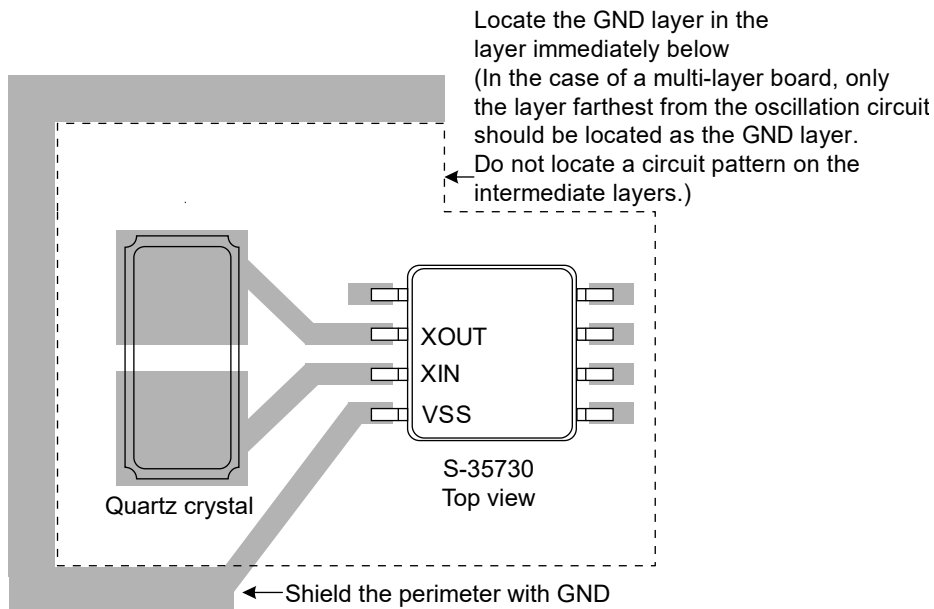


Figure 14 Example of Recommended Connection Pattern Diagram

- Caution**
1. Oscillation characteristics are subject to the variation of each component such as board parasitic capacitance, parasitic resistance, quartz crystal and external capacitor. When configuring the crystal oscillation circuit, pay sufficient attention for them.
  2. When using the product in automobile equipment, select the components which can be automobile carried for each component such as quartz crystal, external capacitor and board.

■ **Cautions When Using Quartz Crystal**

Request a matching evaluation between the IC and a quartz crystal to the quartz crystal maker.  
 Refer to **Table 10** for recommended quartz crystal characteristics values. When using the product in an environment over Ta = +85°C, it is recommended to ensure the oscillation allowance shown in **Table 10** at room temperature.

**Table 10 Quartz Crystal Characteristics**

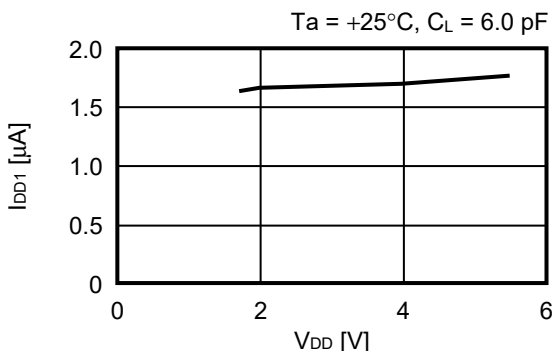
Quartz Crystal C <sub>L</sub> Value (Load Capacitance)	R <sub>1</sub> Value (Equivalent Series Resistance)	Oscillation Allowance at Power-on
9.0 pF	80 kΩ max.	5 times or more
6.0 pF	80 kΩ max.	5 times or more

■ **Precautions**

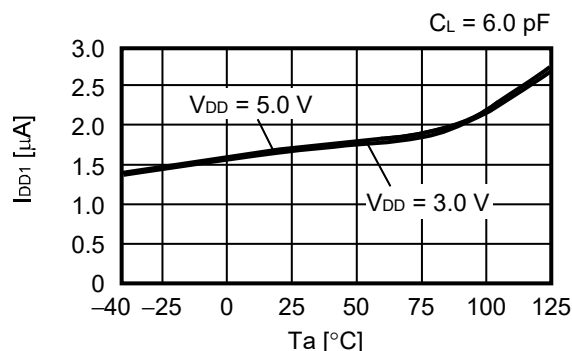
- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.
- ABLIC Inc. claims no responsibility for any disputes arising out of or in connection with any infringement by products including this IC of patents owned by a third party.

**Characteristics (Typical Data)**

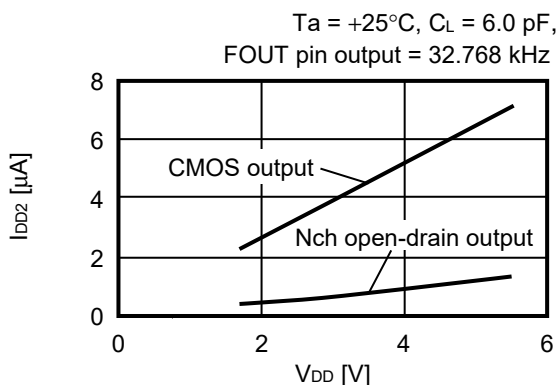
1. Current consumption 1 vs. Power supply voltage characteristics



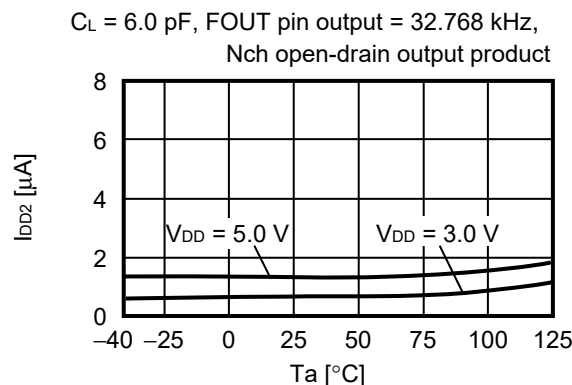
2. Current consumption 1 vs. Temperature characteristics



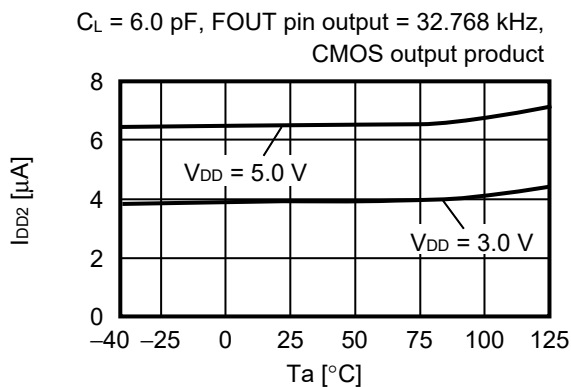
3. Current consumption 2 vs. Power supply voltage characteristics



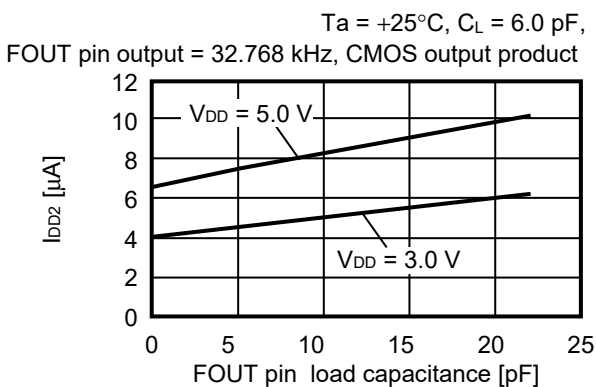
4. Current consumption 2 vs. Temperature characteristics



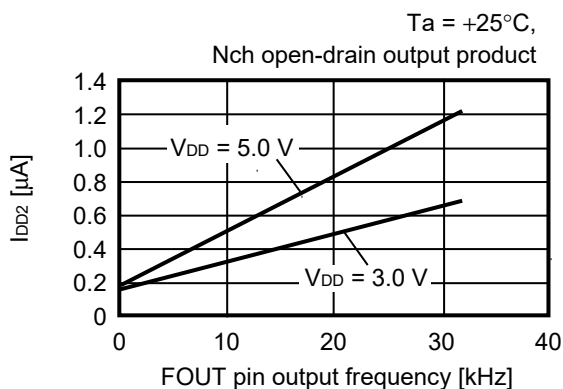
5. Current consumption 2 vs. Temperature characteristics



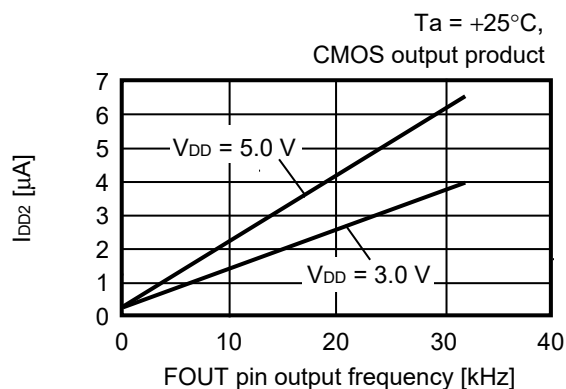
6. Current consumption 2 vs. FOUT pin load capacitance characteristics



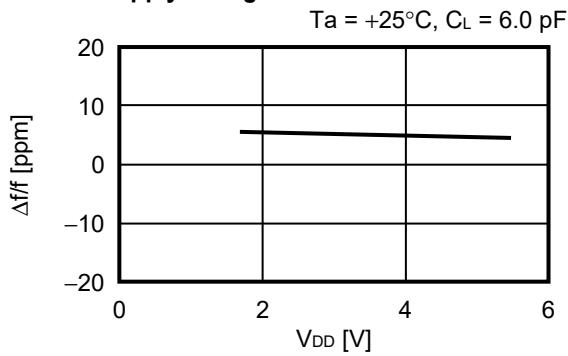
7. Current consumption 2 vs. FOUT pin output frequency characteristics



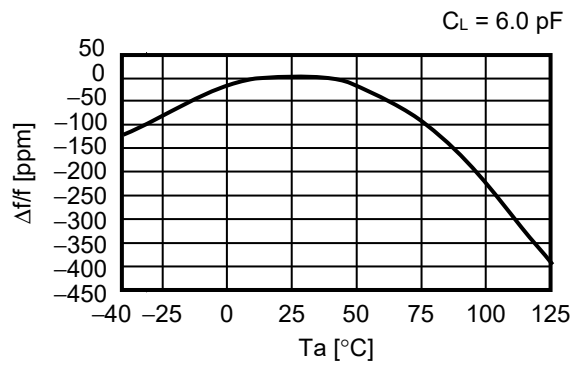
8. Current consumption 2 vs. FOUT pin output frequency characteristics



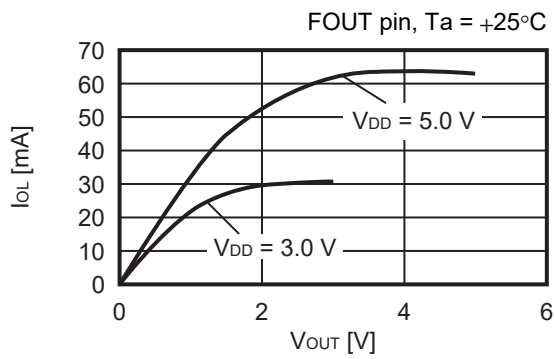
**9. Oscillation frequency vs. Power supply voltage characteristics**



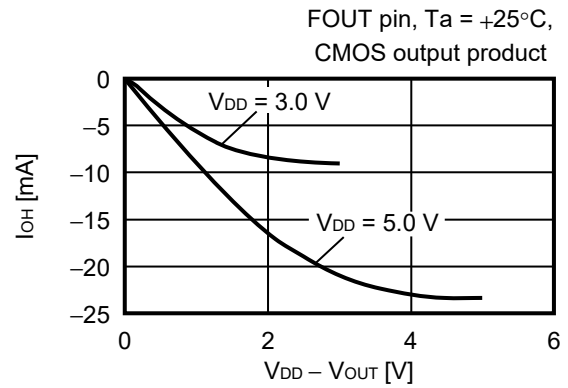
**10. Oscillation frequency vs. Temperature characteristics**

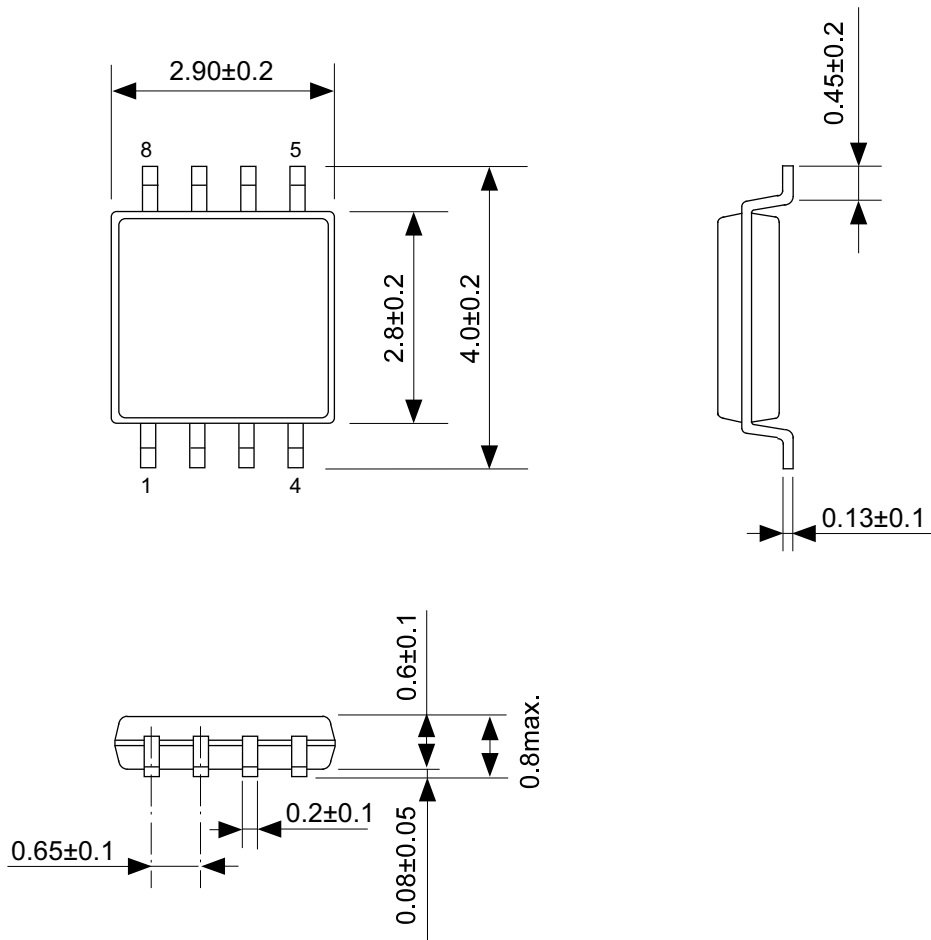


**11. Low level output current vs. Output voltage characteristics**



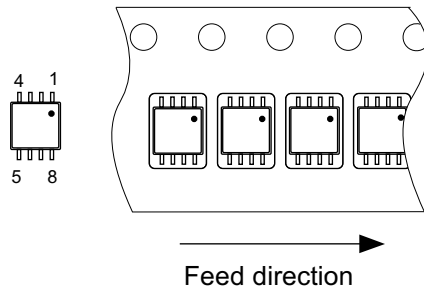
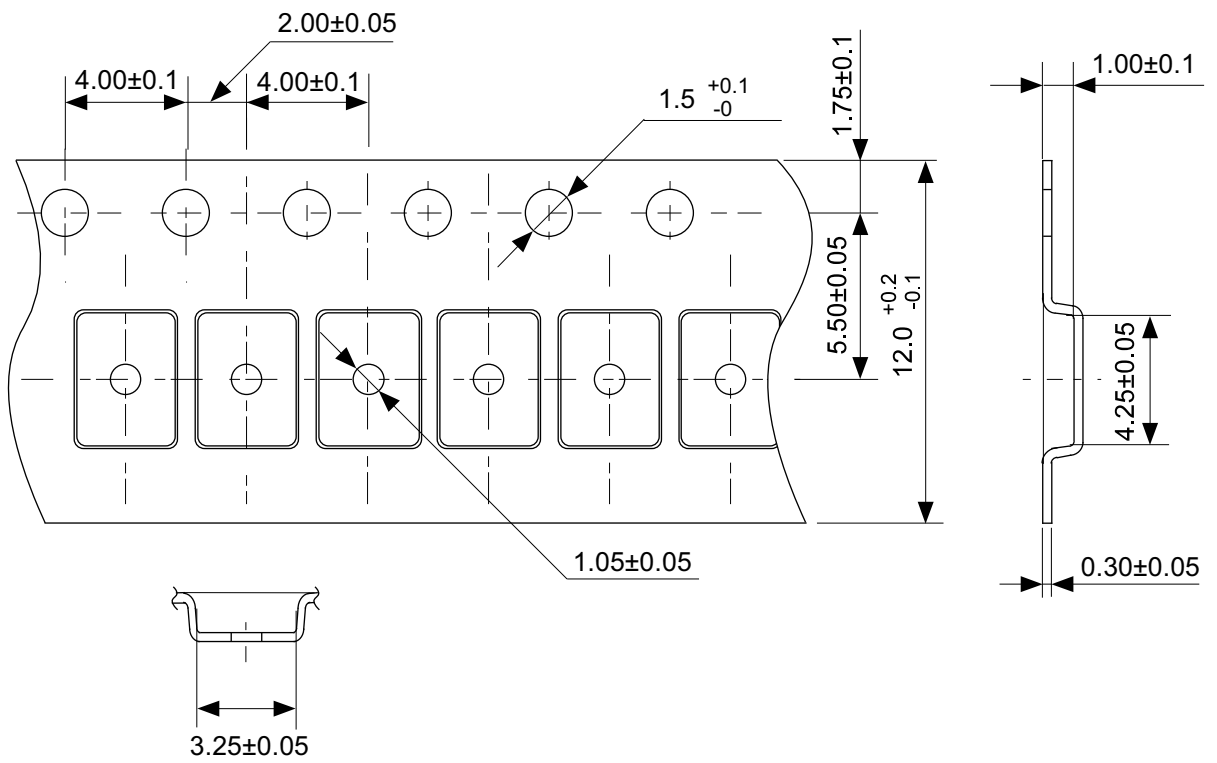
**12. High level output current vs. V<sub>DD</sub> - V<sub>OUT</sub> characteristics**





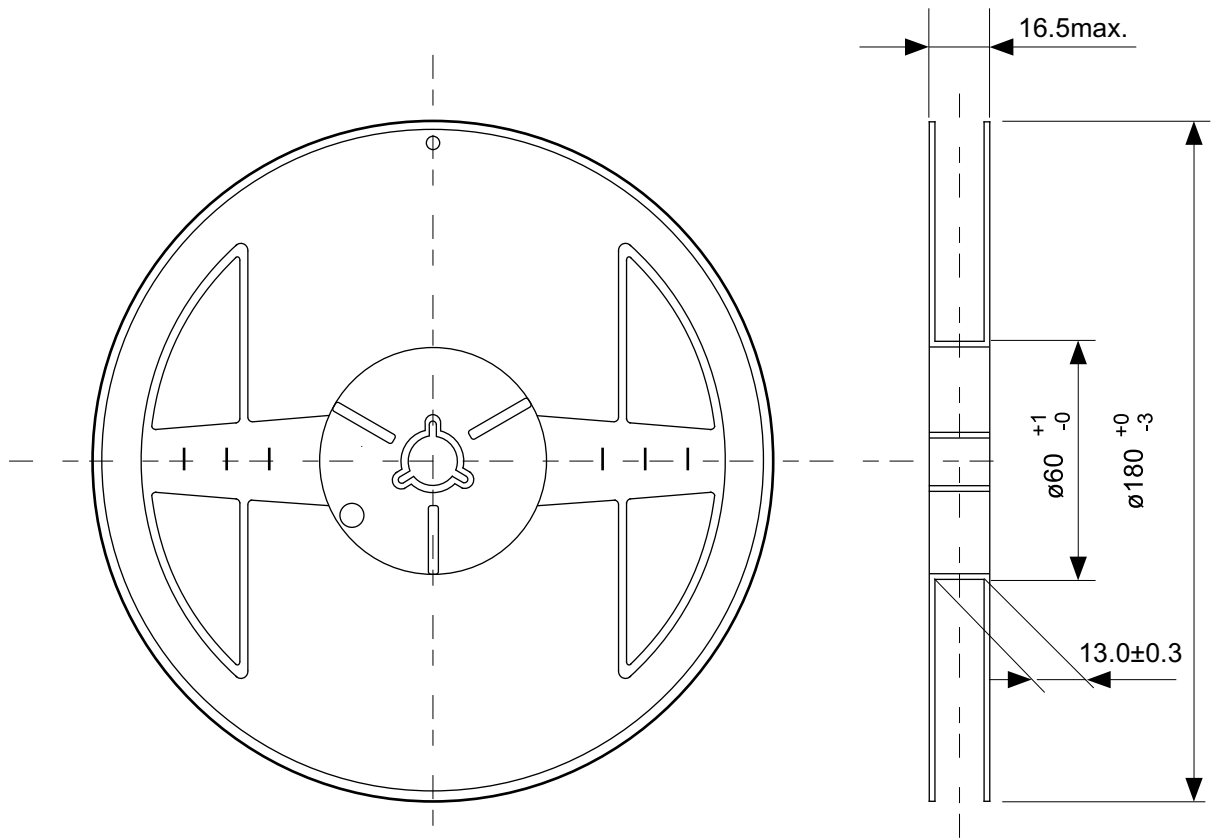
No. FM008-A-P-SD-1.2

TITLE	TMSOP8-A-PKG Dimensions
No.	FM008-A-P-SD-1.2
ANGLE	
UNIT	mm
<b>ABLIC Inc.</b>	

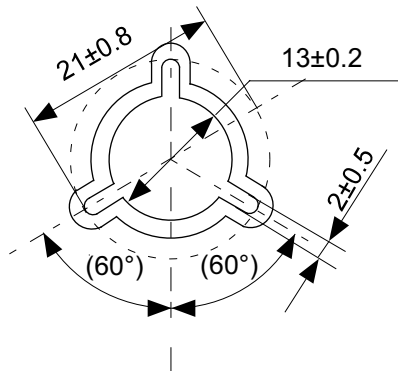


No. FM008-A-C-SD-2.0

TITLE	TMSOP8-A-Carrier Tape
No.	FM008-A-C-SD-2.0
ANGLE	
UNIT	mm
<b>ABLIC Inc.</b>	



Enlarged drawing in the central part



No. FM008-A-R-SD-1.0

TITLE	TMSOP8-A-Reel		
No.	FM008-A-R-SD-1.0		
ANGLE		QTY.	4,000
UNIT	mm		
<b>ABLIC Inc.</b>			

## Disclaimers (Handling Precautions)

1. All the information described herein (product data, specifications, figures, tables, programs, algorithms and application circuit examples, etc.) is current as of publishing date of this document and is subject to change without notice.
2. The circuit examples and the usages described herein are for reference only, and do not guarantee the success of any specific mass-production design.  
ABLIC Inc. is not liable for any losses, damages, claims or demands caused by the reasons other than the products described herein (hereinafter "the products") or infringement of third-party intellectual property right and any other right due to the use of the information described herein.
3. ABLIC Inc. is not liable for any losses, damages, claims or demands caused by the incorrect information described herein.
4. Be careful to use the products within their ranges described herein. Pay special attention for use to the absolute maximum ratings, operation voltage range and electrical characteristics, etc.  
ABLIC Inc. is not liable for any losses, damages, claims or demands caused by failures and / or accidents, etc. due to the use of the products outside their specified ranges.
5. Before using the products, confirm their applications, and the laws and regulations of the region or country where they are used and verify suitability, safety and other factors for the intended use.
6. When exporting the products, comply with the Foreign Exchange and Foreign Trade Act and all other export-related laws, and follow the required procedures.
7. The products are strictly prohibited from using, providing or exporting for the purposes of the development of weapons of mass destruction or military use. ABLIC Inc. is not liable for any losses, damages, claims or demands caused by any provision or export to the person or entity who intends to develop, manufacture, use or store nuclear, biological or chemical weapons or missiles, or use any other military purposes.
8. The products are not designed to be used as part of any device or equipment that may affect the human body, human life, or assets (such as medical equipment, disaster prevention systems, security systems, combustion control systems, infrastructure control systems, vehicle equipment, traffic systems, in-vehicle equipment, aviation equipment, aerospace equipment, and nuclear-related equipment), excluding when specified for in-vehicle use or other uses by ABLIC, Inc. Do not apply the products to the above listed devices and equipments.  
ABLIC Inc. is not liable for any losses, damages, claims or demands caused by unauthorized or unspecified use of the products.
9. In general, semiconductor products may fail or malfunction with some probability. The user of the products should therefore take responsibility to give thorough consideration to safety design including redundancy, fire spread prevention measures, and malfunction prevention to prevent accidents causing injury or death, fires and social damage, etc. that may ensue from the products' failure or malfunction.  
The entire system in which the products are used must be sufficiently evaluated and judged whether the products are allowed to apply for the system on customer's own responsibility.
10. The products are not designed to be radiation-proof. The necessary radiation measures should be taken in the product design by the customer depending on the intended use.
11. The products do not affect human health under normal use. However, they contain chemical substances and heavy metals and should therefore not be put in the mouth. The fracture surfaces of wafers and chips may be sharp. Be careful when handling these with the bare hands to prevent injuries, etc.
12. When disposing of the products, comply with the laws and ordinances of the country or region where they are used.
13. The information described herein contains copyright information and know-how of ABLIC Inc. The information described herein does not convey any license under any intellectual property rights or any other rights belonging to ABLIC Inc. or a third party. Reproduction or copying of the information from this document or any part of this document described herein for the purpose of disclosing it to a third-party is strictly prohibited without the express permission of ABLIC Inc.
14. For more details on the information described herein or any other questions, please contact ABLIC Inc.'s sales representative.
15. This Disclaimers have been delivered in a text using the Japanese language, which text, despite any translations into the English language and the Chinese language, shall be controlling.

2.4-2019.07