E3M0060065D

Silicon Carbide Power MOSFET
E-Series Automotive
N-Channel Enhancement Mode

Features

- 3rd generation SiC MOSFET technology
- High blocking voltage with low on-resistance
- High-speed switching with low capacitances
- Fast intrinsic diode with low reverse recovery (Q_{rr})
- Halogen free, RoHS compliant
- Automotive Qualified (AEC-Q101) and PPAP Capable

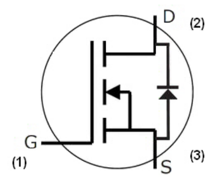
Benefits

- Higher system efficiency
- Reduce cooling requirements
- Increase power density
- Increase system switching frequency

Applications

- EV Battery Chargers
- High Voltage DC/DC Converters

Package



Part Number	Package	Marking
E3M0060065D	TO-247-3L	E3M0060065D

Maximum Ratings (T_C = 25 ˚C unless otherwise specified)

Symbol	Parameter		Value	Unit	Note
V_{DSmax}	Drain - Source Voltage		650	V	
V_{GSmax}	Gate - Source Voltage		-8/+19	V	Note: 1
I_D	Continuous Drain Current, V_{GS} = 15 V	T_C = 25˚C	37	A	Fig. 19 Note: 2
		T_C = 100˚C	26		
$I_{D(pulse)}$	Pulsed Drain Current, Pulse width t_P limited by T_{jmax}		99	A	Fig. 22
P_D	Power Dissipation, T_C=25˚C, T_J = 175 ˚C		131	W	Fig. 20 Note: 2
T_J , T_{stg}	Operating Junction and Storage Temperature		-40 to +175	˚C	
T_L	Solder Temperature, 1.6mm (0.063”) from case for 10s		260	˚C	
M_d	Mounting Torque , M3 or 6-32 screw		1 8.8	Nm lbf-in	

Note (1): Recommended turn off / turn on gate voltage V_{GS} - 4V...0V / +15V
Note (2): Verified by design

Electrical Characteristics (T_C = 25˚C unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions	Note
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	650			V	V_{GS} = 0 V, I_D = 100 μA	
$V_{GS(th)}$	Gate Threshold Voltage	1.8	2.8	3.6	V	V_{DS} = V_{GS}, I_D = 3.6 mA	Fig. 11
			2.2		V	V_{DS} = V_{GS}, I_D = 3.6 mA, T_J = 175ºC	
I_{DSS}	Zero Gate Voltage Drain Current		1	50	μA	V_{DS} = 650 V, V_{GS} = 0 V	
I_{GSS}	Gate-Source Leakage Current		10	250	nA	V_{GS} = 15 V, V_{DS} = 0 V	
$R_{DS(on)}$	Drain-Source On-State Resistance		60	79	mΩ	V_{GS} = 15 V, I_D = 13.2 A	Fig. 4, 5, 6
			83			V_{GS} = 15 V, I_D = 13.2 A, T_J = 175ºC	
g_{fs}	Transconductance		9		S	V_{DS}= 20 V, I_{DS}= 13.2 A	Fig. 7
			9			V_{DS}= 20 V, I_{DS}= 13.2 A, T_J = 175ºC	
C_{iss}	Input Capacitance		1170		pF	V_{GS} = 0 V, V_{DS} = 0V to 600 V F = 1 Mhz V_{AC} = 25 mV	Fig. 17, 18
C_{oss}	Output Capacitance		72				
C_{rss}	Reverse Transfer Capacitance		6				
E_{oss}	C_{oss} Stored Energy		14		μJ		Fig. 16
$C_{o(er)}$	Effective Output Capacitance (Energy Related)		85		pF	V_{GS} = 0 V, V_{DS} = 0... 400V	Note: 3
$C_{o(tr)}$	Effective Output Capacitance (Time Related)		122		pF		
E_{ON}	Turn-On Switching Energy (External Diode)		126		μJ	V_{DS} = 400 V, V_{GS} = -4 V/15 V, I_D = 13.2A, $R_{G(ext)}$ = 2.5 Ω, L= 135 μH, T_J = 175ºC FWD = External SiC DIODE	Fig. 26
E_{OFF}	Turn Off Switching Energy (External Diode)		25				
E_{ON}	Turn-On Switching Energy (Body Diode FWD)		169		μJ	V_{DS} = 400 V, V_{GS} = -4 V/15 V, I_D = 13.2A, $R_{G(ext)}$ = 2.5 Ω, L= 135 μH, T_J = 175ºC FWD = Internal Body Diode	Fig. 26
E_{OFF}	Turn-Off Switching Energy (Body Diode FWD)		23				
$t_{d(on)}$	Turn-On Delay Time		10		ns	V_{DD} = 400 V, V_{GS} = -4 V/15 V I_D = 13.2 A, $R_{G(ext)}$ = 2.5 Ω, Timing relative to V_{DS} Inductive load	Fig. 27
t_r	Rise Time		33				
$t_{d(off)}$	Turn-Off Delay Time		17				
t_f	Fall Time		8				
$R_{G(int)}$	Internal Gate Resistance		4		Ω	f = 1 MHz, V_{AC} = 25 mV	
Q_{gs}	Gate to Source Charge		16		nC	V_{DS} = 400 V, V_{GS} = -4 V/15 V I_D = 13.2 A Per IEC60747-8-4 pg 21	Fig. 12
Q_{gd}	Gate to Drain Charge		13				
Q_g	Total Gate Charge		46				

Note (3): $C_{o(er)}$, a lumped capacitance that gives same stored energy as Coss while Vds is rising from 0 to 400V
$C_{o(tr)}$, a lumped capacitance that gives same charging time as Coss while Vds is rising from 0 to 400V

Reverse Diode Characteristics (T_C = 25˚C unless otherwise specified)

Symbol	Parameter	Typ.	Max.	Unit	Test Conditions	Note
V_{SD}	Diode Forward Voltage	4.6		V	V_{GS} = -4 V, I_{SD} = 6.6 A, T_J = 25 °C	Fig. 8, 9, 10
		4.1		V	V_{GS} = -4 V, I_{SD} = 6.6 A, T_J = 175 °C	
I_S	Continuous Diode Forward Current		23	A	V_{GS} = -4 V, T_C = 25˚C	
$I_{S, pulse}$	Diode pulse Current		99	A	V_{GS} = -4 V, pulse width t_P limited by T_{jmax}	
t_{rr}	Reverse Recover time	23		ns	V_{GS} = -4 V, I_{SD} = 13.2 A, V_R = 400 V dif/dt = 1720 A/µs, T_J = 175 °C	
Q_{rr}	Reverse Recovery Charge	108		nC		
I_{rrm}	Peak Reverse Recovery Current	8		A		
t_{rr}	Reverse Recover time	30		ns	V_{GS} = -4 V, I_{SD} = 13.2 A, V_R = 400 V dif/dt = 790 A/µs, T_J = 175 °C	
Q_{rr}	Reverse Recovery Charge	97		nC		
I_{rrm}	Peak Reverse Recovery Current	6		A		

Thermal Characteristics

Symbol	Parameter	Typ.	Max.	Unit	Test Conditions	Note
$R_{\theta JC}$	Thermal Resistance from Junction to Case	1.02	1.14	°C/W		Fig. 21

Typical Performance

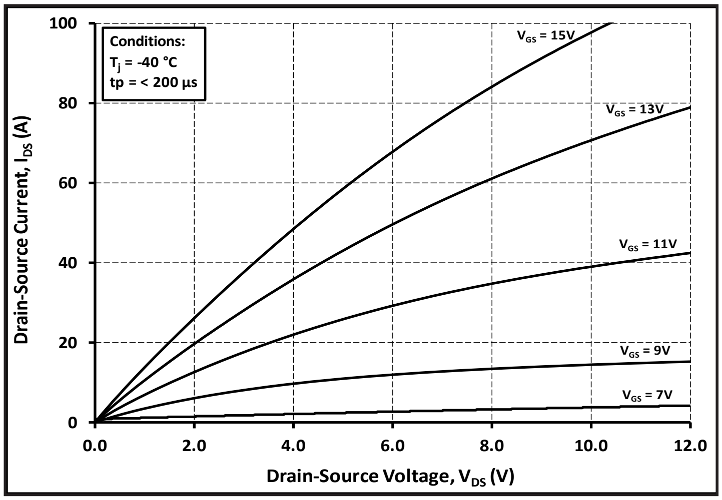


Figure 1. Output Characteristics T_J = -40 °C

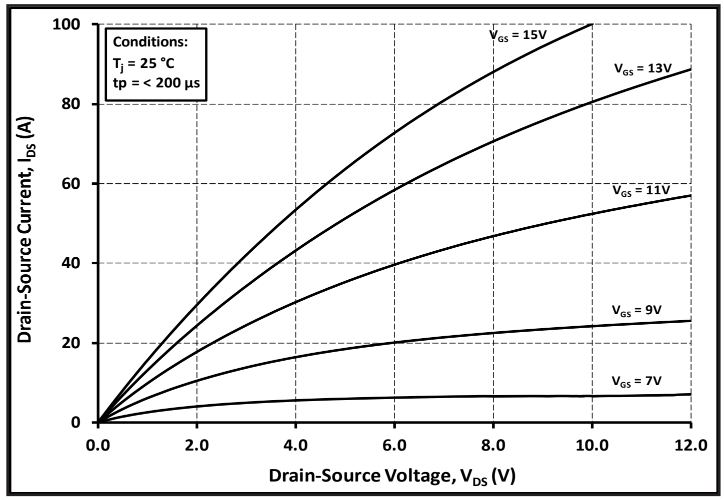


Figure 2. Output Characteristics T_J = 25 °C

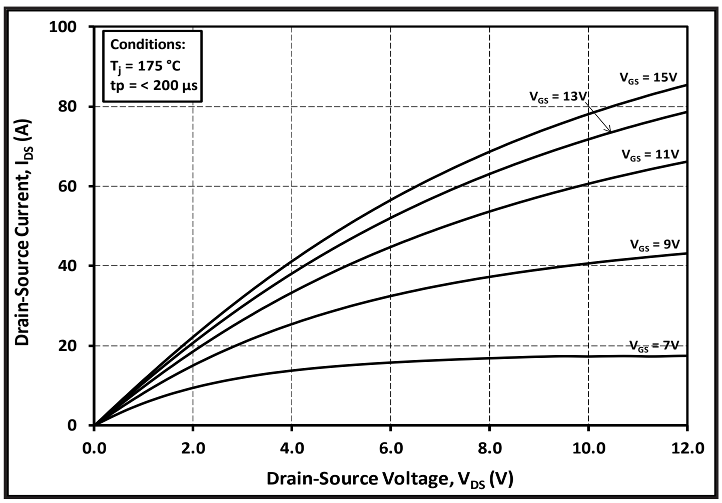


Figure 3. Output Characteristics T_J = 175 °C

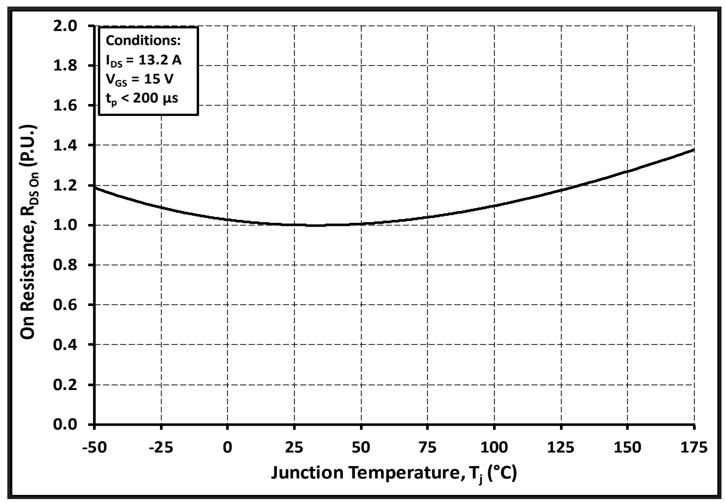


Figure 4. Normalized On-Resistance vs. Temperature

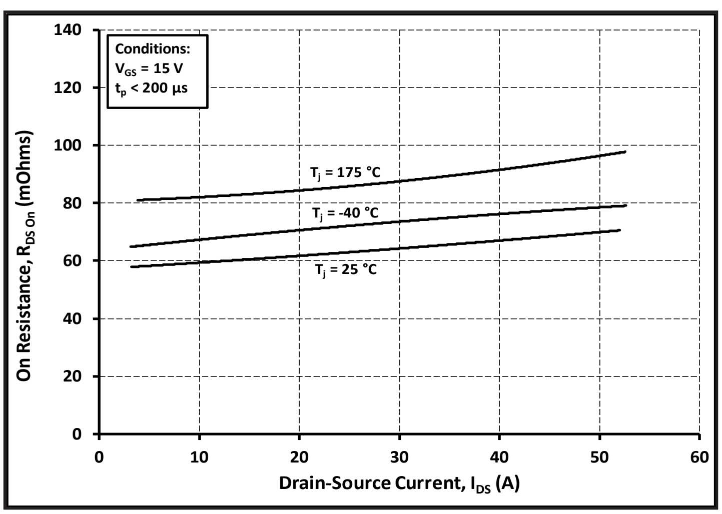


Figure 5. On-Resistance vs. Drain Current
For Various Temperatures

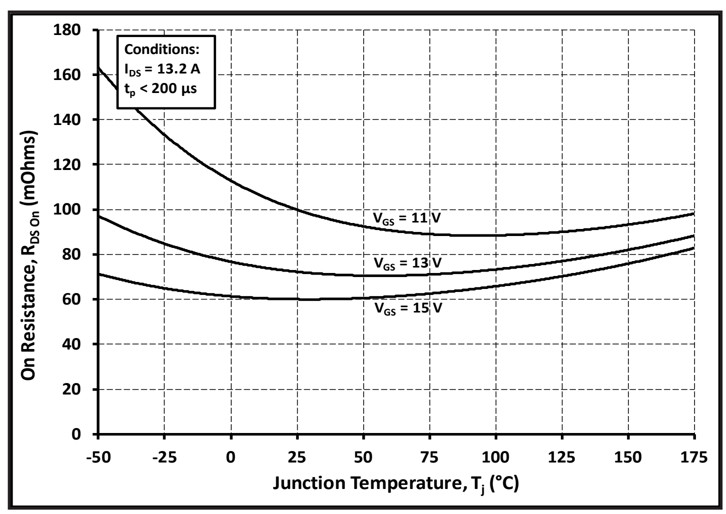


Figure 6. On-Resistance vs. Temperature
For Various Gate Voltage

Typical Performance

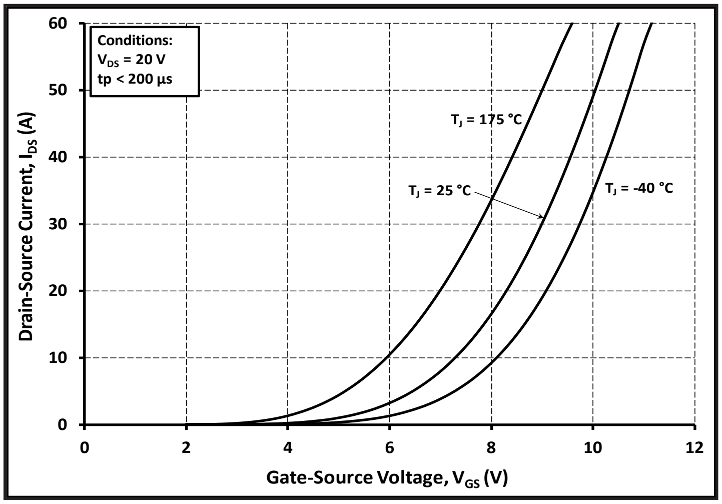


Figure 7. Transfer Characteristic for Various Junction Temperatures

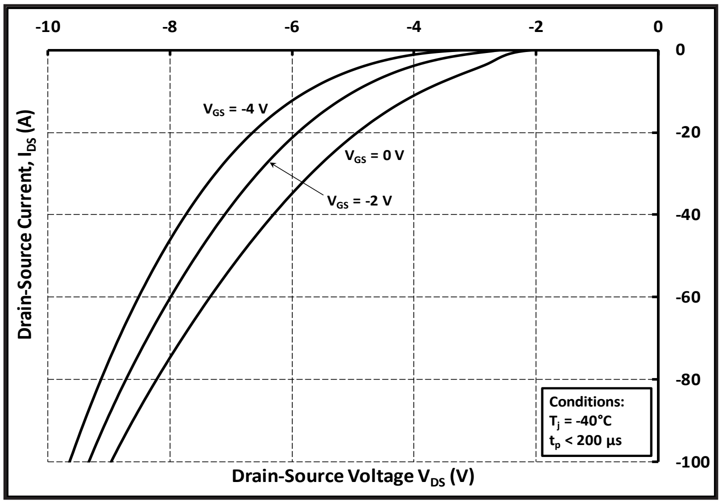


Figure 8. Body Diode Characteristic at -40 °C

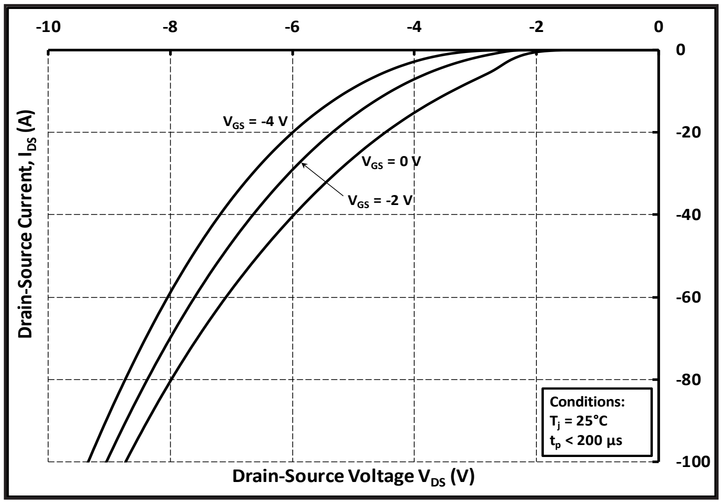


Figure 9. Body Diode Characteristic at 25 °C

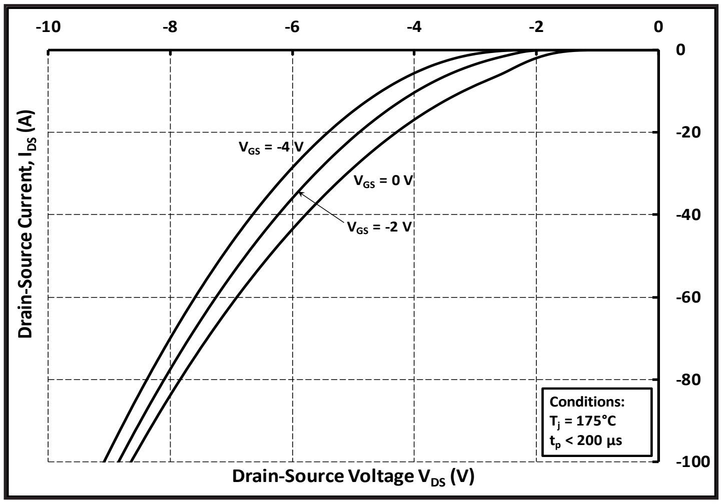


Figure 10. Body Diode Characteristic at 175 °C

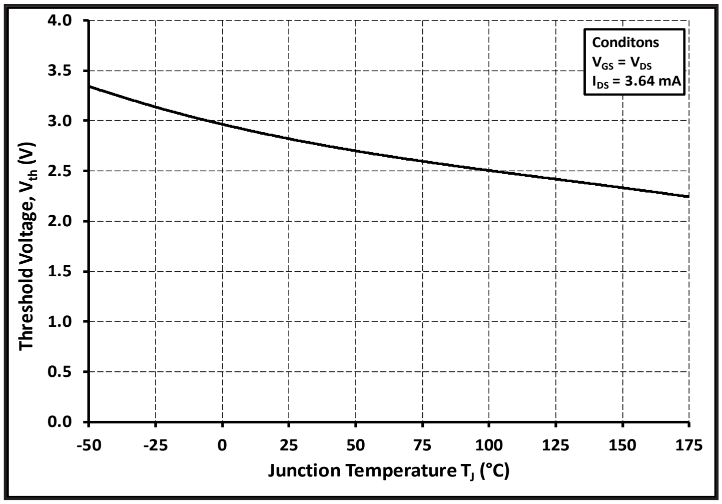


Figure 11. Threshold Voltage vs. Temperature

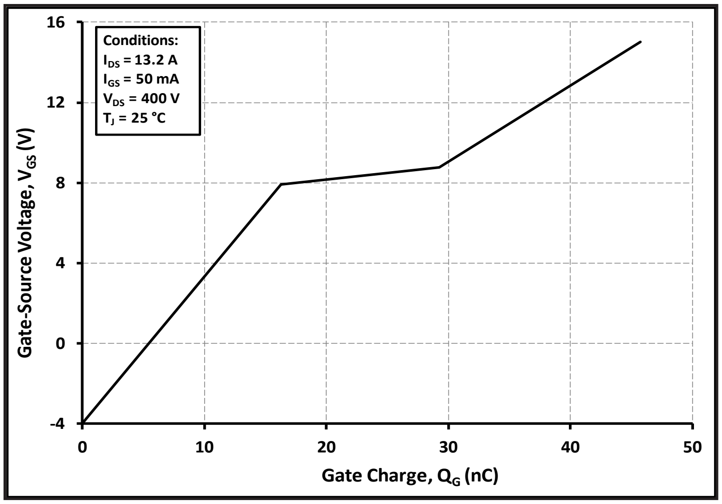


Figure 12. Gate Charge Characteristics

Typical Performance

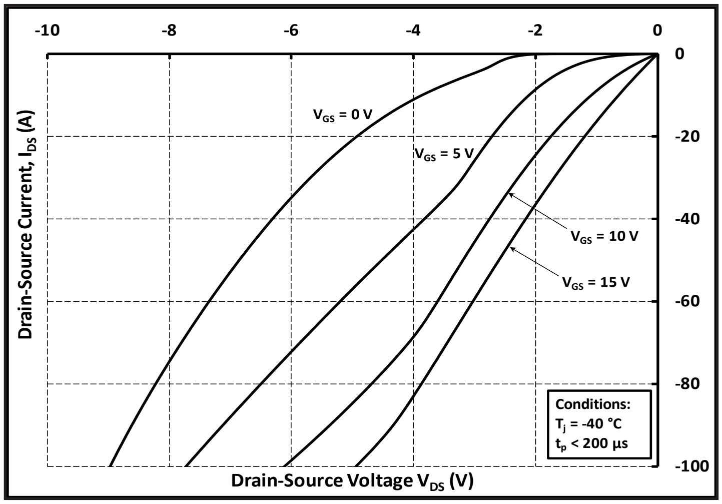


Figure 13. 3rd Quadrant Characteristic at -40 °C

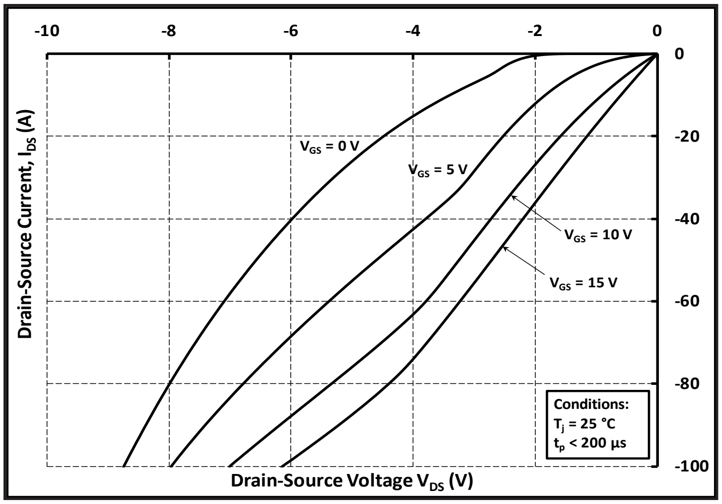


Figure 14. 3rd Quadrant Characteristic at 25 °C

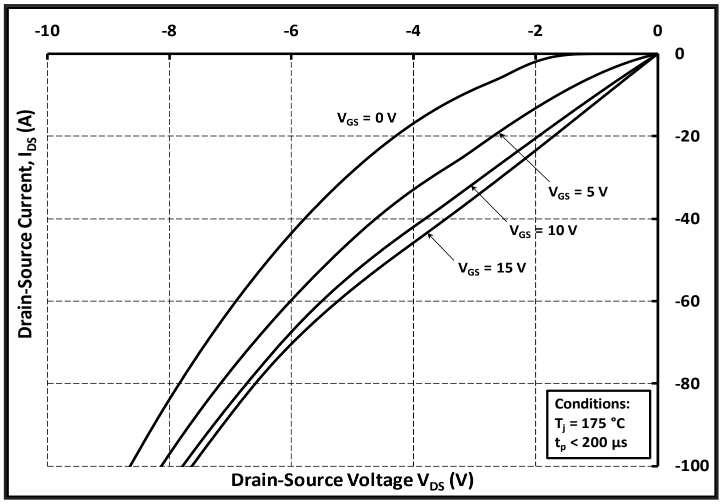


Figure 15. 3rd Quadrant Characteristic at 175 °C

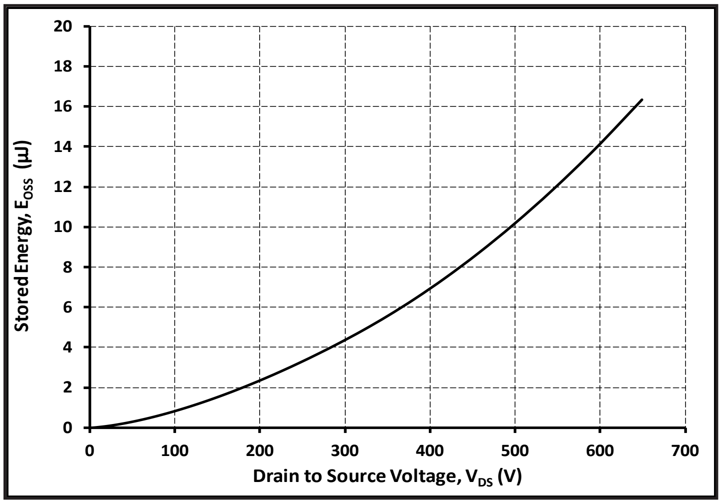


Figure 16. Output Capacitor Stored Energy

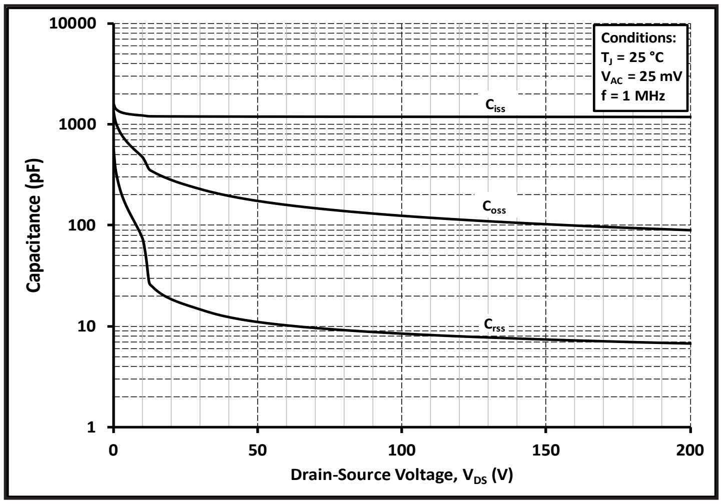


Figure 17. Capacitances vs. Drain-Source Voltage (0 - 200V)

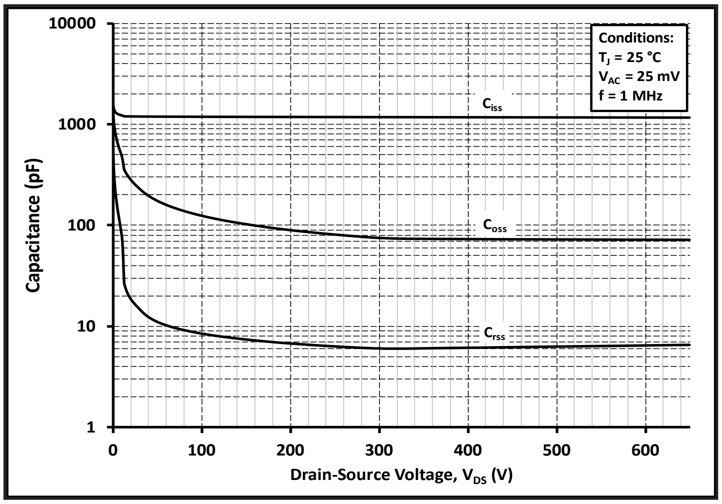


Figure 18. Capacitances vs. Drain-Source Voltage (0 - 650V)

Typical Performance

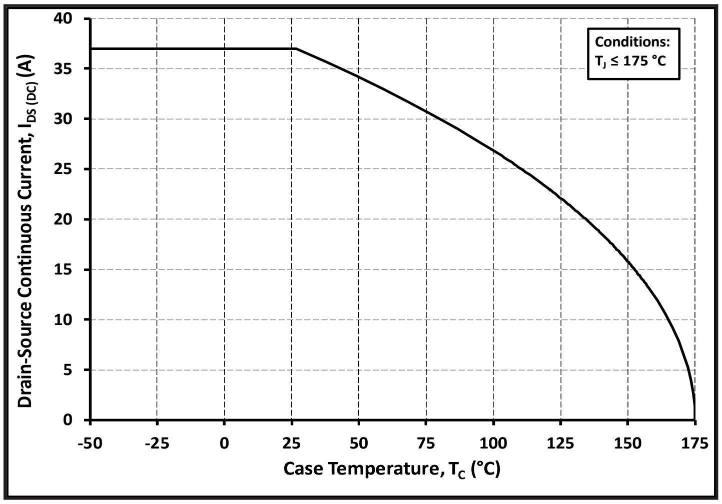


Figure 19. Continuous Drain Current Derating vs. Case Temperature

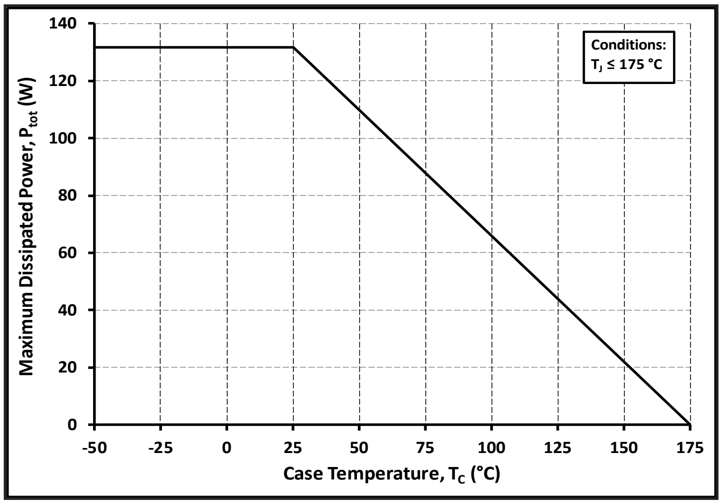


Figure 20. Maximum Power Dissipation Derating vs. Case Temperature

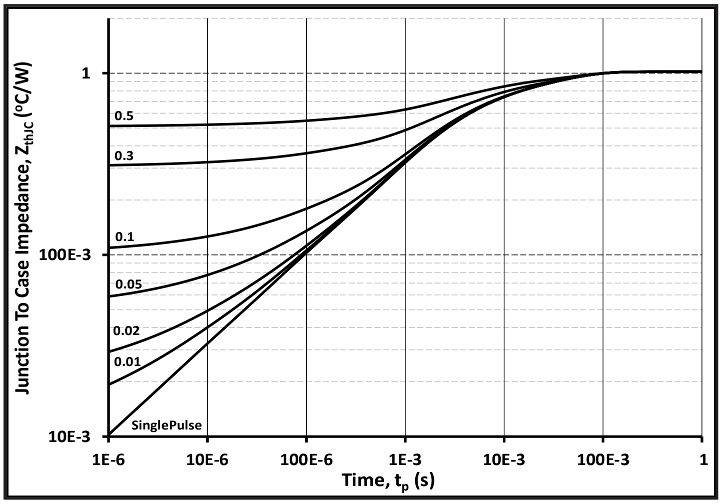


Figure 21. Transient Thermal Impedance (Junction - Case)

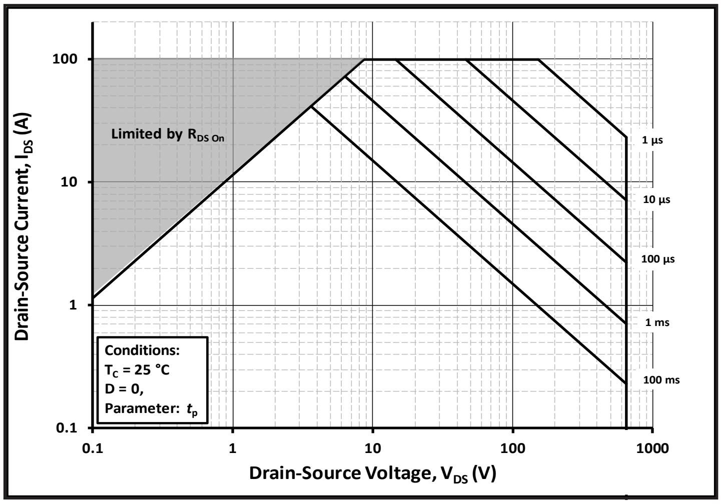


Figure 22. Safe Operating Area

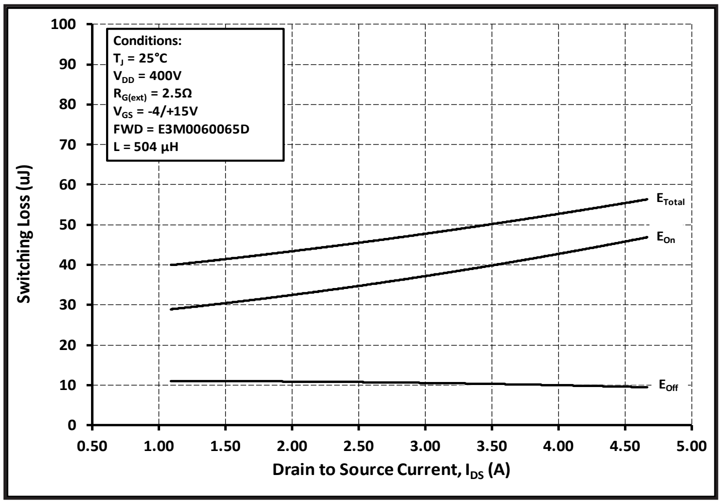


Figure 23. Clamped Inductive Switching Energy vs. Low Drain Current (V_{DD} = 400V)

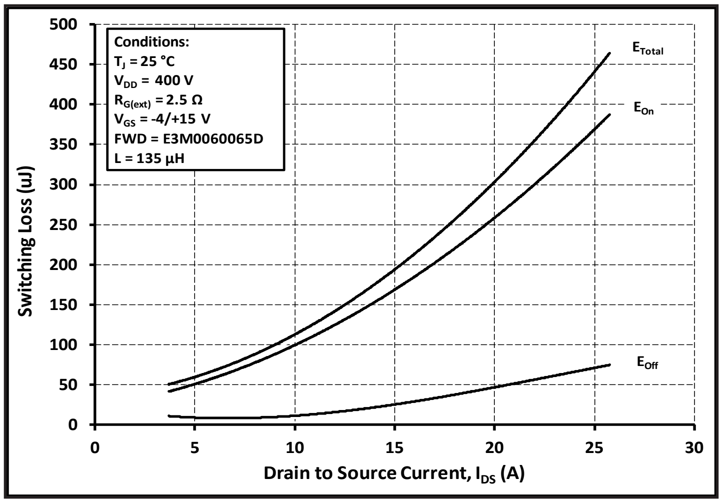


Figure 24. Clamped Inductive Switching Energy vs. High Drain Current (V_{DD} = 400V)

Typical Performance

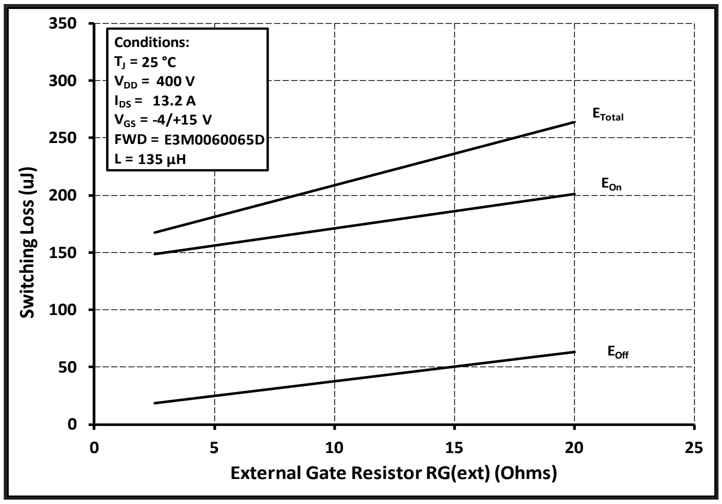


Figure 25. Clamped Inductive Switching Energy vs. $R_{G(ext)}$

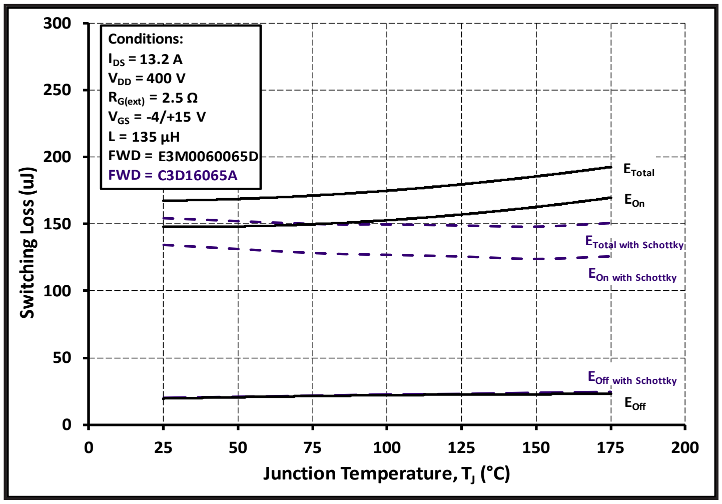


Figure 26. Clamped Inductive Switching Energy vs. Temperature

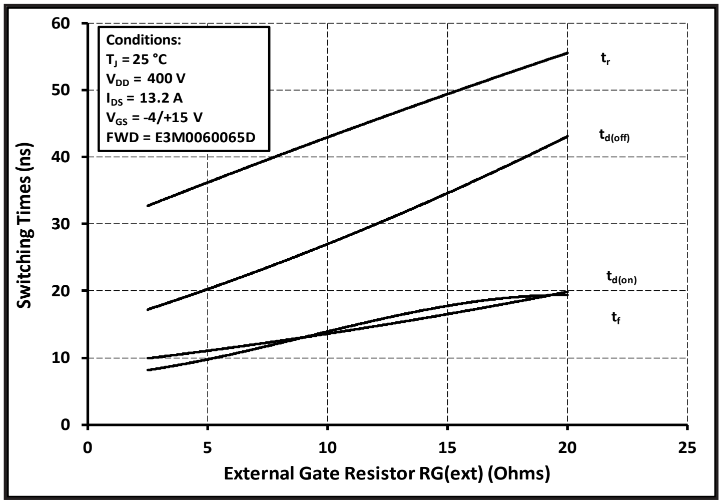


Figure 27. Switching Times vs. $R_{G(ext)}$

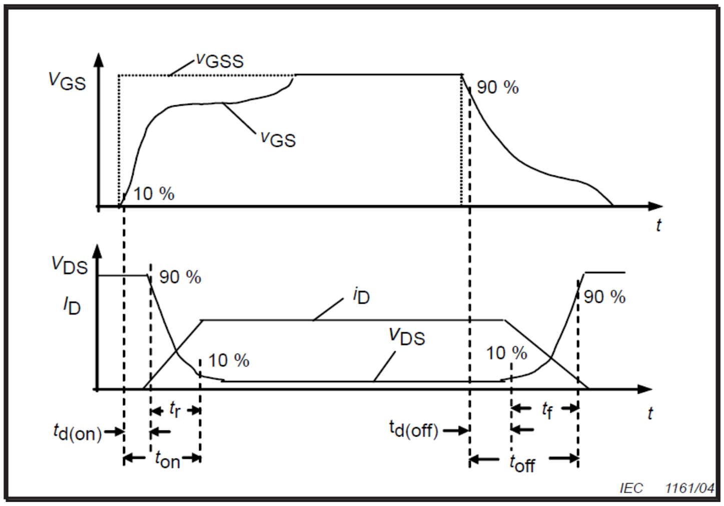


Figure 28. Switching Times Definition

Test Circuit Schematic

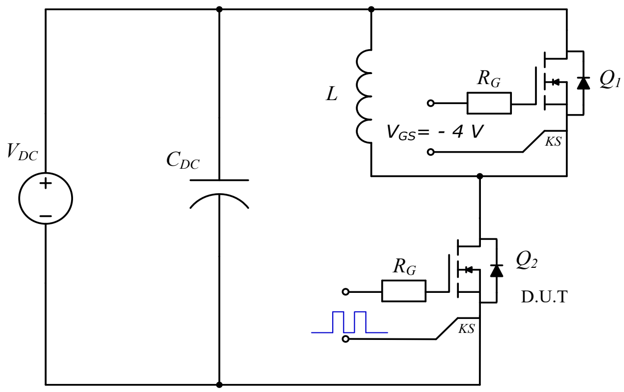
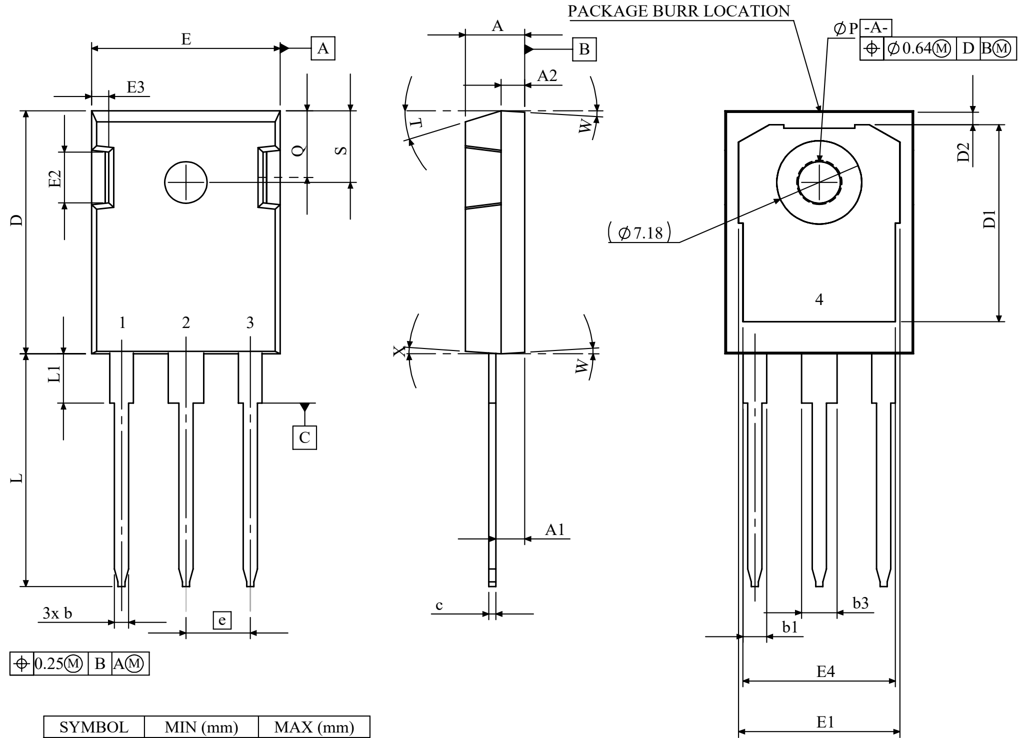


Figure 29. Clamped Inductive Switching Waveform Test Circuit

Package Dimensions



SYMBOL	MIN (mm)	MAX (mm)
A	4.83	5.21
A1	2.29	2.54
A2	1.91	2.16
b	1.07	1.33
b1	1.91	2.41
b3	2.87	3.38
c	0.55	0.68
D	20.8	21.1
D1	16.25	17.65
D2	0.95	1.25
E	15.75	16.13
E1	13.1	14.15
E2	3.68	5.1
E3	1	1.9
E4	12.38	13.43
e	5.44 BSC	
L	19.81	20.32
L1	4.1	4.4
ØP	3.51	3.65
Q	5.49	6
S	6.04	6.3
T	17.5° REF.	
W	3.5° REF.	
X	4° REF.	

1	GATE
2	DRAIN
3	SOURCE
4	DRAIN

NOTES:

1. ALL METAL SURFACES ARE TIN PLATED (MATTE), EXCEPT AREA OF CUT.
2. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
3. ALL DIMENSIONS ARE LISTED IN MILLIMETERS. ANGLES ARE IN DEGREES.
4. BURR OR MOLD FLASH SIZE (0.5 mm) IS NOT INCLUDED IN THE DIMENSIONS

Wolfspeed.

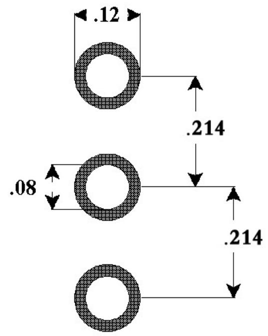
TITLE: PACKAGE OUTLINE DRAWING: TO-247-3L(MOSFET)

Date: 04/13/22

REVISION NO. 01 | A4

SCALE:1:1 | SHEET 1 OF 1

Recommended Solder Pad Layout



TO-247-3

Revision history

Document Version	Date of release	Descriptiion of changes
1.0	June-2022	Initial datasheet

Notes & Disclaimer

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