LCD MODULE

(DEPARTMENT)

SPECIFICATION

T3224C01VR03 – REV. A

(320 x 240 RGB TFT 2.2")

CUSTOMER APPROVAL
……STAMP AND SIGNATURE……
DATE: _____

IMPORTANT NOTE: This document must be approved by customer and send back to CCT by mail, email or fax.
If the approved document is not returned, CCT will assume it has been approved if any Mass Production Order is issued subsequently.

	Designation	Name	Signature/Date
Originator	**Electronic Engineer**	**Christopher Choong**	**24.01.08**
Checked by	**Assistant Manager**	**Azhar Rosdi**	**24.01.08**
Approved by	**Project Manager**	**Jack Ng**	**24.01.08**

LCD Module Specification

1.0 Table of Contents

2.0 Record of revision

Rev	Date	Item	Page	Comment
A	24/01/08			Initial Release

3.0 General specification

Display format	: 240 (W) x RGB x 320 (H) dots
Screen size	: 2.2 inch
Surface treatment	: Anti-glare
Active area	: 33.48mm x 44.64mm
General dimensions	: 39.40mm x 54.85mm x 2.95mm
Pixel pitch	: 0.1395mm x 0.1395mm
Controller	: Solomon SSD1289

LCD type : ☐ CSTN ☒ TFT ☐ OLED

Polarizer mode : ☐ Reflective ☐ Transflective

☒ Transmissive

View angle : ☐ 6 O' clock ☒ 12 O'clock

☐ 9 O'clock ☐ 3 O'clock

Backlight : ☐ NONE ☒ LED ☐ CCFL

Backlight color : ☐ Yellow Green ☐ Amber ☒ White

☐ Blue Green ☐ Others

Temperature range : ☐ Normal temperature ☒ Wide temperature

Operating 0 to 50 C Operating -10 to 60 C

Storage –20 to 70 C Storage –20 to 70 C

4.0 Absolute maximum rating (Ta = 25°C)

Parameter	Symbol	Min.	Max.	Unit	Note
Power supply voltage (VCC,IOVCC)	VCC,IOVCC	-0.3	+4.6	V	1,2
Power supply voltage (VCI ~ VSSA)	VCI ~ VSSA	-0.3	+4.6	V	1,2
Power supply voltage (VLCD ~ VSSA)	VLCD ~ VSSA	-0.3	+6.0	V	3
Power supply voltage (VSSA ~ VCL)	VSSA ~ VCL	-0.3	+4.6	V	4
Power supply voltage (VLCD ~ VCL)	VLCD ~ VCL	-0.3	+9	V	5
Power supply voltage (VGH ~ VSSA)	VGH ~ VSSA	-0.3	+18.5	V	6
Power supply voltage (VSSA ~ VGL)	VSSA ~ VGL	-0.3	+18.5	V	7
Input voltage	Vi	-0.3	VCC+0.3	V	-

Notes:
1. VCC, VSSD must be maintained
2. To make sure IOVCC ≥ VSSD.
3. To make sure VCI ≥ VSSA.
4. To make sure VLCD ≥ VSSA.
5. To make sure VLCD ≥ VCL.
6. To make sure VGH ≥ VSSA.
7. To make sure VSSA ≥ VGL.
8. The modules may be destroyed if they are used beyond the absolute maximum ratings.

5.0 Electrical characteristics (Ta = 25°C)

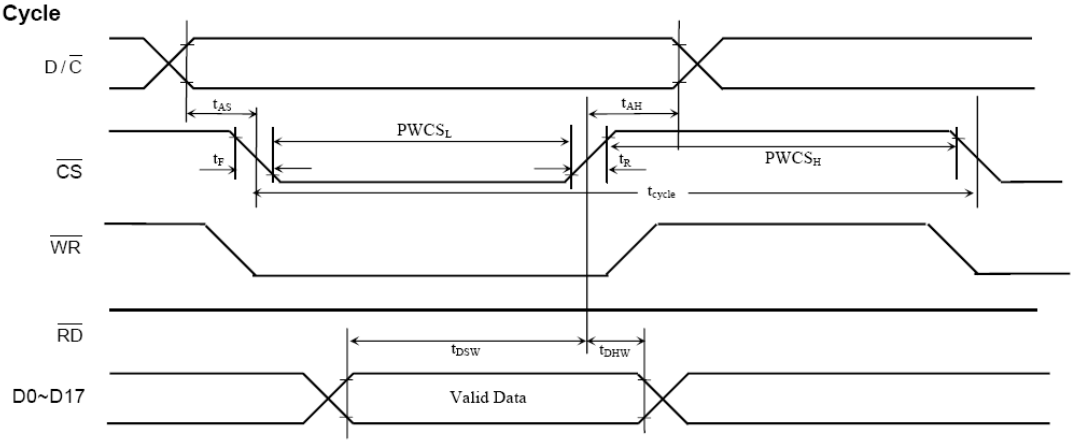
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage (logic)	VCC-GND		2.2	2.8	3.3	V
Supply voltage (for analog power supply)	VCI		2.5	2.8	3.3	V
TFT gate ON voltage	VGH (Note 2)	At Ta=25°C±5°C (Note 4)	-	15	-	V
TFT gate OFF voltage	VGL (Note 3)		-	-10	-	V
TFT common electrode voltage	VcomH		2.5	-	4	V
	VcomL		-1.5	-	0	V
Input signal voltage	V_{IH}	"H" level	0.8xIOVCC	-	IOVCC	V
	V_{IL}	" L" level	-0.3	-	0.2xIOVCC	V
Supply current (Logic & LCD)	ICC	VCC=2.8V	-	-	18.0	mA
Supply voltage of white LED backlight	VLED =V_{AK}	Forward current =15mA	-	13.2	-	V
Luminance (on the backlight surface)		Number of LED dies = 4	3000	3300	-	cd/m^2
Luminance of white LED backlight (through TFT panel)		Forward current =15mA, backlight on, panel no display, measure=~30cm	200	-	-	cd/m^2

Note (1): There is tolerance in optimum LCD driving voltage during production and it will be within the specified range.
Note (2): VGH is TFT Gate operating voltage.
Note (3): VGL is TFT Gate operating voltage. The low voltage level VGL signal must be fluctuates with same phase as Vcom in case of Cadd (Storage on Gate) structure.
Note (4): Vcom must be adjusted to optimize display quality.

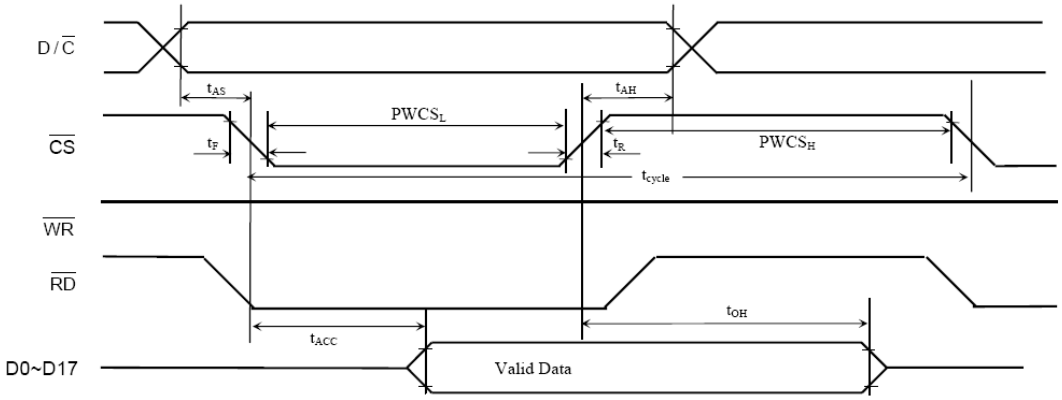
5.1 Driver IC AC Characteristics

5.1.1 8080-Series MPU Parallel Interface Characteristics

Write Cycle



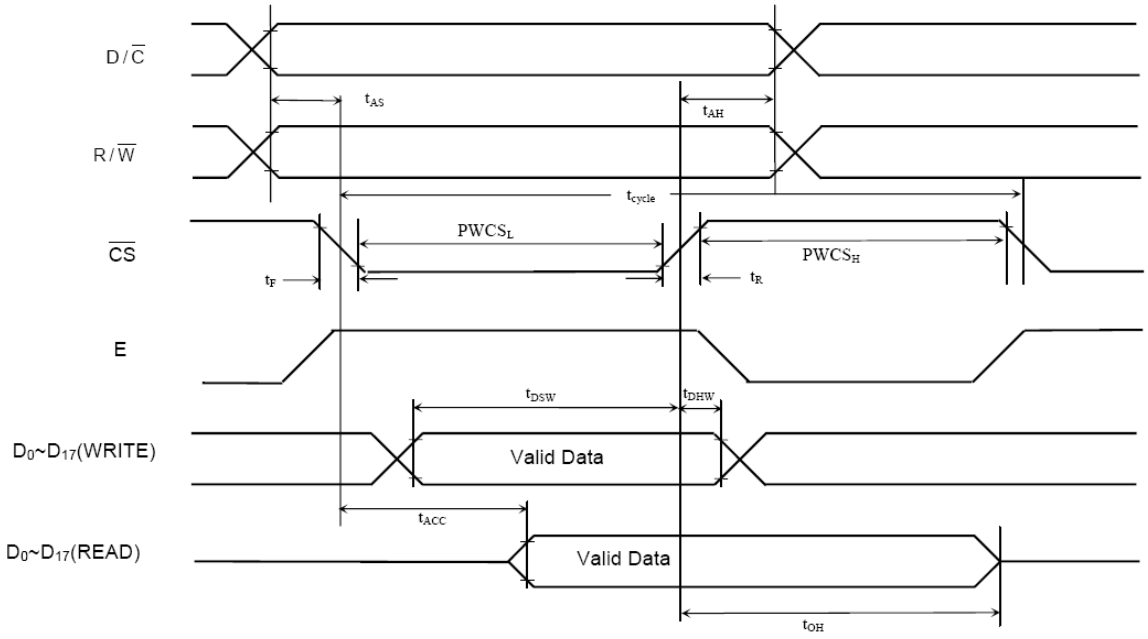
Read Cycle



Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time (write cycle)	100	-	-	ns
t_{cycle}	Clock Cycle Time (read cycle)	1000	-	-	ns
t_{AS}	Address Setup Time	0	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Data Setup Time	5	-	-	ns
t_{DHW}	Data Hold Time	5	-	-	ns
t_{ACC}	Data Access Time	250	-	-	ns
t_{OH}	Output Hold time	100	-	-	ns
$PWCS_L$	Pulse Width /CS low (write cycle)	50	-	-	ns
$PWCS_H$	Pulse Width /CS high (write cycle)	50	-	-	ns
$PWCS_L$	Pulse Width /CS low (read cycle)	500	-	-	ns
$PWCS_H$	Pulse Width /CS high (read cycle)	500	-	-	ns
t_R	Rise time	-	-	4	ns
t_F	Fall time	-	-	4	ns

5.1.2 6800-Series MPU Parallel Interface Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time (write cycle)	100	-	-	ns
t_{cycle}	Clock Cycle Time (read cycle)	1000	-	-	ns
t_{AS}	Address Setup Time	0	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Data Setup Time	5	-	-	ns
t_{DHW}	Data Hold Time	5	-	-	ns
t_{ACC}	Data Access Time	250	-	-	ns
t_{OH}	Output Hold time	100	-	-	ns
$PWCS_L$	Pulse width /CS low (write cycle)	50	-	-	ns
$PWCS_H$	Pulse width /CS high (write cycle)	50	-	-	ns
$PWCS_L$	Pulse width /CS low (read cycle)	500	-	-	ns
$PWCS_H$	Pulse width /CS high (read cycle)	500	-	-	ns
t_R	Rise time	-	-	4	ns
t_F	Fall time	-	-	4	ns



6.0 Environmental requirements

Item	Operating temperature (Topr)		Storage temperature (Tstg) (Note 1)		Remark
	Min.	Max.	Min.	Max.	
Ambient temperature (Ta)	-10°C	+60°C	-20°C	+70°C	Dry
Humidity (Note 1)	90% max. RH for Ta ≤ 40°C < 50% RH for 40°C < Ta ≤ Maximum operating temperature				No condensation
Vibration (IEC 68-2-6) cells must be mounted on a suitable connector	Frequency: 10 ~ 55 Hz Amplitude: 0.75 mm Duration: 20 cycles in each direction.				3 directions
Shock (IEC 68-2-27) Half-sine pulse shape	Pulse duration: 11 ms Peak acceleration: 981 m/s^2 = 100g Number of shocks: 3 shocks in 3 mutually perpendicular axes.				3 directions

Note: The product cannot sustain at extreme storage conditions for long time.

7.0 LCD specification

7.1 Electro-optical characteristic

Item		Symbol	Conditions	Specifications Min.	Typ.	Max.	Unit	Note
Transmittance		T%	Viewing normal angle $\theta_X = \theta_Y = 0°$		6.9		%	All left side data are based on following condition – NTSC: 50% LC: 5066 Light: C light (Machine: BM5A) Normal Polarizer Reference Only
Contrast Ratio		CR		150	200	NA	-	
Response Time		T_R		NA	10	25	ms	
		T_F		NA	20	40	ms	
Chromaticity	Red	X_R		0.615	0.645	0.645	-	
		Y_R		0.343	0.373	0.373	-	
	Green	X_G		0.307	0.337	0.337	-	
		Y_G		0.563	0.593	0.593	-	
	Blue	X_B		0.133	0.163	0.163	-	
		Y_B		0.150	0.180	0.180	-	
	White	X_W		0.309	0.339	0.339	-	
		Y_W		0.350	0.380	0.380	-	
Viewing Angle	Hor.	θ_{X+}	Center CR≥10	-	45	-	deg.	
		θ_{X-}		-	45	-		
	Ver.	θ_{Y+}		-	35	-		
		θ_{Y-}		-	15	-		

*Note (1) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

Contrast Ratio (CR) = L63 / L0

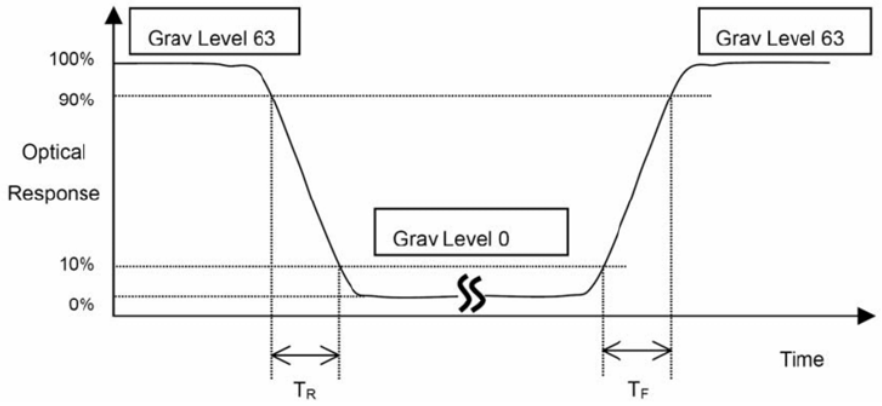
L63: Luminance of gray level 63

L0: Luminance of gray level 0

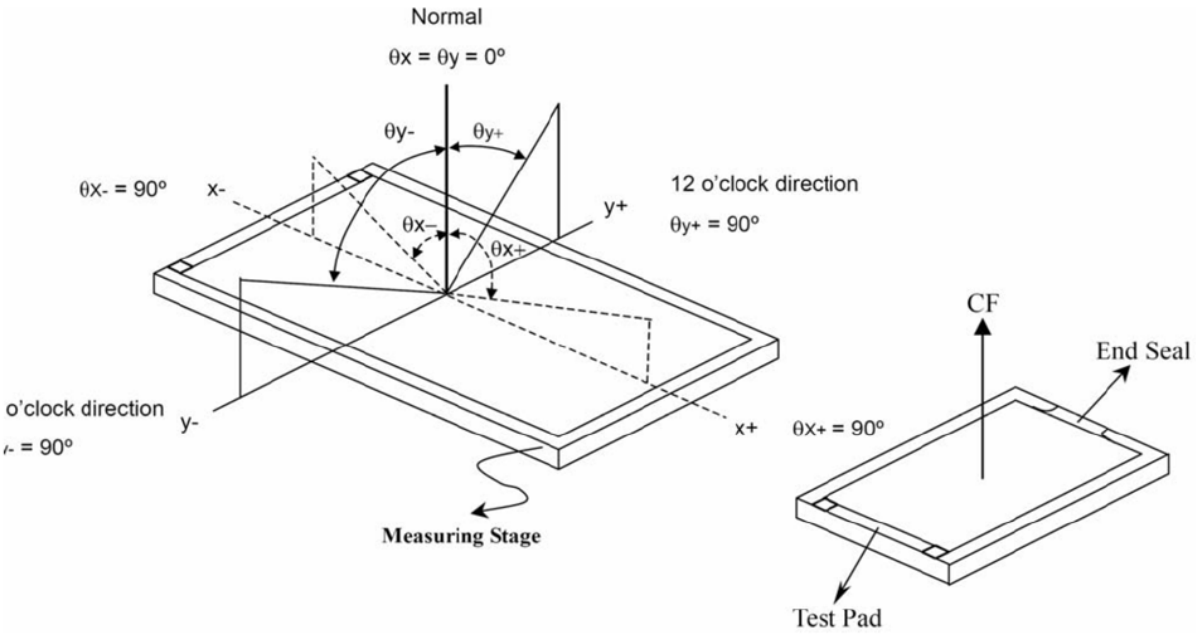
CR = CR (10)

CR (X) is corresponding to the Contrast Ratio of the point X at Figure in Note (6).

*Note (2) Definition of Response Time (TR, TF):



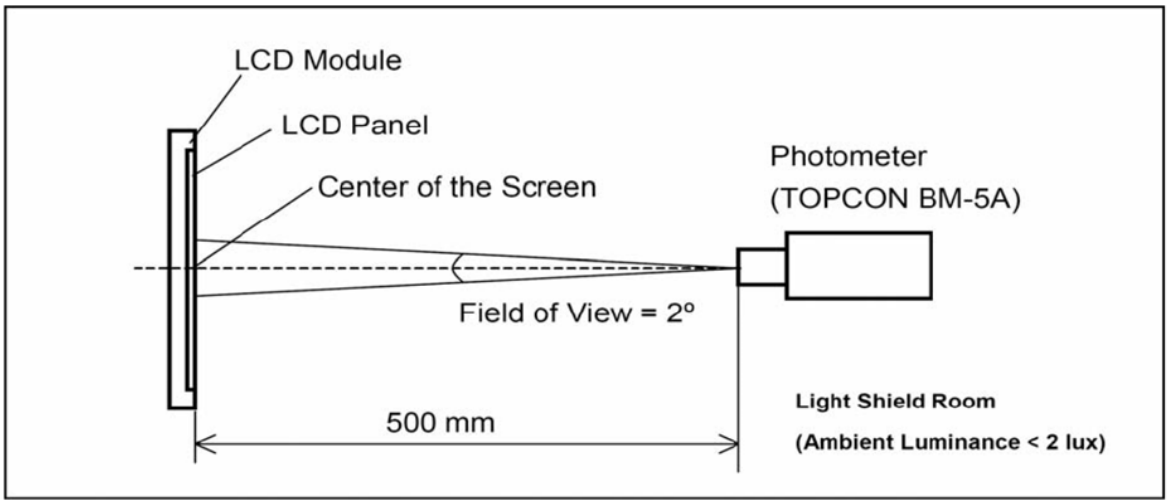
*Note (3) Definition of Viewing Angle



*** The above "Viewing Angle" is the measuring position with Largest Contrast Ratio; not for good image quality. View Direction for good image quality is 6 O'clock. Module maker can increase the "Viewing Angle" by applying Wide View Film.

*Note (4) Measurement Set-Up

The LCD module should be stabilized at a given temperature for 20 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 20 minutes in a windless room.



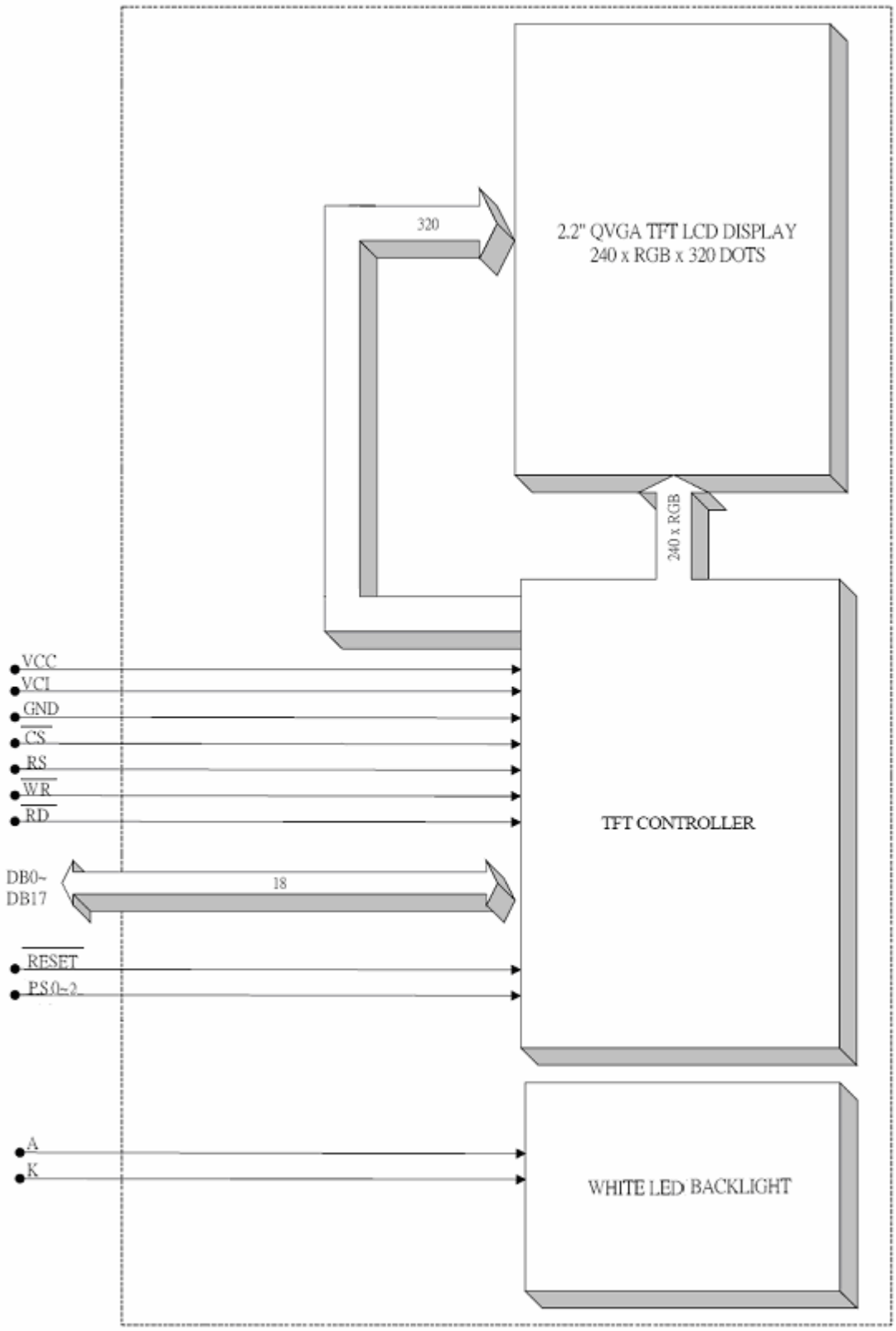
8.0 Interface

Pin no.	Symbol	Description
1	VCC	Power supply for internal logic
2	VCI	Power supply for step-up circuit
3	GND	Ground terminal
4	GND	Ground terminal
5	/CS	Chip select signal (Active low)
6	RS	Command/Data select
7	/WR (R/W)	Write signal (Active low)
8	/RD (E)	Read signal (Active low)
9	DB0	Data bus
10	DB1	
11	DB2	
12	DB3	
13	DB4	
14	DB5	
15	DB6	
16	DB7	
17	DB8	
18	DB9	
19	DB10	
20	DB11	
21	DB12	
22	DB13	
23	DB14	
24	DB15	
25	DB16	
26	DB17	
27	/RESET	Reset signal (Active low)
28	PS0	Selection pin
29	PS1	Selection pin
30	PS2	Selection pin
31	K	Cathode of backlight
32	A	Anode of backlight

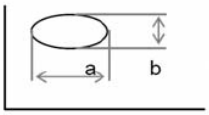
PS2	PS1	PS0	Interface mode
0	1	1	16-bits 6800 parallel interface
0	1	0	8-bits 6800 parallel interface
0	0	1	16-bits 8080 parallel interface
0	0	0	8-bits 8080 parallel interface

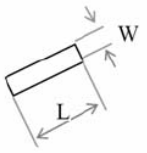
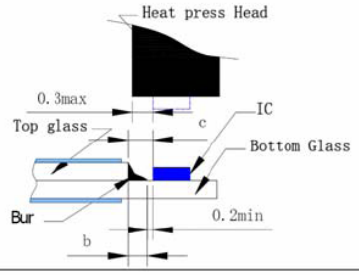
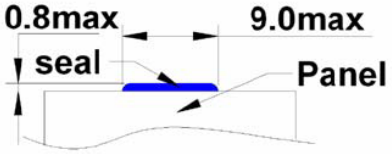
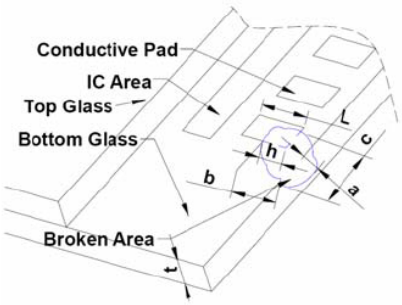
PS3 is set to be high internally on the FPC.
To set PS3 low, please remove R9 and add jumper to R10 on FPC.

9.0. Block Diagram

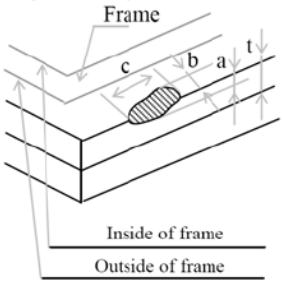
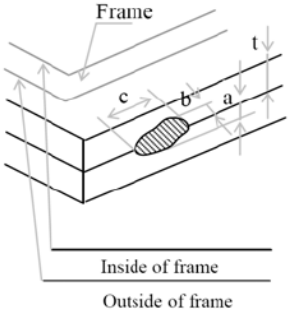
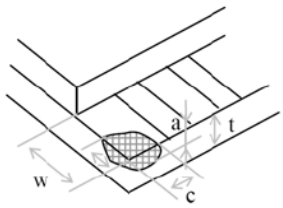


10.0 TFT Panel inspection

<table>
<tr><td rowspan="6">1. Dot Defects</td><td rowspan="6"> 

Φ=(a+b)/2</td><td colspan="2" rowspan="2">Classifications</td><td colspan="2">Acceptable counts</td></tr>
<tr><td>Visible area</td><td>Non-visible area</td></tr>
<tr><td rowspan="2">A grade</td><td>Φ≦0.10</td><td>Don't care</td><td rowspan="4">Don't care</td></tr>
<tr><td>0.10<Φ≦0.15</td><td>1</td></tr>
<tr><td rowspan="2">B grade</td><td>0.15<Φ≦0.2</td><td>3</td></tr>
<tr><td>0.1<Φ≦0.15</td><td>5</td></tr>
<tr><td rowspan="4">2. Line Defects</td><td rowspan="4"> 
</td><td colspan="2" rowspan="2">Classifications</td><td colspan="2">Acceptable counts</td></tr>
<tr><td>Visible area</td><td>Non-visible area</td></tr>
<tr><td rowspan="2">A grade</td><td>W≦0.03,L≦3.0</td><td>Don't care</td><td rowspan="3">Don't care</td></tr>
<tr><td>0.03<W≦0.05,L≦2.0</td><td>1</td></tr>
<tr><td>B grade</td><td>0.03<W≦0.05,L≦3.0</td><td>3</td></tr>
<tr><td rowspan="2">3.Glass bur</td><td> 
</td><td colspan="3">1). b ≦ 1.0, and not affect outline dimension and assemble
2). Around bonding area, b must fulfill b ≦ (c-0.2) max</td></tr>
<tr><td>  </td><td colspan="3">Not affect outline dimension and assemble</td></tr>
<tr><td>4. End seal dimension</td><td> 
</td><td colspan="3">1). Depth =< 0.2 mm, and not enter to the visible area
2). Height =< 0.8 mm
3). Length =< 9.0 mm</td></tr>
<tr><td>5. Glass edges breakage</td><td> 

Breakage on step glass</td><td colspan="3"><table>
<tr><td colspan="2">Categories</td></tr>
<tr><td>A</td><td>If a ≦ t and b ≦ 1.0, c has no limit</td></tr>
<tr><td>B</td><td>a ≦ t, 1≦b≦1.5, c≦3</td></tr>
<tr><td>C</td><td>If damage FPC contacts and /or alignment mark, then b ≦ 0.5, and the FPC contacts h ≦ L x 25% max</td></tr>
<tr><td>D</td><td>Side breakage should not damage alignment mark.</td></tr>
</table></td></tr>
</table>

	Edge breakage 	b should not arrive inside of frame
	Breakage between upper and lower glass 	b should not arrive outside of frame
	Corner breakage 	a ≦ t, b ≦ 2.0, c ≦ 3.0 Corner breakage should not damage track and /or alignment mark.

Items	Position	Inspection Criteria
6.Crack	Whole area	Not allowed
7.Surface cleanness	Step surface	The impurity which is easy to clean is allowed, glass particle is not allowed.
Remark: a: breakage thickness; b: breakage depth; c: breakage length; t: glass thickness; h: damaged FPC contact length; L: total length of FPC contacts (Unit: mm)		

11.0 Mechanical specification