

Multilayer Ceramic Chip Capacitors

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Cross Reference

Catalog

Tech Note

Technical Support Tool

FAQ

C5750X7R1H335K230KM



TDK item description ? C5750X7R1H335KT5***

Applications



Commercial Grade

Feature

Open

Open Mode

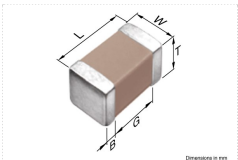
Series

C5750 [EIA 2220]

Status



Production (Not Recommended for New Design)



Images are for reference only and show exemplary products.

PDF file of this page



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Documents

Catalog

Specification

RoHS Certificate

SVHC/REACH Certificate

Characterization Sheet

Promotion Video

Sample Kits

Technical Support Tools

S-parameter

SPICE Netlist (Simple)

SPICE Netlist (Precision)

Equivalent Circuit Model

DC Bias/Superimposition Model (HSPICE)

Size

Length(L) 5.70mm ±0.40mm

Width(W) 5.00mm ±0.40mm

Thickness(T) 2.30mm ±0.20mm

Terminal Width(B) 0.20mm Min.

Terminal Spacing(G)

Recommended Land Pattern (PA) 4.10mm to 4.80mm

Recommended Land Pattern (PB) 1.20mm to 1.40mm

Recommended Land Pattern (PC) 4.00mm to 5.00mm

Electrical Characteristics

Capacitance 3.3μF ±10%

Rated Voltage 50VDC

Temperature Characteristic ? X7R(±15%)

Dissipation Factor (Max.) 3%

Insulation Resistance (Min.) 151MΩ

Other

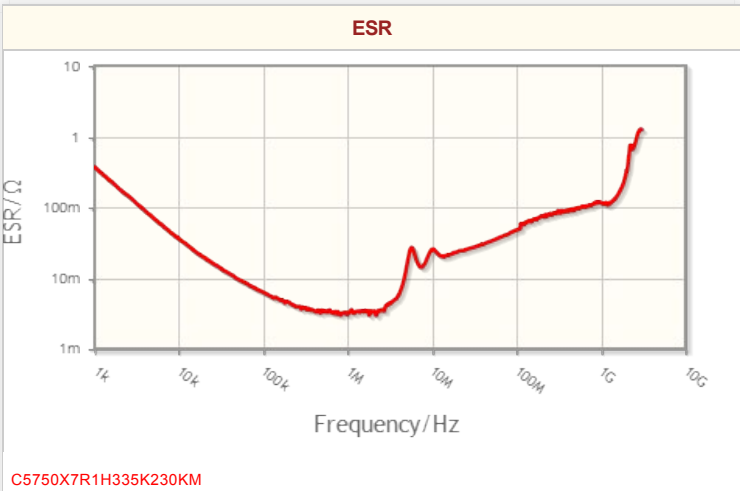
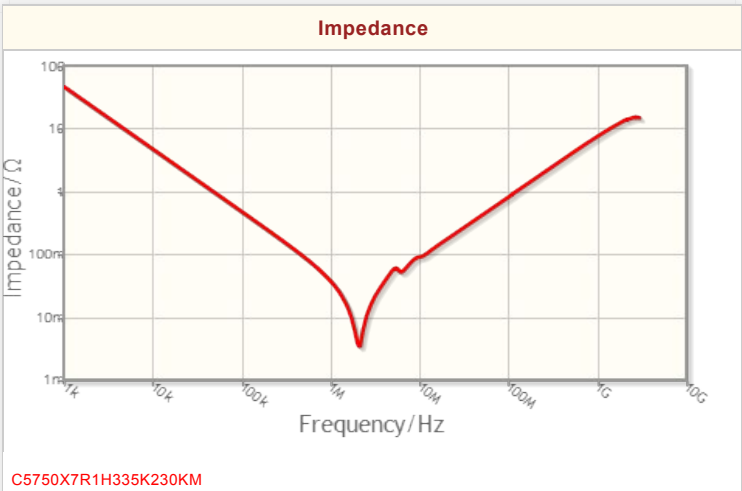
Soldering Method Reflow

AEC-Q200 No

Packing Blister (Plastic)Taping [180mm Reel]

Package Quantity 500pcs

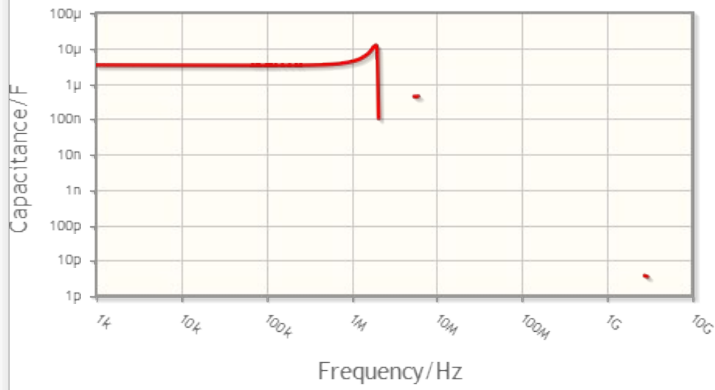
Characteristic Graph (This is reference data, and does not guarantee the products characteristics.)



Change settings

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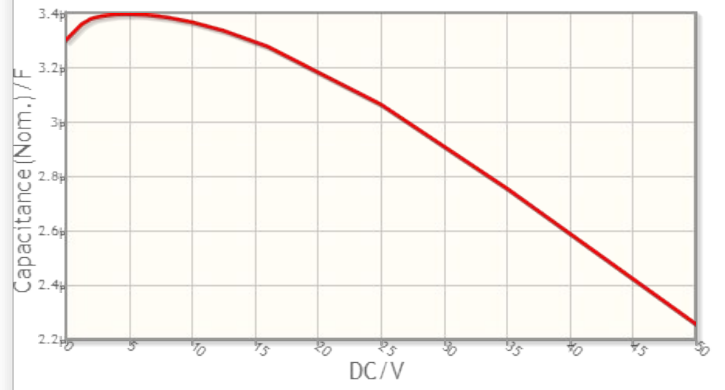
Capacitance



C5750X7R1H335K230KM

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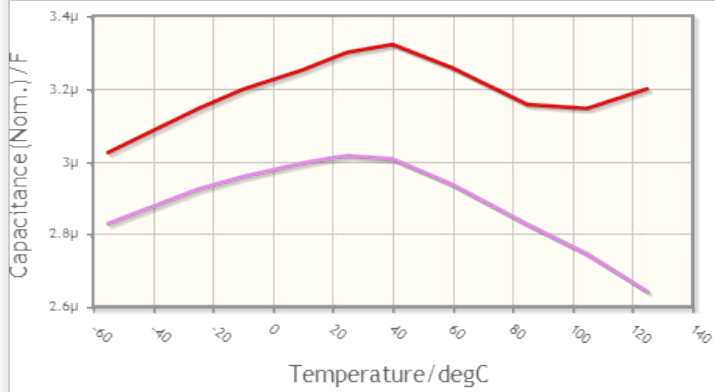
DC Bias Characteristic



C5750X7R1H335K230KM

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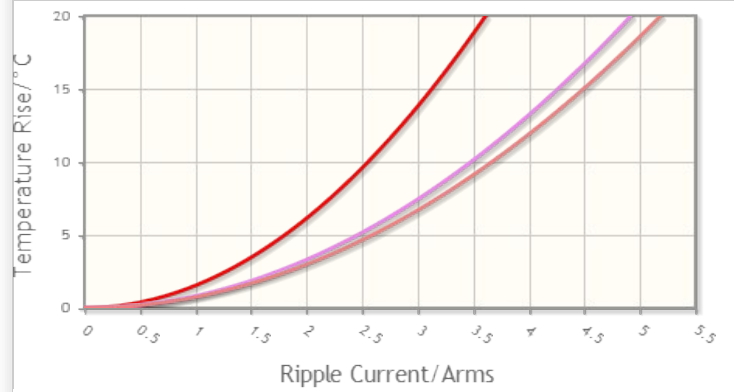
Temperature Characteristic



C5750X7R1H335K230KM(N o Bias) C5750X7R1H335K230KM(DC Bias = 25V)

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Ripple Temperature Rising



C5750X7R1H335K230KM(100k Hz) C5750X7R1H335K230KM(500k Hz) C5750X7R1H335K230KM(1M Hz)

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