CY7B952

SST™ SONET/SDH Serial Transceiver

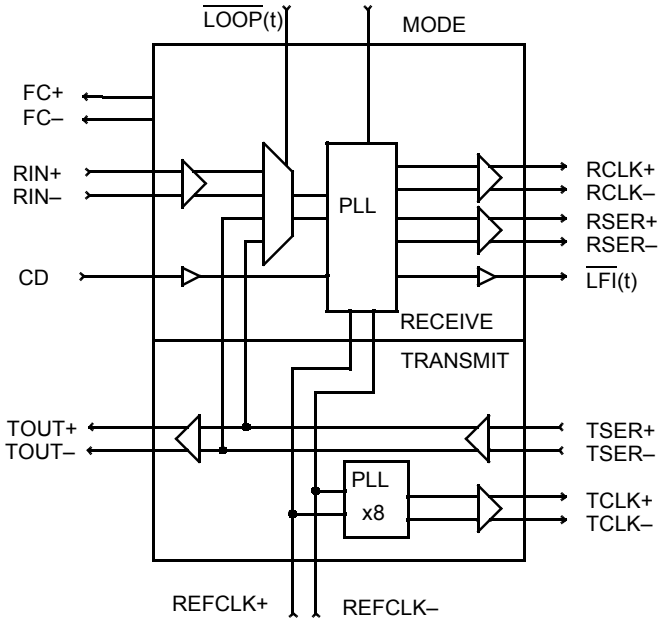
Features

- OC-3 Compliant with Bellcore and CCITT (ITU) specifications on:
  - Jitter Generation (<0.01 UI)
  - Jitter Transfer (<130 kHz)
  - Jitter Tolerance
- SONET/SDH and ATM Compliant
- Compatible with IGT WAC013, IGT WAC413, and PMC-Sierra PM5343
- Clock and data recovery from 51.84- or 155.52-MHz datastream
- 155.52-MHz clock multiplication from 19.44-MHz source
- 51.84-MHz clock multiplication from 6.48-MHz source
- ±1% frequency agility
- Line Receiver Inputs: No external buffering required
- Differential output buffering
- 100K ECL compatible I/O
- No output clock “drift” without data transitions
- Link Status Indication
- Loop-back testing
- Single +5 V supply
- 24-pin SOIC
- Compatible with fiber-optic modules, coaxial cable, and twisted pair media
- Power-down options to minimize power or crosstalk
- Low operating current: <70 mA
- 0.8µ BiCMOS

Functional Description

The SONET/SDH Serial Transceiver (SST) is used in SONET/SDH and ATM applications to recover clock and data information from a 155.52-MHz or 51.84-MHz NRZ or NRZI serial data stream and to provide differential data buffering for the Transmit side of the system.

Logic Block Diagram



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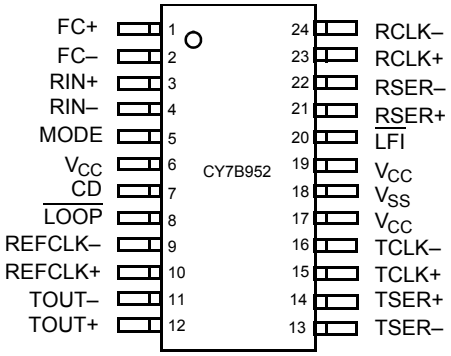
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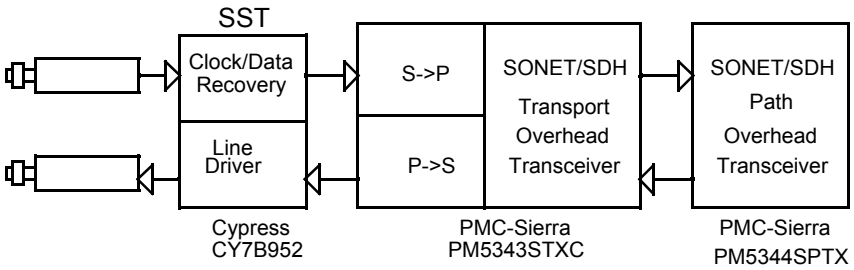
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Pin Configuration

Figure 1. 24-pin SOIC (Top View)



SONET/SDH Overhead Processing Application



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Pin Descriptions

Name	I/O	Description
RIN±	Differential In	**Receive Input**. This line receiver port connects the receive differential serial input data stream to the internal Receive PLL. This PLL will recover the embedded clock (RCLK±) and data (RSER±) information for one of two data rates depending on the state of the MODE pin. These inputs can receive very low amplitude signals and are compatible with all PECL signalling levels. If the RIN± inputs are not being used, connect RIN+ to V_{CC} and RIN– to V_{SS}.
FC±	Passive	**Passive Filter Capacitor Connection**. These pins are used to connect the external loop damping capacitor and resistor for the internal clock and data recovery phase locked loop. A 301K ± 1% resistor and a non-polar 1 µF ± 10% chip capacitor should be used in parallel for this connection.
RSER±	ECL Out	**Recovered Serial Data**. These ECL 100K outputs (+5 V referenced) represent the recovered data from the input data stream (RIN±). This recovered data is aligned with the recovered clock (RCLK±) with a sampling window compatible with most data processing devices.
RCLK±	ECL Out	**Recovered Clock**. These ECL 100K outputs (+5 V referenced) represent the recovered clock from the input data stream (RIN±). This recovered clock is used to sample the recovered data (RSER±) and has timing compatible with most data processing devices. If both the RSER± and the RCLK± are tied to V_{CC} or left unconnected, the entire Receive PLL will be powered down.
CD	TTL/ECL In	**Carrier Detect**. This input controls the recovery function of the Receive PLL and can be driven by the carrier detect output from optical modules or from external transition detection circuitry. When this input is at an ECL HIGH, the input data stream (RIN±) is recovered normally by the Receive PLL. When this input is at an ECL LOW, the Receive PLL no longer aligns to RIN±, but instead aligns with the REFCLK × 8 frequency. Also, the Link Fault Indicator ($\overline{LFI}$) will transition LOW, and the recovered data outputs (RSER) will remain LOW regardless of the signal level on the Receive data-stream inputs (RIN). When the CD input is at a TTL LOW, the internal transitions detection circuitry is disabled.
$\overline{LFI}$	TTL Out	**Link Fault Indicator**. This output indicates the status of the input data stream (RIN±). It is controlled by three functions; the Carrier Detect (CD) input, the internal Transition Detector, and the Out of Lock (OOL) detector. The Transition Detector determines if RIN± contains enough transitions to be accurately recovered by the Receive PLL. The Out of Lock detector determines if RIN± is within the frequency range of the Receive PLL. When CD is HIGH and RIN± has sufficient transitions and is within the frequency range of the Receive PLL, the $\overline{LFI}$ output will be HIGH. If CD is at an ECL LOW or RIN± does not contain sufficient transitions or RIN± is outside the frequency range of the Receive PLL then the $\overline{LFI}$ output will be LOW. If CD is at a TTL LOW then the $\overline{LFI}$ output will only transition LOW when the frequency of RIN± is outside the range of the Receive PLL.
TSER±	Differential In	**Transmit Serial Data**. This line receiver port connects the transmit differential serial input data stream to the TOUT transmit buffers. Depending on the state of the $\overline{LOOP}$ pin, this input port can also be set up to supply the serial input data stream to the Receive PLL. These inputs can receive very low amplitude signals and are compatible with all PECL signalling levels. If the TSER± inputs are not being used, connect TSER+ to V_{CC} and TSER– to V_{SS}.
TOUT±	ECL Out	**Transmit Output**. These ECL 100K outputs (+5 V referenced) represent the buffered version of the Transmit data stream (TSER±). This Transmit path is used to take weak input signals and rebuffer them to drive low impedance copper media.
REFCLK±	Diff/TTL In	**Reference Clock**. This input is the clock frequency reference for the clock and data recovery Receive PLL. REFCLK is multiplied internally by eight and sets the approximate center frequency for the internal Receive PLL to track the incoming bit stream. This input is also multiplied by eight by the frequency multiplier Transmit PLL to produce the bit rate Transmit Clock (TCLK±). REFCLK can be connected to either a differential PECL or single-ended TTL frequency source. When either REFCLK+ or REFCLK– is at a TTL LOW, the opposite REFCLK signal becomes a TTL level input.
TCLK±	ECL Out	**Transmit Clock**. These ECL 100K outputs (+5 V referenced) provide the bit rate frequency source for external Transmit data processing devices. This output is synthesized by the Transmit PLL and is derived by multiplying the REFCLK frequency by eight. When this output is turned off, the entire Transmit PLL is powered down. All PECL outputs can be powered down by connecting both outputs to V_{CC} or leaving them both unconnected.
$\overline{LOOP}$	TTL In	**Loop Back Select**. This input is used to select the input data stream source that the Receive PLL uses for clock and data recovery. When the $\overline{LOOP}$ input is HIGH, the Receive input data stream (RIN±) is used for clock and data recovery. When $\overline{LOOP}$ is LOW, the Transmit input data stream (TSER±) is used by the Receive PLL for clock and data recovery.

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Pin Descriptions (continued)

Name	I/O	Description
MODE	3-Level In	**Frequency Mode Select**. This three-level input selects the frequency range for the clock and data recovery Receive PLL and the frequency multiplier Transmit PLL. When this input is held HIGH the two PLLs operate at the SONET (SDH) STS-3 (STM-1) line rate of 155.52 MHz. When this input is held LOW the two PLLs operate at the SONET STS-1 line rate of 51.84 MHz. The REFCLK± frequency in both operating modes is 1/8 the PLL operating frequency. When the MODE input is left floating or held at $V_{CC}/2$ the TSER± inputs substitute for the internal PLL VCO for use in factory testing.
V_{CC}		**Power**.
V_{SS}		**Ground**.

Description

The CY7B952 Serial SONET/SDH Transceiver (SST) is used in SONET/SDH and ATM applications to recover clock and data information from a 155.52-MHz or 51.84-MHz NRZ (Non Return to Zero) or NRZI (Non Return to Zero Invert on ones) serial data stream. This device also provides a bit-rate Transmit clock, from a byte rate source through the use of a frequency multiplier PLL, and differential data buffering for the Transmit side of the system. This device is compliant with relevant SONET/SDH specifications including OC-3 Bellcore GR-253-Core Issue2, December 1995, ANSI T1X1.6/91-022, and CCITT G958.

Operating Frequency

The SST operates at either of two frequency ranges. The MODE input selects which of the two frequency ranges the Transmit frequency multiplier PLL and the Receive clock and data recovery PLL will operate. The MODE input has three different functional selections. When MODE is connected to VCC, the highest operating range of the device is selected. A 19.44-MHz ±1% source must drive the REFCLK input and the two PLLs will multiply this rate by 8 to provide output clocks that operate at 155.52 MHz ±1%. When the MODE input is connected to ground (GND), the lowest operating range of the device is selected. A 6.48-MHz ±1% source must drive the REFCLK inputs and the two PLLs will multiply this rate by 8 to provide output clocks that operate at 51.84 MHz ±1%. When the MODE input is left unconnected or forced to approximately $V_{CC}/2$, the device enters Test mode.

Transmit Functions

The transmit section of the SST contains a PLL that takes a REFCLK input and multiplies it by 8 (REFCLK × 8) to produce a PECL (Pseudo ECL) differential output clock (TCLK±). The transmitter has two operating ranges that are selectable with the three-level MODE pin as explained above. The SST Transmit frequency multiplier PLL allows low-cost byte rate clock sources to be used to time the upstream serial data transmitter.

The REFCLK± input can be configured three ways. When both REFCLK+ and REFCLK– are connected to a differential 100K-compatible PECL source, the REFCLK input will behave as a differential PECL input. When either the REFCLK– or the REFCLK+ input is at a TTL LOW, the other REFCLK input becomes a TTL-level input allowing it to be connected to a low-cost TTL crystal oscillator. The REFCLK input structure, therefore, can be used as a differential PECL input, a single TTL input, or as a dual TTL clock multiplexing input.

The Transmit PECL differential input pair (TSER±) is buffered by the SST yielding the differential data outputs (TOUT±). These outputs can be used to directly drive transmission media such as Printed Circuit Board (PCB) traces, optical drivers, twisted pair, or coaxial cable.

Receive Functions

The primary function of the receiver is to recover clock (RCLK±) and data (RSER±) from the incoming differential PECL data stream (RIN±) without the need for external buffering. These built-in line receiver inputs, as well as the TSER± inputs mentioned above, have a wide common-mode range (2.5 V) and the ability to receive signals with as little as 50 mV differential voltage. They are compatible with all PECL signals and any copper media.

The clock recovery function is performed using an embedded PLL. The recovered clock is not only passed to the RCLK± outputs, but also used internally to sample the input serial stream in order to recover the data pattern. The Receive PLL uses the REFCLK input as a byte-rate reference. This input is multiplied by 8 (REFCLK × 8) and is used to improve PLL lock time and to provide a center frequency for operation in the absence of input data stream transitions. The receiver can recover clock and data in two different frequency ranges depending on the state of the three-level MODE pin as explained earlier. To insure accurate data and clock recovery, REFCLK×8 must be within 1000 ppm of the transmit bit rate. The standards, however, specify that the REFCLK × 8 frequency accuracy be within 20–100 ppm.

The FC± pins are used to connect an external phase locked loop damping capacitor and resistor. The capacitor should be a 1 µF ± 10% surface mount devices and the resistor should be a 301K ± 1% surface mount devices. To minimize noise, the capacitor and the resistor should be placed on the SST side of the printed circuit board as close to the FC± pins as possible.

The Receive PLL is compliant with the OC-3 Bellcore jitter generation, jitter transfer, and jitter tolerance specifications.

Carrier Detect (CD) and Link Fault Indicator ($\overline{\text{LFI}}$) Functions

The Link Fault Indicator ($\overline{\text{LFI}}$) output is a TTL-level output that indicates the status of the receiver. This output can be used by an external controller for Loss of Signal (LOS), Loss of Frame (LOF), or Out of Frame (OOF) indications. $\overline{\text{LFI}}$ is controlled by the Carrier Detect input, the internal Transitions Detector, and the PLL Out of Lock (OOL) circuitry.

The CD input may be driven by external circuitry that is monitoring the incoming data stream. Optical modules have CD

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outputs that indicate the presence of light on the optical fiber and some copper based systems use external threshold detection circuitry to monitor the incoming data stream. The CD input is a 100K PECL compatible signal that should be held HIGH when the incoming data stream is valid. When CD is pulled to a PECL LOW (≤2.5 V Max.), the LFI output will transition LOW and the Receiver PLL will align itself with the REFCLK×8 frequency and the recovered data outputs (RSER) will remain LOW regardless of the signal level on the Receive data-stream inputs (RIN).

In addition, the SST has a built-in transitions detector that also checks the quality of the incoming data stream. The absence of data transition can be caused by a broken transmission media, a broken transmitter, or a problem with the transmit or receive media coupling. The SST will detect a quiet link by counting the number of bit times that have passed without a data transition. A bit time is defined as the period of RCLK±. When 512 bit times have passed without a data transition on RIN±, LFI will transition LOW. The receiver will assume that the serial data stream is invalid and, instead of allowing the RCLK± frequency to wander in the absence of data, the PLL will lock to the REFCLK × 8 frequency. This will insure that RCLK± is as close to the correct link operating frequency as the REFCLK accuracy. LFI will be driven HIGH again and the receiver will recover clock and data from the incoming data stream when the transition detection circuitry determines that at least 64 transitions have been detected within 512 bit-times.

The Transition Detector can be turned off by pulling the CD input to a TTL LOW (≤0.8 V). When CD is pulled to a TTL LOW the LFI will only be driven LOW if the incoming data stream frequency is not within 1000 ppm of the REFCLK × 8 frequency. LFI LOW in this case will only indicate that the Receiver PLL is Out of Lock (OOL). When this pin is left unconnected, an internal pull-down resistor will pull this input to Ground.

Loop Back Testing

The TTL level $\overline{\text{LOOP}}$ pin is used to perform loop-back testing. When $\overline{\text{LOOP}}$ is asserted (held LOW) the Transmitter serial input (TSER±) is used by the Receiver PLL for clock and data recovery. This allows in-system testing to be performed on the entire device except for the differential Transmit drivers (TOUT±) and the differential Receiver inputs (RIN±). For example, an ATM controller can present ATM cells to the input of the ATM cell processor and check to see that these same cells are received. When the $\overline{\text{LOOP}}$ input is deasserted (held HIGH) the Receive PLL is once again connected to the Receiver serial inputs (RIN±).

The $\overline{\text{LOOP}}$ feature can also be used in applications where clock and data recovery are to be performed from either of two data streams. In these systems the $\overline{\text{LOOP}}$ pin is used to select whether the TSER± or the RIN± inputs are used by the Receive PLL for clock and data recovery.

SONET-compliant Testing

SONET jitter criteria for Bellcore-compliant are specified in three areas: Jitter transfer, jitter tolerance and jitter generation.

Jitter transfer and jitter tolerance measurements were done using sinusoidal jitter applied to the input signal at the maximum amplitude of the jitter tolerance mask for each specific jitter frequency as specified by the Bellcore GR-253-Core Issue 2, Dec 1995 - SONET Common Generic Criteria.

Power Down Modes

There are several power-down features on the SST. Any of the differential output drivers can be powered down by either tying both outputs to V_{CC} or by simply leaving them unconnected where internal pull-up resistors will force these outputs to V_{CC}. This will save approximately 4 mA per output pair in addition to the associated output current. If the TOUT± or ROUT± outputs are tied to V_{CC} or left unconnected, the Transmit buffer or Receive buffer path respectively will be turned off. If the TCLK± outputs are tied to V_{CC} or left unconnected, the entire Transmit PLL will be powered down.

By leaving both the RCLK± and RSER± outputs unconnected or tied to V_{CC}, the entire Receive PLL is turned off. Even though the Receive PLL may be turned off, the Link Fault Indicator (LFI) will still reflect the state of the Carrier Detect (CD) input. This feature can be used for aggressive power management.

Applications

The SST can provide clock and data recovery as well as output buffering for physical layer protocol engines such as those used in WAN SONET/SDH and ATM applications. The operating frequency of the 7B952 is centered around the SONET/SDH STS-1 rate of 51.84 MHz and the SONET/SDH STS-3/STM-1 rate of 155.52 MHz. This device can also be used in data mover, Local Area Network (LAN) applications that operate at these frequencies.

In an ATM system, the SST is used to recover clock and data from an input SONET/SDH serial data stream for subsequent chips to do serial to parallel conversion, SONET/SDH overhead processing, ATM cell processing, and switching. On the Transmit side, ATM cells coming out of a switching matrix goes through ATM cell processing, SONET/SDH overhead processing and parallel to serial conversion before passing to the SST which buffers the data stream and drive the transmission media.

In a more generic telecommunications system (SONET/SDH Overhead Processing Application on page 3), the SST is used to provide clock and data recovery for a pure SONET/SDH system such as a SONET/SDH switch. The SST provides the recovered clock and data to a serial to parallel converter and SONET/SDH Transport Overhead Processor such as the PMC-Sierra PM5343 STXC. The parallel data is then passed to a SONET/SDH Path Overhead Processor such as the PMC-Sierra PM5344 SPTX.

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Maximum Ratings

Exceeding maximum ratings [1] may shorten the useful life of the device. These user guidelines are not tested.

Storage Temperature ..... –65 °C to +150 °C

Ambient Temperature with Power Applied ..... –55 °C to +125 °C

Supply Voltage to Ground Potential ..... –0.5 V to +7.0 V

DC Input Voltage ..... –0.5 V to +7.0 V

Output Current into TTL Outputs (LOW) ..... 30 mA

Output Current into ECL Outputs (HIGH) ..... –50 mA

Static Discharge Voltage (per MIL-STD-883, Method 3015) ..... >2001 V

Latch-up Current ..... >200 mA

Operating Range

Range	Ambient Temperature [2]	V_{CC}
Commercial	0 °C to +70 °C	5 V ± 10%

Electrical Characteristics

Over the Operating Range

Parameter	Description		Test Condition	Min	Max	Unit
TTL-compatible Input Pins (LOOP, REFCLK+, REFCLK–)						
V_{IHT}	Input HIGH Voltage			2.0	V_{CC}	V
V_{ILT}	Input LOW Voltage			–0.5	0.8	V
I_{IHT}	Input HIGH Current	REFCLK	$V_{IN} = V_{CC}$	+0.5	+200	µA
I_{IHT}	Input HIGH Current	LOOP	$V_{IN} = V_{CC}$	–10	+10	µA
I_{ILT}	Input LOW Current	REFCLK	V_{IN} = 0.0 V	–50	+50	µA
I_{ILT}	Input LOW Current	LOOP	V_{IN} = 0.0 V	–500	–	µA
TTL Compatible Output Pins (LFI)						
V_{OHT}	Output HIGH Voltage		I_{OH} = –2 mA	2.4	–	V
V_{OLT}	Output LOW Voltage		I_{OL} = 4 mA	–	0.45	V
I_{OST}	Output Short Circuit Current		V_{OUT} = 0 V [3]	–15	–90	mA
ECL Compatible Input Pins (REFCLK±, CD, TSER±, RIN±)						
I_{IHE}	ECL Input HIGH Current	REFCLK/CD	$V_{IN} = V_{IHE(MAX)}$	–	+250	µA
		TSER/RIN	$V_{IN} = V_{IHE(MAX)}$	–	+750	µA
I_{ILE} [4]	ECL Input LOW Current	REFCLK/CD	$V_{IN} = V_{ILE(MIN)}$	+0.5	–	µA
		TSER/RIN	$V_{IN} = V_{ILE(MIN)}$	–200	–	µA
V_{IDIFF}	Input Differential Voltage	TSER/RIN		50	1200	mV
		REFCLK		100	1200	mV
V_{IHE}	Input High Voltage	TSER/RIN		–	V_{CC}	V
		REFCLK		3.0	V_{CC}	V
		CD		V_{CC} – 1.165	V_{CC}	V
V_{ILE}	Input LOW Voltage	TSER/RIN		2.0	–	V
		REFCLK		2.5	–	V
		CD (ECL)		2.5	V_{CC} – 1.475	V
		CD (Disable)		–0.5	0.8	V

Notes
1. Single Power Supply: The voltage on any input or I/O pin cannot exceed the power pin during power-up.
2. T_A is the “instant on” case temperature.
3. Tested one output at a time, output shorted for less than one second, less than 10% duty cycle.
4. Input currents are always positive at all voltages above $V_{CC}/2$.

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Electrical Characteristics (continued)

Over the Operating Range

Parameter	Description		Test Condition	Min	Max	Unit
ECL Compatible Output Pins (ROUT±, RCLK±, RSER±, TOUT±, TCLK±)						
V_{OHE}	ECL Output HIGH Voltage			V_{CC} – 1.03	V_{CC} – 0.83	V
V_{OLE}	ECL Output LOW Voltage		T > 0 °C	V_{CC} – 1.86	V_{CC} – 1.62	V
V_{ODIFF}	Output Differential Voltage			0.6	–	V
Three-Level Input Pins (MODE)						
V_{IHH}	Three-Level Input HIGH			V_{CC} – 0.75	V_{CC}	V
V_{IMM}	Three-Level Input MID			$V_{CC}/2$ – 0.5	$V_{CC}/2$ + 0.5	V
V_{ILL}	Three-Level Input LOW			0.0	0.75	V
Operating Current [5]						
I_{CCS}	Static Operating Current			–	38	mA
I_{CCR}	Receiver Operating Current			–	50	mA
I_{CCT}	Transmitter Operating Current			–	13	mA
I_{CCE}	ECL Pair Operating Current			–	7.0	mA
I_{CC5}	Additional Current at 51.84 MHz			–	7.0	mA
I_{CCO}	Additional Current $\overline{LFI}$ = LOW			–	3	mA

Note

5. Total Receiver operating current (assuming that the Transmitter is not activated) can be found by adding I_{CCS} + I_{CCR} + x × I_{CCE}; where x is 2 if the ROUT± outputs are not activated and 3 if they are activated. Total Transmitter operating current (assuming that the Receiver is not activated) can be found by adding I_{CCS} + I_{CCT} + x × I_{CCE}; where x is 1 if the TOUT± outputs are not activated and 2 if they are activated. Total device power (assuming that the Transmitter and the Receiver are activated) can be found by adding I_{CCS} + I_{CCR} + I_{CCT} + x × I_{CCE}; where x represents the number of ECL output pairs activated.

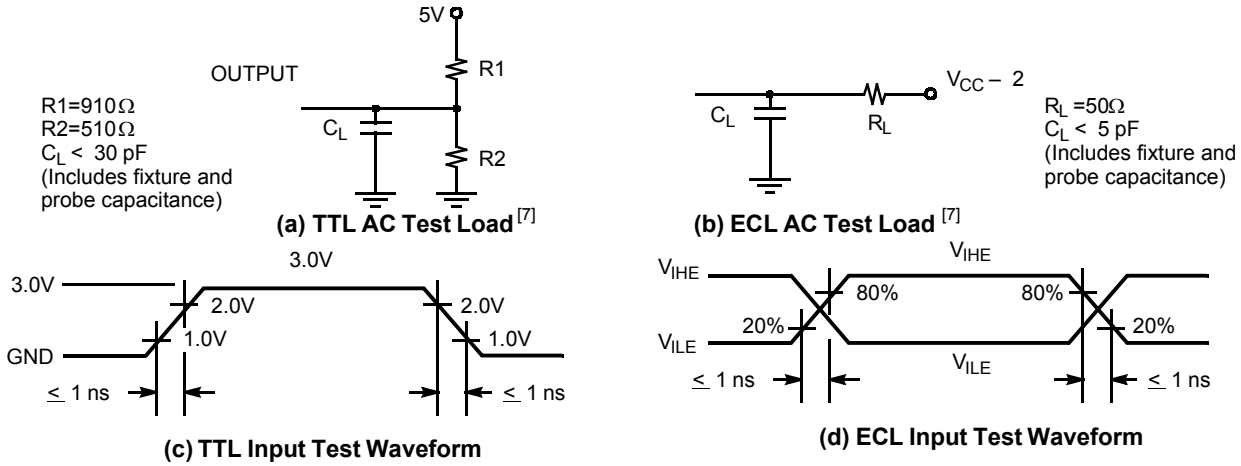
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Capacitance

Parameter [6]	Description	Test Conditions	Max	Unit
C_{IN}	Input Capacitance	T_A = 25 °C, f_0 = 1 MHz, V_{CC} = 5.0 V	10	pF

AC Test Loads and Waveforms

Figure 2. AC Test Loads and Waveforms



Notes
6. Tested initially and after any design or process changes that may affect these parameters.
7. Cypress uses constant current (ATE) load configurations and forcing functions. This figure is for reference only.

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Switching Characteristics

Over the Operating Range

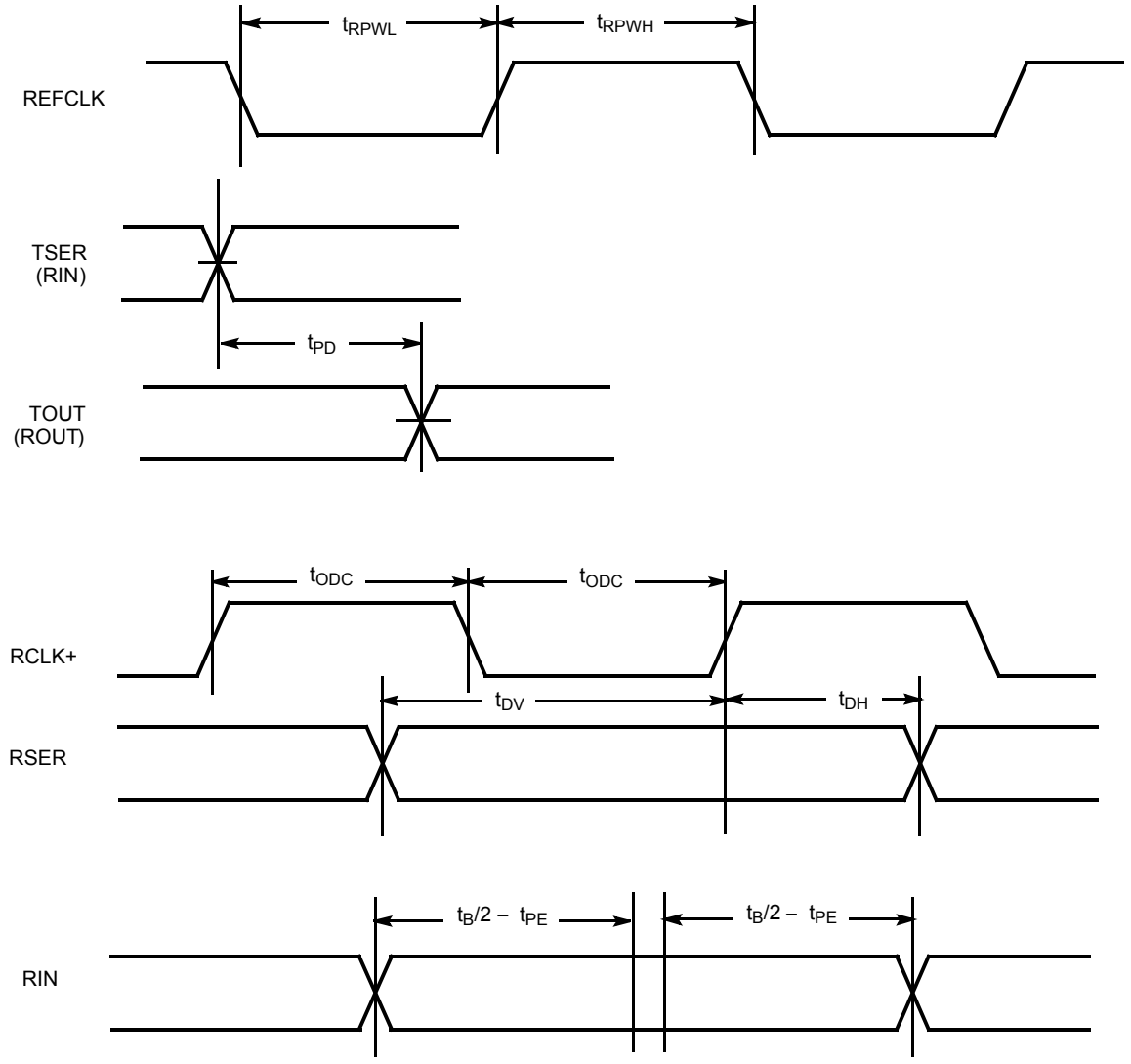
Parameter	Description		Min	Max	Unit
f_{REF}	Reference Frequency	MODE = LOW	6.41	6.55	MHz
		MODE = HIGH	19.24	19.64	MHz
f_B	Bit Time [8]	MODE = LOW	19.5	19.1	ns
		MODE = HIGH	6.50	6.40	ns
t_{ODC}	Output Duty Cycle (TCLK±, RCLK±) [9]		48	52	%
t_{RF}	Output Rise/Fall Time [9]		0.4	1.2	ns
t_{LOCK}	PLL Lock Time (RIN transition density 25%) [10]		–	3	ms
t_{RPWH}	REFCLK Pulse Width HIGH		10	–	ns
t_{RPWL}	REFCLK Pulse Width LOW		10	–	ns
t_{DV}	Data Valid		3	–	ns
t_{DH}	Data Hold		1	–	ns
t_{PD}	Propagation Delay (RIN to ROUT, TSER to TOUT) [11]		–	10	ns
Jitter Generation	Jitter Generation of RX PLL		–	0.01	UIrms
f_{-3dB}	–3 dB Gain Bandwidth of RX PLL (Jitter Transfer Bandwidth)	At 155 MHz	–	130	kHz
f_{-3dB}	–3 dB Gain Bandwidth of RX PLL (Jitter Transfer Bandwidth)	At 52 MHz	–	40	kHz
Gpeak	Maximum Peaking of RX PLL[12]		–	0.1	dB

Notes

8. f_B is calculated a $1/(f_{REF\times 8})$.
9. Tested initially and after any design or process changes that may affect these parameters.
10. t_{LOCK} is the time needed for transitioning from lock to REFCLK × 8 to lock to data.
11. The ECL switching threshold is the differential zero crossing (i.e., the place where + and – signals cross).
12. Maximum Peaking is measured using a maximum of 1.2 ns peak to peak duty cycle distortion for RIN± and applying sinusoidal jitter to the input signal at the maximum amplitude of the jitter tolerance mask for each specific jitter frequency as specified by the Bellcore GR-253-Core issue 2, Dec 1995 - SONET Common Generic Criteria for OC-3.

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Switching Waveforms for the CY7B952 SONET/SDH Serial Transceiver

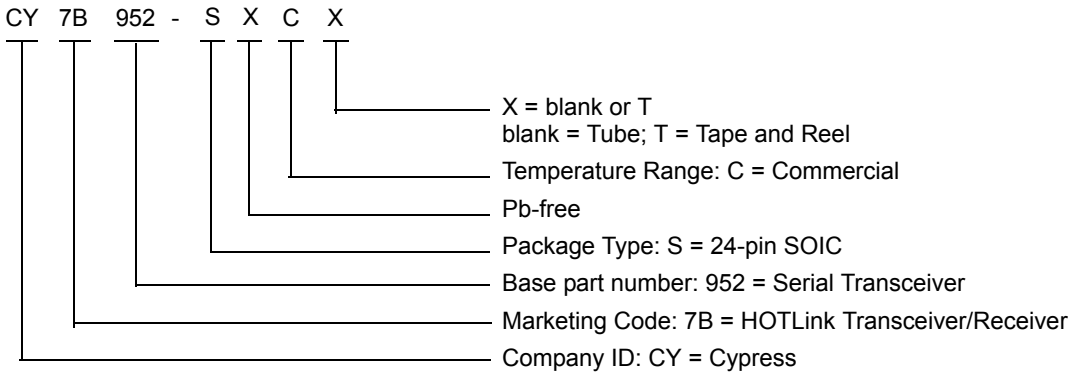


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Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
25	CY7B952-SXC	S13	24-pin (300-Mil) Molded SOIC	Commercial
	CY7B952-SXCT	S13	24-pin (300-Mil) Molded SOIC	Commercial

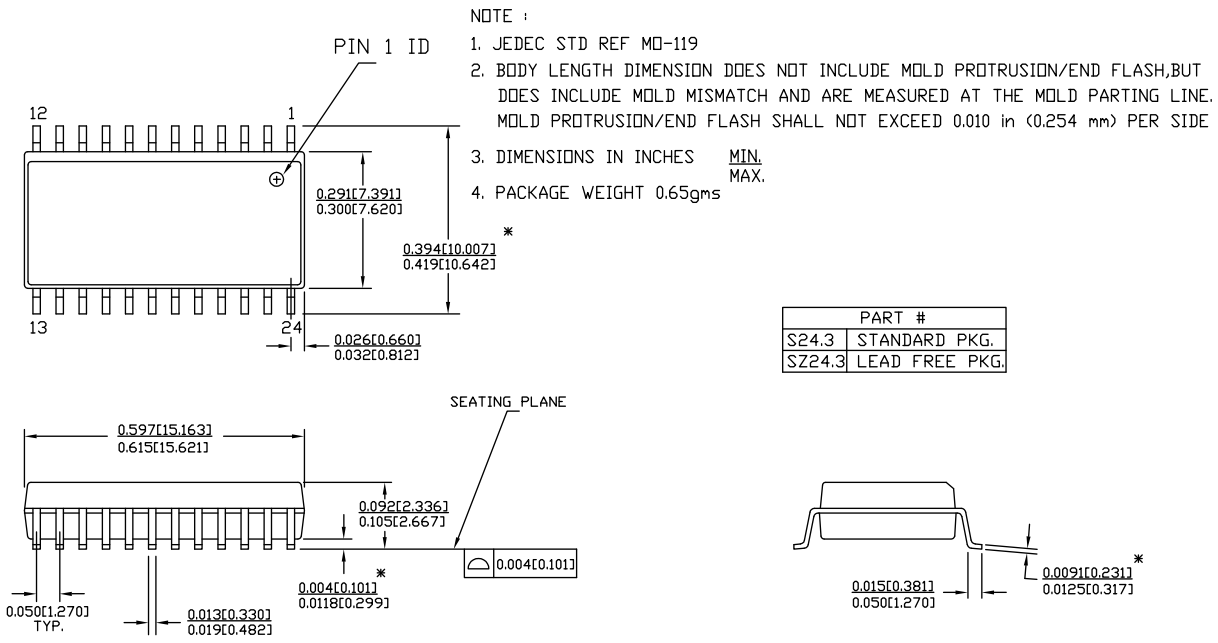
Ordering Code Definitions



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Package Diagram

Figure 3. 24-pin SOIC (0.615 × 0.300 × 0.0932 Inches) Package Outline, 51-85025



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Acronyms

Acronym	Description
AC	alternating current
CD	carrier detect
DC	direct current
ECL	emitter coupled logic
I/O	input/output
LFI	link fault indicator
PCB	printed circuit board
PECL	positive emitter coupled logic
PLL	phase locked loop
SOIC	small-outline integrated circuit
TTL	transistor-transistor logic
VCO	voltage controlled oscillator

Document Conventions

Units of Measure

Symbol	Unit of Measure
dB	decibel
°C	degree Celsius
kHz	kilohertz
MHz	megahertz
µA	microampere
µF	microfarad
mA	milliampere
mV	millivolt
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
ppm	parts per million
V	volt

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Document History Page

Document Title: CY7B952, SST™ SONET/SDH Serial Transceiver Document Number: 38-02018				
Rev.	**ECN.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	105981	03/28/01	SZV	Change from Spec. number: 38-00502 to 38-02018
*A	122206	12/28/02	RBI	Add power up requirements to maximum ratings information.
*B	283371	See ECN	BCD	Removed Preliminary from the data sheet
*C	2896206	03/19/10	CGX	Removed obsolete part and added the following parts: CY7B952-SXC and CY7B952-SXCT Updated package diagram
*D	3092301	11/22/10	SAAC	Ordering Information update. Added Ordering Code Definitions.
*E	3434099	11/09/2011	SAAC	Updated Package Diagram. Added Acronyms and Units of Measure. Updated in new template.

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