

SX1242 - Low Cost Integrated Transmitter IC

344.940 MHz RF Transmitter

GENERAL DESCRIPTION

The SX1242 is an ultra-low-cost, fully integrated standalone OOK transmitter suitable for operation at 344.940 MHz

The SX1242 is designed for use without the requirement for configuration via an MCU.

The SX1242 offers integrated radio performance with cost efficiency and is suited for operation in North America (FCC part 15.231).

ORDERING INFORMATION

Part Number	Temperature Range	Qty. per Reel	Package
SX1242ISETRT	-40 °C to +85 °C	2500	SOIC8-EP

Pb-Free, Halogen Free, RoHS/WEEE compliant product.

APPLICATIONS

- ◆ Low-Cost Consumer Electronic Applications
- ◆ Remote Keyless Entry (RKE)
- ◆ Remote Control / Security Systems
- ◆ Audio Accessories
- ◆ Process and building / home control

KEY PRODUCT FEATURES

- ◆ +12 dBm Output Power
- ◆ 344.940 MHz Operation
- ◆ OOK Bit Rates up to 10 kbps
- ◆ Pre-Configured Modes for Operation without MCU
- ◆ 1.8 to 3.7 V Supply Range
- ◆ Low BOM Fully Integrated TX

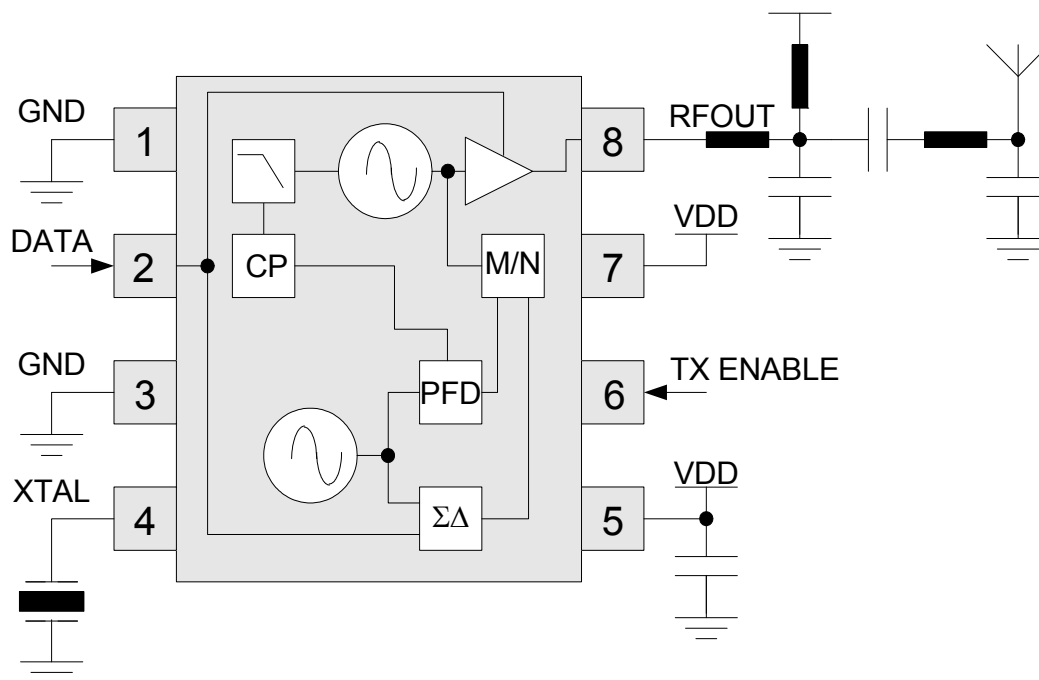


Table of contents

Section	Page
1. General Description	3
1.1. Pin Diagram	3
1.2. Marking Diagram.....	4
1.3. Pin Description	4
2. Electrical Characteristics	5
2.1. ESD Notice	5
2.2. Absolute Maximum Ratings	5
2.3. Operating Range.....	5
2.4. Electrical Specifications	6
3. Circuit Description.....	7
4. Application Information	9
4.1. Crystal Specification	9
4.2. Reference Design Schematic	9
4.3. Reference Design PCB Layout	10
4.4. Reference Design BOM	10
5. Packaging Information	11
5.1. Package Outline Drawing	11
5.2. Land Pattern	11
5.3. Thermal Impedance	12
5.4. Tape & Reel Specification.....	12
6. Revision History.....	13

This product datasheet contains a detailed description of the SX1242 performance and functionality.

1. General Description

The SX1242 is a fully-integrated multi-band, single chip transmitter IC capable of OOK modulation of an input data stream. The SX1242 is configured, by default, to operate without a microcontroller at a pre-configured RF setting of 344.940 MHz.

Another key feature of the SX1242 is its low current consumption in transmit and sleep modes and its wide voltage operating range from 1.8 V to 3.7 V. This makes the SX1242 suitable for low-cost battery chemistries or energy harvesting applications.

The internal architecture of the SX1242 is shown in Figure 1. The SX1242 comprises a low-consumption PLL and power amplifier. OOK Modulation is performed via ramping of the PA reference DAC.

The SX1242 is designed for use with a variety of low-cost antenna technologies including PCB-etched loop or electrically-short stub.

Further application information may be found in Section 4.

1.1. Pin Diagram

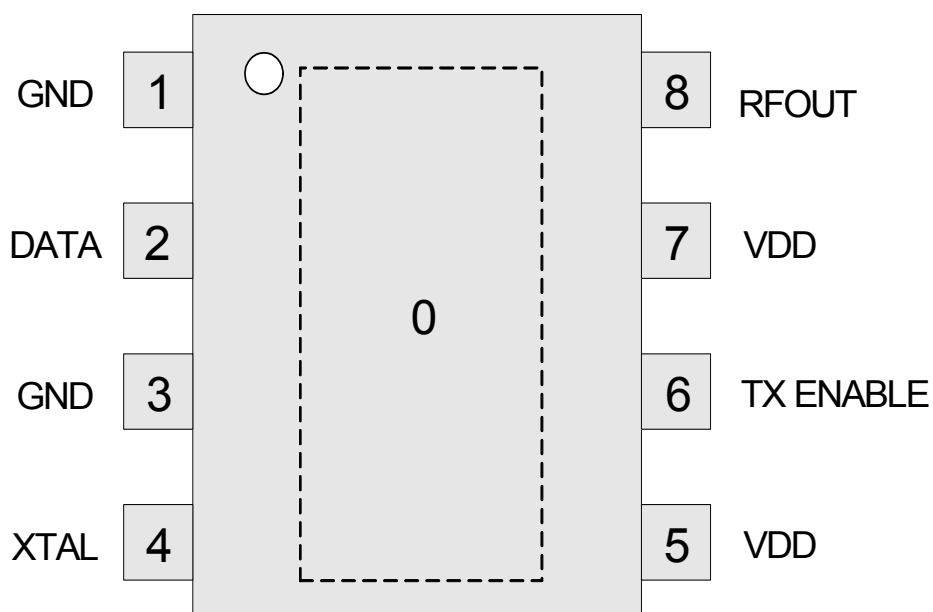


Figure 1. Pinouts, Top View

1.2. Marking Diagram

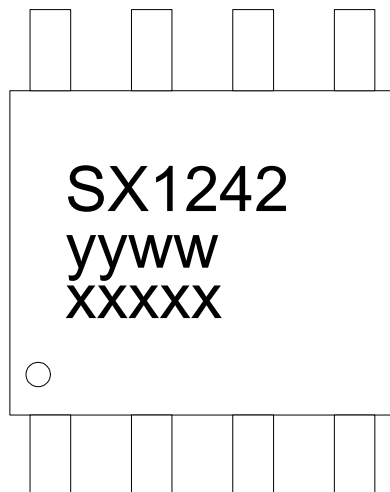


Figure 2. Marking Diagram

Notes:

yyww refers to the date code

xxxxx refers to lot numbers

1.3. Pin Description

Table 1 SX1242 Pinout Description

Number	Name	Type	Function
0	GND	I	Exposed Pad, Ground
1	GND	I	Ground
2	DATA	I	Transmit Data
3	GND	I	Ground
4	XTAL	I/O	Reference Crystal
5	VDD	I	Power Supply, 1.8 V to 3.7 V
6	TX ENABLE	I	Control Pin for Transmitter
7	VDD	I	Power Supply, 1.8 V to 3.7 V
8	RFOUT	O	Transmitter RF Output

2. Electrical Characteristics

2.1. ESD Notice

The SX1242 is a high performance radio frequency device, and satisfies Class 2 of the JEDEC standard JESD22-A114-B (human body model) on all pins.

It should thus be handled with all necessary ESD precautions to avoid any permanent damage.



2.2. Absolute Maximum Ratings

Stresses above the values listed below may cause permanent device failure. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Table 2 Absolute Maximum Ratings

Symbol	Description	Min	Max	Unit
VDDmr	Supply Voltage	-0.5	3.9	V
Tmr	Temperature	-55	+115	° C
Tjunc	Junction Temperature	-55	+125	° C
Tstor	Storage Temperature	-55	150	° C

2.3. Operating Range

Operating ranges define the limits for functional operation and the parametric characteristics of the device as described in this section. Functionality outside these limits is not implied.

Table 3 Operating Range

Symbol	Description	Min	Max	Unit
VDDop	Supply voltage	1.8	3.7	V
Top	Operational temperature range	-40	85	° C
Clop	Load capacitance on digital ports	-	25	pF

2.4. Electrical Specifications

The table below gives the electrical specifications of the transmitter under the following conditions: Supply voltage = 3.3 V, temperature = 25 °C, f_{XOSC} = 26 MHz, f_{RF} = 344.94 MHz, bit rate = 5 kbit/s and output power = +12 dBm terminated in a matched 50 ohm impedance, unless otherwise specified.

Table 4 Transmitter Specifications

Symbol	Description	Conditions	Min	Typ	Max	Unit
Current Consumption						
IDDSL	Supply current in sleep mode		-	0.5	1	µA
IDDT	Supply current in transmit mode with appropriate external matching.	Logic "1" or "Mark" frequency transmitted*	-	22	-	mA
RF and Baseband Specifications						
BRO	Bit rate, OOK	Permissible range	0.5	-	10	kbps
OOK_B	OOK modulation depth		-	50	-	dB
RFOP	RF output power into 50 ohms	Optimized matching network	9	12	-	dBm
DRFOPV	Variation in RF output power with supply voltage	2.5 V to 3.3 V 1.8 V to 3.7 V	- -	- -	3 7	dB dB
PHN	Transmitter phase noise	100 kHz Offset from carrier	-	-	-76	dBc/Hz
FCN	Carrier frequency		-	344.94	-	MHz
FXOSC	Crystal Oscillator Frequency		26	26	26	MHz
DFXOSC	Frequency Variation of the Oscillator Circuit	No crystal contribution	-	-	+/-25	ppm
Timing Specifications						
TS_TR	Time from Sleep to Tx mode		-	-	2	ms
RAMP	PA Ramp up and down time**		-	20	-	us

* Logic "1" transmission indicated by transmission of carrier frequency at power level RFOP.

** Ramp-up time of the internal regulator turning the PA on. The typical 10% - 90% power ramp-up time is 10us

3. Circuit Description

The SX1242 comprises a low-consumption fractional-N Sigma-Delta type PLL and power amplifier.

A simplified block diagram of the internal architecture and application schematic is illustrated below in Figure 3

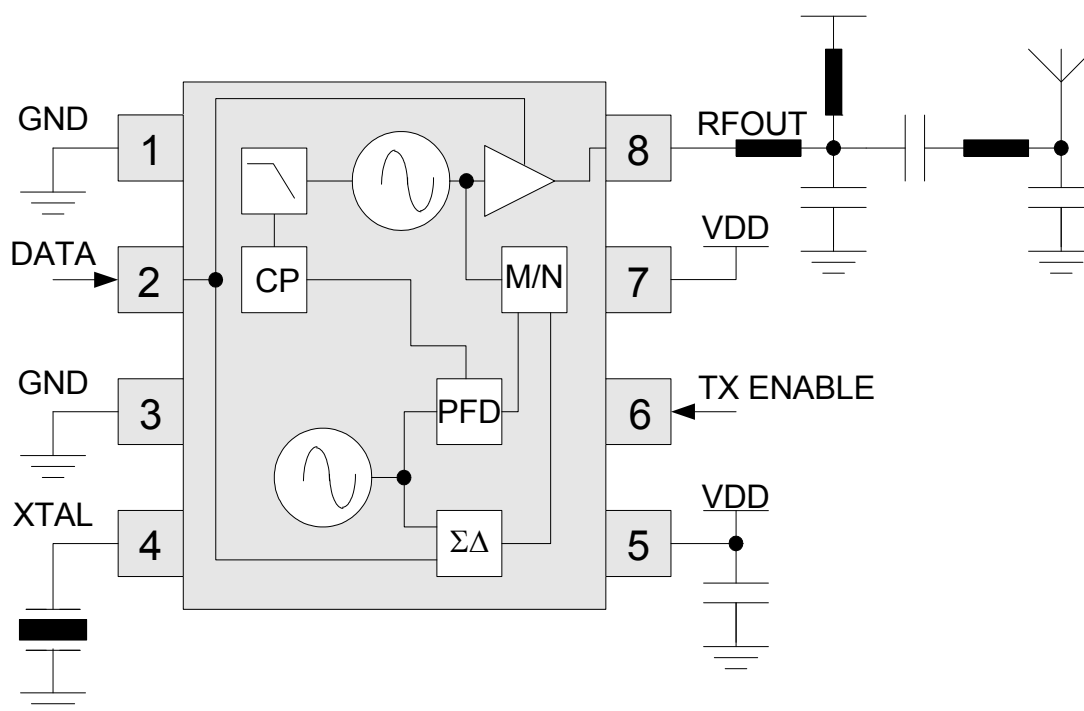


Figure 3. SX1242 Simplified Block Diagram and Application Schematic

3.1. PLL

The VCO operates at twice the RF channel frequency and is derived from a 26 MHz crystal oscillator reference

3.2. Transmitter

The Power Amplifier (PA) is connected to the RFOUT pin and delivers 12 dBm in a 50 ohm load. The bit stream to be transmitted over the air is sent to the chip via the pin DATA. During modulation, the rising and falling transitions are smoothed with a ramp-up/ramp-down time of typically 20 μ s via the PA reference DAC.

3.3. SX1242 Operating Modes

The SX1242 operating modes are defined by the status of the pin TX ENABLE and are documented in Table 5.

Table 5 SX1242 Operating Modes

TX Enable Status	Mode	Enabled Blocks
0 (GND)	Sleep	All blocks are off
1 (VDD)	Transmit	The blocks are switched on according to a predefined sequence and the data is transmitted once the sequence is completed

The behavior of the SX1242 is illustrated in the timing diagram below:

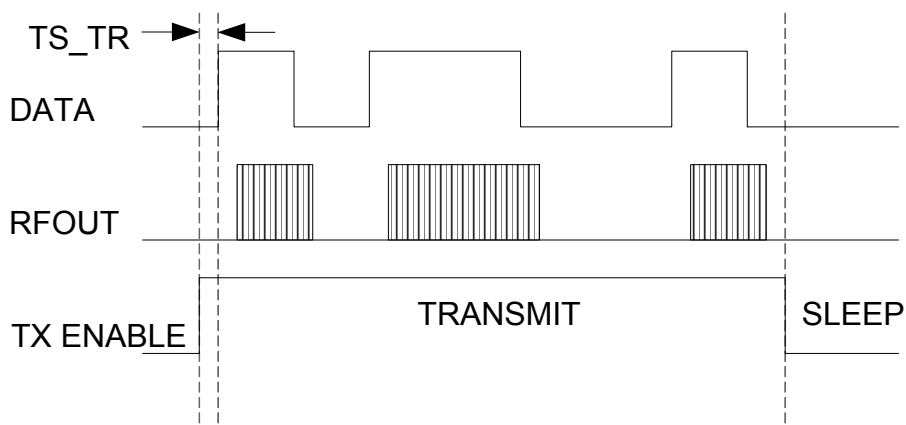


Figure 4. SX1242 Timing Diagram(Not to scale)

4. Application Information

4.1. Crystal Specification

The SX1242 is designed to operate with a low-cost 26 MHz crystal. The recommended crystal specification is tabulated below in Table 6.

Table 6 *SX1242 Quartz Crystal Reference Oscillator Specification*

Symbol	Description	Conditions	Min	Typ	Max	Unit
FXOSC	Crystal Frequency		26	26	26	MHz
LM	Crystal Motional Inductance		-	12.655	-	mH
CM	Crystal Motional Capacitance		-	2.962	-	fF
RS	Crystal Serial Resistance		-	20	100	Ohms
C0	Crystal Shunt Capacitance		-	1.0	7.0	pF
CL	Load Capacitance		-	15	-	pF

4.2. Reference Design Schematic

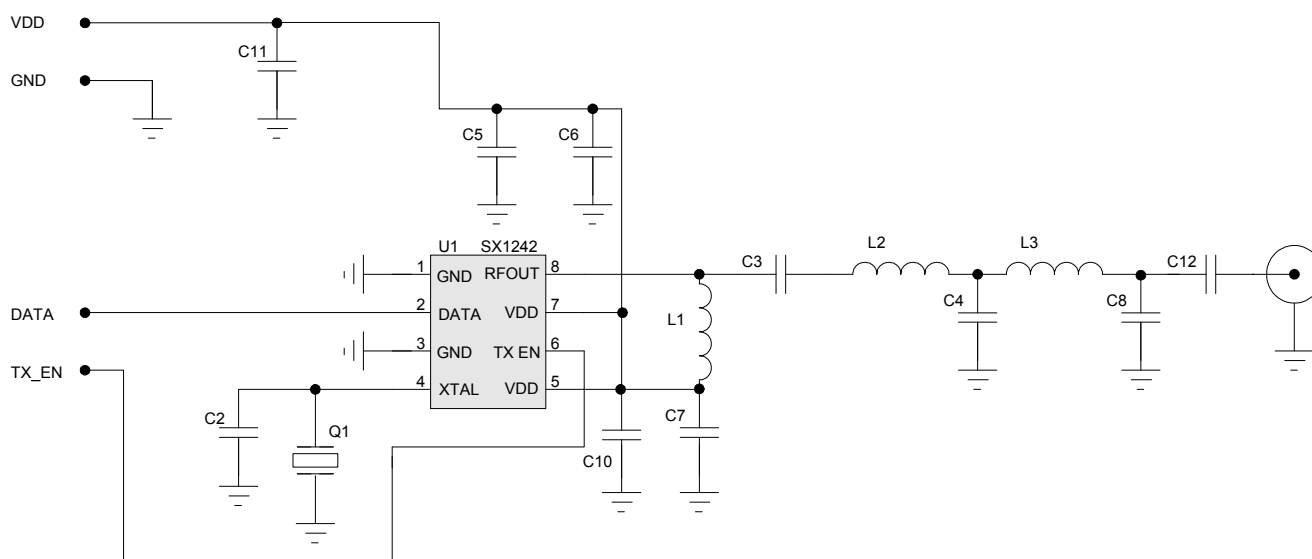


Figure 5. Application Module Schematic

4.3. Reference Design PCB Layout

The SX1242 reference design PCB layout is illustrated below:

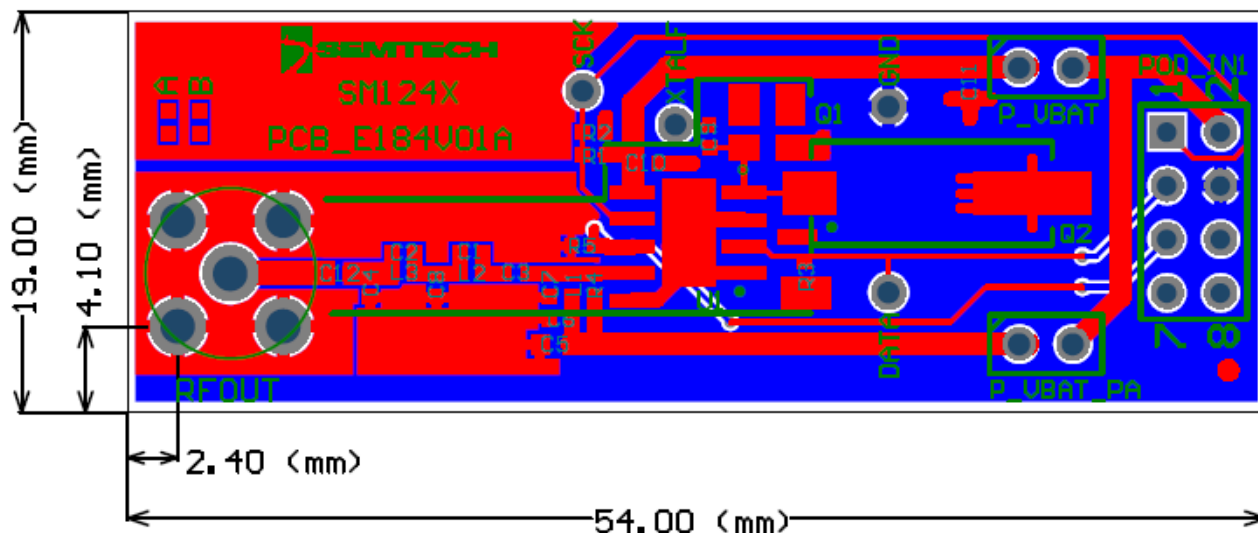


Figure 6. Reference Design PCB Layout

4.4. Reference Design BOM

The following table summarizes the reference design BOM:

Table 7 Reference Design BOM

RefDes	MPN	Package	Value	Qty	Description
U1	SX1242ISETRT	SO8	SX1242	1	RF transmitter IC
Q1	-	HC49	26 MHz	1	Crystal 26 MHz CL= 15 pF
C3	-	0402	100pF	1	Capacitor NPO (+/-5%)
C4	-	0402	12pF	1	Capacitor NPO (+/-5%)
C5	-	0402	100nF	1	Capacitor X7R (+/-5%)
C6	-	0402	100pF	1	Capacitor NPO (+/-5%)
C7	-	0402	4.7pF	1	Capacitor NPO (+/-0.25pF)
C8	-	0402	12pF	1	Capacitor NPO (+/-5%)
C9	-	0402	2.2pF	1	Capacitor NPO (+/-0.25pF)
C10	-	0402	100nF	1	Capacitor X7R (+/-5%)
C11	-	0402	1uF	1	Capacitor X5R (+/-5%)
C12	-	0402	Zero ohm	1	Resistor Zero Ohm
L1	LQG15- or equivalent	0402	120nH	1	Multilayer chip inductor (+/-5%)
L2	LQG15- or equivalent	0402	39nH	1	Multilayer chip inductor (+/-5%)
L3	LQG15- or equivalent	0402	22n	1	Multilayer chip inductor (+/-5%)

5. Packaging Information

The SX1242 is delivered in an SOIC package with 8 leads and an exposed pad. See details below.

5.1. Package Outline Drawing

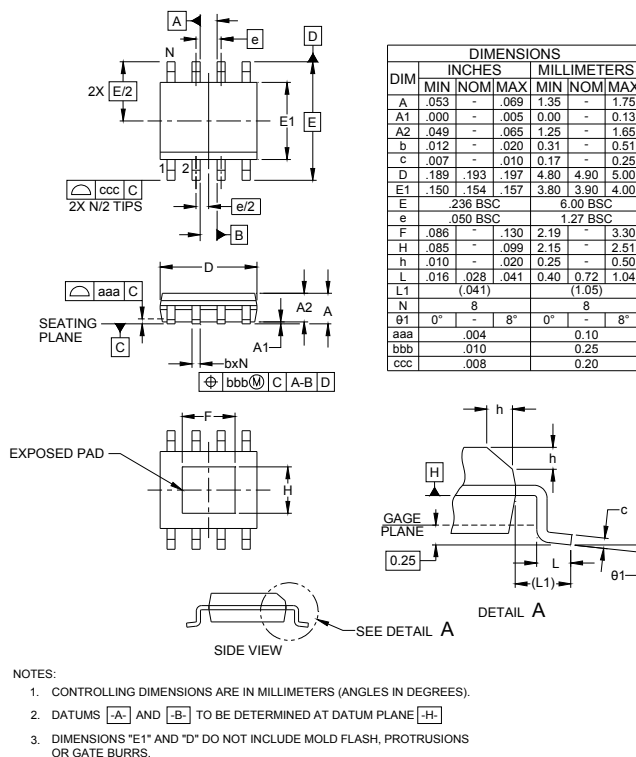


Figure 7. Package Outline Drawing

5.2. Land Pattern

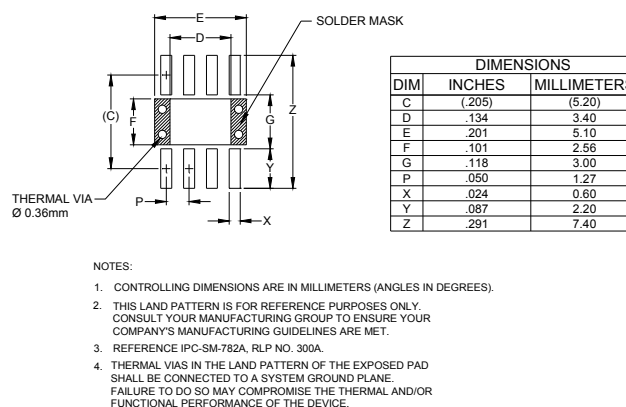
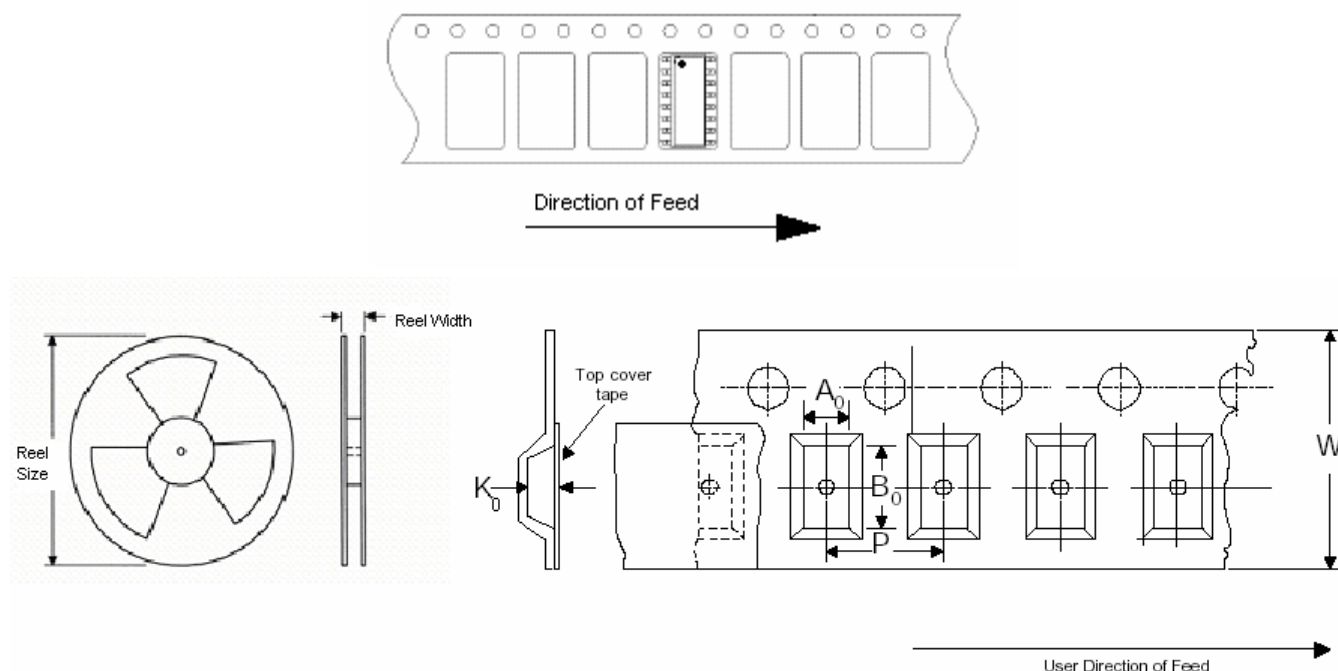


Figure 8. Land Pattern

5.3. Thermal Impedance

The thermal impedance of this package is: **$\Theta_{ja} = 36^{\circ} \text{C/W typ.}$** , calculated from a package in still air, on a 4-layer FR4 PCB, as per the Jedec standard.

5.4. Tape & Reel Specification



Carrier Tape				Reel		Min. Trailer Length	Min. Leader Length	QTY per	Unit
Tape Width (W)	Pocket Pitch (P)	A ₀ / B ₀	K ₀	Reel Size	Reel Width				
12 +/-0.30	8 +/-0.10	6.5 / 5.4 +/-0.30	2.00 +/-0.15	330.2	12.4	400	400	2500	mm

Figure 9. Tape & Reel Specification

Note Single Sprocket Holes

6. Revision History

Table 8 Revision History

Revision	Date	Comment
1	November 2010	First FINAL datasheet version
2	March 2011	Modified Application Schematic (Figure 5)

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