

# General Purpose CMOS Logic IC

## 8bit Static Shift Resister

**BU4021BF**

### General Description

BU4021BF is an 8bit static shift resister. It consists of eight resister stages and each register has an parallel input. A serial input/serial output function or a parallel input/serial output function can be selected by a parallel/serial input selection pin (P/S).

### Features

- Low Power Consumption
- Wide Operating Supply Voltage Range
- High Input Impedance
- High Fan Out
- 2 L-TTL Inputs or 1 LS-TTL Input can be directly driven

### Key Specifications

- Operating Supply Voltage Range: +3V to +16V
- Input Voltage Range: 0V to  $V_{DD}$
- Operating Temperature Range: -40°C to +85°C

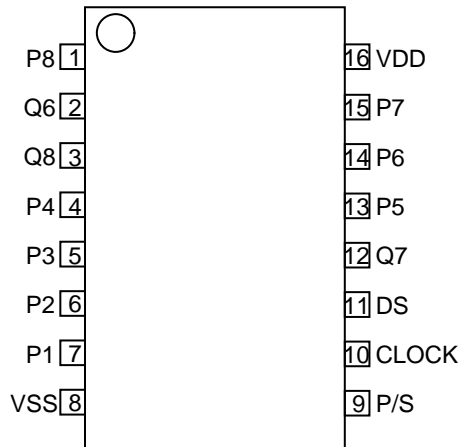
**Packages**  
SOP16

W(Typ) x D(Typ) x H(Max)  
10.00mm x 6.20mm x 1.71mm



### Pin Configurations

(Top View)



### Truth Table

#### Serial Input—Serial Output

Input					Output	
CLOCK	P/S	P1	$P_n$	DS	Q1	$Q_n$
	L	X	X	L	L	$Q_{n-1}$
	L	X	X	H	H	$Q_{n-1}$
	L	X	X	X	No Change	

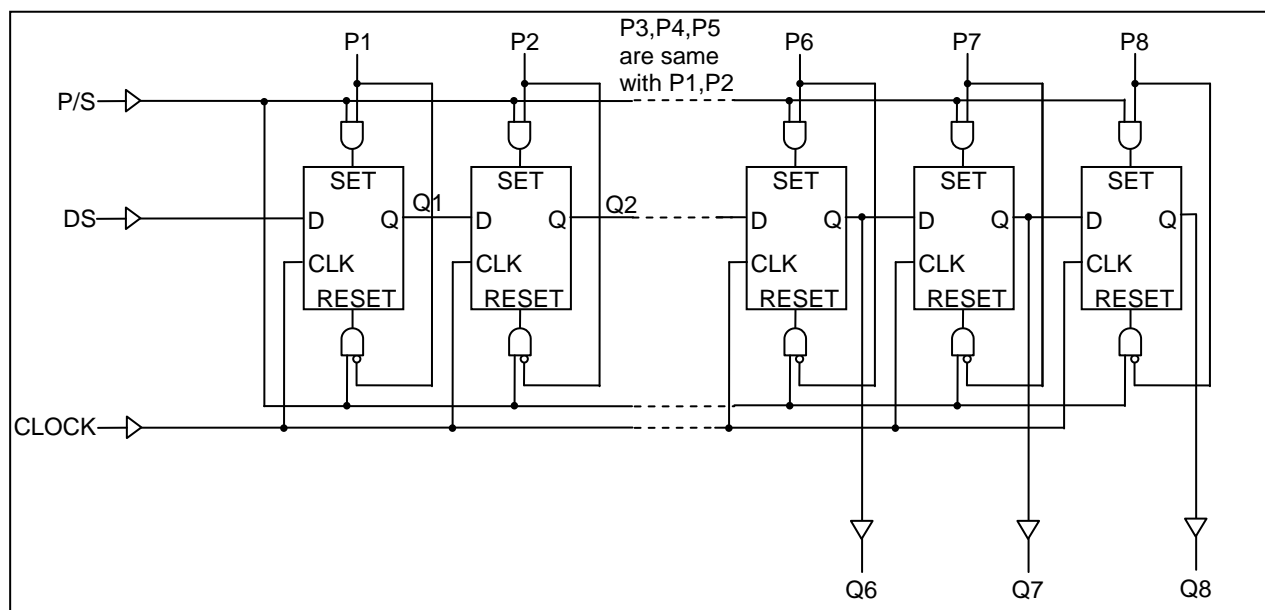
#### Parallel Input—Serial Output

Input					Output	
CLOCK	P/S	P1	$P_n$	DS	Q1	$Q_n$
X	H	L	L	X	L	L
X	H	L	H	X	L	H
X	H	H	L	X	H	L
X	H	H	H	X	H	H

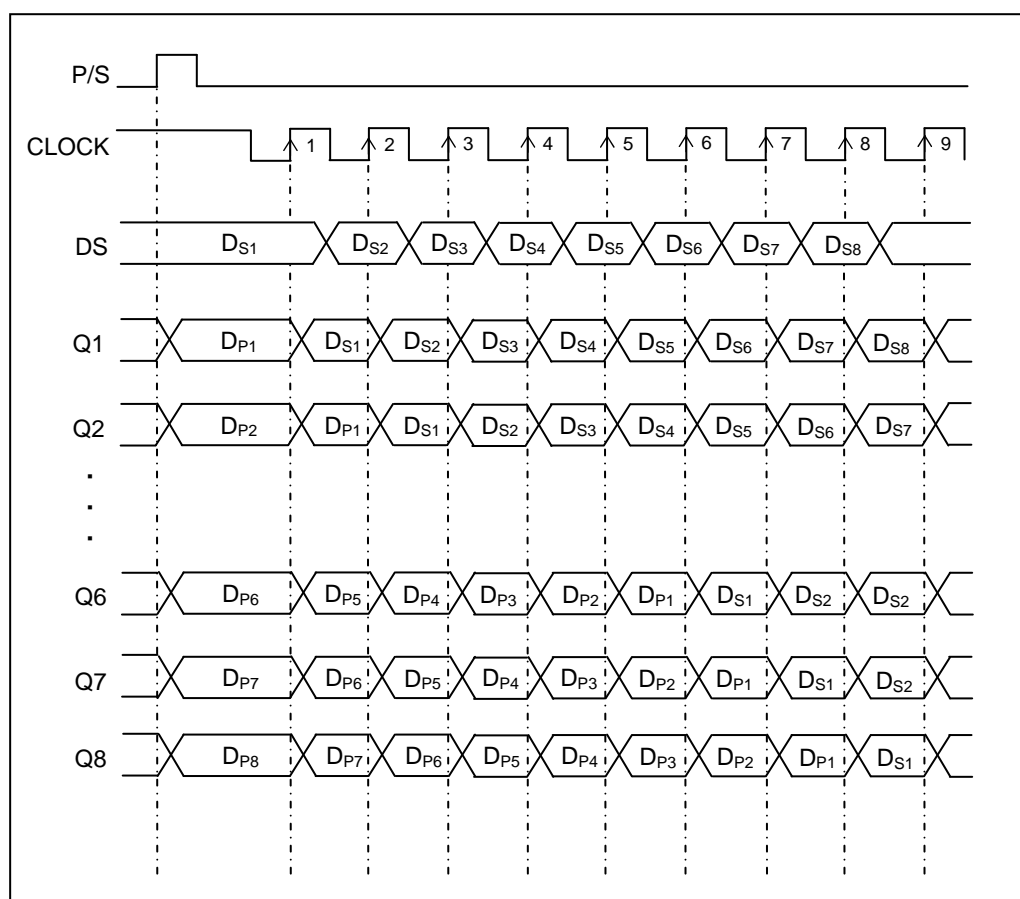
X: Don't Care

$Q_n$ : Q6, Q7, Q8 are outside of IC

## Logic Diagram



## Timing Chart



## Pin Descriptions

Pin No.	Pin Name	I/O	Function
1	P8	I	Parallel data input 8
2	Q6	O	Output 6
3	Q8	O	Output 8
4	P4	I	Parallel data input 4
5	P3	I	Parallel data input 3
6	P2	I	Parallel data input 2
7	P1	I	Parallel data input 1
8	VSS	—	Ground
9	P/S	I	Parallel/serial input selection
10	CLOCK	I	Clock input
11	DS	I	Serial data input
12	Q7	O	Output 7
13	P5	I	Parallel data input 5
14	P6	I	Parallel data input 6
15	P7	I	Parallel data input 7
16	VDD	—	Power supply

## Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply Voltage	$V_{DD}$	-0.3 to +18.0	V
Input Voltage	$V_{IN}$	-0.3 to ( $V_{DD}+0.3$ )	V
Input Current	$I_{IN}$	$\pm 10$	mA
Operating Temperature	$T_{opr}$	-40 to +85	°C
Storage Temperature	$T_{stg}$	-55 to +150	°C
Maximum Junction Temperature	$T_{Jmax}$	+150	°C
Power Dissipation	$P_D$	0.56 (Note 1)	W

(Note 1) Mounted on 70mm x 70mm x 1.6mm glass epoxy board. Reduce 4.5mW per 1°C above 25°C.

**Caution:** Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings

## Recommended Operating Conditions

Parameter	Symbol	Rating	Unit
Supply Voltage	$V_{DD}$	+3.0 to +16.0	V
Input Voltage	$V_{IN}$	0 to $V_{DD}$	V

## Electrical Characteristics

(Unless otherwise specified,  $V_{SS}=0V$ ,  $T_A=25^{\circ}C$ )

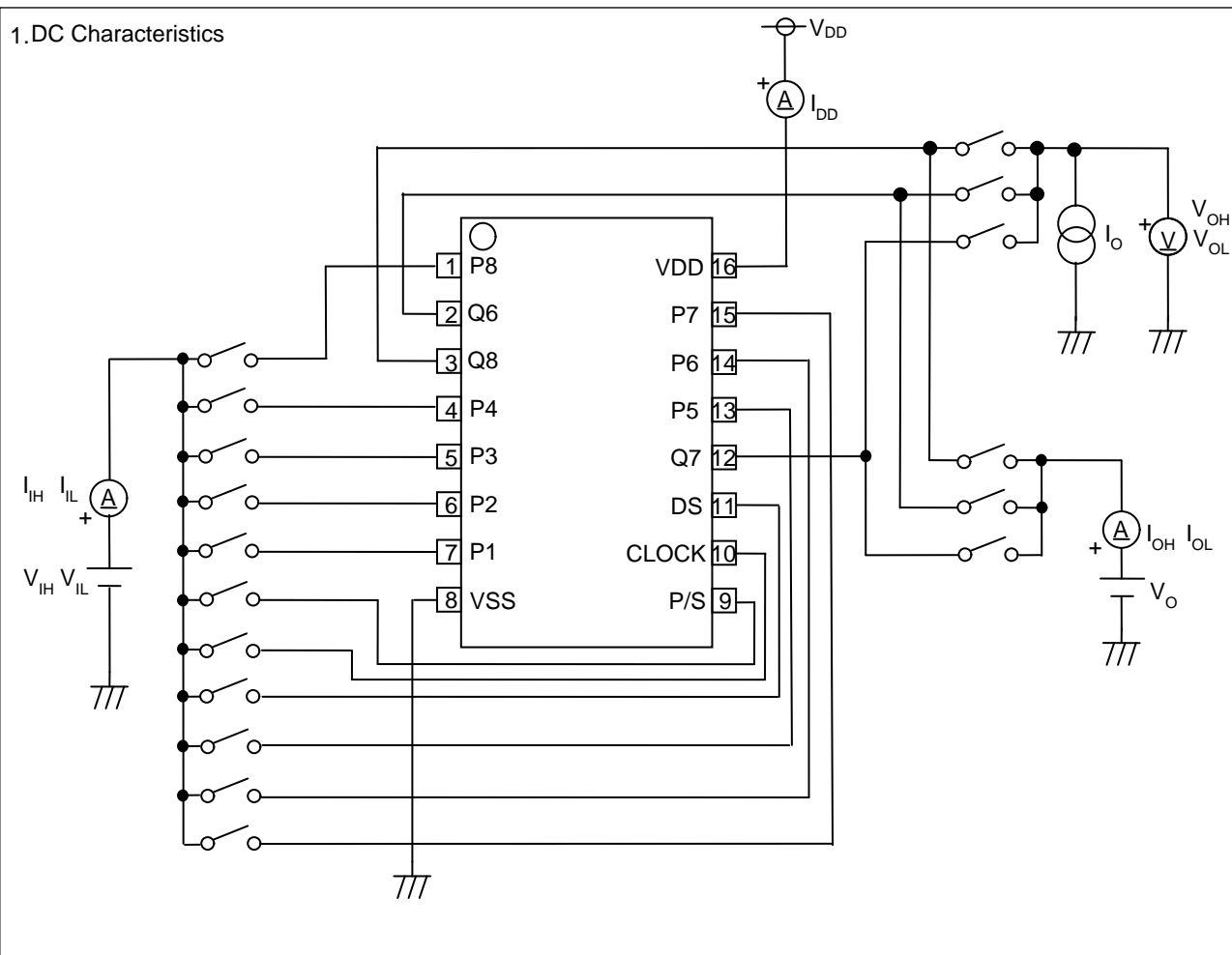
	Parameter	Symbol	Limits			Unit	$V_{DD}$ (V)	Conditions	Figure No.
			Min	Typ	Max				
DC Characteristics	Input "H" voltage	$V_{IH}$	3.5	-	-	V	5	-	-
			7.0	-	-		10		
			11.0	-	-		15		
	Input "L" voltage	$V_{IL}$	-	-	1.5	V	5	-	-
			-	-	3.0		10		
			-	-	4.0		15		
	Input "H" current	$I_{IH}$	-	-	0.3	$\mu A$	15	$V_{IH}=15V$	-
	Input "L" current	$I_{IL}$	-	-	-0.3	$\mu A$	15	$V_{IL}=0V$	-
	Output "H" voltage	$V_{OH}$	4.95	-	-	V	5	$I_O=0mA$	1
			9.95	-	-		10		
			14.95	-	-		15		
	Output "L" voltage	$V_{OL}$	-	-	0.05	V	5	$I_O=0mA$	2
			-	-	0.05		10		
			-	-	0.05		15		
	Output "H" current	$I_{OH}$	-0.16	-	-	mA	5	$V_O=4.6V$	1
			-0.4	-	-		10	$V_O=9.5V$	
			-1.2	-	-		15	$V_O=13.5V$	
	Output "L" current	$I_{OL}$	0.44	-	-	mA	5	$V_O=0.4V$	2
			1.1	-	-		10	$V_O=0.5V$	
			3.0	-	-		15	$V_O=1.5V$	
	Quiescent supply current	$I_{DD}$	-	-	20	$\mu A$	5	$V_I=V_{DD}$ or $0V$	-
			-	-	40		10		
			-	-	80		15		

(Unless otherwise specified  $V_{SS}=0V$ ,  $T_A=25^{\circ}C$ ,  $C_L=50pF$ )

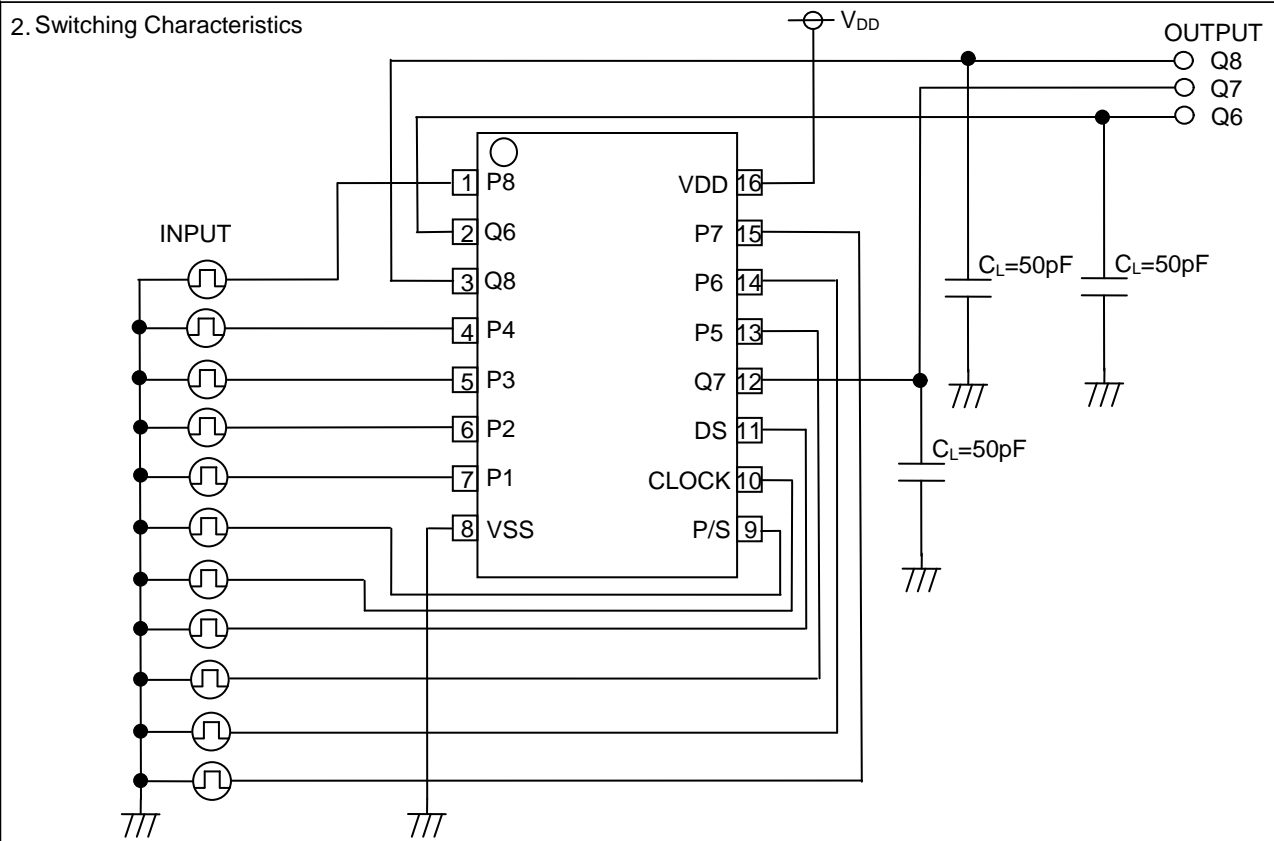
	Parameter	Symbol	Limits			Unit	$V_{DD}$ (V)	Conditions	Figure No.
			Min	Typ	Max				
Switching Characteristics	Output rising time	$t_{TLH}$	-	180	-	ns	5	-	-
			-	90	-		10		
			-	65	-		15		
	Output falling time	$t_{THL}$	-	100	-	ns	5	-	-
			-	50	-		10		
			-	40	-		15		
	Propagation delay time L to H	$t_{PLH}$	-	400	-	ns	5	-	3 • 5
			-	170	-		10		
			-	115	-		15		
	Propagation delay time H to L	$t_{PHL}$	-	400	-	ns	5	-	4 • 6
			-	170	-		10		
			-	115	-		15		
	Set up time	$t_{SU}$	-	150	-	ns	5	-	7
			-	50	-		10		
			-	30	-		15		
	Minimum clock pulse width	$t_W(\text{CLK})$	-	150	-	ns	5	-	9
			-	75	-		10		
			-	40	-		15		
	Maximum clock frequency	$f(\text{CLK})$	-	3.0	-	MHz	5	-	-
			-	6.0	-		10		
			-	8.0	-		15		
	Maximum clock rising time Maximum clock falling time	$t_R(\text{CLK})$ $t_F(\text{CLK})$	-	-	15	$\mu s$	5	-	-
			-	-	5.0		10		
			-	-	4.0		15		
	Minimum P/S pulse width	$t_W(\text{P/S})$	-	150	-	ns	5	-	10
			-	75	-		10		
			-	40	-		15		
	Input capacitance	$C_{IN}$	-	5	-	pF	-	-	-

## Test Circuits

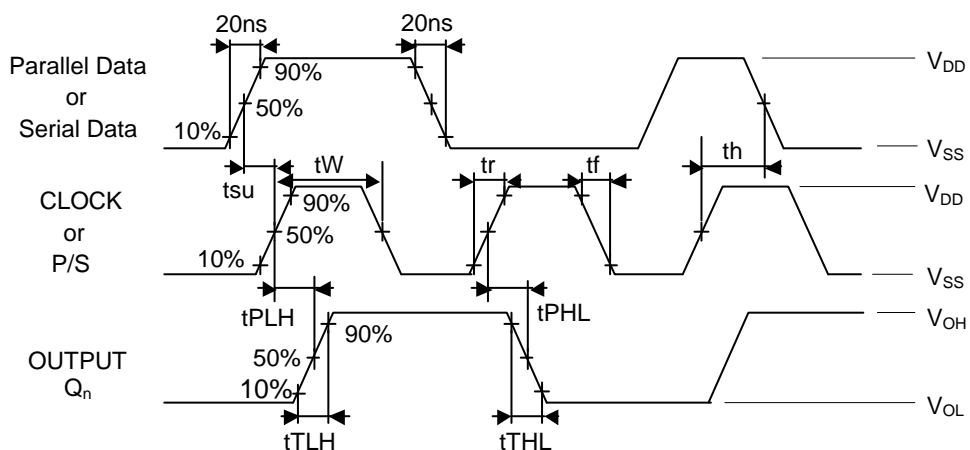
## 1. DC Characteristics



## 2. Switching Characteristics



## Waveforms of Switching Characteristics



## Typical Performance Curves

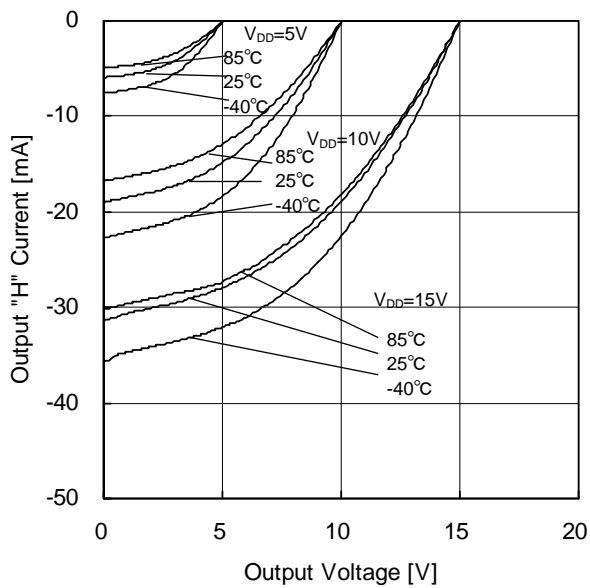


Figure 1.  
Output "H" Current vs Output Voltage

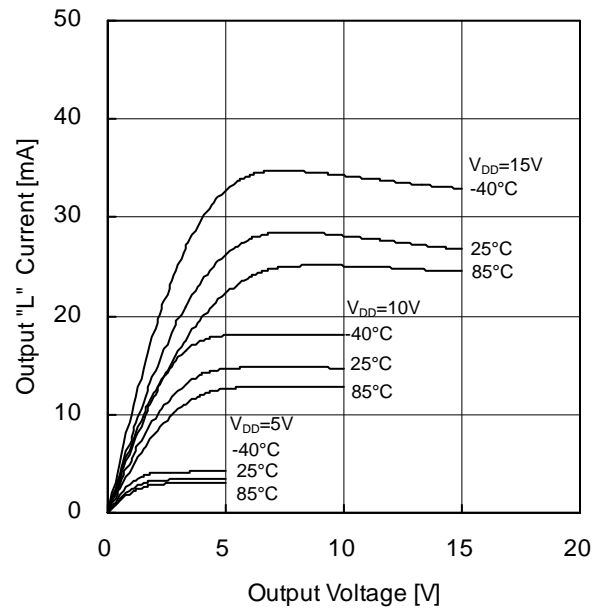


Figure 2.  
Output "L" Current vs Output Voltage

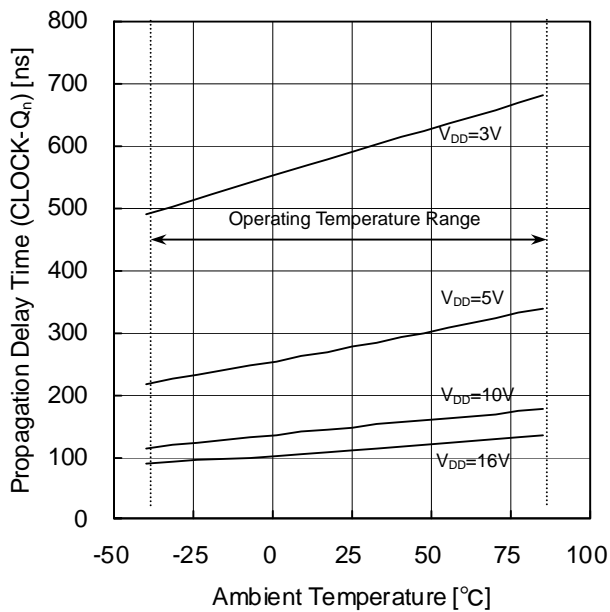


Figure 3.  
Propagation Delay Time :tPLH (CLOCK - Q<sub>n</sub>)

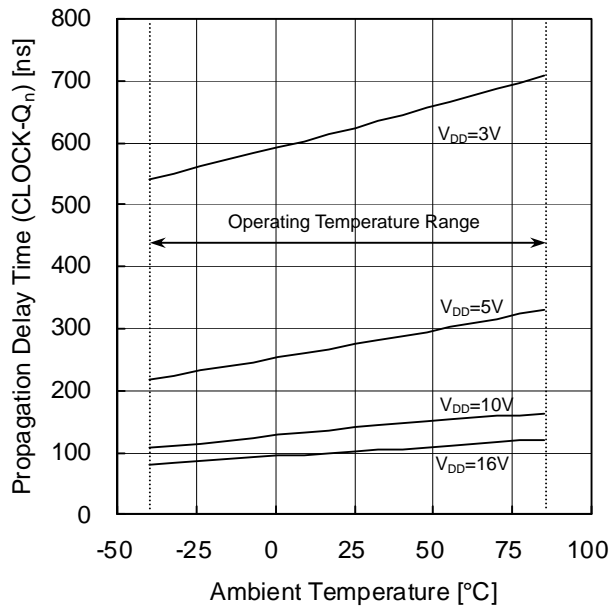


Figure 4.  
Propagation Delay Time :tPHL (CLOCK - Q<sub>n</sub>)

(\*)The above characteristics are measurements of typical sample, they are not guaranteed.

## Typical Performance Curves - continued

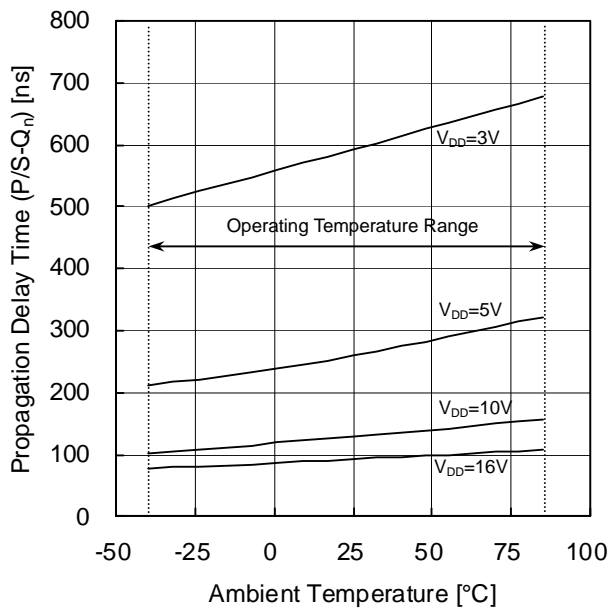


Figure 5.  
Propagation Delay Time :tPLH (P/S – Q<sub>n</sub>)

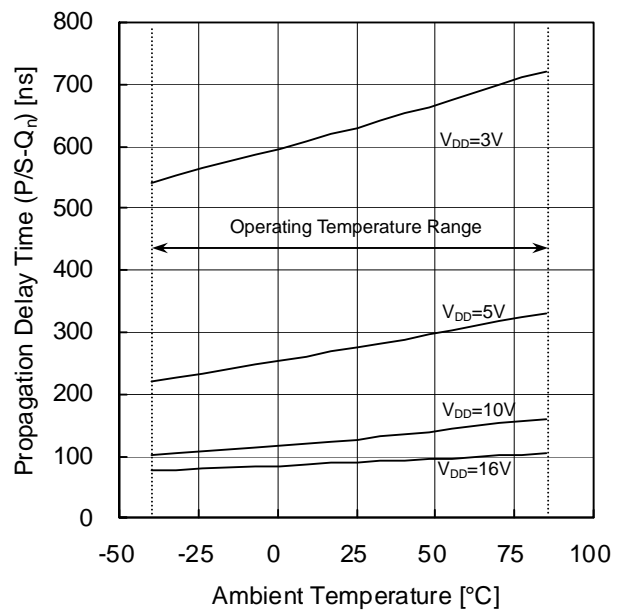


Figure 6.  
Propagation Delay Time :tPHL (P/S – Q<sub>n</sub>)

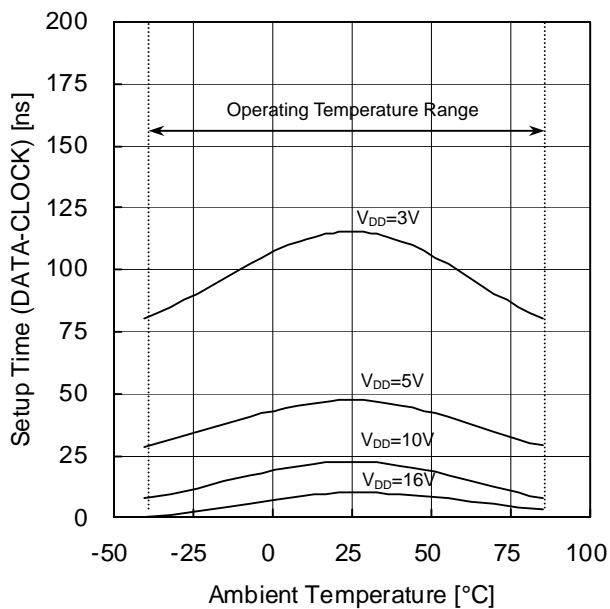


Figure 7.  
Setup Time :tsu (DATA – CLOCK)

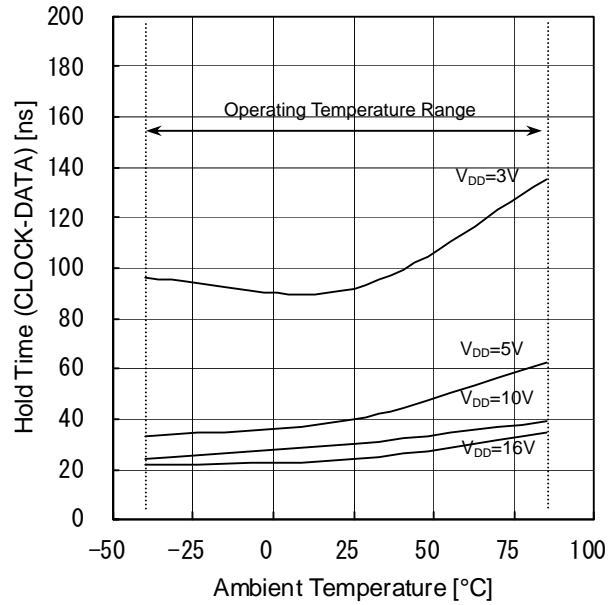


Figure 8.  
Hold Time :th (CLOCK – DATA)

(\*)The above characteristics are measurements of typical sample, they are not guaranteed.



## Typical Performance Curves - continued

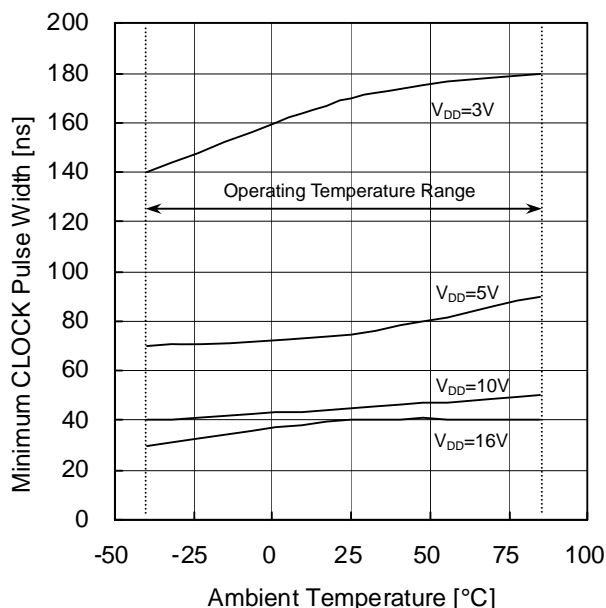


Figure 9.  
Minimum CLOCK Pulse Width

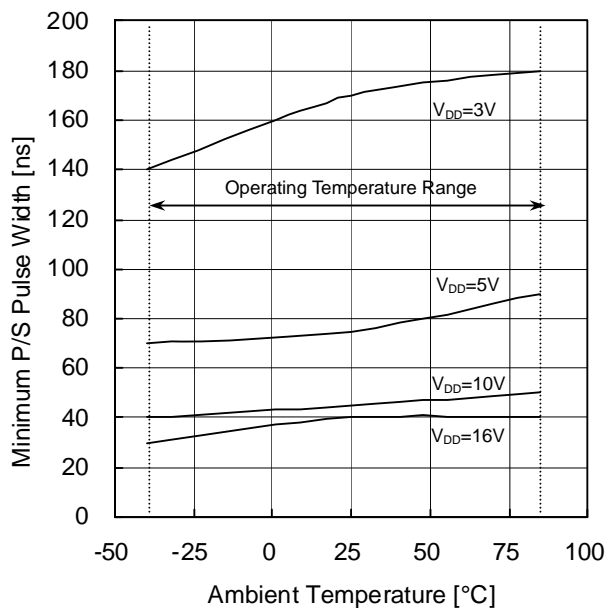


Figure 10.  
Minimum P/S Pulse Width

(\*)The above characteristics are measurements of typical sample, they are not guaranteed.

## Power Dissipation

Power dissipation (total loss) indicates the power that can be consumed by IC at  $T_A=25^\circ\text{C}$  (normal temperature). IC is heated when it consumed power, and the temperature of IC chip becomes higher than ambient temperature. The temperature that can be accepted by IC chip depends on circuit configuration, manufacturing process, and consumable power is limited. Power dissipation is determined by the temperature allowed in IC chip (maximum junction temperature) and thermal resistance of package (heat dissipation capability). The maximum junction temperature is typically equal to the maximum value in the storage temperature range. Heat generated by consumed power of IC radiates from the mold resin or lead frame of the package. The parameter which indicates this heat dissipation capability (hardness of heat release) is called thermal resistance, represented by the symbol  $\theta_{JA}$  ( $^\circ\text{C}/\text{W}$ ). The temperature of IC inside the package can be estimated by this thermal resistance. Figure 11 shows the model of thermal resistance of the package. Thermal resistance  $\theta_{JA}$ , ambient temperature  $T_A$ , maximum junction temperature  $T_{Jmax}$ , and power dissipation  $P_D$  can be calculated by the equation below:

$$\theta_{JA} = (T_{Jmax} - T_A) / P_D \quad (^\circ\text{C}/\text{W})$$

Derating curve in Figure 12 indicates power that can be consumed by IC with reference to ambient temperature. Power that can be consumed by IC begins to attenuate at certain ambient temperature. This gradient is determined by thermal resistance  $\theta_{JA}$ . Thermal resistance  $\theta_{JA}$  depends on chip size, power consumption, package, ambient temperature, package condition, wind velocity, etc even when the same of package is used. Thermal reduction curve indicates a reference value measured at a specified condition.

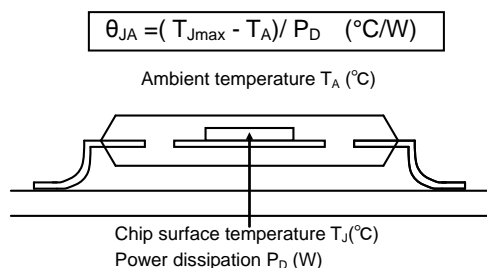


Figure 11. Thermal resistance

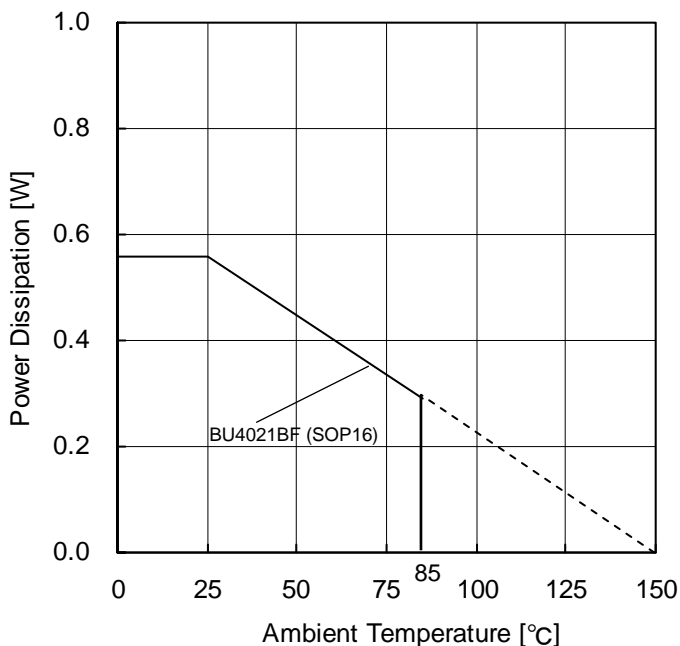


Figure 12. Derating Curve

## I/O Equivalence Circuit

Pin No.	Input Terminal	Output Terminal
	1,4,5,6,7,9,10,11,13,14,15	2,3,12
Equivalence Circuit		

## Operational Notes

## 1. Reverse Connection of Power Supply

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

## 2. Power Supply Lines

Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

## 3. Ground Voltage

Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

## 4. Ground Wiring Pattern

When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

## 5. Thermal Consideration

Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. The absolute maximum rating of the  $P_D$  stated in this specification is when the IC is mounted on a 70mm x 70mm x 1.6mm glass epoxy board. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the  $P_D$  rating.

## 6. Recommended Operating Conditions

These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

## 7. Inrush Current

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

## 8. Operation Under Strong Electromagnetic Field

Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

## Operational Notes - continued

**9. Testing on Application Boards**

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

**10. Inter-pin Short and Mounting Errors**

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

**11. Unused Input Pins**

Input terminals of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

**12. Regarding the Input Pin of the IC**

In the construction of this IC, P-N junctions are inevitably formed creating parasitic diodes or transistors. The operation of these parasitic elements can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions which cause these parasitic elements to operate, such as applying a voltage to an input pin lower than the ground voltage should be avoided. Furthermore, do not apply a voltage to the input terminals when no power supply voltage is applied to the IC. Even if the power supply voltage is applied, make sure that the input pins have voltages within the values specified in the electrical characteristics of this IC.

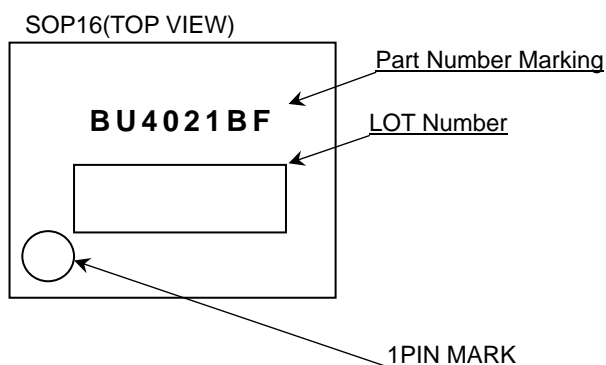
**13. Ceramic Capacitor**

When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

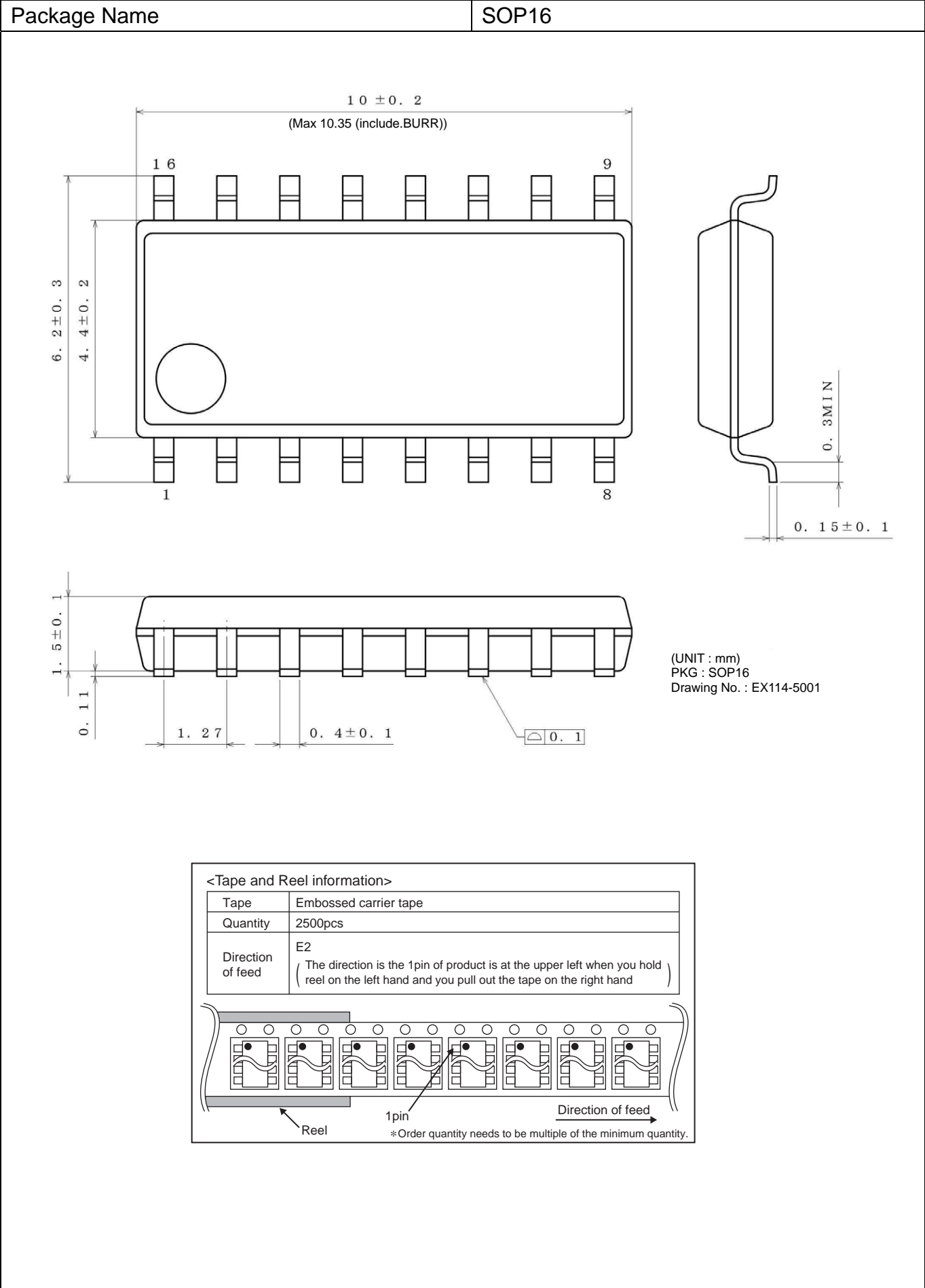
## Ordering Information

B U 4 0 2 1 B F	-	E 2
Part Number	Package F : SOP16	Packaging and forming specification E2 : Embossed tape and reel

## Marking Diagram



Physical Dimension, Tape and Reel Information – continued



## Revision History

Date	Revision	Changes
04.Sep.2013	001	New Release

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JAPAN	USA	EU	CHINA
CLASS III	CLASS III	CLASS II b	CLASS III
CLASS IV		CLASS III	

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  - Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
  - Sealing or coating our Products with resin or other coating materials
  - Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
  - Use of the Products in places subject to dew condensation
- The Products are not subject to radiation-proof design.
- Please verify and confirm characteristics of the final or mounted products in using the Products.
- In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.
- De-rate Power Dissipation (Pd) depending on Ambient temperature (Ta). When used in sealed area, confirm the actual ambient temperature.
- Confirm that operation temperature is within the specified range described in the product specification.
- ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

## Precaution for Mounting / Circuit board design

- When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.
- In principle, the reflow soldering method must be used; if flow soldering method is preferred, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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## Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
  - [a] the Products are exposed to sea winds or corrosive gases, including Cl<sub>2</sub>, H<sub>2</sub>S, NH<sub>3</sub>, SO<sub>2</sub>, and NO<sub>2</sub>
  - [b] the temperature or humidity exceeds those recommended by ROHM
  - [c] the Products are exposed to direct sunshine or condensation
  - [d] the Products are exposed to high Electrostatic
2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.
3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.
4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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