SY89465U

Precision LVDS 1:10 Fanout with 2:1 Runt Pulse Eliminator MUX and Internal Termination

General Description

The SY89465U is a low jitter, 1:10 LVDS fanout buffer with a 2:1 differential input multiplexer (MUX) optimized for redundant source switchover applications. Unlike standard multiplexers, the SY89465Us 2:1 Runt Pulse Eliminator (RPE) MUX prevents any short cycles or "runt" pulses during switchover. In addition, a unique Fail-Safe Input (FSI) protection prevents metastable conditions when the selected input clock fails to a DC voltage (voltage between the pins of the differential input drops below 100mV).

The differential input includes Micrel's, 3-pin internal termination architecture that allows customers to interface to any differential signal (AC- or DC-coupled) as small as 100mV ($200mV_{PP}$) without any level shifting or termination resistor networks in the signal path. The outputs are LVDS-compatible with fast rise/fall times guaranteed to be less than 220ps.

The SY89465U operates from a 2.5V ±5% supply and is guaranteed over the full industrial temperature range of –40°C to +85°C. The SY89465U is part of Micrel's high-speed, Precision Edge® product line.

All support documentation can be found on Micrel's web site at: www.micrel.com.

Precision Edge®

Features

- Selects between two sources, and provides 10 precision LVDS copies
- Guaranteed AC performance over temperature and supply voltage:
  - Wide operating frequency: 1kHz to >1.5GHz
  - < 1200ps In-to-Out t_{pd}
  - < 220ps t_r/t_f
- Unique, patent-pending input isolation design minimizes adjacent channel crosstalk
- Fail-Safe Input prevents oscillations
- Ultra-low jitter design:
  - <1ps$_{RMS}$ random jitter
  - <1ps$_{RMS}$ cycle-to-cycle jitter
  - <10ps$_{PP}$ total jitter (clock)
  - <0.7ps$_{RMS}$ MUX crosstalk induced jitter
- Unique patented input termination and VT pin accepts DC- and AC-coupled inputs (CML, PECL, LVDS)
- 325mV LVDS output swing
- 2.5V ±5% supply voltage
- -40°C to +85°C industrial temperature range
- Output enable
- Available in 44-pin (7mm x 7mm) MLF™ package

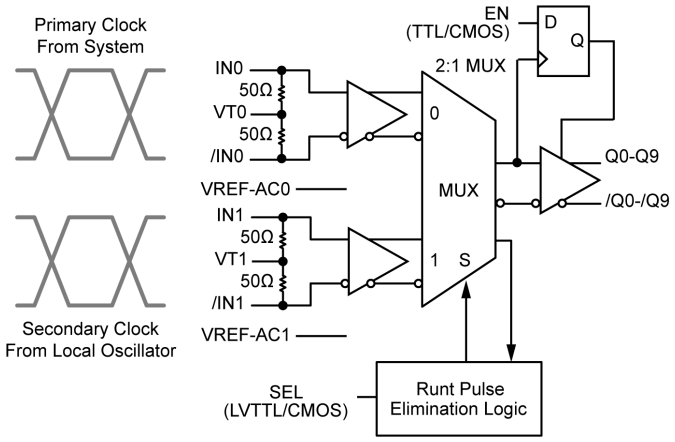
Applications

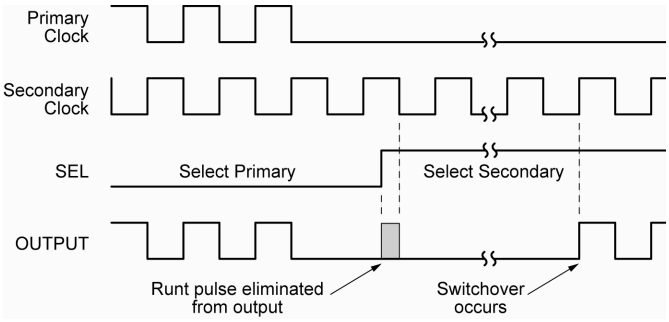
- Redundant clock switchover
- Fail-safe clock protection

Markets

- LAN/WAN
- Enterprise servers
- ATE
- Test and measurement

Typical Application





Simplified Example Illustrating Runt Pulse Eliminator (RPE) when Primary Clock Fails

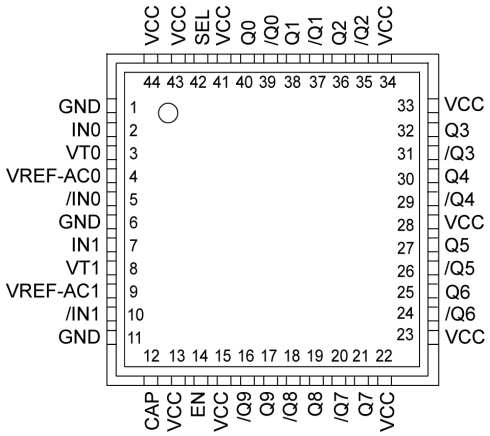
Ordering Information[1]

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY89465UMG	MLF-44	Industrial	SY89465U with Pb-Free bar-line Indicator	NiPdAu Pb-Free
SY89465UMGTR[2]	MLF-44	Industrial	SY89465U with Pb-Free bar-line Indicator	NiPdAu Pb-Free

Notes:

1. Contact factory for die availability. Dice are guaranteed at T_A = 25°C, DC Electricals only.
2. Tape and Reel.

Pin Configuration



44-Pin MLF™ (MLF-44)

Pin Description

Pin Number	Pin Name	Pin Function
2, 5 7, 10	IN0, /IN0 IN1, /IN1	Differential Inputs: These input pairs are the differential signal inputs to the device. These inputs accept AC- or DC-coupled signals as small as 100mV (200mV$_{pp}$). Each pin of a pair internally terminates to a V_T pin through 50Ω. Please refer to the "Input Interface Applications" section for more details.
4, 9	VREF-AC0 VREF-AC1	Reference Voltage: These outputs bias to V_{CC} –1.2V. They are used for AC-coupling inputs IN and /IN. Connect V_{REF-AC} directly to the corresponding V_T pin. Bypass with 0.01µF low ESR capacitor to V_{CC}. Due to the limited drive capability, the V_{REF-AC} pin is only intended to drive its respective V_T pin. Maximum sink/source current is ±1.5mA. Please refer to the "Input Interface Applications" section for more details.
3, 8	VT0, VT1	Input Termination Center-Tap: Each side of the differential input pair terminates to a V_T pin. The V_{T0} and V_{T1} pins provide a center-tap to a termination network for maximum interface flexibility. Please refer to the "Input Interface Applications" section for more details.
13, 15, 22, 23 28, 33, 34, 41, 43, 44	VCC	Positive Power Supply: Bypass with 0.1µF||0.01µF low ESR capacitors as close to the V_{CC} pins as possible.
39, 40 37, 38 35, 36 31, 32 29, 30 26, 27 24, 25 20, 21 18, 19 16, 17	/Q0, Q0 /Q1, Q1 /Q2, Q2 /Q3, Q3 /Q4, Q4 /Q5, Q5 /Q6, Q6 /Q7, Q7 /Q8, Q8 /Q9, Q9	Differential Outputs: These differential LVDS outputs are a logic function of the IN0, IN1, and SEL inputs. Please refer to the "Truth Table" below for details.
42	SEL	This single-ended TTL/CMOS-compatible input selects the inputs to the multiplexer. Note that this input is internally connected to a 25kΩ pull-up resistor and will default to logic HIGH state if left open. $V_{TH} = V_{CC}/2$.
1, 11, 6	GND, Exposed Pad	Ground: Ground and exposed pad must be connected to the same ground plane.
12	CAP	Power-On Reset (POR) initialization capacitor. When using the multiplexer with RPE capability, this pin is tied to a capacitor to V_{CC}. The purpose is to ensure the internal RPE logic starts up in a known state. See "Power-On Reset (POR) Description" section for more details regarding capacitor selection. If this pin is tied directly to V_{CC}, the RPE function will be disabled and the multiplexer will function as a normal multiplexer. The CAP pin should never be left open or tied directly to GND.
14	EN	Single-Ended Input: This TTL/CMOS input disables and enables the Q0-Q9 outputs. It is internally connected to a 25kΩ pull-up resistor and will default to a logic HIGH state if left open. When disabled, CLK output goes LOW and /CLK goes HIGH. EN being synchronous, outputs will be enabled/disabled when they are in LOW state. Thus, a runt pulse is avoided if the device is enabled/disabled by an asynchronous control. $V_{TH} = V_{CC}/2$.

Truth Table

Inputs					Outputs	
IN0	**/IN0**	**IN1**	**/IN1**	**SEL**	**Q**	**/Q**
0	1	X	X	0	0	1
1	0	X	X	0	1	0
X	X	0	1	1	0	1
X	X	1	0	1	1	0

Absolute Maximum Ratings[1]

Supply Voltage (V_{CC}) ..... –0.5V to +4.0V
Input Voltage (V_{IN}) ..... –0.5V to V_{CC}
Input Current (I_{IN}) .....
  Source/Sink Current on IN, /IN..... ±50mA
  Source/Sink Current on V_T ..... ±100mA
V_{REF-AC} Current
  Source/Sink Current on V_{REF-AC}..... ±2mA
Lead Temperature (soldering, 20 sec.)..... +260°C
Storage Temperature (T_s) .....–65°C to 150°C

Operating Ratings[2]

Supply Voltage (V_{CC}) ..... +2.375V to +2.625V
Ambient Temperature (T_A) .....–40°C to +85°C
Package Thermal Resistance[3]
MLF™ (θ_{JA})
  Still-Air ..... 24.4°C/W
MLF™ (ψ_{JB})
  Junction-to-Board ..... 8.1°C/W

DC Electrical Characteristics[4]

T_A = –40°C to +85°C, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{CC}	Power Supply		2.375	2.5	2.625	V
I_{CC}	Power Supply Current	No load, max V_{CC}		250	325	mA
R_{IN}	Input Resistance (IN-to-V_T)		45	50	55	Ω
R_{DIFF_IN}	Differential Input Resistance (IN-to-/IN)		90	100	110	Ω
V_{IH}	Input High Voltage (IN, /IN)		1.2		V_{CC}	V
V_{IL}	Input Low Voltage (IN, /IN)		0		V_{IH}–0.1	V
V_{IN}	Input Voltage Swing (IN, /IN)	See Figure 1a. Note 5.	0.1		2.5	V
V_{DIFF_IN}	Differential Input Voltage Swing |IN-/IN|	See Figure 1b.	0.2			V
V_{IN_FSI}	Input Voltage Threshold that Triggers FSI			30	100	mV
V_{T_IN}	IN-to-V_T (IN, /IN)				1.28	V
V_{REF-AC}	Output Reference Voltage		V_{CC}–1.3	V_{CC}–1.2	V_{CC}–1.1	V

Notes:

1. Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. Package thermal resistance assumes exposed pad is soldered (or equivalent) to the devices most negative potential on the PCB. θ_{JA} and ψ_{JB} values are determined for a 4-layer board in still air unless otherwise stated.
4. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.
5. V_{IN} (max) is specified when V_T is floating.

LVDS Outputs DC Electrical Characteristics[6]

V_{CC} = 2.5V ±5%; R_L = 100Ω across output pair or equivalent; T_A = –40°C to + 85°C, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OCM}	Output Common Mode Voltage		1.125		1.275	V
ΔV_{OCM}	Change in VOCM between complementing output states		–50		+50	mV
V_{OUT}	Output Voltage Swing	See Figure 1a.	250	325		mV
$V_{DIFF-OUT}$	Differential Output Voltage Swing	See Figure 1b.	500	650		mV

LVTTL/CMOS DC Electrical Characteristics[6]

V_{CC} = 2.5V ±5%; T_A = –40°C to + 85°C, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	Input HIGH Voltage		2.0			V
V_{IL}	Input LOW Voltage				0.8	V
I_{IH}	Input HIGH Current		-125		30	µA
I_{IL}	Input LOW Current		-300			µA

Note:

6. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

AC Electrical Characteristics[7]

V_{CC} = 2.5V ±5%; R_L = 100Ω across the output pair; T_A = –40°C to + 85°C, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{MAX}	Maximum Operating Frequency	V_{OUT} ≥ 200mV, Clock	1.5	2.0		GHz
t_{pd}	Differential Propagation Delay					
	In-to-Q	100mV < V_{IN} ≤ 200mV[8]	550	800	1200	ps
	In-to-Q	200mV < V_{IN} ≤ 800mV[8]	500	700	1100	ps
	SEL-to-Q	RPE enabled, see Timing Diagram			17	cycles
	SEL-to-Q	RPE disabled (V_{SEL} = V_{CC}/2)	600		1200	ps
t_{PD} Tempco	Differential Propagation Delay Temperature Coefficient			500		fs/°C
t_S EN	Set-up Time EN-to-CLK	Note 9	0			ps
t_H EN	Hold Time CLK-to-EN	Note 9	650			ps
t_{SKEW}	Output-to-Output Skew	Note 10		5	25	ps
	Part-to-Part Skew	Note 11			300	ps
t_{JITTER}	Clock					
	Random Jitter	Note 12			1	ps_{RMS}
	Cycle-to-Cycle Jitter	Note 13			1	ps_{RMS}
	Total Jitter	Note 14			10	ps_{PP}
	Crosstalk-Induced Jitter	Note 15			0.7	ps_{RMS}
t_r, t_f	Output Rise/Fall Time (20% to 80%)	At full output swing.	70	120	220	ps

Notes:

7. High-frequency AC-parameters are guaranteed by design and characterization.
8. Propagation delay is measured with input t_r, t_f ≤ 300ps (20% to 80%) and V_{IL} ≥ 800mV. The propagation delay is function of the rise and fall times at IN. See “Typical Operating Characteristics” for details.
9. Set-up and hold times apply to synchronous applications that intend to enable/disable before the next clock cycle. For asynchronous applications, set-up and hold do not apply.
10. Output-to-Output skew is measured between two different outputs under identical transitions.
11. Part-to-Part skew is defined for two parts with identical power supply voltages at the same temperature and with no skew of the edges at the respective inputs.
12. Random Jitter is measured with a K28.7 character pattern, measured at <f_{MAX}.
13. Cycle-to-Cycle Jitter definition: the variation of periods between adjacent cycles, T_n – T_{n-1} where T is the time between rising edges of the output signal.
14. Total Jitter definition: with an ideal clock input of frequency <f_{MAX}, no more than one output edge in 10^{12} output edges will deviate by more than the specified peak-to-peak jitter value.
15. Crosstalk is measured at the output while applying two similar differential clock frequencies that are asynchronous with respect to each other at the inputs.

Functional Description

RPE MUX and Fail-Safe Input

The SY89465U is optimized for clock switchover applications where switching from one clock to another clock without runt pulses (short cycles) is required. It features two unique circuits:

Runt-Pulse Eliminator (RPE) Circuit

The RPE MUX provides a "glitchless" switchover between two clocks and prevents any runt pulses from occurring during the switchover transition. The design of both clock inputs is identical (i.e., the switchover sequence and protection is symmetrical for both input pairs, IN0 or IN1. Thus, either input pair may be defined as the primary input). If not required, the RPE function can be permanently disabled to allow the switchover between inputs to occur immediately. If the CAP pin is tied directly to V_{CC}, the RPE function will be disabled and the multiplexer will function as a normal multiplexer.

Fail-Safe Input (FSI) Circuit

The FSI function provides protection against a selected input pair that drops below the minimum amplitude requirement. If the selected input pair drops sufficiently below the 100mV minimum single-ended input amplitude limit (V_{IN}), or 200mV differentially (V_{DIFF_IN}), the output will latch to the last valid clock state.

RPE and FSI Functionality

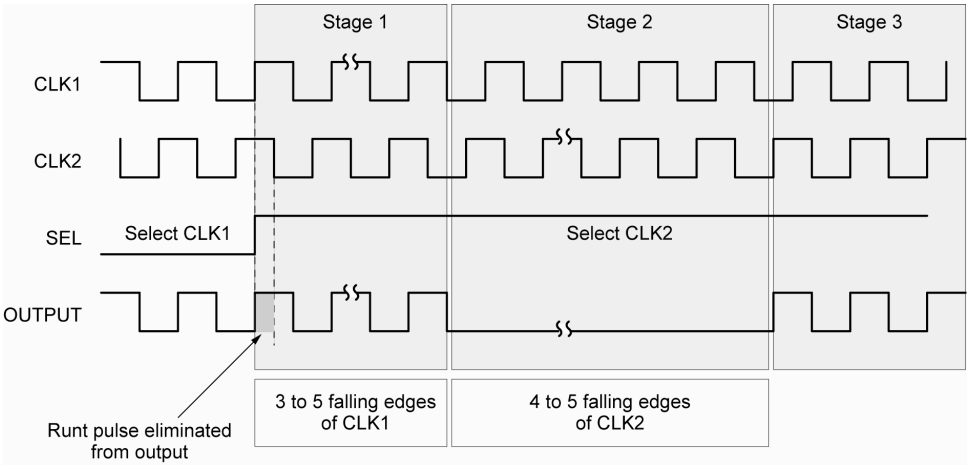
The basic operation of the RPE MUX and FSI functionality is described with the following four case descriptions. All descriptions are related to the true inputs and outputs. The primary (or selected) clock is called CLK1; the secondary (or alternate) clock is called CLK2. Due to the totally asynchronous relation of the IN and SEL signals and an additional internal protection against metastability, the number of pulses required for the operations described in cases 1-4 can vary within certain limits. Refer to "Timing Diagrams" section for detailed information.

Case #1: Two Normal Clocks and RPE Enabled

In this case, the frequency difference between the two running clocks, IN0 and IN1, must not be greater than 1.5:1. For example, if the IN0 clock is 500MHz, the IN1 clock must be within the range of 334MHz to 750MHz.

If the SEL input changes state to select the alternate clock, the switchover from CLK1 to CLK2 will occur in three stages.

- Stage 1: The output will continue to follow CLK1 for a limited number of pulses.
- Stage 2: The output will remain LOW for a limited number of pulses of CLK2.
- Stage 3: The output follows CLK2.

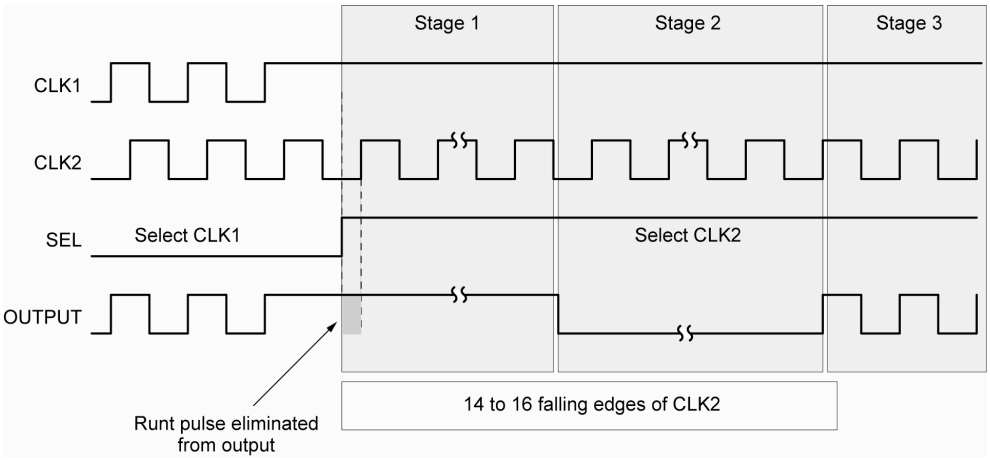


Timing Diagram 1

Case #2: Input Clock Failure: Switching from a selected clock stuck HIGH to a valid clock (RPE enabled).

If CLK1 fails HIGH before the RPE MUX selects CLK2 (using the SEL pin), the switchover will occur in three stages.

- Stage 1: The output will remain HIGH for a limited number of pulses of CLK2.
- Stage 2: The output will switch to LOW and then remain LOW for a limited number of falling edges of CLK2.
- Stage 3: The output will follow CLK2.



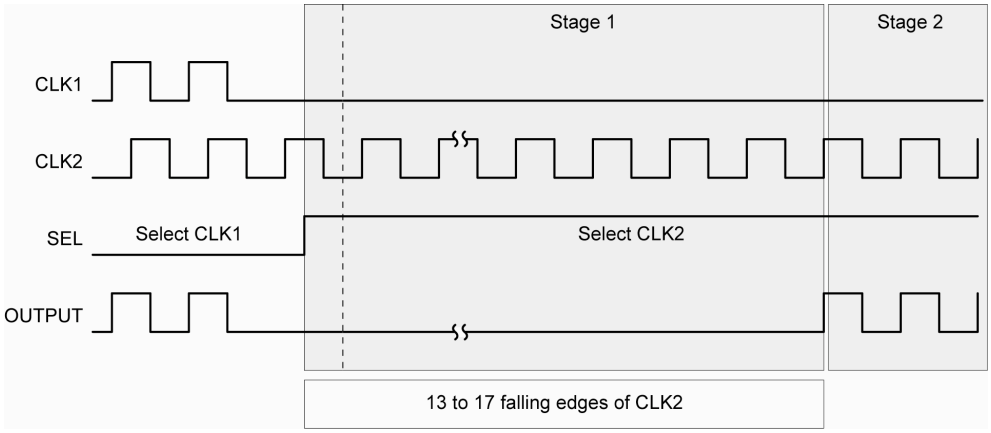
Timing Diagram 2

Note: Output shows extended clock cycle during switchover. Pulse width for both high and low of this cycle will always be greater than 50% of the CLK2 period.

Case #3: Input Clock Failure: Switching from a selected clock stuck Low to a valid clock (RPE-enabled).

If CLK1 fails LOW before the RPE MUX selects CLK2 (using the SEL pin), the switchover will occur in two stages.

- Stage 1: The output will remain LOW for a limited number of falling edges of CLK2.
- Stage 2: The output will follow CLK2.



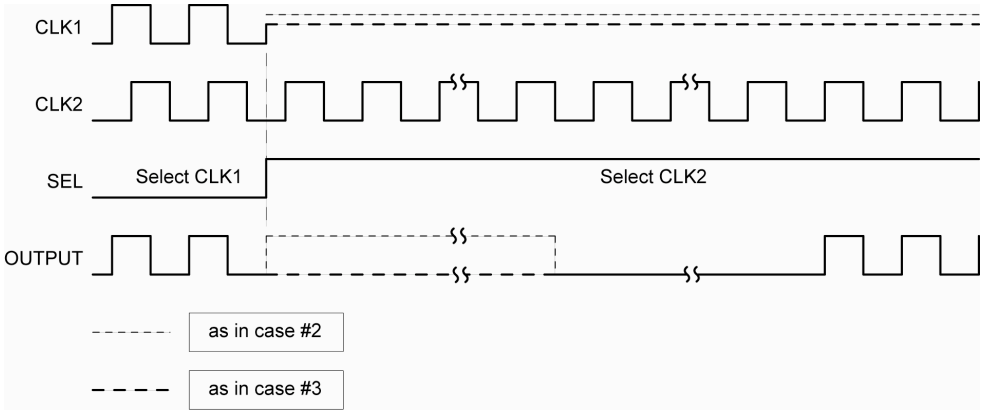
Timing Diagram 3

Case #4: Input Clock Failure: Switching from the selected clock input stuck in an undetermined state to a valid clock input (RPE-enabled).

If CLK1 fails to an undetermined state (e.g., amplitude falls below the 100mV (V_{IN}) minimum single-ended input limit, or 200mV differentially) before the RPE MUX selects CLK2 (using the SEL pin), the switchover to the valid clock CLK2 will occur either following Case #2 or Case #3, depending upon the last valid state at the CLK1.

If the selected input clock fails to a floating, static, or extremely low signal swing, including 0mV, the FSI function will eliminate any metastable condition and guarantee a stable output signal. No ringing and no undetermined state will occur at the output under these conditions.

Please note that the FSI function will not prevent duty cycle distortions or runt pulses in case of a slowly deteriorating (but still toggling) input signal. Due to the FSI function, the propagation delay will depend upon rise and fall time of the input signal and on its amplitude. Refer to “Typical Operating Characteristics” for detailed information.



Timing Diagram 4

Enable Output (EN) Description

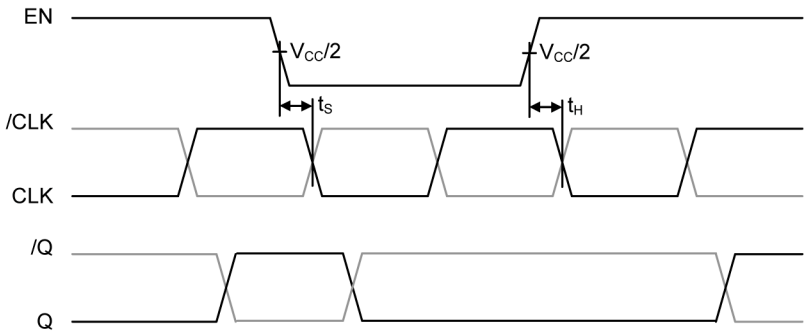
The enable function is synchronous so that the outputs will be enabled/disabled when they are already in the LOW state. This avoids any chance of generating a runt pulse when the device is enabled/disabled as can happen with asynchronous control.

Disable Output(s):

1. EN toggles from High-to-Low
2. Output(s) follow the selected Clock input
3. Output (CLK) goes to a logic LOW level (/CLK goes to a logic HIGH), after next High-to-Low transition of the selected input. See Timing Diagram 5.

Enable Output(s):

1. EN toggles from Low-to-High.
2. Output(s) follow the selected clock after next HIGH-to-LOW transition of the selected input. See “Timing Diagram 5.”



Timing Diagram 5

Power-On Reset (POR) Description

The SY89465U includes an internal power-on reset (POR) function to ensure that the RPE logic starts-up in a known logic state once the power-supply voltage is stable. An external capacitor connected between V_{CC} and the CAP pin (pin 12) controls the delay for the power-on reset function.

The required capacitor value calculation is based upon the time the system power supply needs to power up to a minimum of 2.3V. The time constant for the internal power-on-reset must be greater than the time required for the power supply to ramp up to a minimum of 2.3V.

The following formula describes this relationship:

$$C(\mu F) \geq \frac{t_{dPS}(ms)}{12(ms/\mu F)}$$

As an example, if the time required for the system power supply to power up past 2.3V is 12ms, then the required capacitor value on pin 12 would be:

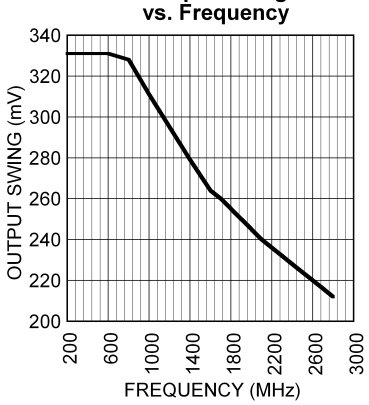
$$C(\mu F) \geq \frac{12ms}{12(ms/\mu F)}$$

$C(\mu F) \geq 1\mu F$

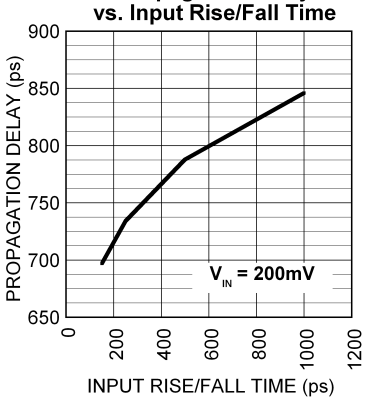
Typical Operating Characteristics

V_{CC} = 2.5V, GND = 0V, $V_{IN} \geq 400mV$, $t_r / t_f \leq 300ps$, R_L = 50Ω to V_{CC}–2V; T_A = 25°C, unless otherwise stated.

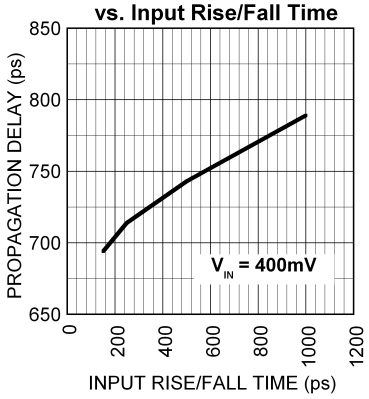
Output Swing vs. Frequency



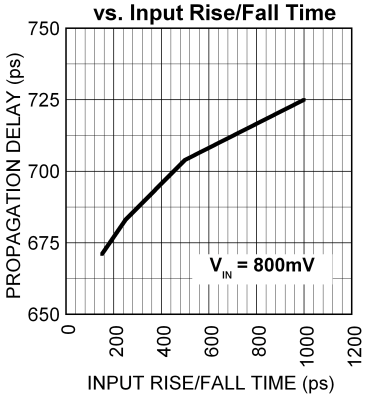
Propagation Delay vs. Input Rise/Fall Time



Propagation Delay vs. Input Rise/Fall Time



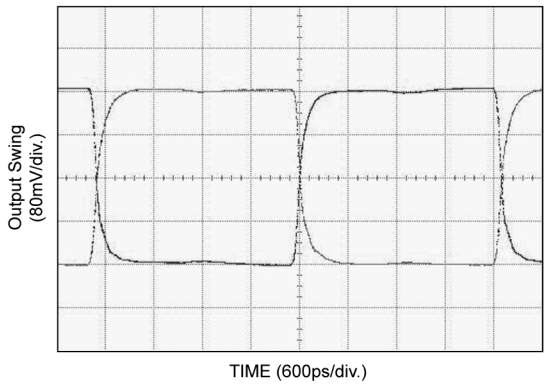
Propagation Delay vs. Input Rise/Fall Time



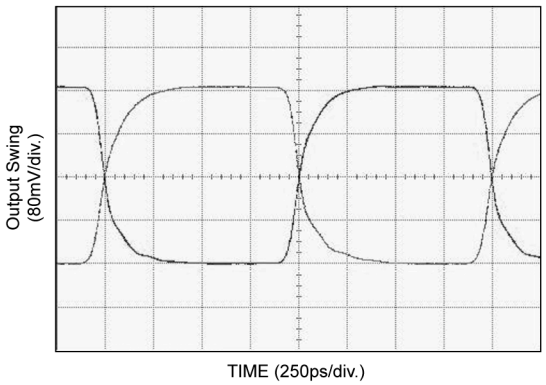
Functional Characteristics

V_{CC} = 2.5V, GND = 0V, $V_{IN} \geq 400mV_{pk}$, $t_r/t_f \leq 300ps$, $R_L = 100\Omega$ across output pair; $T_A = 25°C$, unless otherwise stated.

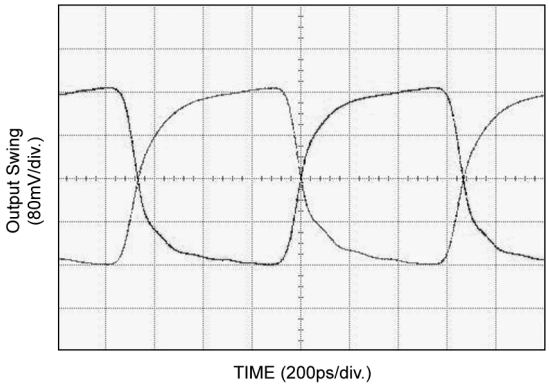
200MHz Clock



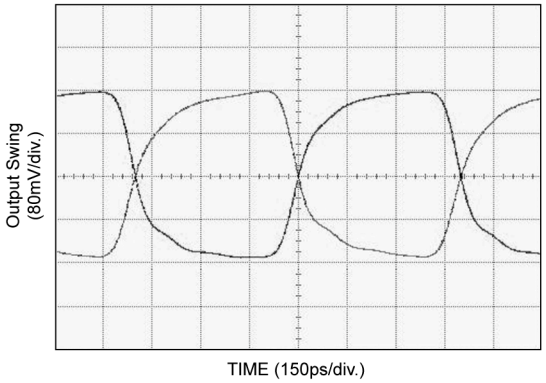
500MHz Clock



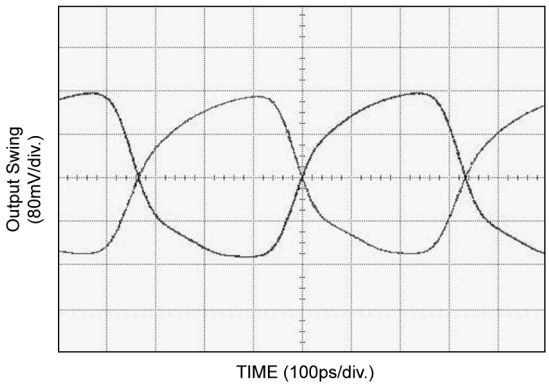
750MHz Clock



1GHz Clock



1.5GHz Clock



Single-Ended and Differential Swings

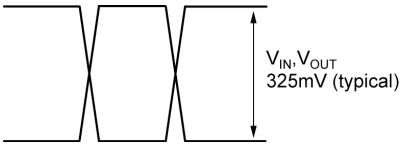


Figure 1a. Single-Ended Voltage Swing

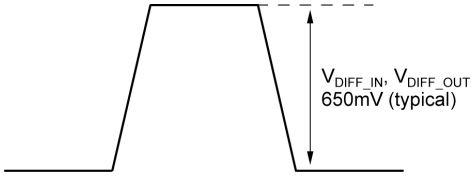


Figure 1b. Differential Voltage Swing

Input and Output Stages

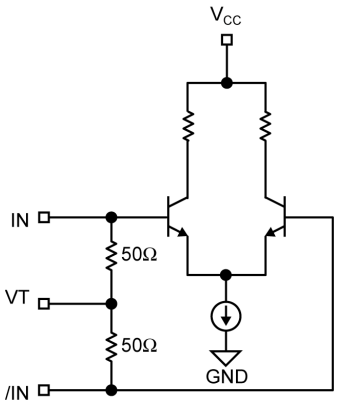


Figure 2a. Simplified Differential Input Stage

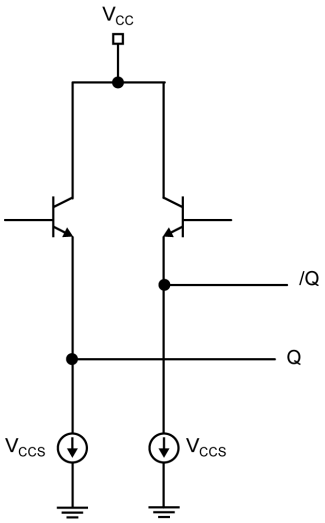


Figure 2b. Simplified Differential Output Stage

Input Interface Applications

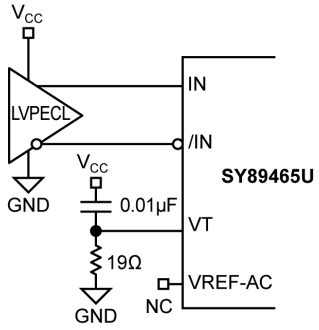


Figure 3a. LVPECL Interface (DC-Coupled)

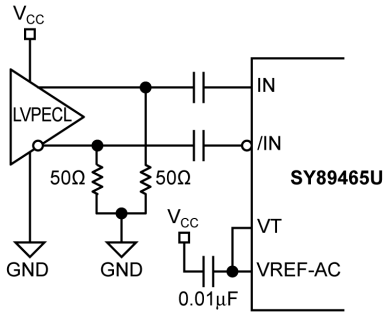
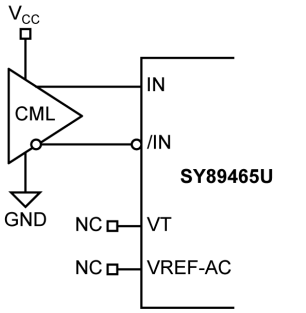


Figure 3b. LVPECL Interface (AC-Coupled)



Option: may connect V_T to V_{CC}

Figure 3c. CML Interface (DC-Coupled)

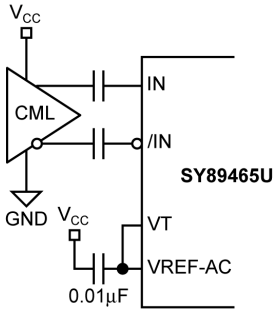


Figure 3d. CML Interface (AC-Coupled)

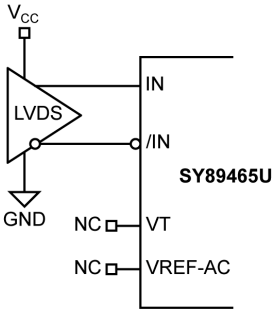


Figure 3e. LVDS Interface (DC-Coupled)

LVDS Output Interface Applications

LVDS specifies a small swing of 325mV typical, on a nominal 1.20V common mode above ground. The common mode voltage has tight limits to permit large variations in ground between an LVDS driver and receiver. Also, change in common mode voltage, as a function of data input, is kept to a minimum, to keep EMI low.

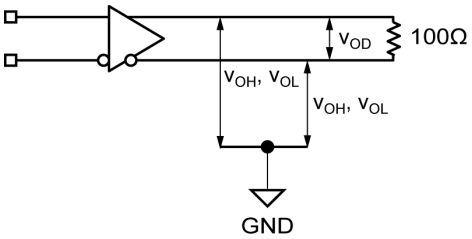


Figure 4a. LVDS Differential Measurement

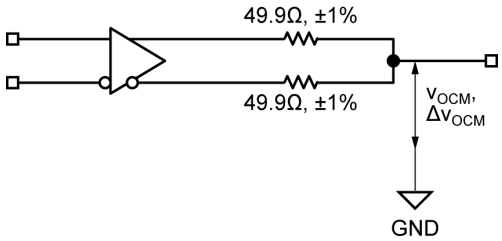
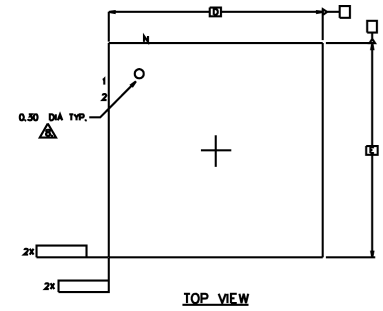


Figure 4b. LVDS Common Mode Measurement

Related Product and Support Documentation

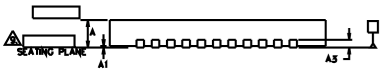
Part Number	Function	Data Sheet Link
SY89464U	Precision LVPECL Runt Pulse Eliminator 2 :1 MUX with 1:10 Fanout Buffer and Internal Termination	www.micrel.com/product-info/products/sy89464u.shtml.
	MLF™ Application Note	www.amkor.com/products/notes_papers/MLFAppNote.pdf
HBW Solutions	New Products and Applications	www.micrel.com/product-info/products/solutions.shtml

44 Lead *Micro*LeadFrame™ (MLF-44)

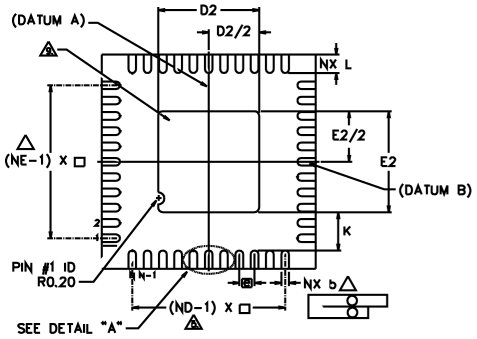


TOP VIEW

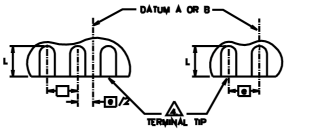
NOTES :
1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M. – 1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. θ IS IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
5. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
6. MAX. PACKAGE WARPAGE IS 0.05 mm.
7. MAXIMUM ALLOWABLE BURRS IS 0.076 mm IN ALL DIRECTIONS.
8. PIN #1 ID ON TOP WILL BE LASER MARKED.
9. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
10. THIS DRAWING CONFORMES TO JEDEC REGISTERED OUTLINE MO-220



SIDE VIEW



BOTTOM VIEW



EVEN TERMINAL/SIDE ODD TERMINAL/SIDE

DETAIL "A"

SYMBOL	DIMENSIONS			NOTE
	MIN.	NOM.	MAX.	
e		0.50 BSC		
N		44		3
ND		11		5
NE		11		
L	0.55	0.60	0.65	
b	0.18	0.25	0.30	4
D2	3.20	3.30	3.40	
E2	3.20	3.30	3.40	
D		7.00 BSC		
E		7.00 BSC		
A	0.80	0.85	1.00	
A1	0.00	0.02	0.05	
K		0.20 MIN.		
θ	0	——	12	2

Packages Notes:

1. Package meets Level 2 Moisture Sensitivity Classification.
2. All parts are dry-packed before shipment.
3. Exposed pad must be soldered to a ground for proper thermal management.

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