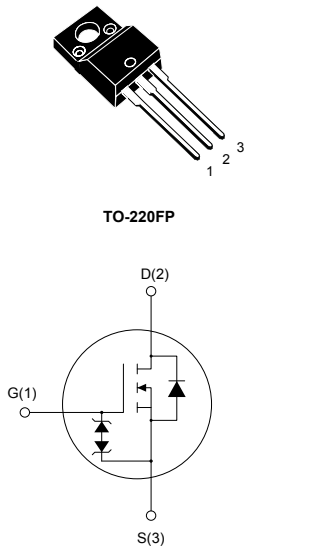


## N-channel 650 V, 0.75 $\Omega$ typ., 10 A MDmesh K3 Power MOSFET in a TO-220FP package



### Features

Order code	$V_{DS}$	$R_{DS(on)}$ max.	$I_D$
STF10N65K3	650 V	1 $\Omega$	10 A

- 100% avalanche tested
- Extremely high dv/dt capability
- Very low intrinsic capacitance
- Improved diode reverse recovery characteristics
- Zener-protected

### Applications

- Switching applications

### Description

This MDmesh K3 Power MOSFET is the result of improvements applied to STMicroelectronics' MDmesh technology, combined with a new optimized vertical structure. This device boasts an extremely low on-resistance, superior dynamic performance and high avalanche capability, rendering it suitable for the most demanding applications.

#### Product status link

[STF10N65K3](#)

#### Product summary

<b>Order code</b>	STF10N65K3
<b>Marking</b>	10N65K3
<b>Package</b>	TO-220FP
<b>Packing</b>	Tube

# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage	650	V
$V_{GS}$	Gate-source voltage	±30	V
$I_D$	Drain current (continuous) at $T_C = 25\text{ °C}$	10	A
	Drain current (continuous) at $T_C = 100\text{ °C}$	6.3	
$I_{DM}^{(1)}$	Drain current (pulsed)	40	A
$P_{TOT}$	Total power dissipation at $T_C = 25\text{ °C}$	35	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	12	V/ns
ESD	Gate-source human body model ( $R = 1.5\text{ k}\Omega$ , $C = 100\text{ pF}$ )	2.5	kV
$V_{ISO}$	Insulation withstand voltage (RMS) from all three leads to external heat sink ( $t = 1\text{ s}$ , $T_C = 25\text{ °C}$ )	2.5	kV
$T_{stg}$	Storage temperature range	-55 to 150	°C
$T_J$	Operating junction temperature range		°C

1. Pulse width is limited by safe operating area.

2.  $I_{SD} \leq 10\text{ A}$ ,  $di/dt = 100\text{ A}/\mu\text{s}$ ,  $V_{DS}(\text{peak}) < V_{(BR)DSS}$ .

**Table 2. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thJC}$	Thermal resistance, junction-to-case	3.57	°C/W
$R_{thJA}$	Thermal resistance, junction-to-ambient	62.5	°C/W

**Table 3. Avalanche characteristics**

Symbol	Parameter	Value	Unit
$I_{AR}$	Avalanche current, repetitive or non-repetitive (pulse width limited by $T_J$ max.)	7.2	A
$E_{AS}$	Single pulse avalanche energy (starting $T_J = 25\text{ °C}$ , $I_D = I_{AR}$ , $V_{DD} = 50\text{ V}$ )	212	mJ

## 2 Electrical characteristics

$T_C = 25\text{ °C}$  unless otherwise specified.

**Table 4. Static**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$ , $I_D = 1\text{ mA}$	650	-	-	V
$I_{DSS}$	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$ , $V_{DS} = 650\text{ V}$	-	-	1	$\mu\text{A}$
		$V_{GS} = 0\text{ V}$ , $V_{DS} = 650\text{ V}$ , $T_C = 125\text{ °C}^{(1)}$	-	-	50	
$I_{GSS}$	Gate-body leakage current	$V_{DS} = 0\text{ V}$ , $V_{GS} = \pm 20\text{ V}$	-	-	$\pm 10$	$\mu\text{A}$
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 100\text{ }\mu\text{A}$	3	3.75	4.5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$ , $I_D = 3.6\text{ A}$	-	0.75	1	$\Omega$

1. Specified by design, not tested in production.

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 25\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0\text{ V}$	-	1180	-	pF
$C_{oss}$	Output capacitance		-	125	-	pF
$C_{rss}$	Reverse transfer capacitance		-	14	-	pF
$C_{oss\ eq.}^{(1)}$	Equivalent capacitance time related	$V_{DS} = 0\text{ to }520\text{ V}$ , $V_{GS} = 0\text{ V}$	-	77	-	pF
$R_g$	Intrinsic gate resistance	$f = 1\text{ MHz}$ , $I_D = 0\text{ A}$	-	3	-	$\Omega$
$Q_g$	Total gate charge	$V_{DD} = 520\text{ V}$ , $I_D = 7.2\text{ A}$ , $V_{GS} = 0\text{ to }10\text{ V}$ (see the <a href="#">Figure 15. Test circuit for gate charge behavior</a> )	-	42	-	nC
$Q_{gs}$	Gate-source charge		-	7.4	-	nC
$Q_{gd}$	Gate-drain charge		-	23	-	nC

1.  $C_{oss\ eq.}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$ .

**Table 6. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 310\text{ V}$ , $I_D = 3.5\text{ A}$ , $R_G = 4.7\text{ }\Omega$ , $V_{GS} = 10\text{ V}$	-	14.5	-	ns
$t_r$	Rise time		-	14	-	ns
$t_{d(off)}$	Turn-off delay time	(see the <a href="#">Figure 14. Test circuit for resistive load switching times and Figure 19. Switching time waveform</a> )	-	44	-	ns
$t_f$	Fall time		-	35	-	ns

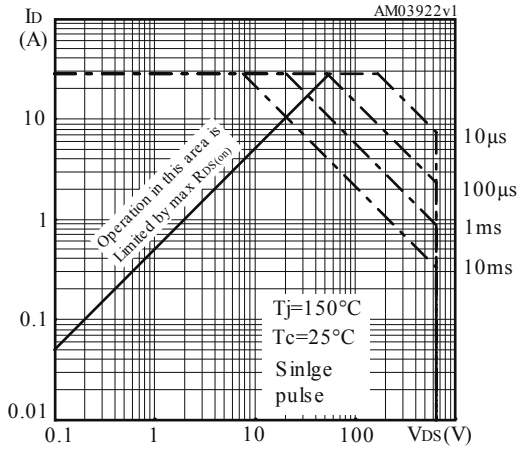
**Table 7. Source-drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-	-	7.2	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-	-	28.8	A
$V_{SD}^{(2)}$	Forward on voltage	$V_{GS} = 0\text{ V}$ , $I_{SD} = 7\text{ A}$	-	-	1.5	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 7\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ ,	-	320	-	ns
$Q_{rr}$	Reverse recovery charge	$V_{DD} = 60\text{ V}$	-	2	-	$\mu\text{C}$
$I_{RRM}$	Reverse recovery current	(see the Figure 16. Test circuit for inductive load switching and diode recovery times)	-	13	-	A
$t_{rr}$	Reverse recovery time	$I_{SD} = 7\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ ,	-	410	-	ns
$Q_{rr}$	Reverse recovery charge	$V_{DD} = 60\text{ V}$ , $T_J = 150\text{ }^\circ\text{C}$	-	2.9	-	$\mu\text{C}$
$I_{RRM}$	Reverse recovery current	(see the Figure 16. Test circuit for inductive load switching and diode recovery times)	-	14	-	A

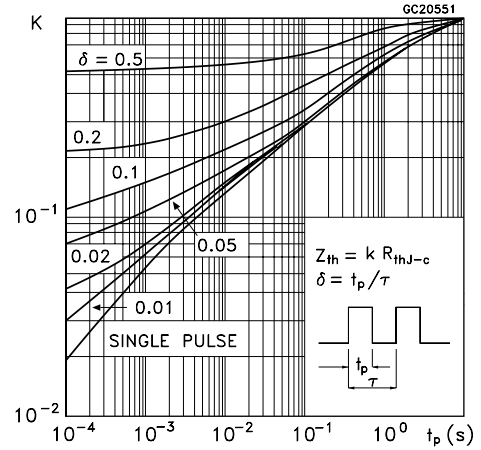
1. Pulse width is limited by safe operating area.
2. Pulse test: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%.

## 2.1 Electrical characteristics (curves)

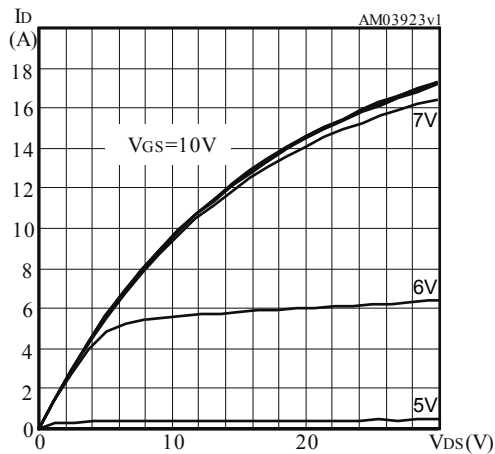
**Figure 1. Safe operating area**



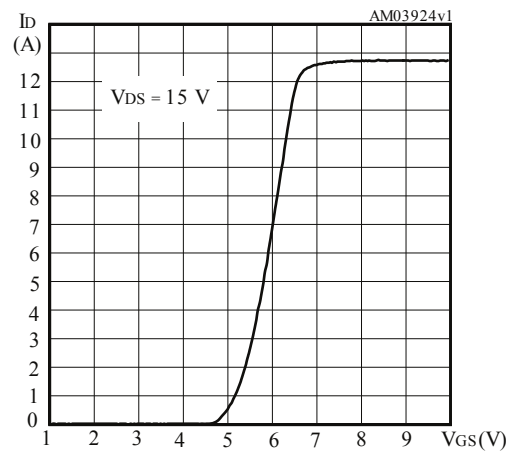
**Figure 2. Normalized transient thermal impedance**



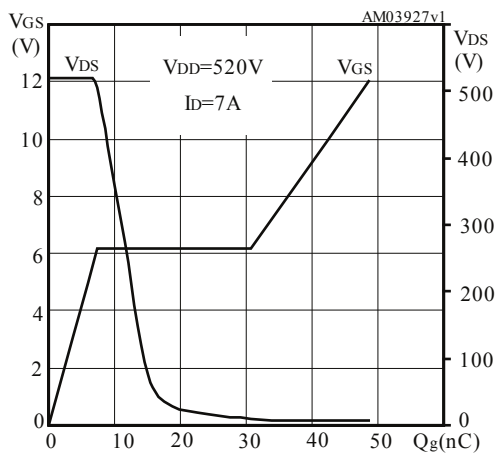
**Figure 3. Typical output characteristics**



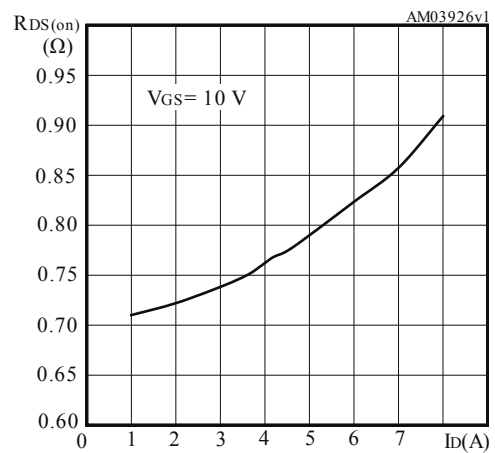
**Figure 4. Typical transfer characteristics**



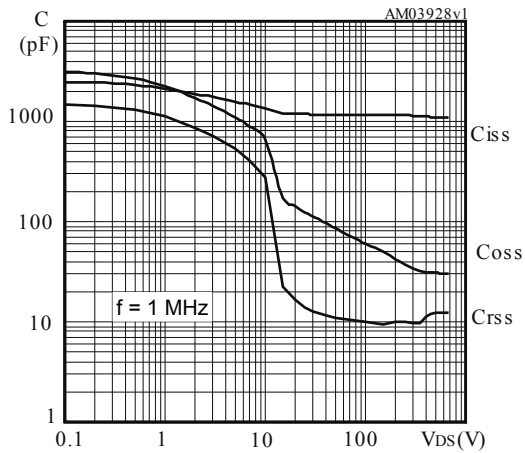
**Figure 5. Typical gate charge characteristics**



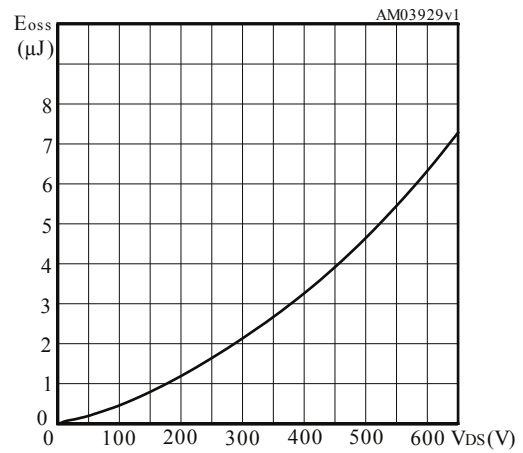
**Figure 6. Typical drain-source on-resistance**



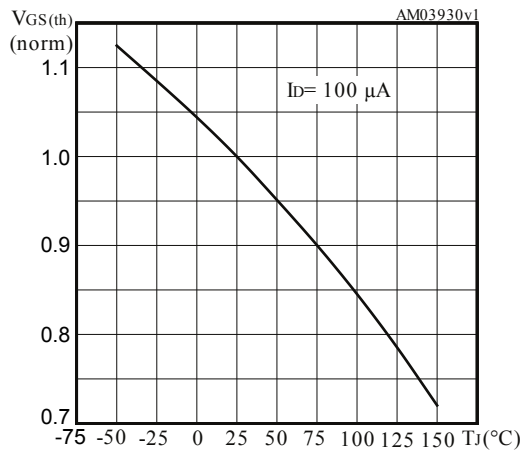
**Figure 7. Typical capacitance characteristics**



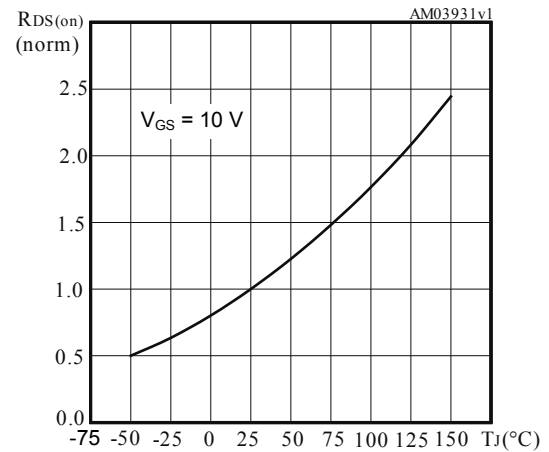
**Figure 8. Typical output capacitance stored energy**



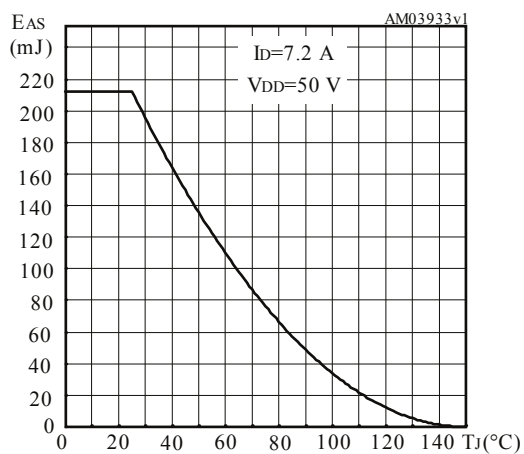
**Figure 9. Normalized gate threshold vs temperature**



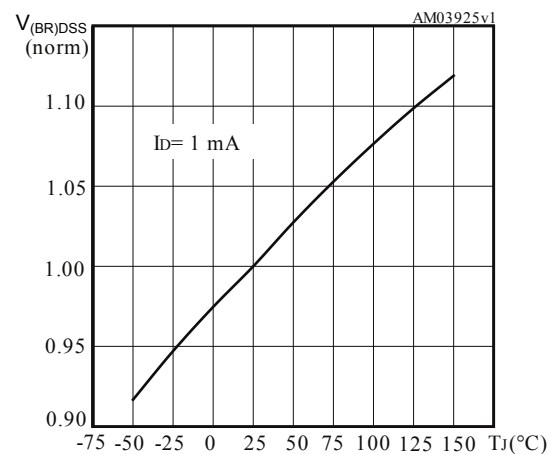
**Figure 10. Normalized on-resistance vs temperature**



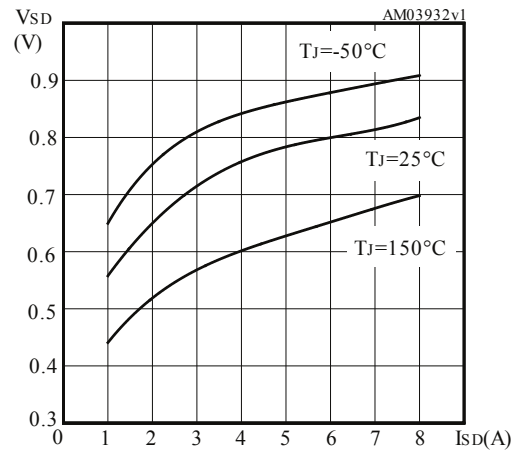
**Figure 11. Maximum avalanche energy vs temperature**



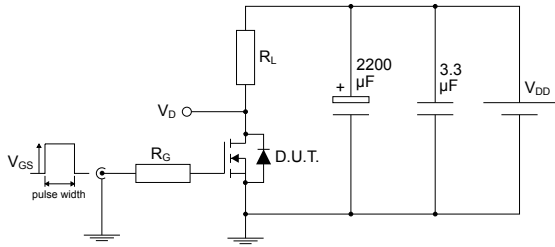
**Figure 12. Normalized breakdown voltage vs temperature**



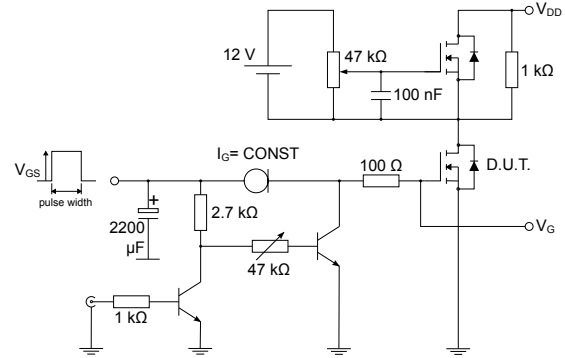
**Figure 13. Typical reverse diode forward characteristics**



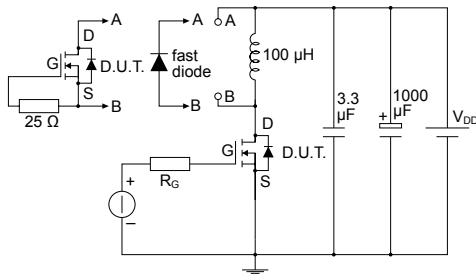
### 3 Test circuits

**Figure 14. Test circuit for resistive load switching times**


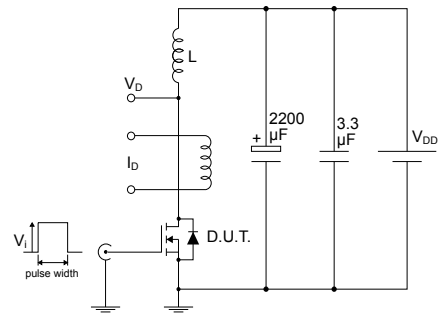
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**Figure 15. Test circuit for gate charge behavior**


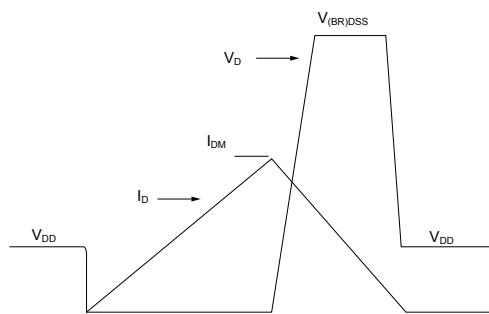
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**Figure 16. Test circuit for inductive load switching and diode recovery times**


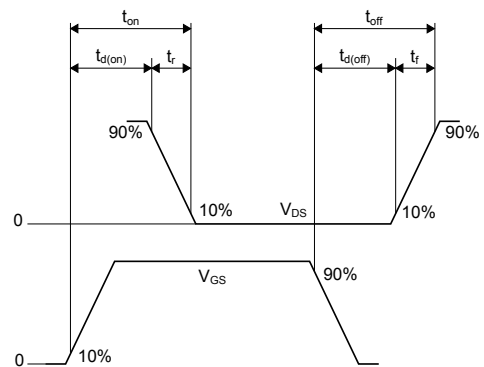
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**Figure 17. Unclamped inductive load test circuit**


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**Figure 18. Unclamped inductive waveform**


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**Figure 19. Switching time waveform**


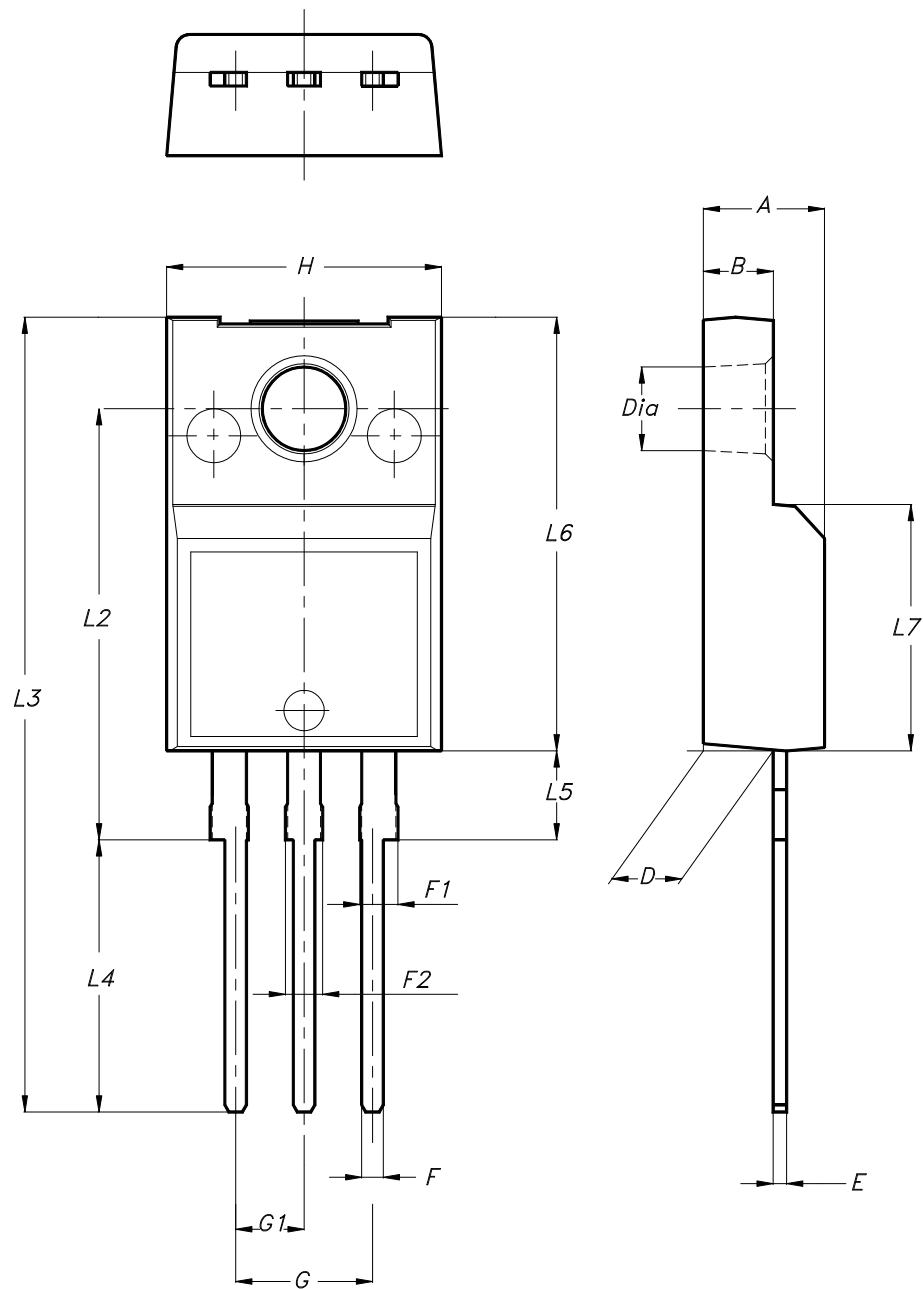
AM01473v1

## 4 Package information

To meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

### 4.1 TO-220FP type B package information

Figure 20. TO-220FP type B package outline



7012510\_B\_rev.14

**Table 8. TO-220FP type B package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
B	2.50		2.70
D	2.50		2.75
E	0.45		0.70
F	0.75		1.00
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.20
G1	2.40		2.70
H	10.00		10.40
L2		16.00	
L3	28.60		30.60
L4	9.80		10.60
L5	2.90		3.60
L6	15.90		16.40
L7	9.00		9.30
Dia	3.00		3.20

## Revision history

**Table 9. Document revision history**

Date	Revision	Changes
30-Jun-2009	1	First release.
14-Nov-2011	2	Updated mechanical data and <i>Section 2.1: Electrical characteristics (curves)</i> . Minor text changes.
14-Nov-2012	3	Added: I2PAKFP and TO-220. Deleted: $T_1$ row Added: $R_{DS(on)}$ typical value, <i>Figure 2</i> and <i>3</i> . Modified: <i>Figure 2</i> . Updated: <i>Section 4: Package mechanical data</i> .
05-Aug-2013	4	Added: D <sup>2</sup> PAK package. Added: $R_{thj-pcb}$ in <i>Table 3</i> . Updated: figure <i>Figure 17, 18, 19</i> and <i>20</i> . Updated: <i>Section 4: Package mechanical data</i> and <i>Section 5: Packaging mechanical data</i> . Minor text changes.
27-Jan-2026	5	Removed order code STB10N65K3, STF10N65K3 and STP10N65K3. Updated <i>Section 4: Package information</i> . Minor text changes.



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