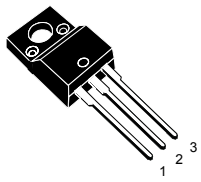
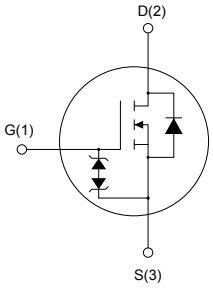
N-channel 650 V, 0.75 Ω typ., 10 A MDmesh K3 Power MOSFET in a TO-220FP package



TO-220FP



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Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STF10N65K3	650 V	1 Ω	10 A

- 100% avalanche tested
- Extremely high dv/dt capability
- Very low intrinsic capacitance
- Improved diode reverse recovery characteristics
- Zener-protected

Applications

- Switching applications

Description

This MDmesh K3 Power MOSFET is the result of improvements applied to STMicroelectronics' MDmesh technology, combined with a new optimized vertical structure. This device boasts an extremely low on-resistance, superior dynamic performance and high avalanche capability, rendering it suitable for the most demanding applications.

Product status link
STF10N65K3

Product summary	
Order code	STF10N65K3
Marking	10N65K3
Package	TO-220FP
Packing	Tube

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	650	V
V_{GS}	Gate-source voltage	±30	V
I_D	Drain current (continuous) at T_C = 25 °C	10	A
	Drain current (continuous) at T_C = 100 °C	6.3	
I_{DM}(1)	Drain current (pulsed)	40	A
P_{TOT}	Total power dissipation at T_C = 25 °C	35	W
dv/dt(2)	Peak diode recovery voltage slope	12	V/ns
ESD	Gate-source human body model (R = 1.5 kΩ, C = 100 pF)	2.5	kV
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t = 1 s, T_C = 25 °C)	2.5	kV
T_{stg}	Storage temperature range	-55 to 150	°C
T_J	Operating junction temperature range		°C

1. *Pulse width is limited by safe operating area.*
2. *I_{SD} ≤ 10 A, di/dt = 100 A/µs, V_{DS} (peak) < $V_{(BR)DSS}$.*

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case	3.57	°C/W
R_{thJA}	Thermal resistance, junction-to-ambient	62.5	°C/W

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or non-repetitive (pulse width limited by T_J max.)	7.2	A
E_{AS}	Single pulse avalanche energy (starting T_J = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	212	mJ

2 Electrical characteristics

T_C = 25 °C unless otherwise specified.

Table 4. Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	650	-	-	V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 650 V	-	-	1	µA
		V_{GS} = 0 V, V_{DS} = 650 V, T_C = 125 °C(1)	-	-	50	
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = ±20 V	-	-	±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 100 µA	3	3.75	4.5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 3.6 A	-	0.75	1	Ω

1. *Specified by design, not tested in production.*

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0 V	-	1180	-	pF
C_{oss}	Output capacitance		-	125	-	pF
C_{rss}	Reverse transfer capacitance		-	14	-	pF
$C_{oss\ eq.}$(1)	Equivalent capacitance time related	V_{DS} = 0 to 520 V, V_{GS} = 0 V	-	77	-	pF
R_g	Intrinsic gate resistance	f = 1 MHz, I_D = 0 A	-	3	-	Ω
Q_g	Total gate charge	V_{DD} = 520 V, I_D = 7.2 A, V_{GS} = 0 to 10 V (see the Figure 15. Test circuit for gate charge behavior)	-	42	-	nC
Q_{gs}	Gate-source charge		-	7.4	-	nC
Q_{gd}	Gate-drain charge		-	23	-	nC

1. *$C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.*

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 310 V, I_D = 3.5 A, R_G = 4.7 Ω, V_{GS} = 10 V (see the Figure 14. Test circuit for resistive load switching times and Figure 19. Switching time waveform)	-	14.5	-	ns
t_r	Rise time		-	14	-	ns
$t_{d(off)}$	Turn-off delay time		-	44	-	ns
t_f	Fall time		-	35	-	ns

Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-	-	7.2	A
I_{SDM}(1)	Source-drain current (pulsed)		-	-	28.8	A
V_{SD}(2)	Forward on voltage	V_{GS} = 0 V, I_{SD} = 7 A	-	-	1.5	V
t_{rr}	Reverse recovery time	I_{SD} = 7 A, di/dt = 100 A/µs, V_{DD} = 60 V (see the Figure 16. Test circuit for inductive load switching and diode recovery times)	-	320	-	ns
Q_{rr}	Reverse recovery charge		-	2	-	µC
I_{RRM}	Reverse recovery current		-	13	-	A
t_{rr}	Reverse recovery time	I_{SD} = 7 A, di/dt = 100 A/µs, V_{DD} = 60 V, T_J = 150 °C (see the Figure 16. Test circuit for inductive load switching and diode recovery times)	-	410	-	ns
Q_{rr}	Reverse recovery charge		-	2.9	-	µC
I_{RRM}	Reverse recovery current		-	14	-	A

1. *Pulse width is limited by safe operating area.*
2. *Pulse test: pulse duration = 300 µs, duty cycle 1.5%.*

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

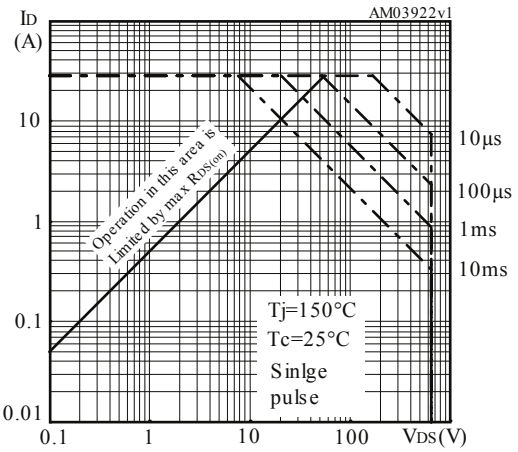


Figure 2. Normalized transient thermal impedance

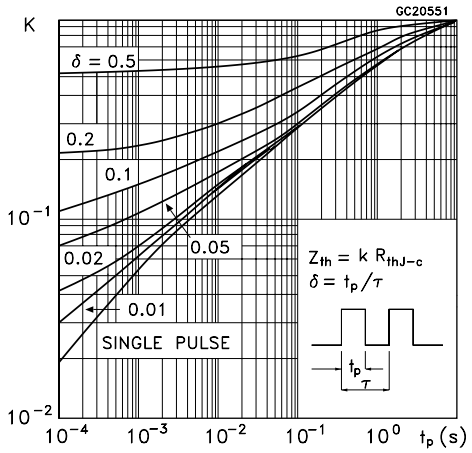


Figure 3. Typical output characteristics

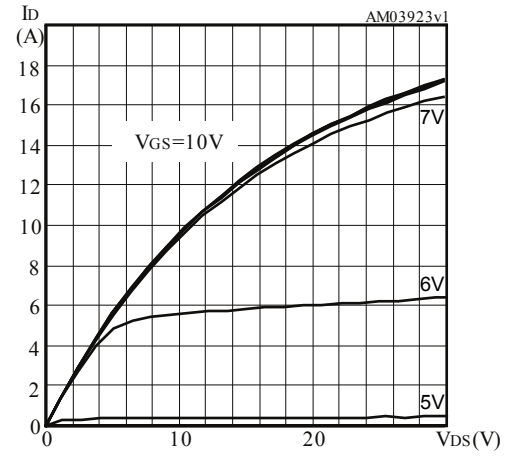


Figure 4. Typical transfer characteristics

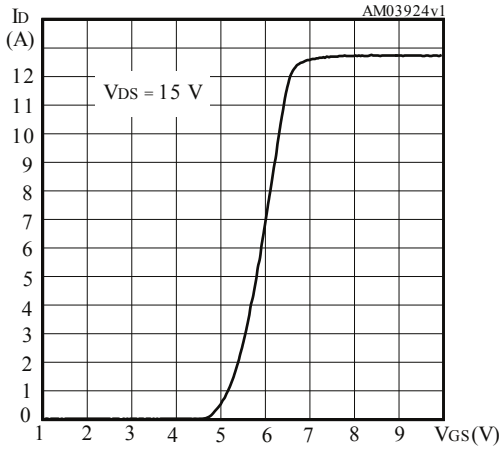


Figure 5. Typical gate charge characteristics

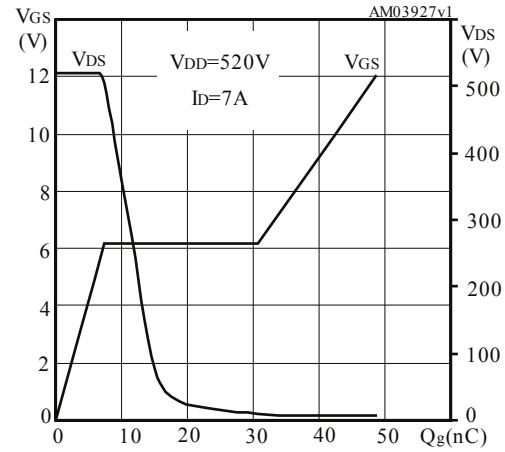


Figure 6. Typical drain-source on-resistance

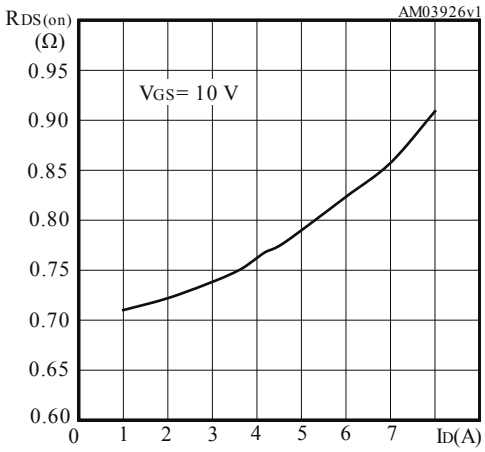


Figure 7. Typical capacitance characteristics

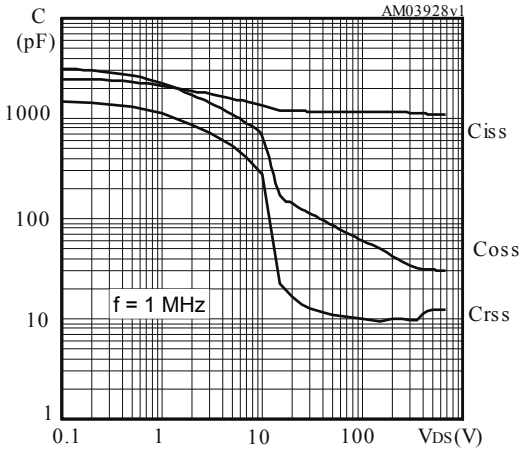


Figure 8. Typical output capacitance stored energy

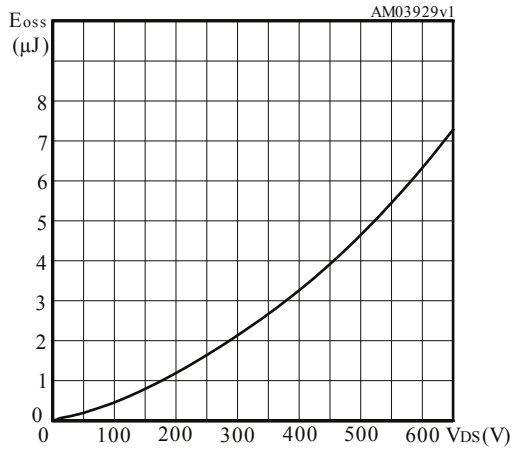


Figure 9. Normalized gate threshold vs temperature

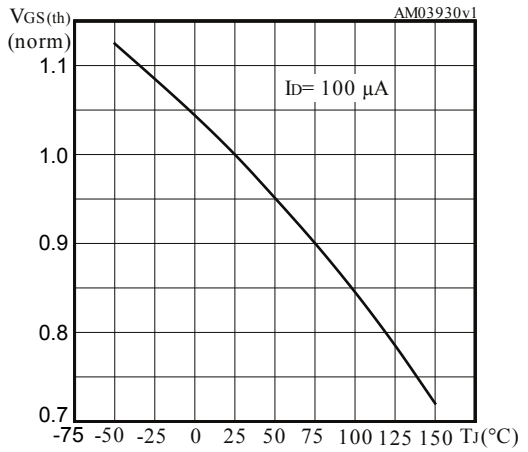


Figure 10. Normalized on-resistance vs temperature

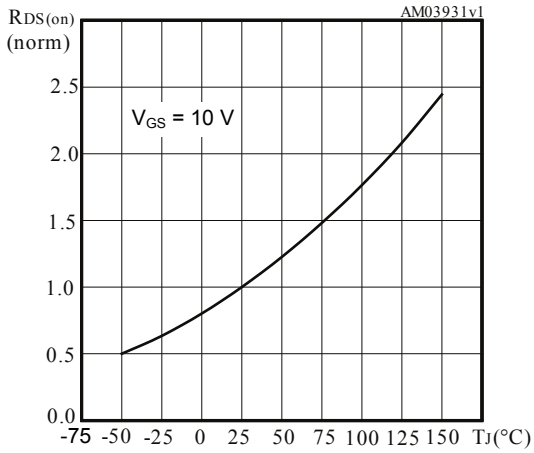


Figure 11. Maximum avalanche energy vs temperature

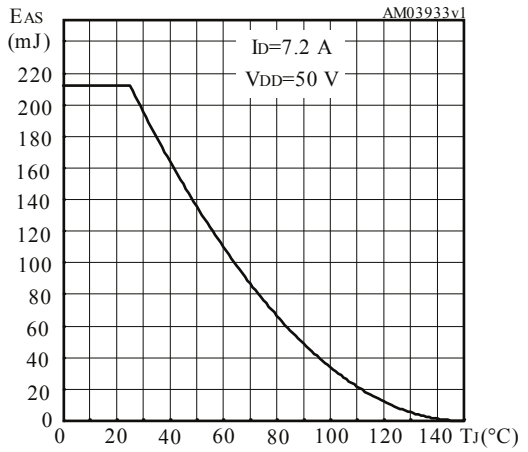


Figure 12. Normalized breakdown voltage vs temperature

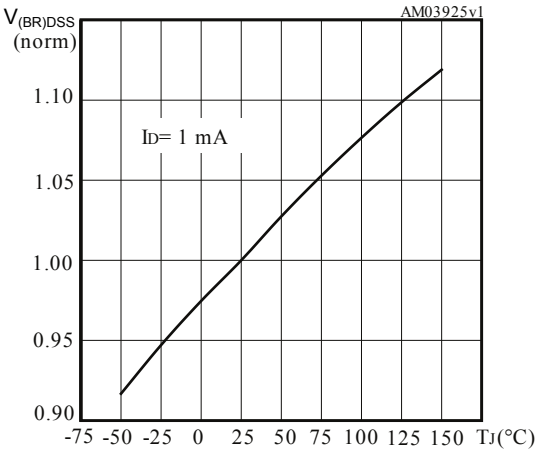
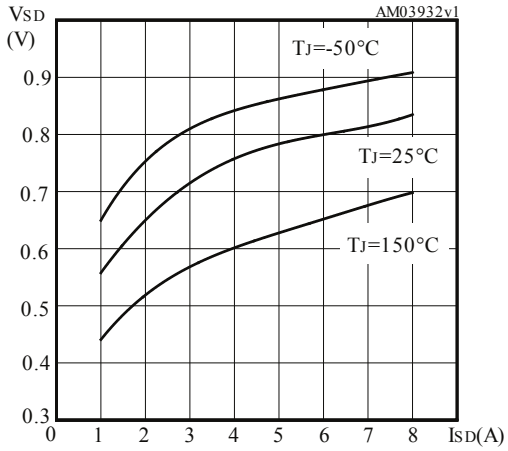


Figure 13. Typical reverse diode forward characteristics



3 Test circuits

Figure 14. Test circuit for resistive load switching times

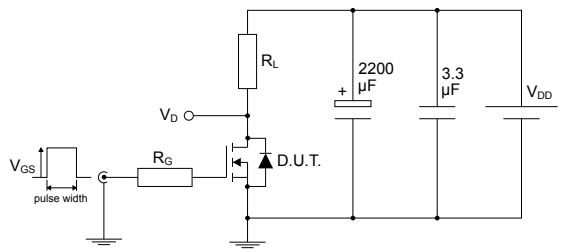


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Figure 15. Test circuit for gate charge behavior

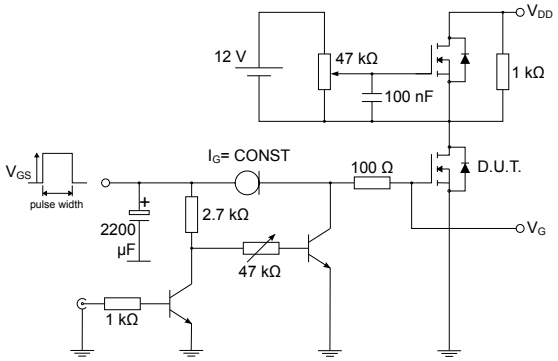

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Figure 16. Test circuit for inductive load switching and diode recovery times

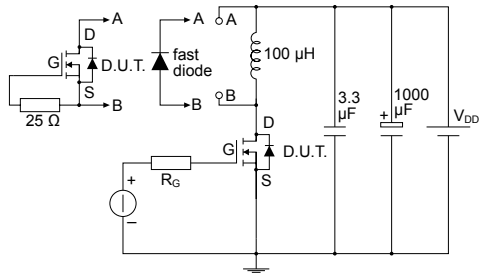

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Figure 17. Unclamped inductive load test circuit

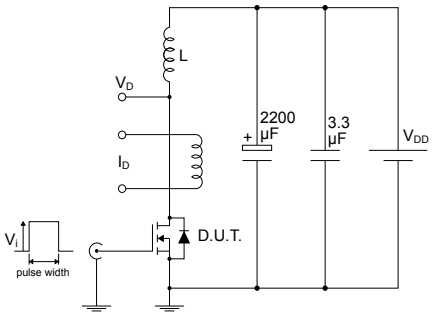

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Figure 18. Unclamped inductive waveform

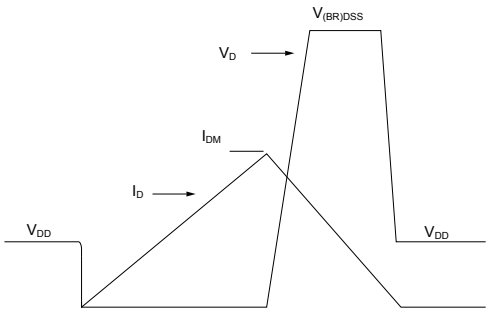

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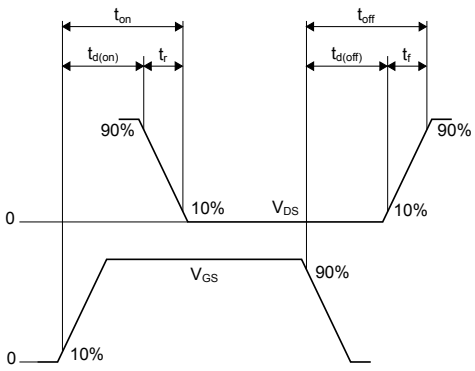
Figure 19. Switching time waveform



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4 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 TO-220FP type B package information

Figure 20. TO-220FP type B package outline

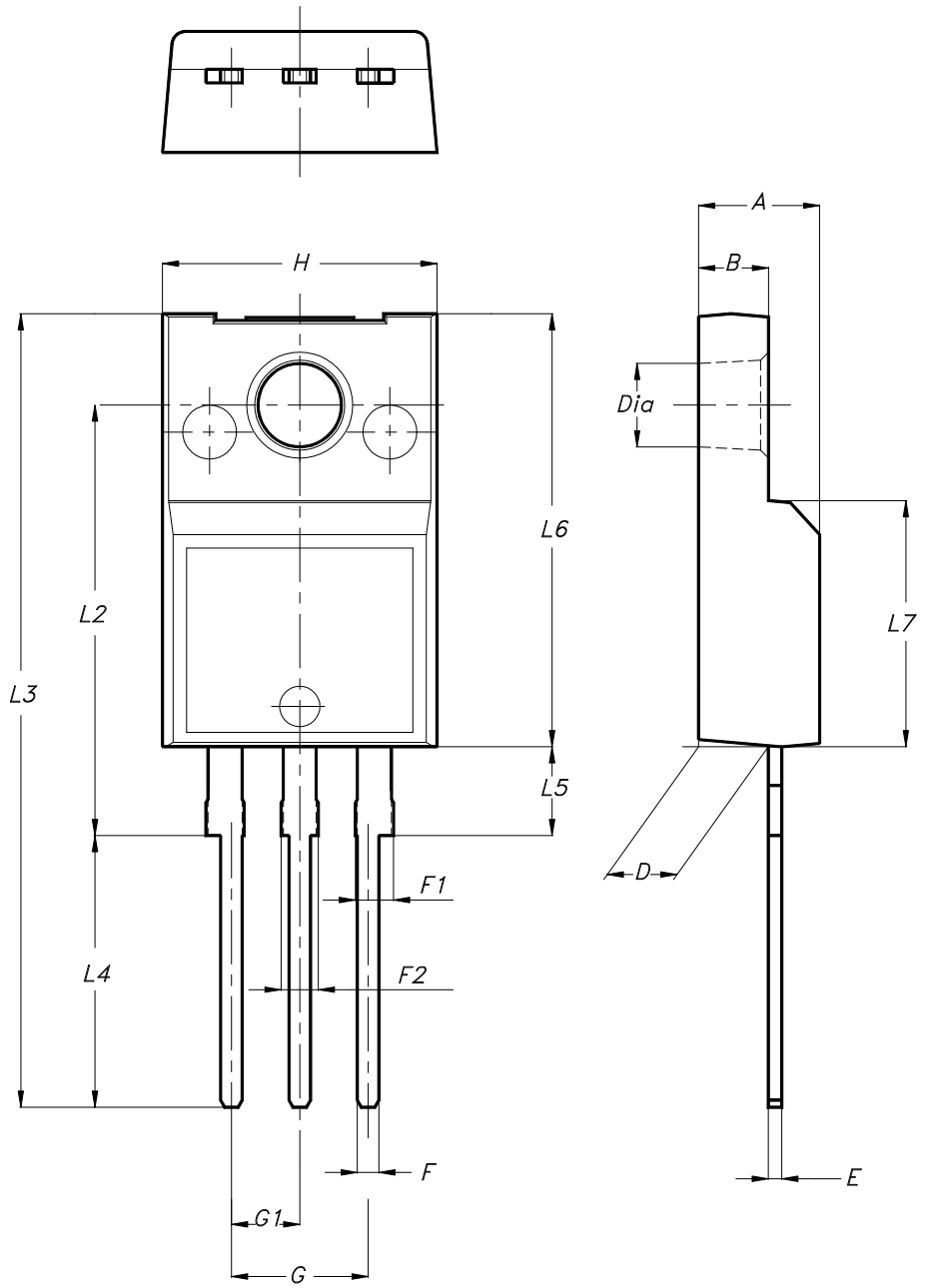

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Table 8. **TO-220FP type B package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
B	2.50		2.70
D	2.50		2.75
E	0.45		0.70
F	0.75		1.00
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.20
G1	2.40		2.70
H	10.00		10.40
L2		16.00	
L3	28.60		30.60
L4	9.80		10.60
L5	2.90		3.60
L6	15.90		16.40
L7	9.00		9.30
Dia	3.00		3.20

Revision history

Table 9. **Document revision history**

Date	Revision	Changes
30-Jun-2009	1	First release.
14-Nov-2011	2	Updated mechanical data and *Section 2.1: Electrical characteristics (curves)*. Minor text changes.
14-Nov-2012	3	Added: I2PAKFP and TO-220. Deleted: T_I row Added: $R_{DS(on)}$ typical value, *Figure 2* and *3*. Modified: *Figure 2*. Updated: *Section 4: Package mechanical data*.
05-Aug-2013	4	Added: D^2PAK package. Added: $R_{thj\text{-}pcb}$ in *Table 3*. Updated: figure *Figure 17*, *18*, *19* and *20*. Updated: *Section 4: Package mechanical data* and *Section 5: Packaging mechanical data*. Minor text changes.
27-Jan-2026	5	Removed order code STB10N65K3, STFI10N65K3 and STP10N65K3. Updated Section 4: Package information. Minor text changes.

Contents