TOSHIBA BiCD Processor IC Silicon Monolithic

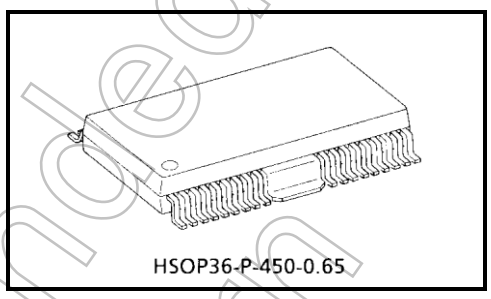
TB62209FG

Stepping Motor Driver IC Using PWM Chopper Type

The TB62209FG is a stepping motor driver driven by chopper micro-step pseudo sine wave.

The TB62209FG integrates a decoder for CLK input in micro steps as a system to facilitate driving a two-phase stepping motor using micro-step pseudo sine waves. Micro-step pseudo sine waves are optimal for driving stepping motors with low-torque ripples and at low oscillation. Thus, the TB62209FG can easily drive stepping motors with low-torque ripples and at high efficiency.

Also, TB62209FG consists of output steps by DMOS (Power MOS FET), and that makes it possible to control the output power dissipation much lower than ordinary IC with bipolar transistor output.



Weight: 0.79 g (typ.)

The IC supports Mixed Decay mode for switching the attenuation ratio at chopping. The switching time for the attenuation ratio can be switched in four stages according to the load.

Features

- Bipolar stepping motor can be controlled by a single driver IC
- Monolithic BiCD IC
- Low ON-resistance of R_{on} = 0.5 Ω (T_j = 25°C @1.0 A: typ.)
- Built-in decoder and 4-bit DA converters for micro steps
- Built-in ISD, TSD, V_{DD} &V_M power monitor (reset) circuit for protection
- Built-in charge pump circuit (two external capacitors)
- 36-pin power flat package (HSOP36-P-450-0.65)
- Output voltage: 40 V max
- Output current: 1.8 A/phase max
- 2-phase, 1-2 (type 2) phase, W1-2 phase, 2W1-2 phase, 4W1-2 phase, or motor lock mode can be selected.
- Built-in Mixed Decay mode enables specification of four-stage attenuation ratio.
- Chopping frequency can be set by external resistors and capacitors.
  High-speed chopping possible at 100 kHz or higher.

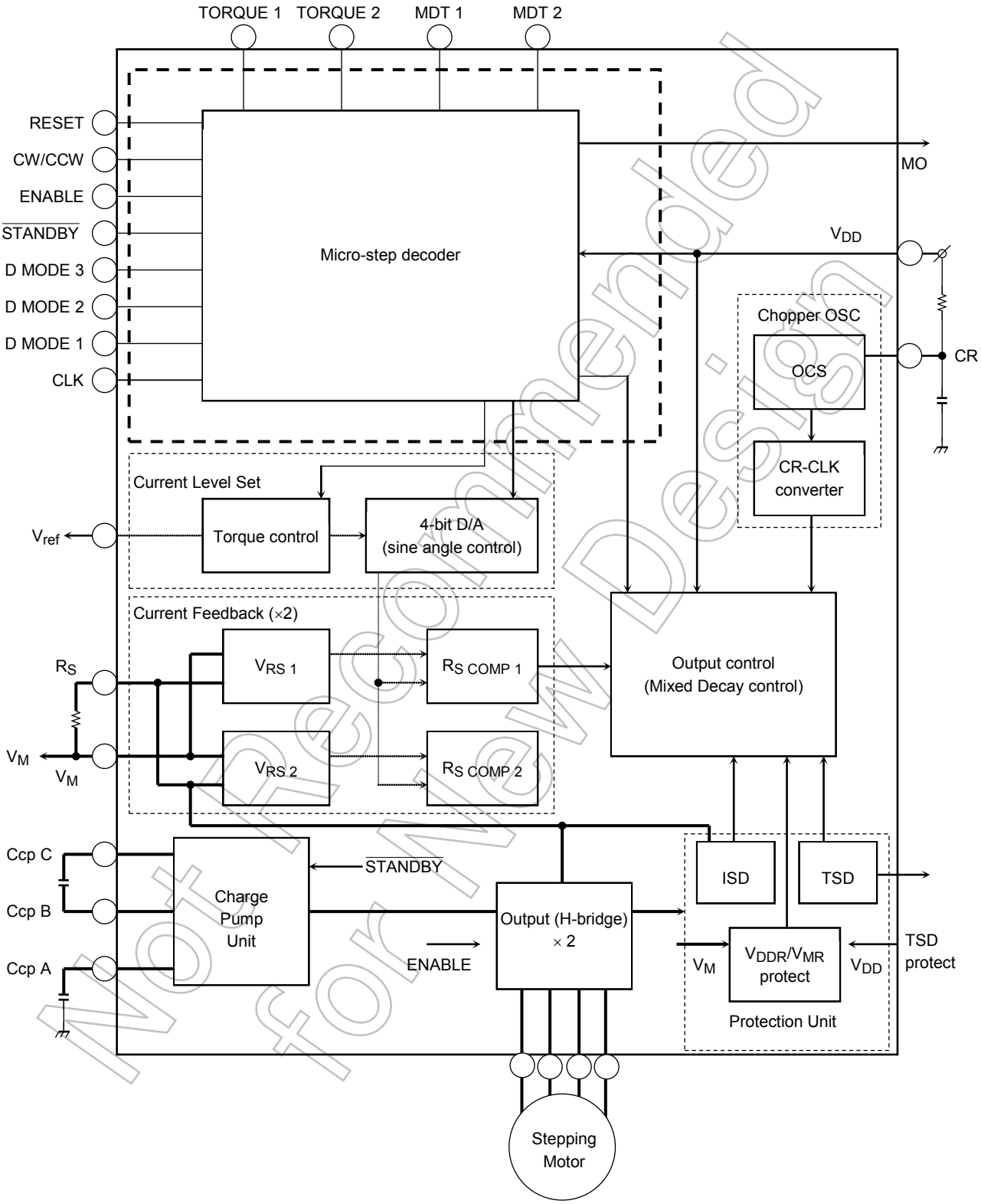
Note: When using the IC, pay attention to thermal conditions.

This device is easily damaged by high static voltage, please handle with care.

This product is RoHS compatible.

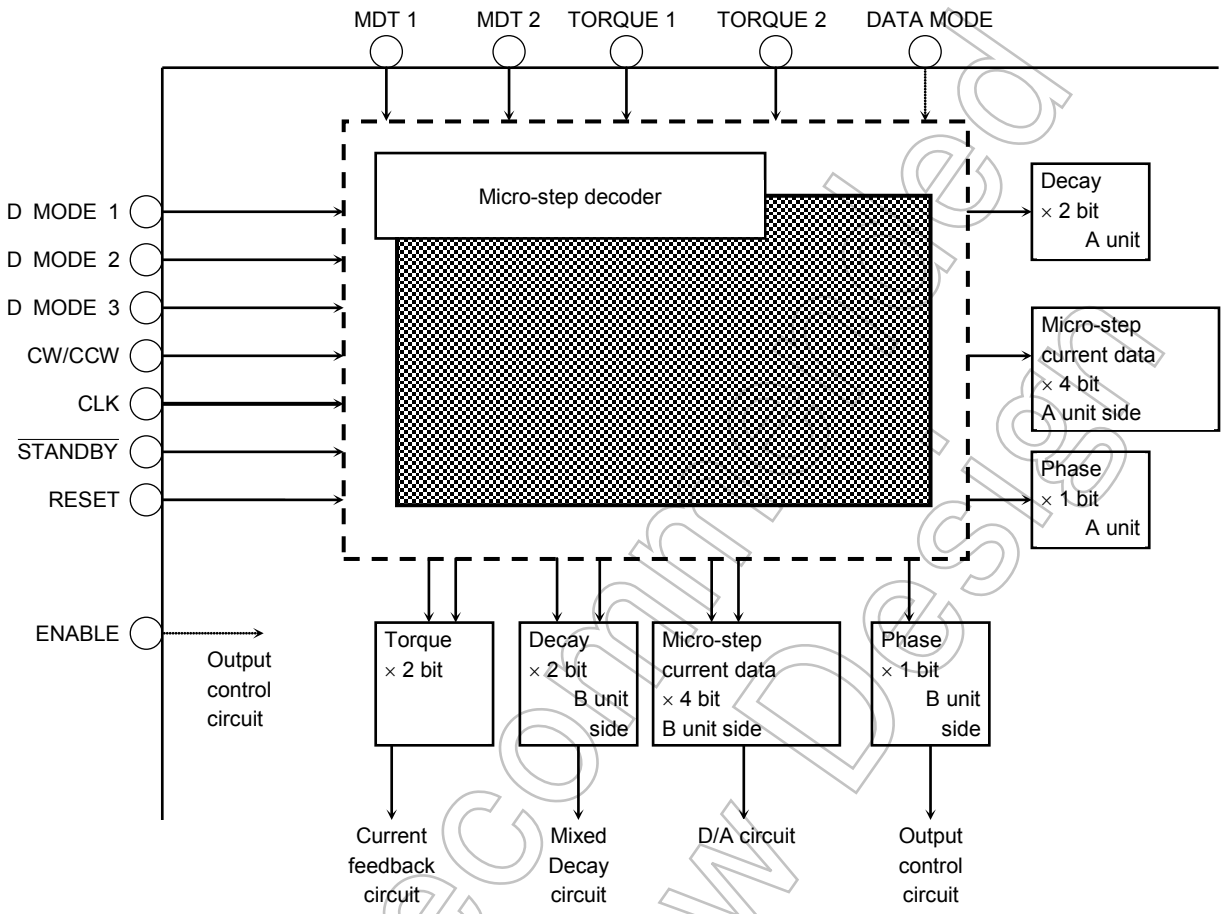
Block Diagram

1. Overview



2. LOGIC UNIT Function

The microstep electrical angle is output according to the logic of the PIN settings.



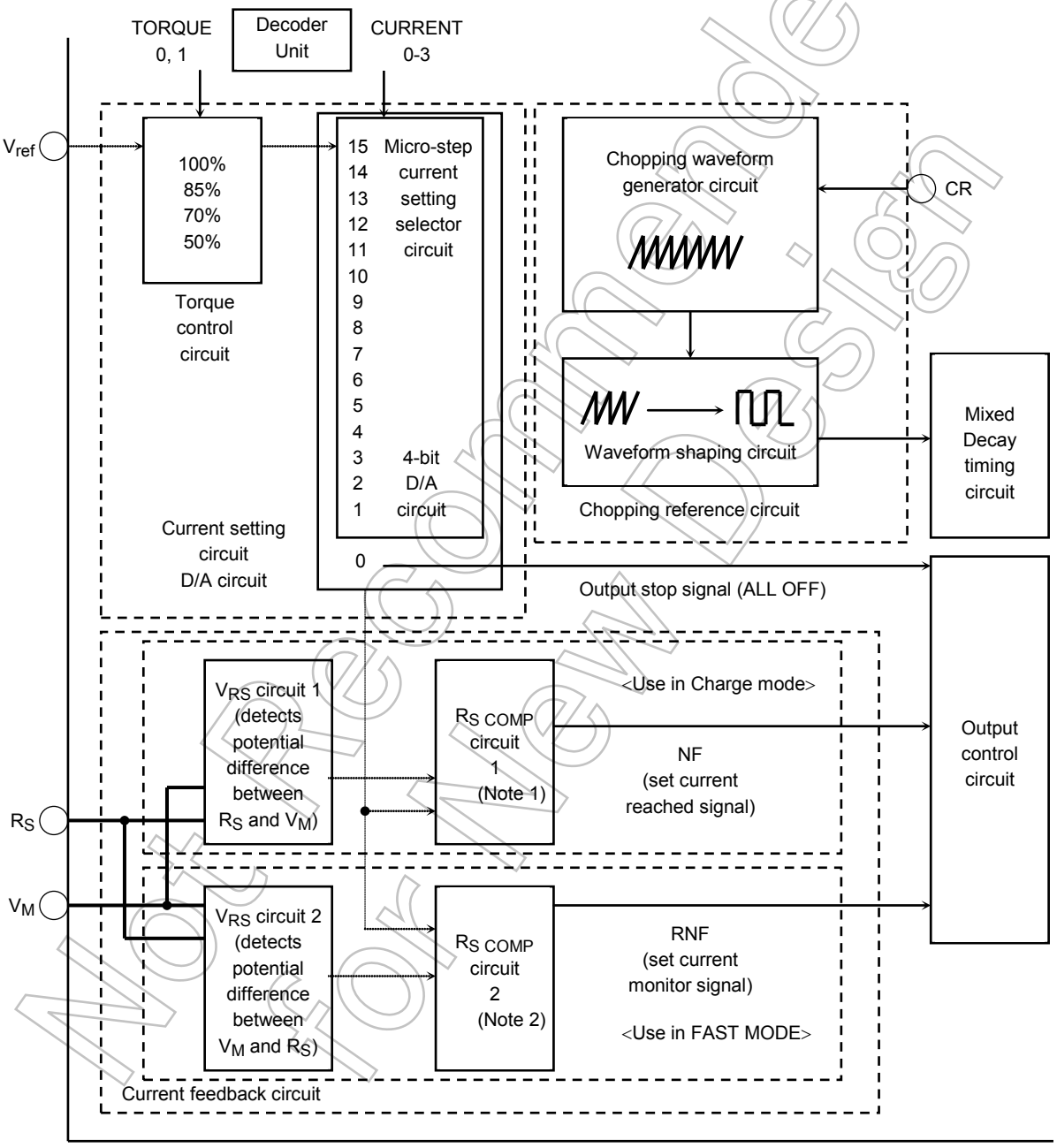
3. Current feedback circuit and current setting circuit

Function

The current setting circuit is used to set the reference voltage of the output current using the current setting decoder.

The current feedback circuit is used to output to the output control circuit the relation between the set current value and output current. This is done by comparing the reference voltage output to the current setting circuit with the potential difference generated when current flows through the current sense resistor connected between R_S and V_M.

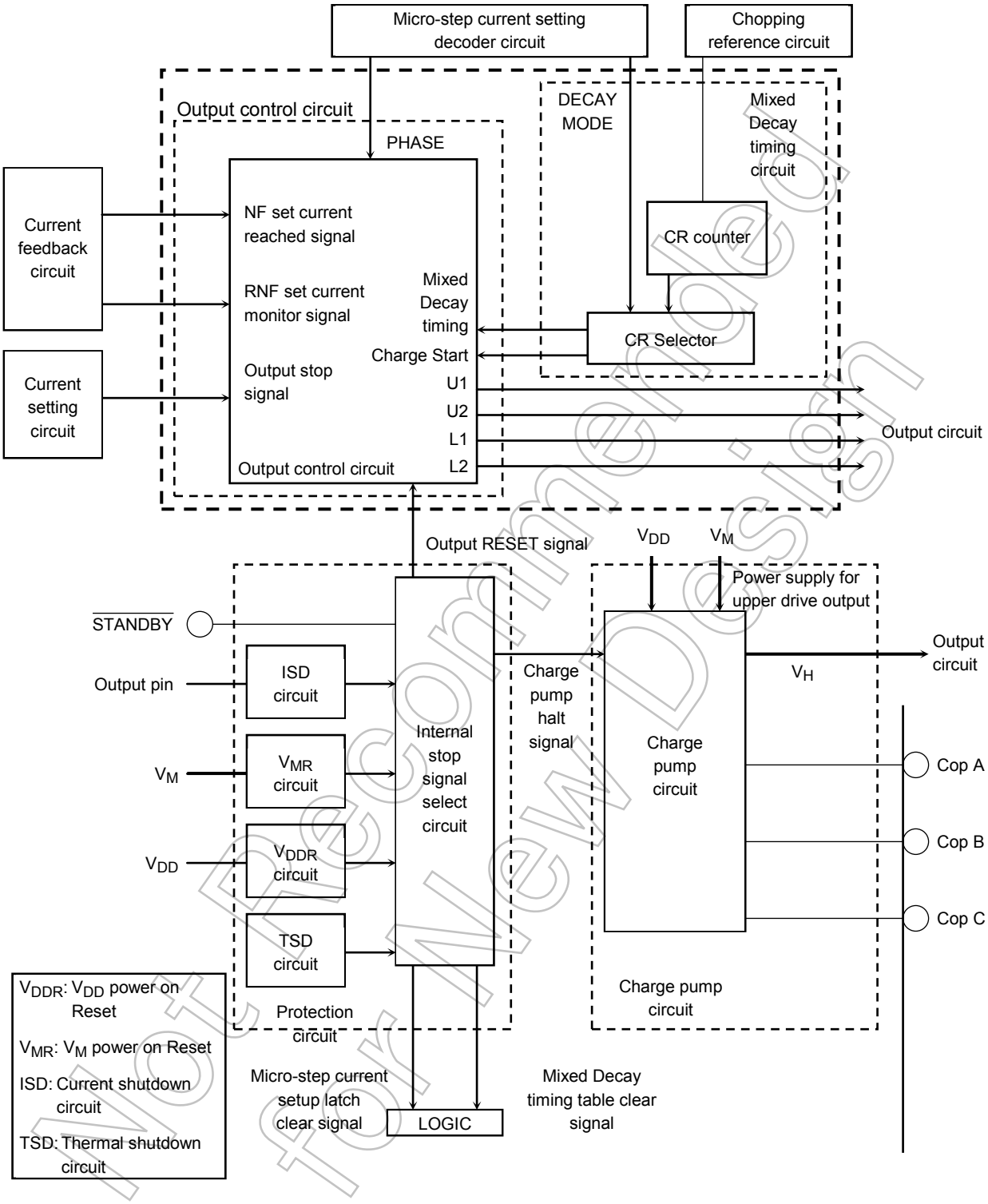
The chopping waveform generator circuit to which CR is connected is used to generate clock used as reference for the chopping frequency.



Note 1: $R_{S\ COMP1}$: Compares the set current with the output current and outputs a signal when the output current reaches the set current.

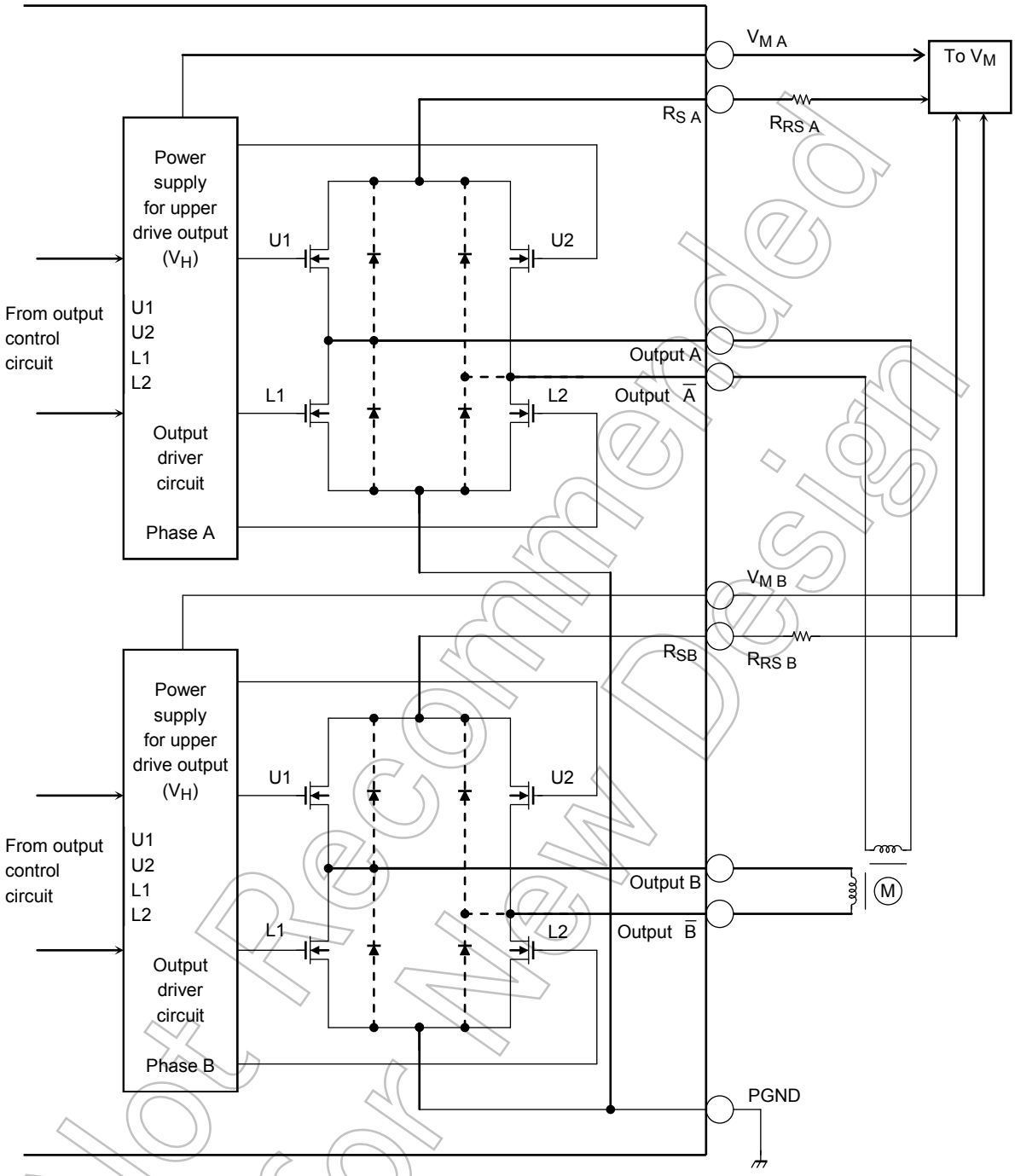
Note 2: $R_{S\ COMP2}$: Compares the set current with the output current at the end of Fast mode during chopping. Outputs a signal when the set current is below the output current.

4. Output control circuit, current feedback circuit and current setting circuit



Note: The $\overline{\text{STANDBY}}$ pins are pulled down in the IC by 100-kΩ resistor.
When not using the pin, connect it to GND. Otherwise, malfunction may occur.

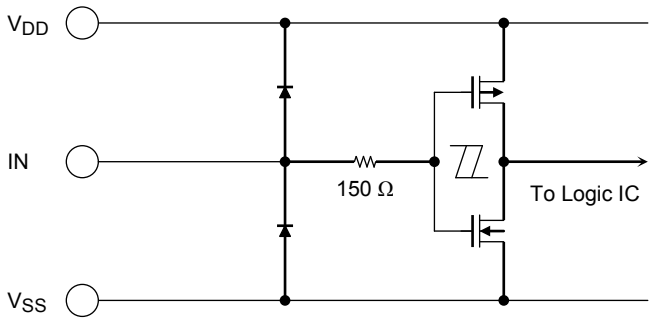
5. Output equivalent circuit



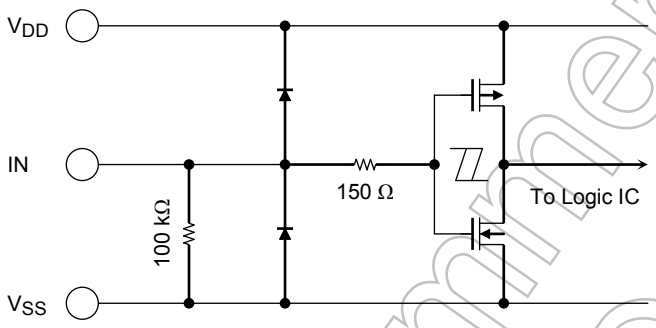
Note: The diode on the dotted line is a body diode.

6. Input equivalent circuit

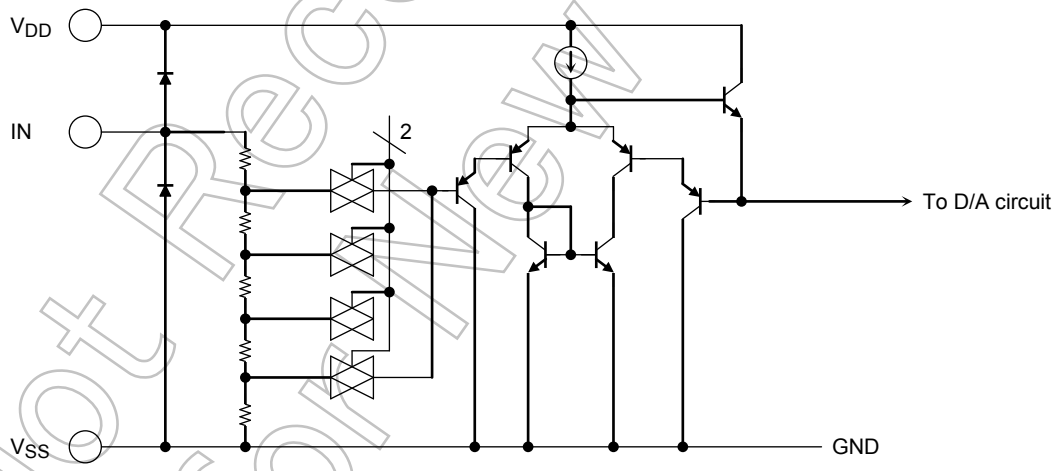
1. Input circuit (CLK, TORQUE, MDT, CW/CCW)



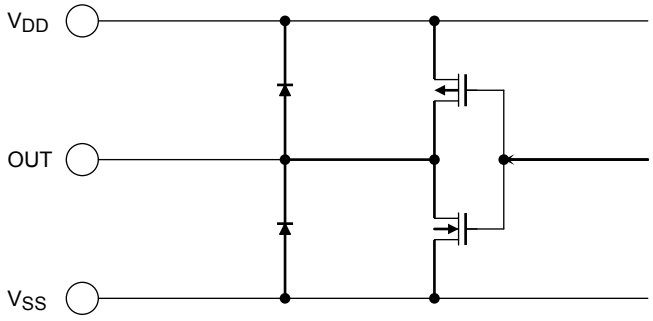
2. Input circuit (RESET, ENABLE, $\overline{\text{STANDBY}}$, DATA MODE, Drive Mode)



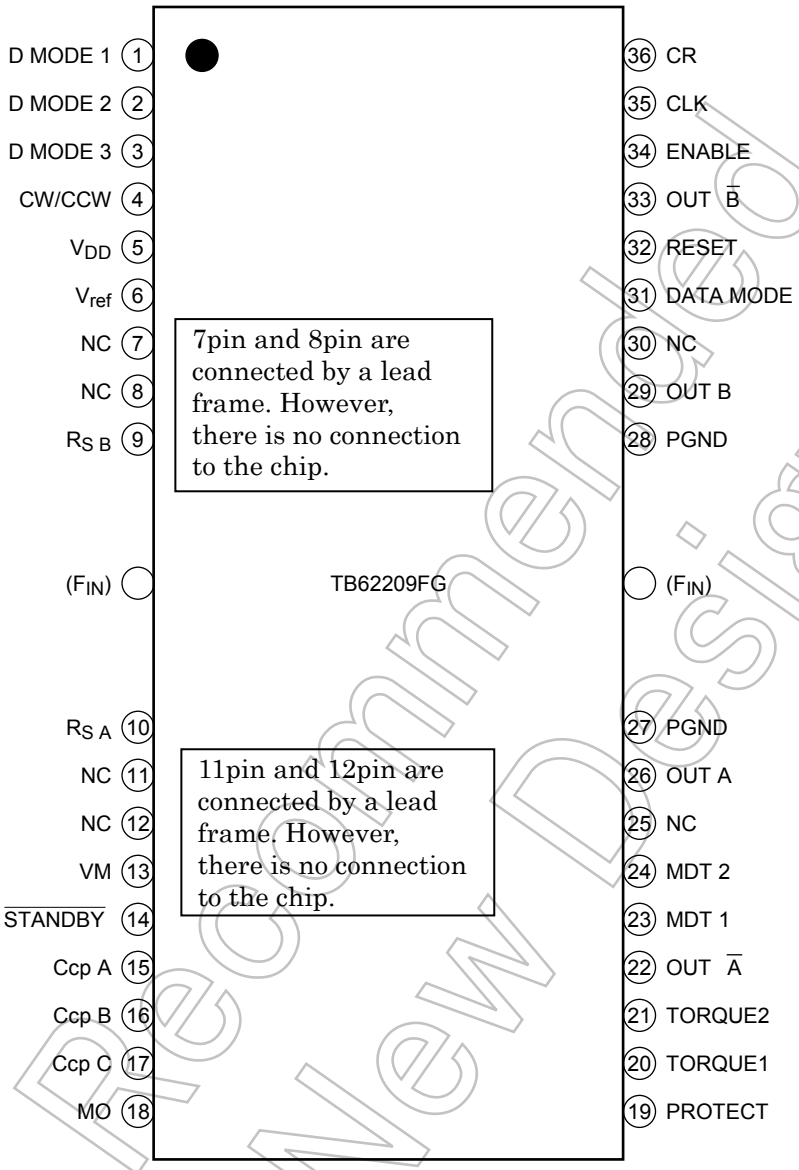
3. V_{ref} input circuit



4. Output circuit (MO, PROTECT)



Pin Assignment (top view)



Pin Assignment for PWM in Data Mode

D MODE 1 → GA+ (OUT A, $\overline{A}$)
D MODE 2 → GA− (OUT A, $\overline{A}$)
D MODE 3 → GB+ (OUT B, $\overline{B}$)
CW/CCW → GB− (OUT B, $\overline{B}$)

Note: Pin assignment above is different at data mode and PWM.

Pin Description 1

Pin Number	Pin Name	Function	Remarks
1	D MODE 1	Motor drive mode setting pin	D MODE 3, 2, 1 = LLL: Same function as that of $\overline{\text{STANDBY}}$ pin LLH: Motor Lock mode LHL: 2-Phase Excitation mode LHH: 1-2 Phase Excitation (A) mode HLL: 1-2 Phase Excitation (B) mode HLH: W1-2 Phase Excitation mode HHL: 2W1-2 Phase Excitation mode HHH: 4W1-2 Phase Excitation mode
2	D MODE 2		
3	D MODE 3		
4	CW/CCW	Sets motor rotation direction	CW: Forward rotation CCW: Reverse rotation
5	V_{DD}	Logic power supply connecting pin	Connect to logic power supply (5 V)
6	V_{ref}	Reference power supply pin for setting output current	Connect to supply voltage for setting current.
7	NC	Not connected	Not wired
8	NC	Not connected	Not wired
9	$R_{S\ B}$	Unit-B power supply pin (connecting pin for power detection resistor)	Connect current sensing resistor between this pin and V_M
F_{IN}	F_{IN}	FIN Logic ground pin	Connect to power ground The pin functions as a heat sink. Design pattern taking heat into consideration.
10	$R_{S\ A}$	Unit-A power supply pin (pin connecting power detection resistor)	Connect current sensing resistor between this pin and V_M
11	NC	Not connected	Not wired
12	NC	Not connected	Not wired

Pin Assignment for PWM in Data Mode

D MODE 1 → GA+ (OUT A, $\overline{\text{A}}$)
D MODE 2 → GA− (OUT A, $\overline{\text{A}}$)
D MODE 3 → GB+ (OUT B, $\overline{\text{B}}$)
CW/CCW → GB− (OUT B, $\overline{\text{B}}$)

Pin Description 2

Pin Number	Pin Name	Function	Remarks
13	V_M	Motor power supply monitor pin	Connect to motor power supply
14	$\overline{\text{STANDBY}}$	All-function-initializing and Low Power Dissipation mode pin	H: Normal operation L: Operation halted Charge pump output halted
15	Ccp A	Pin connecting capacitor for boosting output stage drive power supply (storage side connected to GND)	Connect capacitor for charge pump (storage side) V_M and V_{DD} are generated.
16	Ccp B	Pin connecting capacitor for boosting output stage drive power supply	Connect capacitor for charge pump (charging side) between this pin and Ccp C
17	Ccp C	(charging side)	Connect capacitor for charge pump (charging side) between this pin and Ccp B
18	MO	Electrical angle (0°) monitor pin	Outputs High level in 4W1-2, 2W1-2, W1-2, or 1-2 Phase Excitation mode with electrical angle of 0° (phase B: 100%, phase A: 0%) In 2-Phase Excitation mode, outputs High level with electrical angle of 0° (phase B: 100%, phase A: 100%)
19	PROTECT	TSD operation detector pin	Detects thermal shut down (TSD) and outputs High level
20	TORQUE 1	Motor torque switch setting pin	Torque 2, 1 = HH: 100% LH: 85% HL: 70% LL: 50%
21	TORQUE 2		
22	OUT $\overline{A}$	Channel $\overline{A}$ output pin	—
23	MDT 1	Mixed Decay mode setting pins	MDT 2, 1 = HH: 100% HL: 75% LH: 37.5% LL: 12.5%
24	MDT 2		

Pin Description 3

Pin Number	Pin Name	Function	Remarks
25	NC	Not connected	Not wired
26	OUT A	Channel A output pin	—
27	PGND	Power ground pin	Connect all power ground pins and V_{SS} to GND.
F_{IN}	F_{IN}	Logic ground pin	The pin functions as a heat sink. Design pattern taking heat into consideration.
28	PGND	Power ground pin	Connect all power ground pins to GND.
29	OUT B	Channel B output pin	—
30	NC	Not connected	Not wired
31	DATA MODE	Clock input and PWM	H: Controls external PWM. L: CLK-IN mode We recommend this pin normally be used as CLK-IN mode pin (Low). In PWM mode, functions such as constant current control do not operate. Fix DATA MODE at the L level.
32	RESET	Initializes electrical angle.	Forcibly initializes electrical angle. At this time we recommend ENABLE pin be set to Low to prevent miss operation. H: Resets electrical angle. L: Normal operation
33	OUT $\overline{B}$	Channel $\overline{B}$ output pin	—
34	ENABLE	Output enable pin	Forcibly turns all output transistors off.
35	CLK	Inputs CLK for determining number of motor rotations.	Electrical angle is incremented by one for each CLK input. CLK is reflected at rising edge.
36	CR	Chopping reference frequency reference pin (for setting chopping frequency)	Determines chopping frequency.

1. Function of CW/CCW

CW/CCW switches the direction of stepping motor rotation.

Input	Function
H	Forward (CW)
L	Reverse (CCW)

2. Function of MDT X

MDT X specifies the current attenuation speed at constant current control.

The larger the rate (%), the larger the attenuation of the current. Also, the peak current value (current ripple) becomes larger. (Typical value is 37.5%.)

MDT 2	MDT 1	Function
L	L	12.5% Mixed Decay mode
L	H	37.5% Mixed Decay mode
H	L	75% Mixed Decay mode
H	H	100% Mixed Decay mode (Fast Decay mode)

3. Function of TORQUE X

TORQUE X changes the current peak value in four steps. Used to change the value of the current used, for example, at startup and fixed-speed rotation.

TORQUE 2	TORQUE 1	Comparator Reference Voltage
H	H	100%
L	H	85%
H	L	70%
L	L	50%

4. Function of RESET (forced initialization of electrical angle)

With the CLK input method (decoder method), unless CLKs are counted, except MO, where the electrical angle is at that time not known. Thus, this method is used to forcibly initialize the electrical angle.

For example, it is used to change the excitation mode to another drive mode during output from MO (electrical angle = 0°).

Input	Function
H	Initializes electrical angle to 0°
L	Normal operation

5. Function of ENABLE (output operation)

ENABLE forcibly turns OFF all output transistors at operation.
Data such as electrical angle and operating mode are all retained.

Input	Function
H	Operation enabled (active)
L	Output halted (operation other than output active)

6. Function of $\overline{\text{STANDBY}}$

STANDBY halts the charge pump circuit (power supply booster circuit) as well as halts output.
We recommend setting to Standby mode at power on.
(At this time, data on the electrical angle are retained.)

Input	Function
H	Operation enabled (active)
L	Output halted (Low Power Dissipation mode)Charge pump halted

7. Functions of D Mode X (Excitation Mode)

	Excitation Mode	D Mode 3	D Mode 2	D Mode 1	Remarks
1	Low Power Dissipation mode	L	L	L	($\overline{\text{Standby}}$ mode) Charge pump halted
2	Motor Lock mode	L	L	H	Locks only at 0° electrical angle.
3	2-Phase Excitation mode	L	H	L	45° → 135° → 225° → 315° → 45°
4	1-2 Phase Excitation (A)	L	H	H	0%, 100% type 1-2 Phase Excitation
5	1-2 Phase Excitation (B)	H	L	L	0%, 71%, 100% type 1-2 Phase Excitation
6	W1-2 Phase Excitation	H	L	H	2-bit micro-step change
7	2W1-2 Phase Excitation	H	H	L	3-bit micro-step change
8	4W1-2 Phase Excitation	H	H	H	4-bit micro-step change

8. Function of DATA MODE

DATA MODE switches external duty control (forced PWM control) and constant current CLK-IN control. In Phase mode, H-bridge can be forcibly inverted and output only can be turned off. Constant current drive including micro-step drive can only be controlled in CLK-IN mode.

Input	Function
H	PHASE MODE
L	CLK-IN MODE

Note : Normally, use CLK-IN mode.

9. Electrical Angle Setting immediately after Initialization

In Initialize mode (immediately after RESET is released), the following currents are set.

In Low Power Dissipation mode, the internal decoder continues incrementing the electrical angle but current is not output.

Note that the initial electrical angle value in 2-Phase Excitation mode differs from that in nW1-2 (n = 0, 1, 2, 4) Phase Excitation mode.

	Excitation Mode	IB (%)	IA (%)	Remarks
1	Low Power Dissipation mode	100	0	Electrical angle incremented but no current output
2	Motor Lock mode	100	0	Electrical angle incremented but no motor rotation due to no IA output
3	2-Phase Excitation	100	100	45°
4	1-2 Phase Excitation (A)	100	0	0°
5	1-2 Phase Excitation (B)	100	0	0°
6	W1-2 Phase Excitation	100	0	0°
7	2W1-2 Phase Excitation	100	0	0°
8	4W1-2 Phase Excitation	100	0	0°

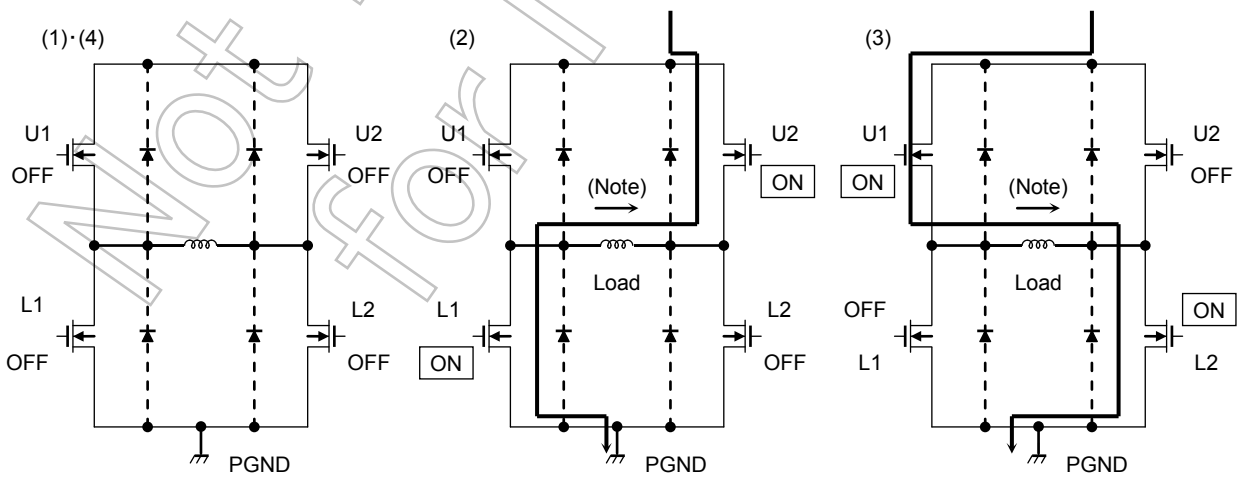
Note : Where, IB = 100% and IA = 0%, the electrical angle is 0°. Where, IB = 0% and IA = 100%, the electrical angle is +90°.

10. Function of DATA MODE (Phase A mode used for explanation)

DATA MODE inputs the external PWM signal (duty signal) and controls the current. Functions such as constant current control and overcurrent protector do not operate.

Use this mode only when control cannot be performed in CLK-IN mode.

	GA+	GA−	Output State
(1)	L	L	Output off
(2)	L	H	A+ phase: Low A− phase: High
(3)	H	L	A+ phase: High A− phase: Low
(4)	H	H	Output off



Note: Output is off at (1) and (4).

D MODE 1 → GA+ (OUT A, $\overline{A}$)

D MODE 2 → GA− (OUT A, $\overline{A}$)

D MODE 3 → GB+ (OUT B, $\overline{B}$)

CW/CCW → GB− (OUT B, $\overline{B}$)

Absolute Maximum Ratings (Ta = 25°C)

Characteristics		Symbol	Rating	Unit
Logic supply voltage		V_{DD}	7	V
Motor supply voltage		V_M	40	V
Output current	(Note 1)	I_{OUT}	1.8	A/phase
Current detect pin voltage		V_{RS}	$V_M \pm 4.5$ V	V
Charge pump pin maximum voltage (CCP1 Pin)		V_H	$V_M + 7.0$	V
Logic input voltage	(Note 2)	V_{IN}	-0.4 to V_{DD}+ 0.4	V
Power dissipation	(Note 3)	P_D	1.4	W
	(Note 4)		3.2	
Operating temperature		T_{opr}	−40 to 85	°C
Storage temperature		T_{stg}	−55 to 150	°C
Junction temperature		T_j	150	°C

Note 1: Perform thermal calculations for the maximum current value under normal conditions. Use the IC at 1.5 A or less per phase.
The current value may be controlled according to the ambient temperature or board conditions.

Note 2: Input 7 V or less as V_{IN}.

Note 3: Measured for the IC only. (Ta = 25°C)

Note 4: Measured when mounted on the board. (Ta = 25°C)

Ta: IC ambient temperature

T_{opr}: IC ambient temperature when starting operation

T_j: IC chip temperature during operation. T_j (max) is controlled by TSD (thermal shut down circuit).

Operating Conditions (Ta = 0 to 85°C, (Note 5))

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Power supply voltage	V_{DD}	—	4.5	5.0	5.5	V
Motor supply voltage	V_M	V_{DD} = 5.0 V, Ccp1 = 0.22 μF, Ccp2 = 0.022 μF	13	24	34	V
Output current	$I_{OUT\ (1)}$	Ta = 25°C, per phase	—	1.2	1.5	A
Logic input voltage	V_{IN}	—	GND	—	V_{DD}	V
Clock frequency	f_{CLK}	V_{DD} = 5.0 V	—	1.0	150	KHz
Chopping frequency	f_{chop}	V_{DD} = 5.0 V	50	100	150	KHz
Reference voltage	V_{ref}	V_M = 24 V, Torque = 100%	2.0	3.0	V_{DD}	V
Current detect pin voltage	V_{RS}	V_{DD} = 5.0 V	0	±1.0	±4.5	V

Note 5: Because the maximum value of T_j is 120°C, please design the maximum current to the value from which Tj becomes under 120°C.

Electrical Characteristics 1 (Ta = 25°C, V_{DD} = 5 V, V_M = 24 V, unless otherwise specified)

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Input voltage	HIGH	$V_{IN\ (H)}$	—	Data input pins	2.0	V_{DD}	V_{DD} + 0.4	V
	LOW	$V_{IN\ (L)}$			GND − 0.4	GND	0.8	
Input hysteresis voltage		$V_{IN\ (HIS)}$	—	Data input pins	200	400	700	mV
Input current		$I_{IN\ (H)}$	—	Data input pins with resistor	35	50	75	μA
		$I_{IN\ (H)}$		Data input pins without resistor	—	—	1.0	
		$I_{IN\ (L)}$			—	—	1.0	
Power dissipation (V_{DD} Pin)		I_{DD1}	—	V_{DD} = 5 V (STROBE, RESET, DATA = L), RESET = L, Logic, output all off	1.0	2.0	3.0	mA
		I_{DD2}		Output OPEN, f_{CLK} = 1.0 kHz LOGIC ACTIVE, V_{DD} = 5 V, Charge Pump = charged	1.0	2.5	3.5	
Power dissipation (V_M Pin)		I_{M1}	—	Output OPEN (STROBE, RESET, DATA = L), RESET = L, Logic, output all off, Charge Pump = no operation	1.0	2.0	3.0	mA
		I_{M2}		Output OPEN, f_{CLK} = 1 kHz LOGIC ACTIVE, V_{DD} = 5 V, V_M = 24 V, Output off, Charge Pump = charged	2.0	4.0	5.0	
		I_{M3}		Output OPEN, f_{CLK} = 4 kHz LOGIC ACTIVE, 100 kHz chopping (emulation), Output OPEN, Charge Pump = charged	—	10	13	
Output standby current	Upper	I_{OH}	—	V_{RS} = V_M = 24 V, V_{OUT} = 0 V, $\overline{STANDBY}$ = H, RESET = L, CLK = L	−200	−150	—	μA
Output bias current	Upper	I_{OB}	—	V_{OUT} = 0 V, $\overline{STANDBY}$ = H, RESET= L, CLK = L	−100	−50	—	μA
Output leakage current	Lower	I_{OL}	—	V_{RS} = V_M = CcpA = V_{OUT} = 24 V, LOGIC IN = ALL = L	—	—	1.0	μA
Comparator reference voltage ratio	HIGH (Reference)	$V_{RS\ (H)}$	—	V_{ref} = 3.0 V, V_{ref} (Gain) = 1/5.0 TORQUE = (H) = 100% set	—	100	—	%
	MID HIGH	$V_{RS\ (MH)}$		V_{ref} = 3.0 V, V_{ref} (Gain) = 1/5.0 TORQUE = (MH) = 85% set	83	85	87	
	MID LOW	$V_{RS\ (ML)}$		V_{ref} = 3.0 V, V_{ref} (Gain) = 1/5.0 TORQUE = (ML) = 70% set	68	70	72	
	LOW	$V_{RS\ (L)}$		V_{ref} = 3.0 V, V_{ref} (Gain) = 1/5.0 TORQUE = (L) = 50% set	48	50	52	
Output current differential		ΔI_{OUT1}	—	Differences between output current channels	−5	—	5	%
Output current setting differential		ΔI_{OUT2}	—	I_{OUT} = 1000 mA	−5	—	5	%
RS pin current		I_{RS}	—	V_{RS} = 24 V, V_M = 24 V, RESET= L (RESET state)	—	1	2	μA
Output transistor drain-source ON-resistance		$R_{ON\ (D\text{-}S)\ 1}$	—	I_{OUT} = 1.0 A, V_{DD} = 5.0 V T_j = 25°C, Drain-Source	—	0.5	0.6	Ω
		$R_{ON\ (D\text{-}S\ )\ 1}$		I_{OUT} = 1.0 A, V_{DD} = 5.0 V T_j = 25°C, Source-Drain	—	0.5	0.6	
		$R_{ON\ (D\text{-}S)\ 2}$		I_{OUT} = 1.0 A, V_{DD} = 5.0 V T_j = 105°C, Drain-Source	—	0.6	0.75	
		$R_{ON\ (D\text{-}S\ )\ 2}$		I_{OUT} = 1.0 A, V_{DD} = 5.0 V T_j = 105°C, Source-Drain	—	0.6	0.75	

Electrical Characteristics 2 (Ta = 25°C, V_{DD} = 5 V, V_M = 24 V, I_{OUT} = 1.0 A)

Characteristics	Symbol	Test Circuit	Test Condition		Min	Typ.	Max	Unit
Chopper current	Vector	—	θA = 90 (θ16)	—	—	100	—	%
			θA = 84 (θ15)		—	100	—	
			θA = 79 (θ14)		93	98	—	
			θA = 73 (θ13)		91	96	—	
			θA = 68 (θ12)		87	92	97	
			θA = 62 (θ11)		83	88	93	
			θA = 56 (θ10)		78	83	88	
			θA = 51 (θ9)		72	77	82	
			θA = 45 (θ8)		66	71	76	
			θA = 40 (θ7)		58	63	68	
			θA = 34 (θ6)		51	56	61	
			θA = 28 (θ5)		42	47	52	
			θA = 23 (θ4)		33	38	43	
			θA = 17 (θ3)		24	29	34	
			θA = 11 (θ2)		15	20	25	
			θA = 6 (θ1)		5	10	15	
			θA = 0 (θ0)		—	0	—	

Electrical Characteristics 3 (Ta = 25°C, V_{DD} = 5 V, V_M = 24 V, unless otherwise specified)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
V_{ref} input voltage	V_{ref}	9	V_M = 24 V, V_{DD} = 5 V, $\overline{STANDBY}$ = H, RESET = L, Output on, CLK = 1 kHz	2.0	—	V_{DD}	V
V_{ref} input current	I_{ref}	9	$\overline{STANDBY}$ = H, RESET = L, Output on, V_M = 24 V, V_{DD} = 5 V, V_{ref} = 3.0 V	20	35	50	μA
V_{ref} attenuation ratio	V_{ref} (GAIN)	—	V_M = 24 V, V_{DD} = 5 V, $\overline{STANDBY}$ = H, RESET= L, Output on, V_{ref} = 2.0 to V_{DD} − 1.0 V	1/4.8	1/5.0	1/5.2	—
TSD temperature (Note 1)	T_jTSD	—	V_{DD} = 5 V, V_M = 24 V	130	—	170	°C
TSD return temperature difference (Note 1)	ΔT_jTSD	—	T_jTSD = 130 to 170°C	T_jTSD − 50	T_jTSD − 35	T_jTSD − 20	°C
V_{DD} return voltage	V_{DDR}	10	V_M = 24 V, $\overline{STANDBY}$ = H	2.0	3.0	4.0	V
V_M return voltage	V_{MR}	11	V_{DD} = 5 V, $\overline{STANDBY}$ = H	2.0	3.5	5.0	V
Over current protected circuit operation current (Note 2)	ISD	—	V_{DD} = 5 V, V_M = 24 V	—	3.0	—	A
High temperature monitor pin output current	$I_{protect}$	12	V_{DD} = 5 V, TSD = operating condition	1.0	3.0	5.0	mA
Electrical angle monitor pin output current	I_{MO}	12	V_{DD} = 5 V, electrical angle = 0° (IB = 100%, IA = 0%)	1.0	3.0	5.0	mA
High temperature monitor pin output voltage	$V_{protect\ (H)}$	12	V_{DD} = 5 V, TSD = operating condition	—	—	5.0	V
	$V_{protect\ (L)}$	—	V_{DD} = 5 V, TSD = not operating condition	0.0	—	—	
Electrical angle monitor pin output voltage	$V_{MO2\ (H)}$	12	V_{DD} = 5 V, electrical angle = except 0° (IB = 100%, IA = Except 0% set)	—	—	5.0	V
	$V_{MO2\ (L)}$	—	V_{DD} = 5 V, electrical angle = 0° (IB = 100%, IA = 0%)	0.0	—	—	

Note 1: Thermal shut down circuit (TSD)
When the IC junction temperature reaches the specified value and the TSD circuit is activated, the internal reset circuit is activated switching the outputs of both motors to off.
When the temperature is set between 130°C (min) to 170°C (max), the TSD circuit operates. When the TSD is activated, the output of motors is stopped until the stand-by function is reset.
When the TSD circuit is activated, the charge pump is halted, and PROTECT pin outputs V_{DD} voltage.
Even if the TSD circuit is activated and $\overline{Standby}$ goes H → L → H instantaneously, the IC is not reset until the IC junction temperature drops −20°C (typ.) below the TSD operating temperature (hysteresis function).

Note 2: Overcurrent protection circuit (ISD)
When current exceeding the specified value flows to the output, the internal reset circuit is activated, and the ISD turns off the output.
Until the $\overline{Standby}$ signal goes Low to High, the overcurrent protection circuit remains activated.
During ISD, IC turns $\overline{Standby}$ mode and the charge pump halts.

AC Characteristics (Ta = 25°C, V_M = 24 V, V_{DD} = 5 V, 6.8 mH/5.7Ω)

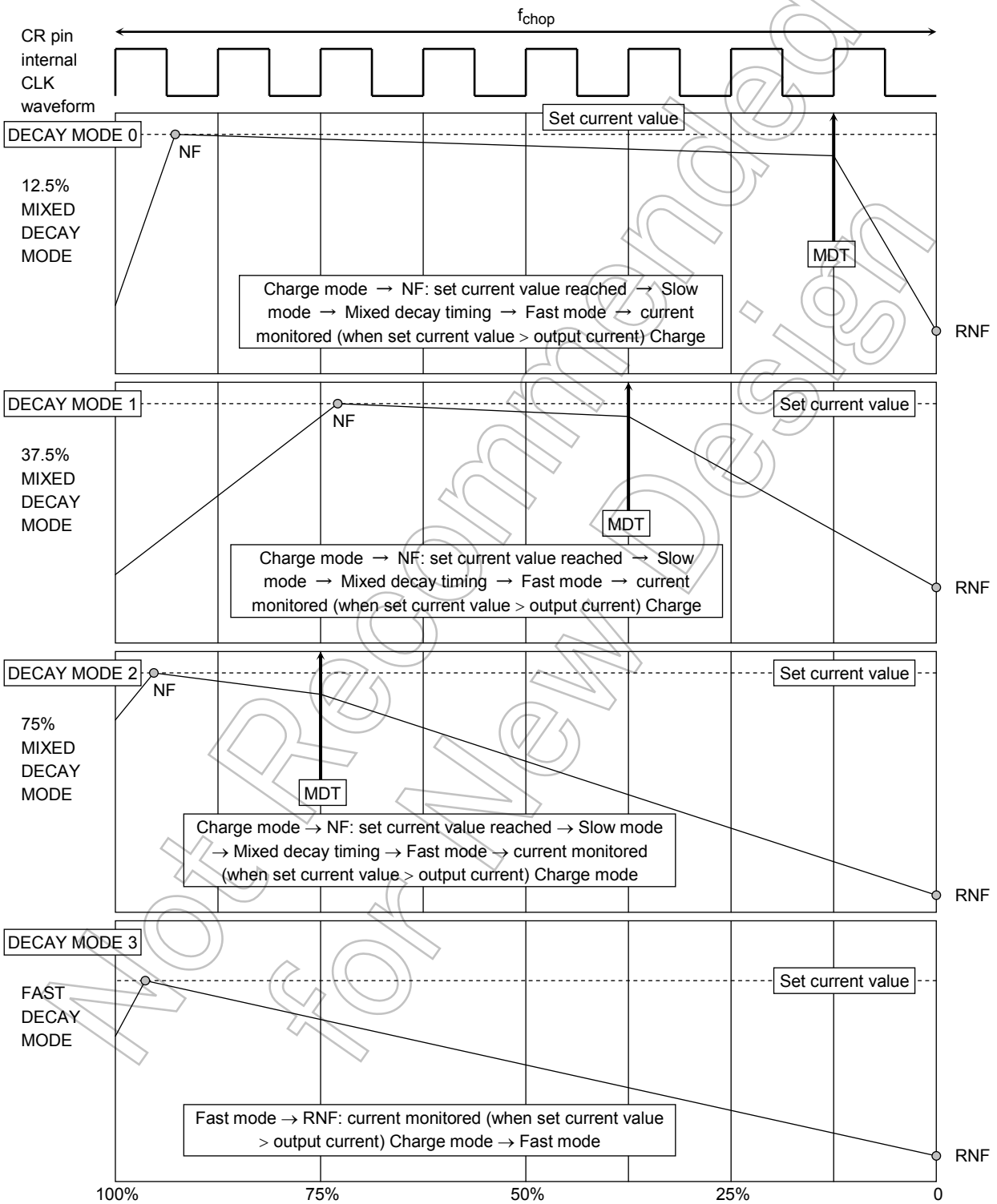
Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Clock frequency	f_{CLK}	—	—	—	—	120	kHz
Minimum clock pulse width	t_w (t_{CLK})	—	—	100	—	—	ns
	t_{wp}	—	—	50	—	—	
	t_{wn}	—	—	50	—	—	
Output transistor switching characteristic	t_r	—	Output Load: 6.8 mH/5.7 Ω	—	100	—	ns
	t_f	—	—	—	100	—	
	t_{pLH}	—	CLK to OUT	—	1000	—	
	t_{pHL}	—	Output Load: 6.8 mH/5.7 Ω	—	2000	—	
	t_{pLH}	—	CR to OUT	—	500	—	
	t_{pHL}	—	Output Load: 6.8 mH/5.7 Ω	—	1000	—	
Transistor switching characteristics (MO, PROTECT)	t_r	—	—	—	20	—	ns
	t_f	—	—	—	20	—	
	t_{pLH}	—	—	—	20	—	
	t_{pHL}	—	—	—	20	—	
Noise rejection dead band time	t_{BRANK}	—	I_{OUT} = 1.0 A	200	300	400	ns
CR reference signal oscillation frequency	f_{CR}	—	C_{osc} = 560 pF, R_{osc} = 3.6 kΩ	—	800	—	kHz
Chopping frequency range	$f_{chop\ (min)}$ $f_{chop\ (max)}$	—	V_M = 24 V, V_{DD} = 5 V, Output ACTIVE (I_{OUT} = 1.0 A) Step fixed, Ccp1 = 0.22 μF, Ccp2 = 0.022 μF	40	100	150	kHz
Chopping frequency	f_{chop}	—	Output ACTIVE (I_{OUT} = 1.0 A), CR CLK = 800 kHz	—	100	—	kHz
Charge pump rise time	t_{ONG}	—	Ccp = 0.22 μF, Ccp = 0.022 μF V_M = 24 V, V_{DD} = 5 V, $\overline{STANDBY}$ = ON L→ H	—	100	200	μs

11. Current Waveform and Setting of Mixed Decay Mode

At constant current control, in current amplitude (pulsating current) Decay mode, a point from 0 to 3 can be set using 2-bit parallel data.

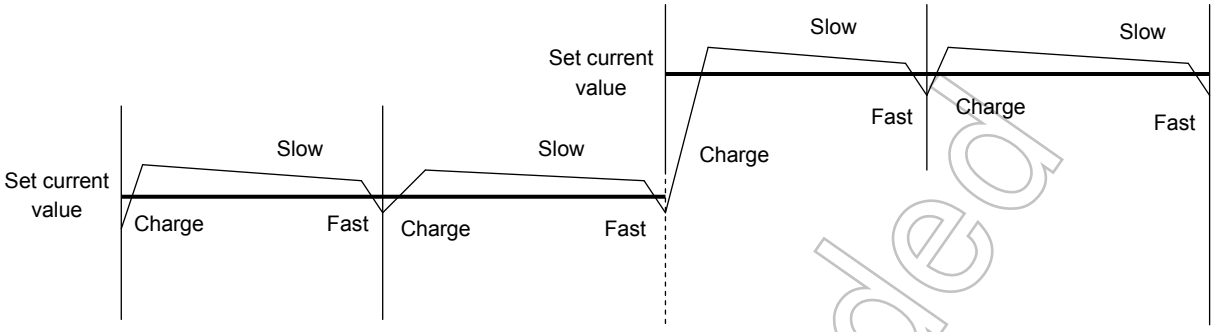
NF is the point where the output current reaches the set current value. RNF is the timing for monitoring the set current.

The smaller the MDT value, the smaller the current ripple (peak current value). Note that current decay capability deteriorates.

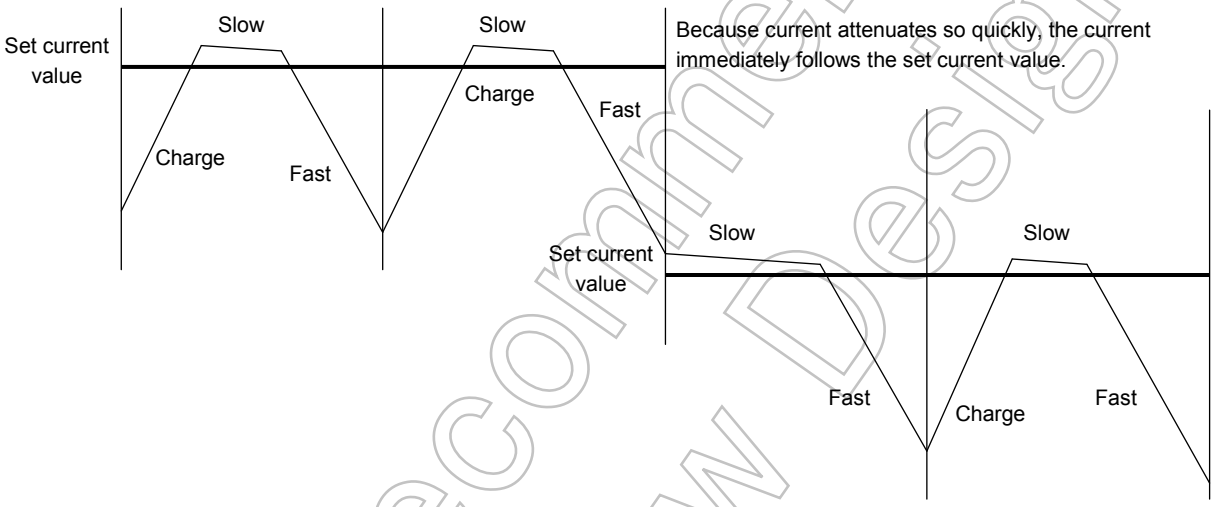


12. CURRENT MODES
(MIXED (SLOW + FAST) DECAY MODE Effect)

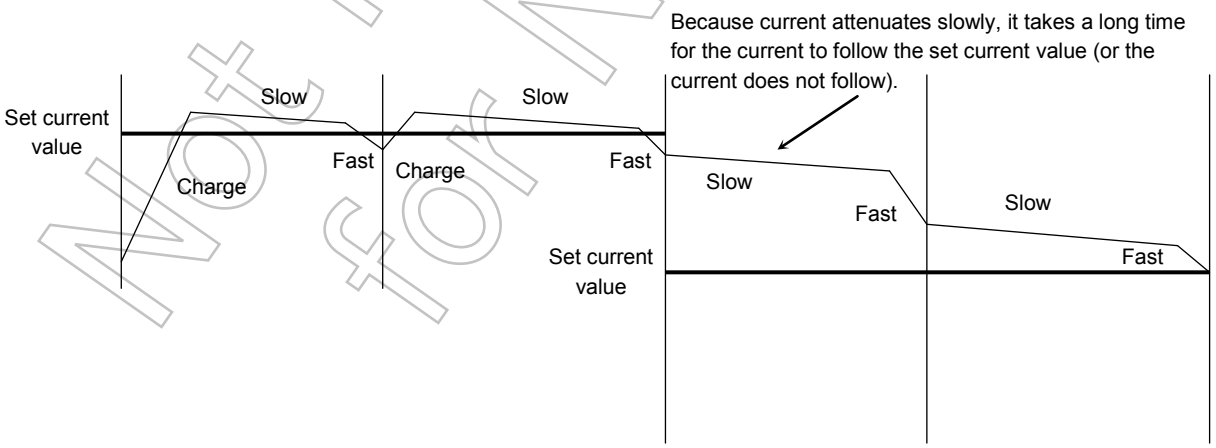
○ Current value in increasing (Sine wave)



○ Sine wave in decreasing (When using MIXED DECAY Mode with large attenuation ratio (MDT%) at attenuation)



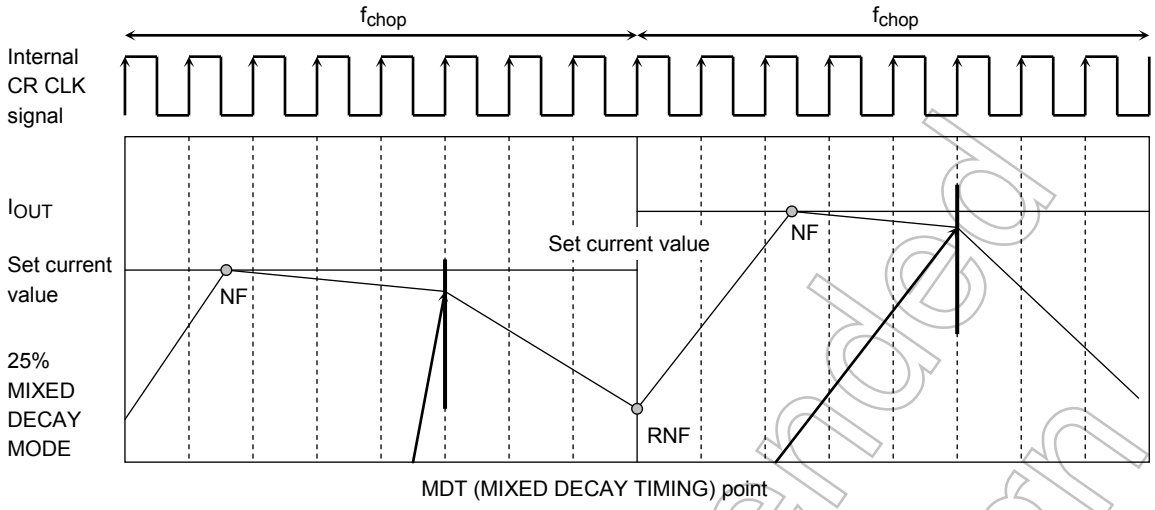
○ Sine wave in decreasing (When using MIXED DECAY Mode with small attenuation ratio (MDT%) at attenuation)



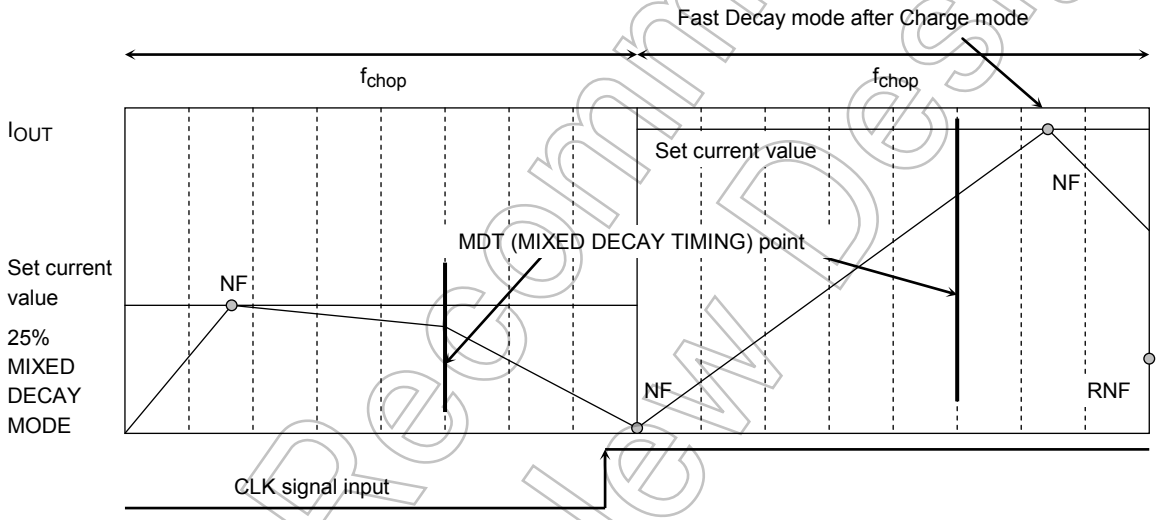
If RNF, current watching point, was the set current value (output current) in the mixed decay mode and in the fast decay mode, there is no charge mode but the slow + fast mode (slow to fast is at MDT) in the next chopping cycle.

Note: The above charts are schematics. The actual current transient responses are curves.

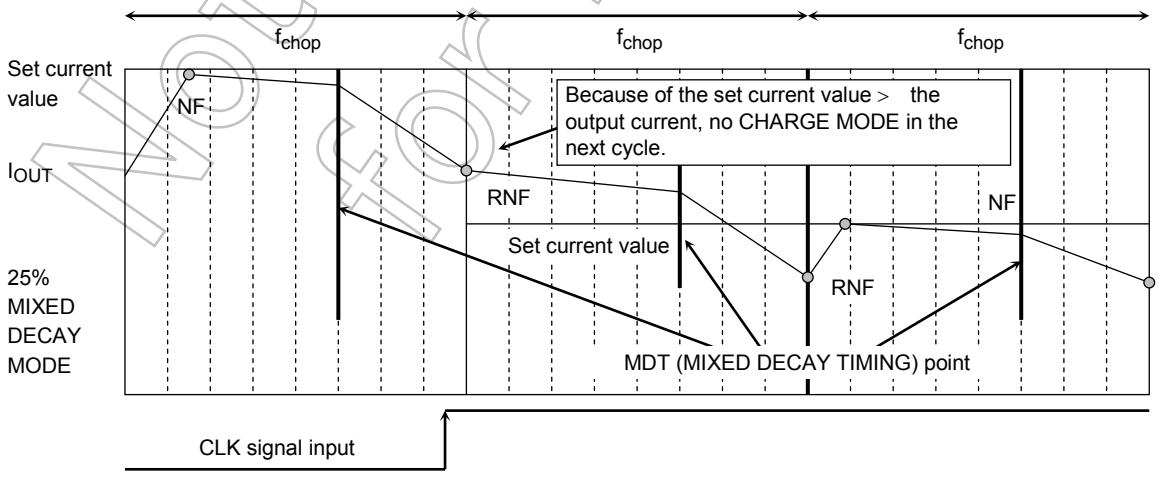
13. MIXED DECAY MODE waveform (Current Waveform)



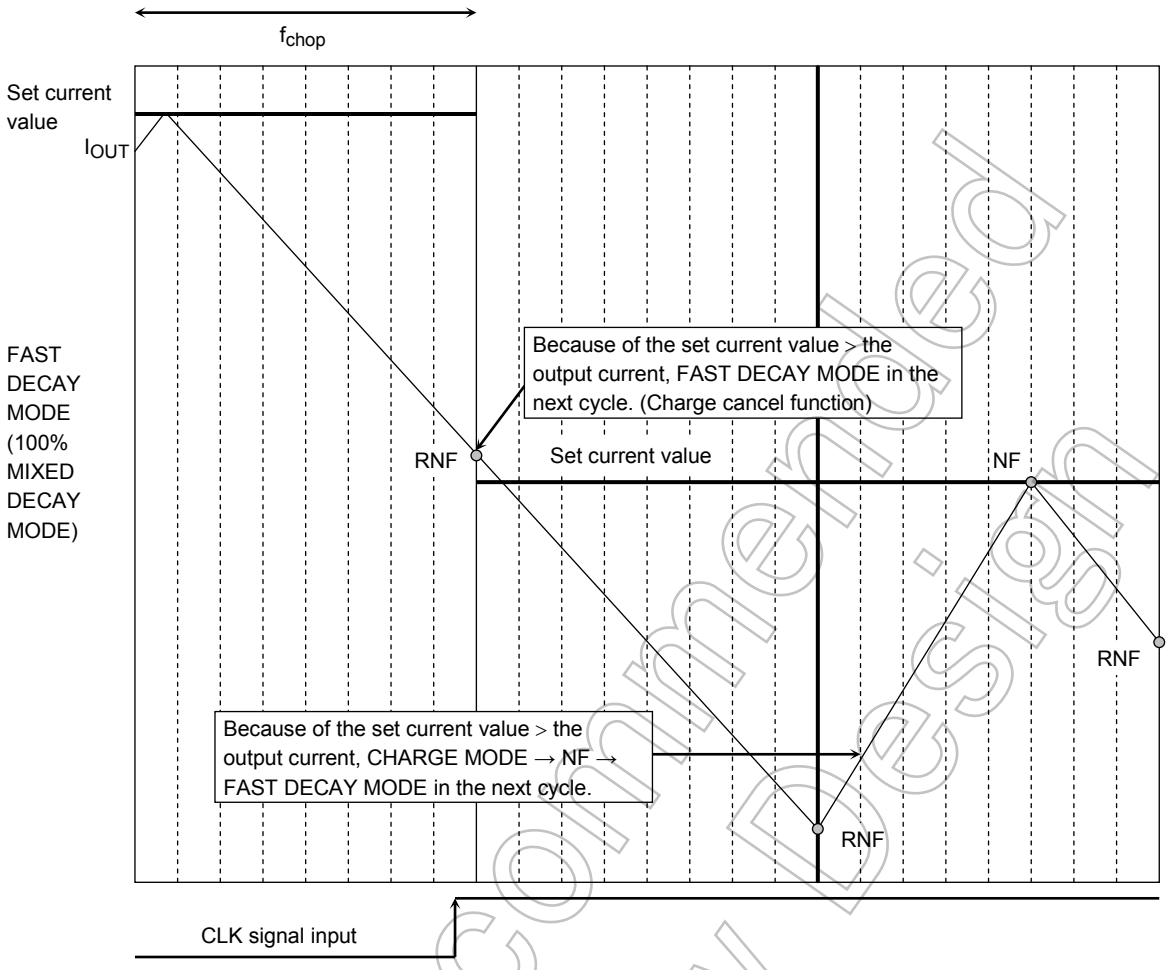
- When NF is after MIXED DECAY TIMING



- In MIXED DECAY MODE, when the output current > the set current value



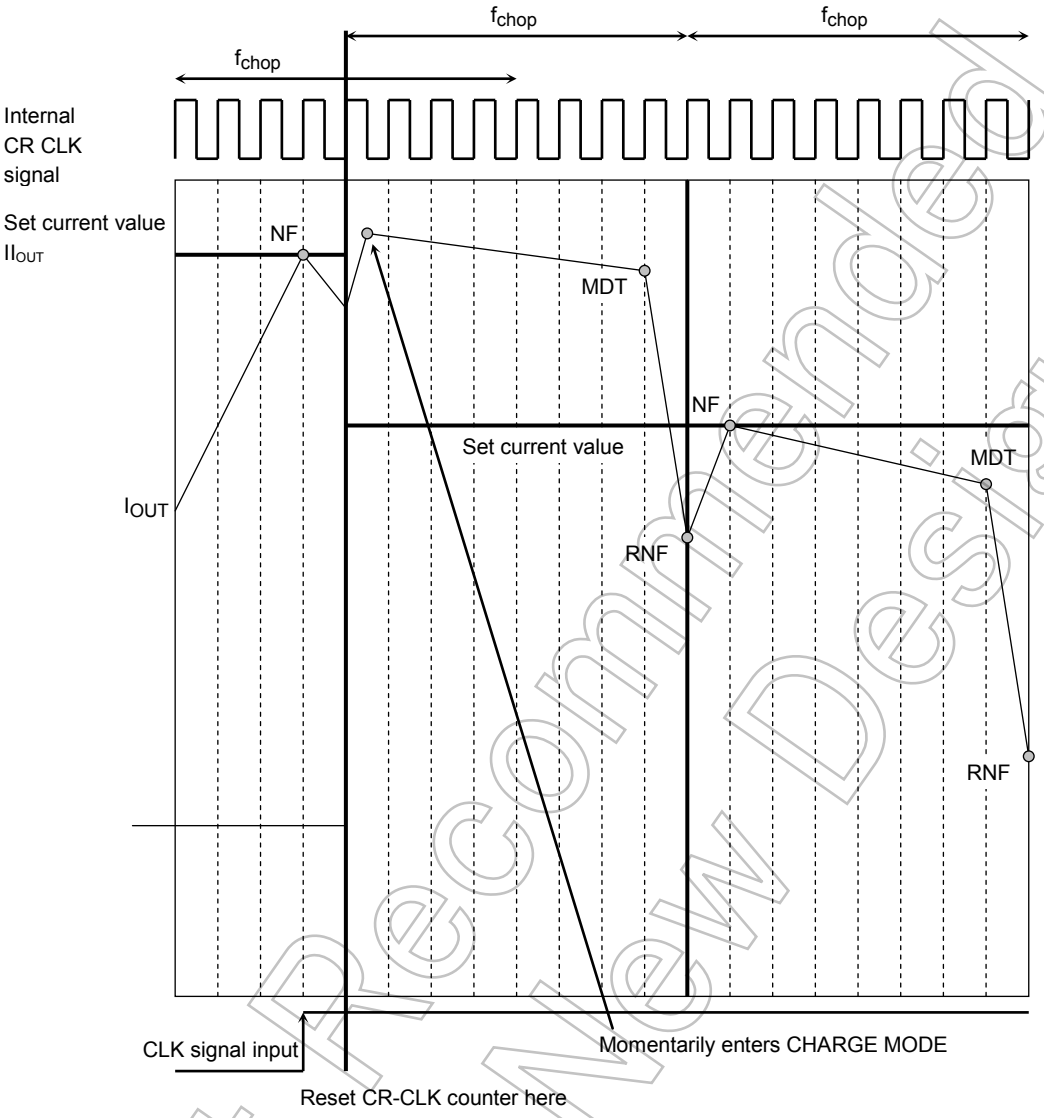
14. FAST DECAY MODE waveform



The output current to the motor is in supply voltage mode after the current value set by V_{ref}, R_{RS}, or Torque reached at the set current value.

15. CLK SIGNAL, INTERNAL CR CLK, AND OUTPUT CURRENT waveform (When CLK signal is input in SLOW DECAY MODE)

When CLK signal is input, the chopping counter (CR-CLK counter) is forced to reset at the next CR-CLK



timing.

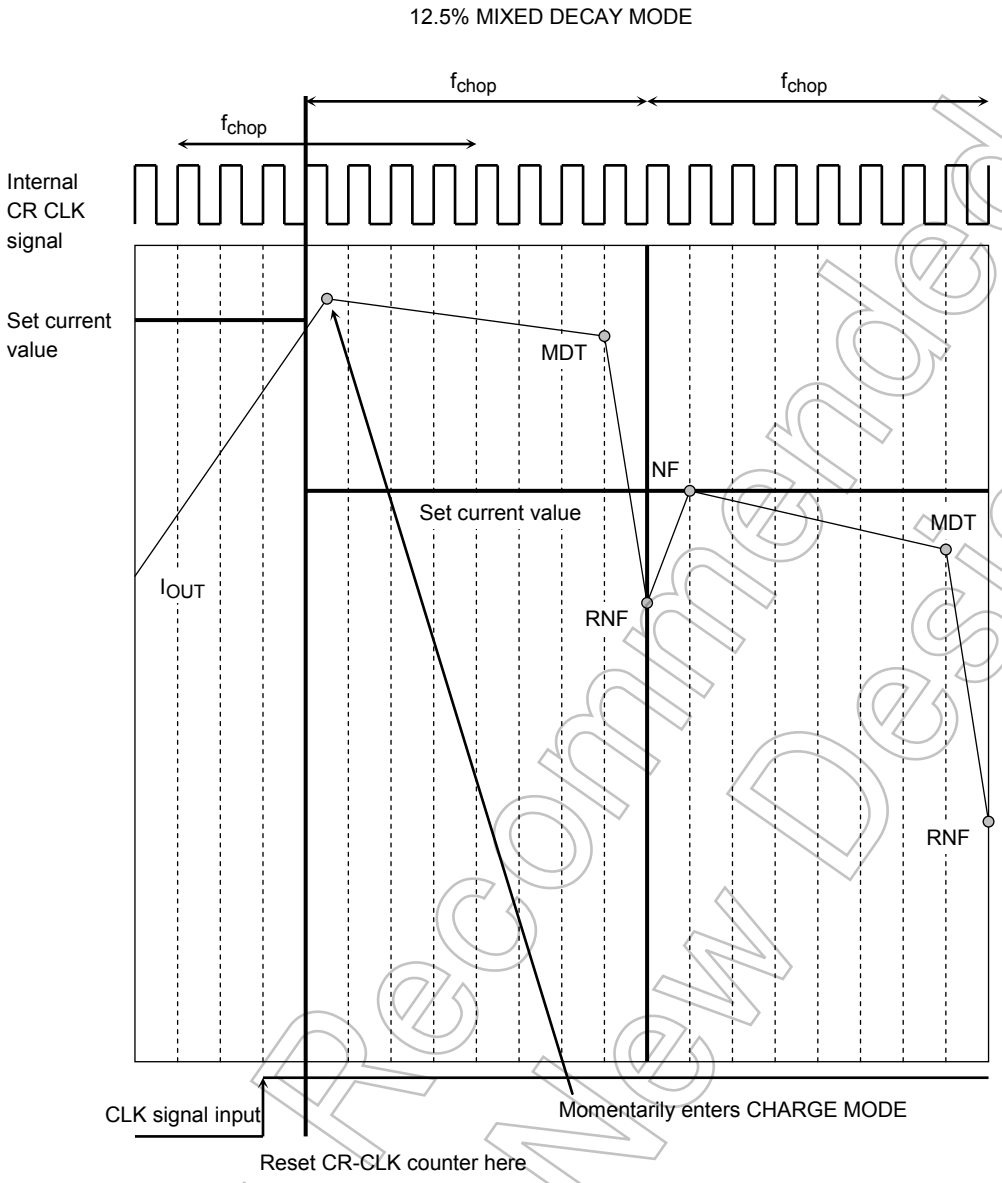
Because of this, compared with a method in which the counter is not reset, response to the input data is faster.

The delay time, the theoretical value in the logic portion, is expected to be a one-cycle CR waveform: 5 μs at 100 kHz CHOPPING.

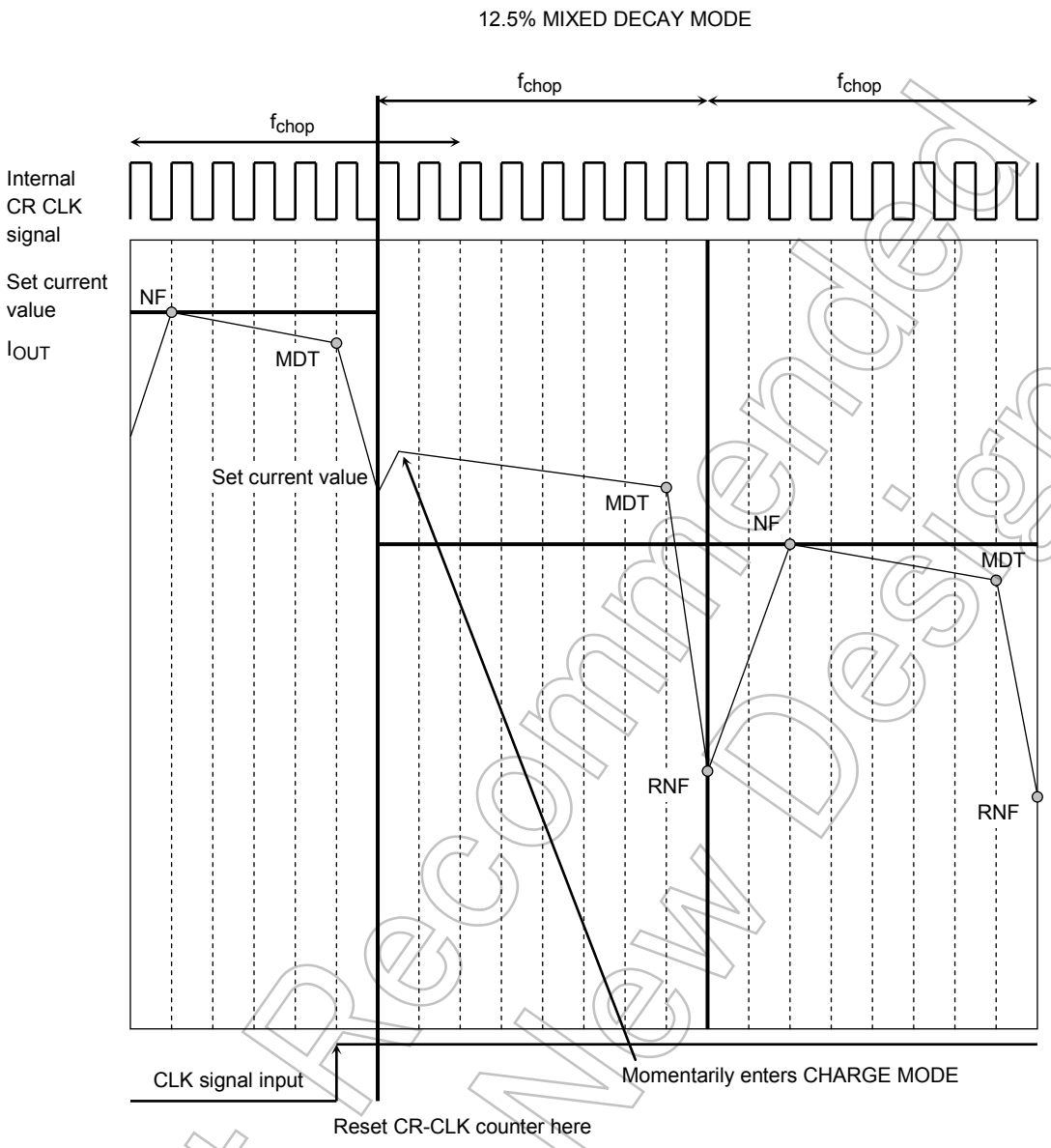
When the CR counter is reset due to CLK signal input, CHARGE MODE is entered momentarily due to current comparison.

Note: In FAST DECAY MODE, too, CHARGE MODE is entered momentarily due to current comparison.

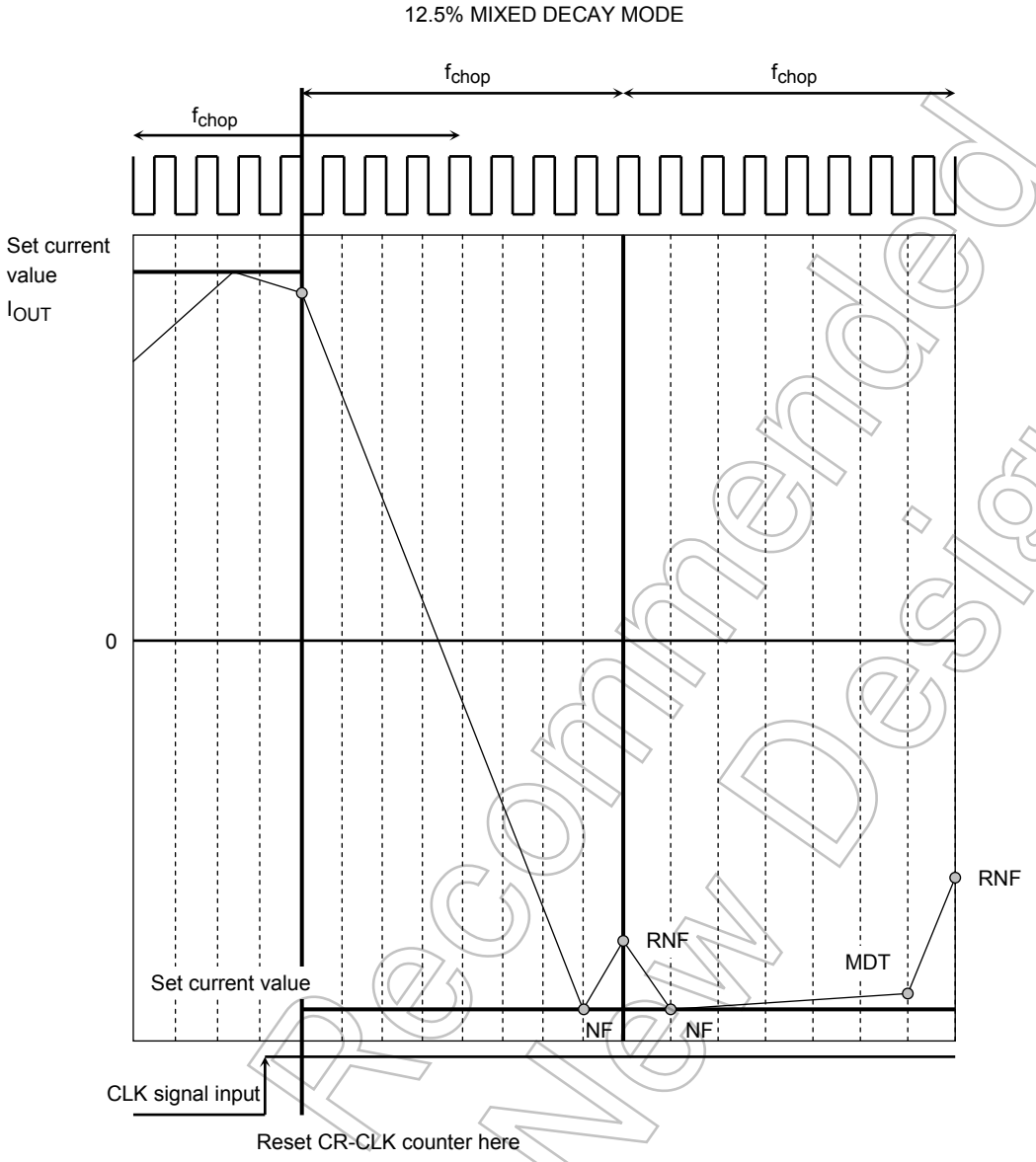
16. CLK SIGNAL, INTERNAL CR CLK, AND OUTPUT CURRENT waveform (When CLK signal is input in CHARGE MODE)



17. CLK SIGNAL, INTERNAL CR CLK, AND OUTPUT CURRENT waveform (When CLK signal is input in FAST DECAY MODE)



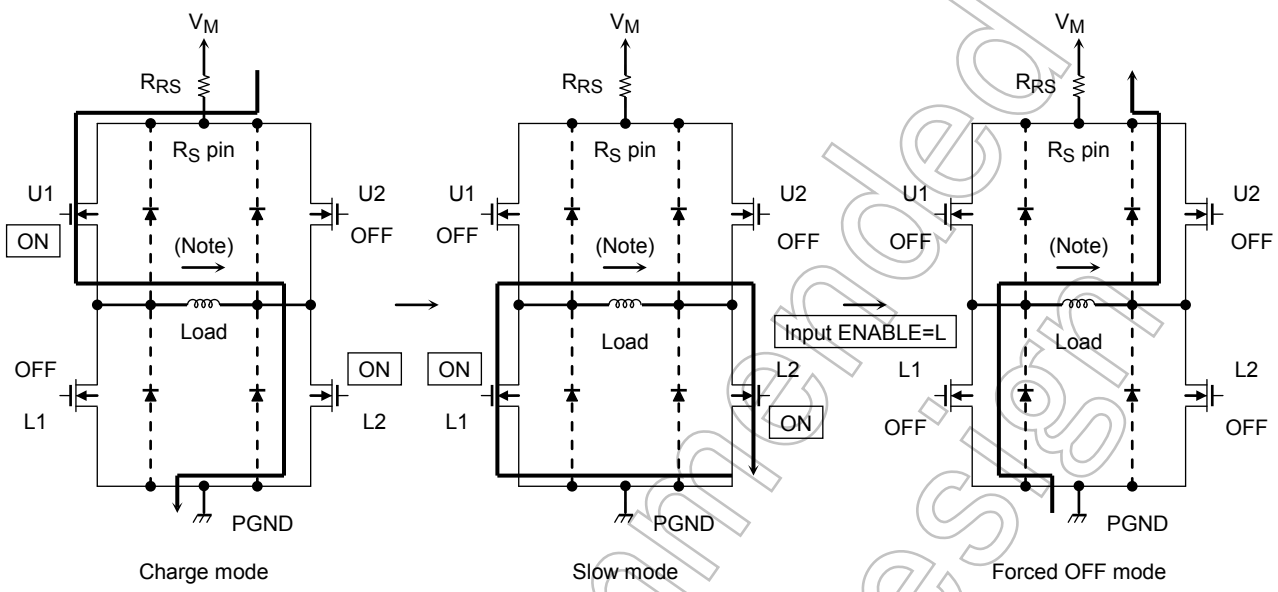
18. CLK SIGNAL, INTERNAL CR CLK, AND OUTPUT CURRENT waveform (When CLK signal is input in 2 EXCITATION MODE)



Current Discharge Path when ENABLE=L Input During Operation

In Slow Mode, when all output transistors are forced to switch off, coil energy is discharged in the following MODES:

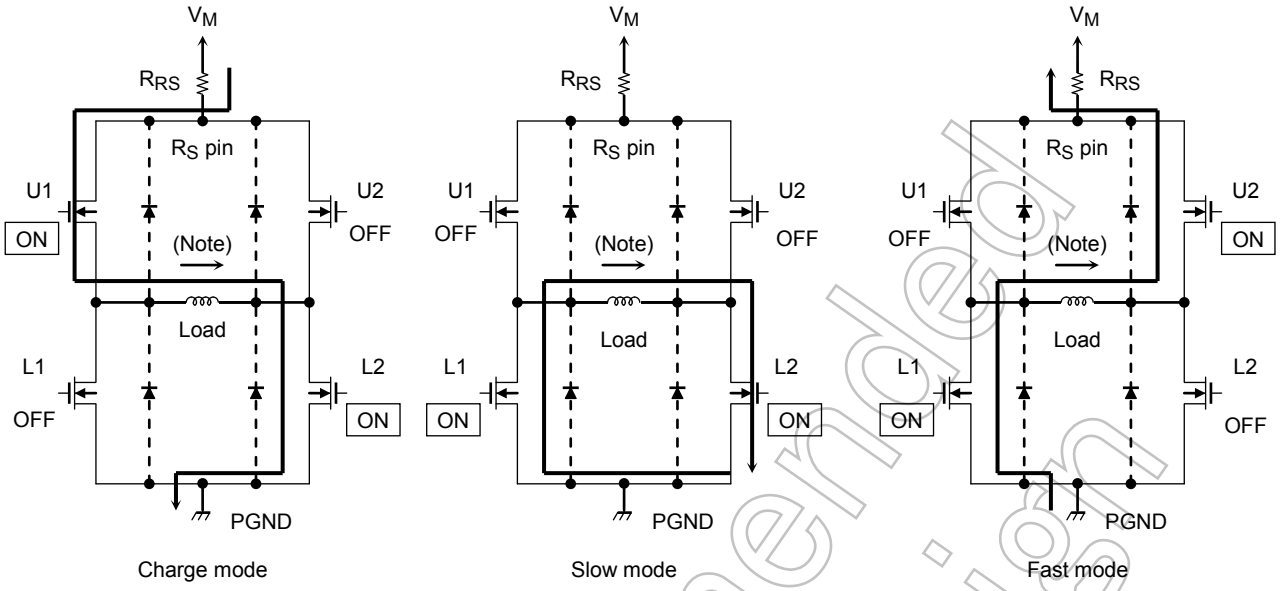
Note: Parasitic diodes are located on dotted lines. In normal MIXED DECAY MODE, the current does not flow to the parasitic diodes.



As shown in the figure at above, an output transistor has parasitic diodes.

To discharge energy from the coil, each transistor is switched on allowing current to flow in the reverse direction to that of normal operation. As a result, the parasitic diodes are not used. If all the output transistors are forced to switch off, the energy of the coil is discharged via the parasitic diodes.

Output Transistor Operating Mode



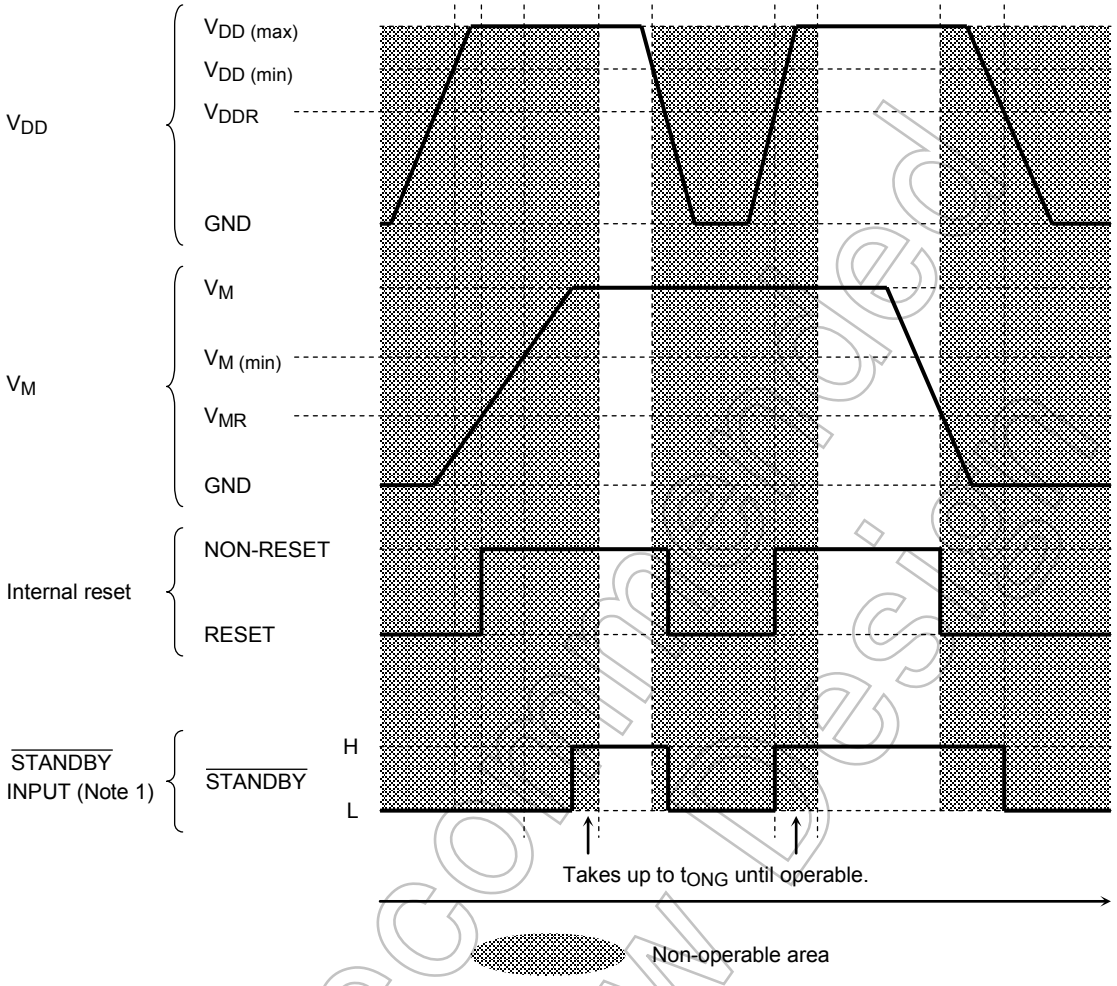
Output Transistor Operation Functions

CLK	U1	U2	L1	L2
CHARGE	ON	OFF	OFF	ON
SLOW	OFF	OFF	ON	ON
FAST	OFF	ON	ON	OFF

Note: The above table is an example where current flows in the direction of the arrows in the above figures. When the current flows in the opposite direction of the arrows, see the table below.

CLK	U1	U2	L1	L2
CHARGE	OFF	ON	ON	OFF
SLOW	OFF	OFF	ON	ON
FAST	ON	OFF	OFF	ON

Power Supply Sequence (Recommended)



Note 1: If the V_{DD} drops to the level of the V_{DDR} or below while the specified voltage is input to the V_M pin, the IC is internally reset.
This is a protective measure against malfunction. Likewise, if the V_M drops to the level of the V_{MR} or below while regulation voltage is input to the V_{DD}, the IC is internally reset as a protective measure against malfunction.
To avoid malfunction, when turning on V_M or V_{DD}, to input the $\overline{\text{Standby}}$ signal at the above timing is recommended.
It takes time for the output control charge pump circuit to stabilize. Wait up to t_{ONG} time after power on before driving the motors.

Note 2: When the V_M value is between 3.3 to 5.5 V, the internal reset is released, thus output may be on. In such a case, the charge pump cannot drive stably because of insufficient voltage. The $\overline{\text{Standby}}$ state should be maintained until V_M reaches 13 V or more.

Note 3: Since V_{DD} = 0 V and V_M = voltage within the rating are applied, output is turned off by internal reset.
At that time, a current of several mA flows due to the Pass between V_M and V_{DD}.
When voltage increases on V_{DD} output, make sure that specified voltage is input.

How to Calculate Set Current

This IC controls constant current in CLK-IN mode.

At that time, the maximum current value (set current value) can be determined by setting the sensing resistor (R_{RS}) and reference voltage (V_{ref}).

1/5.0 is V_{ref} (gain): V_{ref} attenuation ratio. (For the specifications, see the electrical characteristics.)

For example, when inputting V_{ref} = 3 V and torque = 100% to output I_{OUT} = 0.8 A, R_{RS} = 0.75 Ω (0.5 W or more) is required.

How to Calculate the Chopping and OSC Frequencies

At constant current control, this IC chops frequency using the oscillation waveform (saw tooth waveform) determined by external capacitor and resistor as a reference.

The TB62209FG requires an oscillation frequency of eight times the chopping frequency.

The oscillation frequency is calculated as follows:

$$f_{CR} = \frac{1}{0.523 \times (C \times R + 600 \times C)}$$

For example, when C_{osc} = 560 pF and R_{osc} = 3.6 kΩ are connected, f_{CR} = 813 kHz.

At this time, the chopping frequency f_{chop} is calculated as follows:

$f_{chop} = f_{CR}/8 = 101$ kHz

When determining the chopping frequency, make the setting taking the above into consideration.

IC Power Dissipation

IC power dissipation is classified into two: power consumed by transistors in the output block and power consumed by the logic block and the charge pump circuit.

- Power consumed by the Power Transistor (calculated with R_{ON} = 0.60 Ω)

  In Charge mode, Fast Decay mode, or Slow Decay mode, power is consumed by the upper and lower transistors of the H bridges.

  The following expression expresses the power consumed by the transistors of an H bridge.

  $P\ (out) = 2\ (T_r) \times I_{OUT}\ (A) \times V_{DS}\ (V) = 2 \times I_{OUT}^2 \times R_{ON}$ ..... (1)

  The average power dissipation for output under 4-bit micro step operation (phase difference between phases A and B is 90°) is determined by expression (1).

  Thus, power dissipation for output per unit is determined as follows (2) under the conditions below.

  R_{ON} = 0.60 Ω (@ 1.0 A)

  I_{OUT} (Peak: max) = 1.0 A

  V_M = 24 V

  V_{DD} = 5 V

  $P\ (out) = 2\ (T_r) \times 1.0^2\ (A) \times 0.60\ (\Omega) = 1.20\ (W)$ ..... (2)

  Power consumed by the logic block and IM

  The following standard values are used as power dissipation of the logic block and IM at operation.

  I (LOGIC) = 2.5 mA (typ.):

  $I\ (I_{M3})$ = 10.0 mA (typ.): operation/unit

  $I\ (I_{M1})$ = 2.0 mA (typ.): stop/unit

  The logic block is connected to V_{DD} (5 V). IM (total of current consumed by the circuits connected to V_M and current consumed by output switching) is connected to V_M (24 V). Power dissipation is calculated as follows:

  $P\ (Logic\&IM) = 5\ (V) \times 0.0025\ (A) + 24\ (V) \times 0.010\ (A) = 0.25\ (W)$ ..... (3)

  Thus, the total power dissipation (P) is

  $P = P\ (out) + P\ (Logic\&IM) = 1.45\ (W)$

  Power dissipation at standby is determined as follows:

  $P\ (standby) + P\ (out) = 24\ (V) \times 0.002\ (A) + 5\ (V) \times 0.0025\ (A) = 0.06\ (W)$

  For thermal design on the board, evaluate by mounting the IC.

Test Waveforms

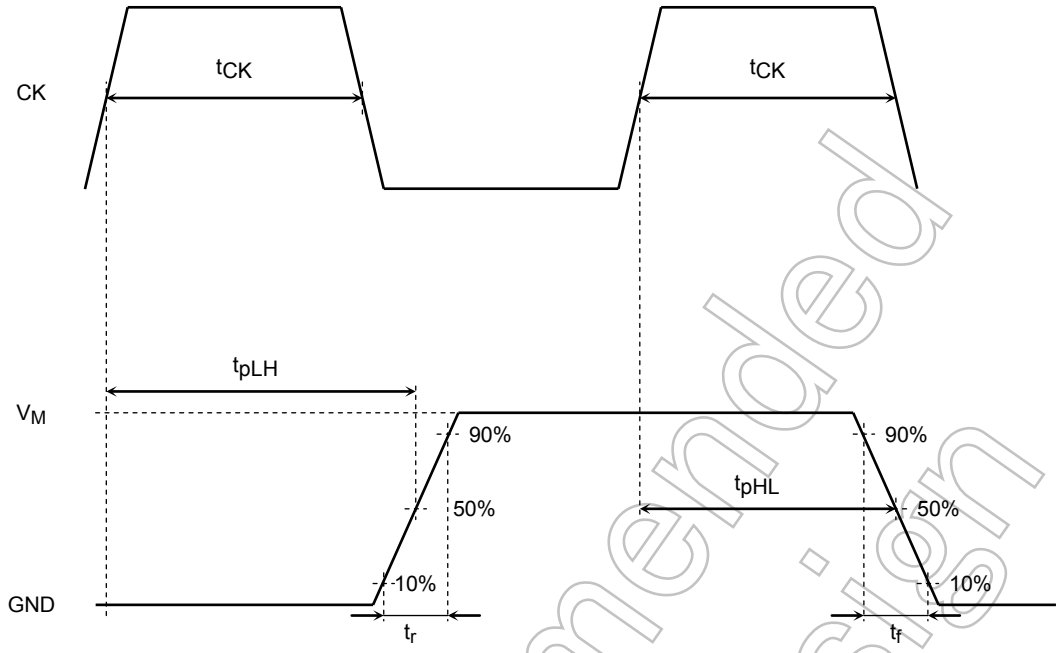
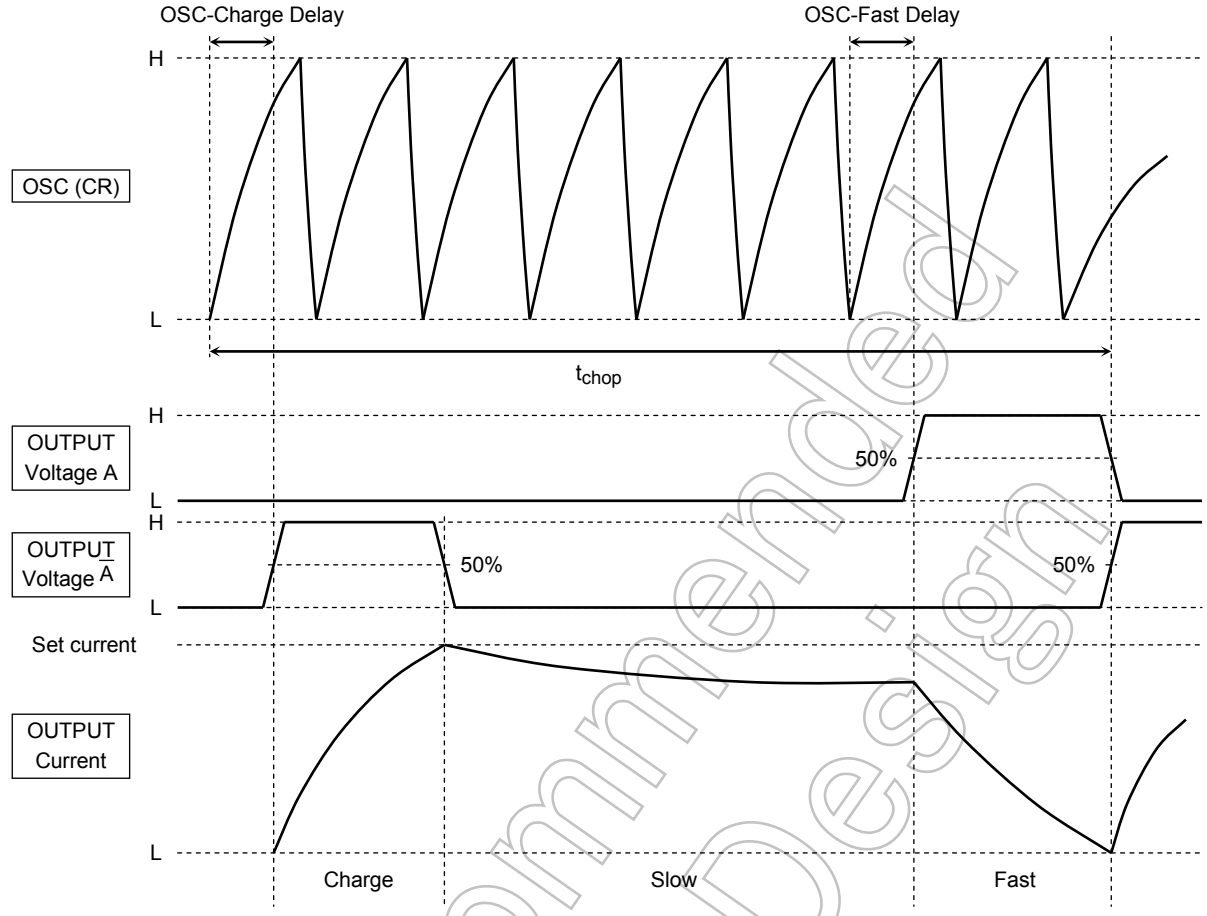


Figure 1 Timing Waveforms and Names



OSC-charge delay:

Because the rising edge level of the OSC waveform is used for converting the OSC waveform to the internal CR CLK, a delay of up to 1.25 ns (@f_{chop} = 100 kHz: f_{CR} = 400 kHz) occurs between the OSC waveform and the internal CR CLK.

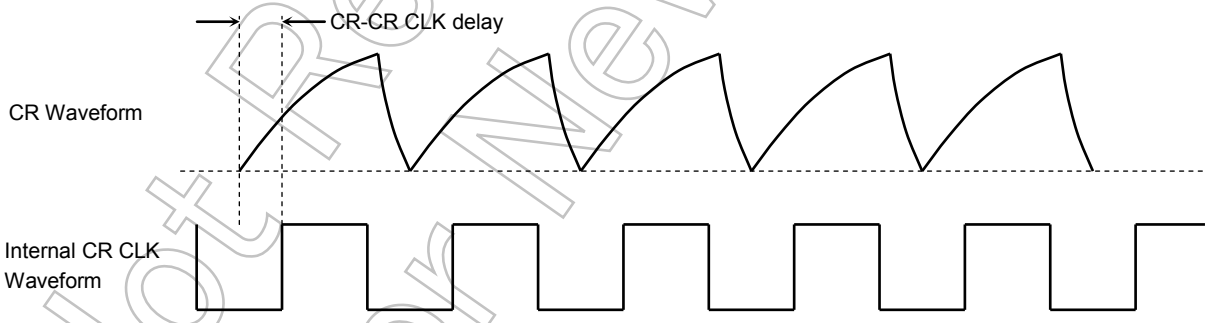
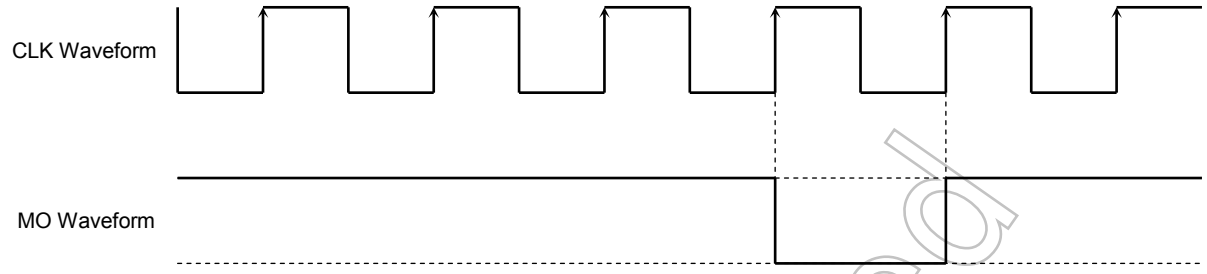
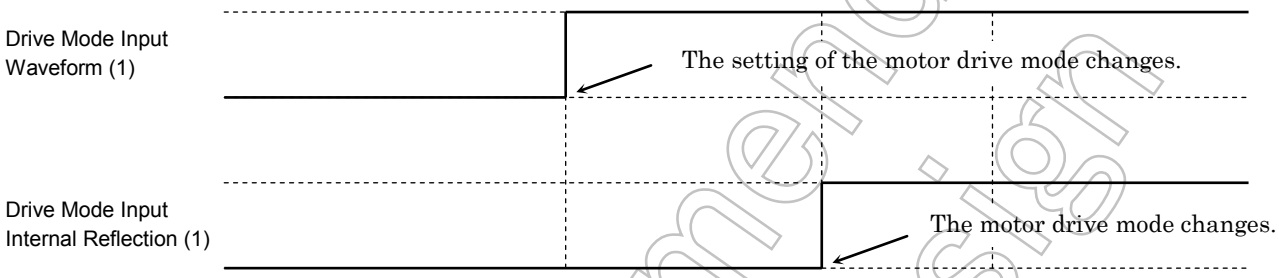


Figure 2 Timing Waveforms and Names (CR and output)

Relationship between Drive Mode Input Timing and MO

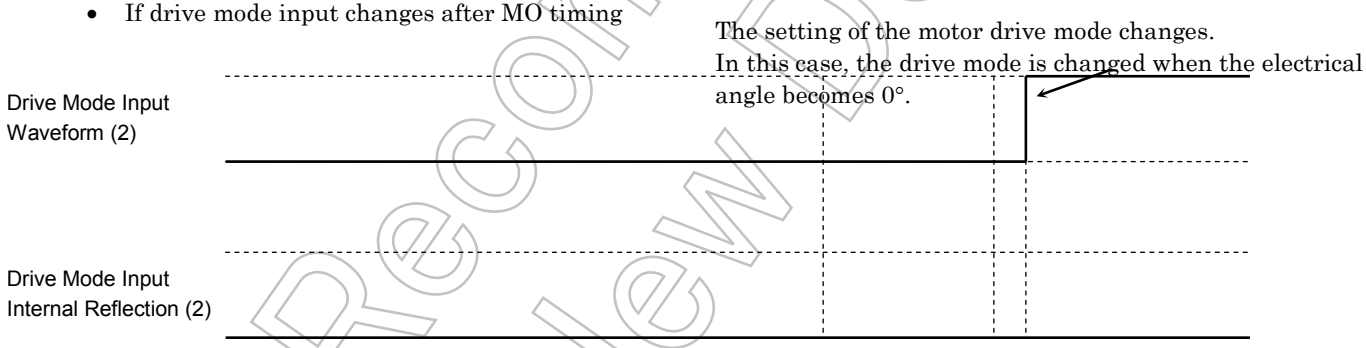


- If drive mode input changes before MO timing



Parallel set signal is reflected.

- If drive mode input changes after MO timing



Parallel set signal occurs after the rising edge of CLK, therefore, it is not reflected. The drive mode is changed when the electrical angle becomes 0°.

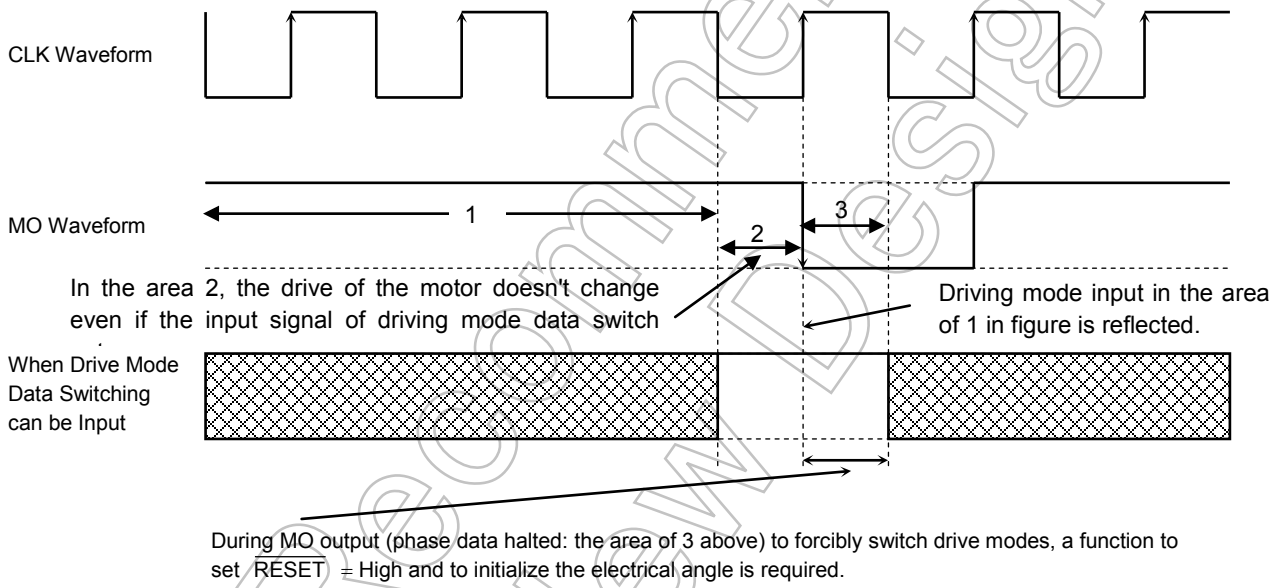
Note: The TB62209FG uses the drive mode change reserve method to prevent the motor from step out when changing drive modes.
Note that the following rules apply when switching drive modes at or near the MO signal output timing.

Reflecting Points of Signals

	Point where Drive Mode Setting Reflected (area of 1 in figure)	CW/CCW
2-Phase Excitation mode	45° (MO) Before half-clock of phase B = phase A = 100%	At rising edge of CLK input
1-2 Phase Excitation mode W1-2 Phase Excitation mode 2W1-2 Phase Excitation mode 4W1-2 Phase Excitation mode	0° (MO) Before half-clock of phase B = 100%	At rising edge of CLK input

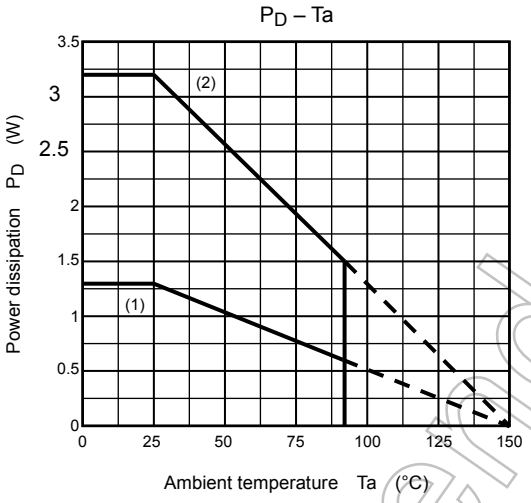
Other parallel set signals can be changed at any time (they are reflected immediately).

Recommended Point for Switching Drive Mode



During MO output (phase data halted: the area of 3 above) to forcibly switch drive modes, a function to set $\overline{\text{RESET}}$ = High and to initialize the electrical angle is required.

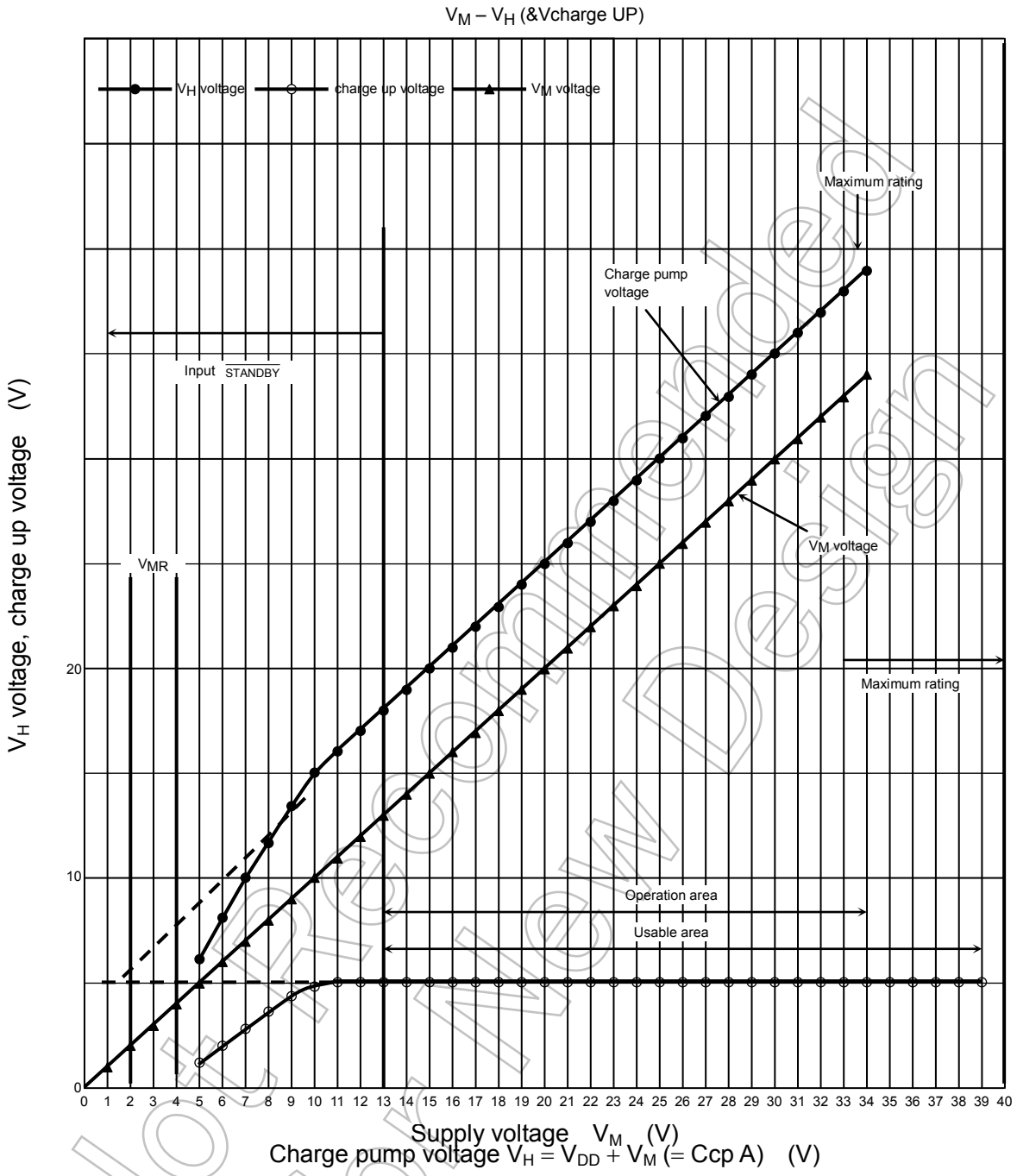
P_D – Ta (Package power dissipation)



(1) HSOP36 $R_{th\ (j\text{-}a)}$ (96°C/W)
(2) When mounted on the board (140 mm × 70 mm × 1.6 mm: 38°C/W: typ.)

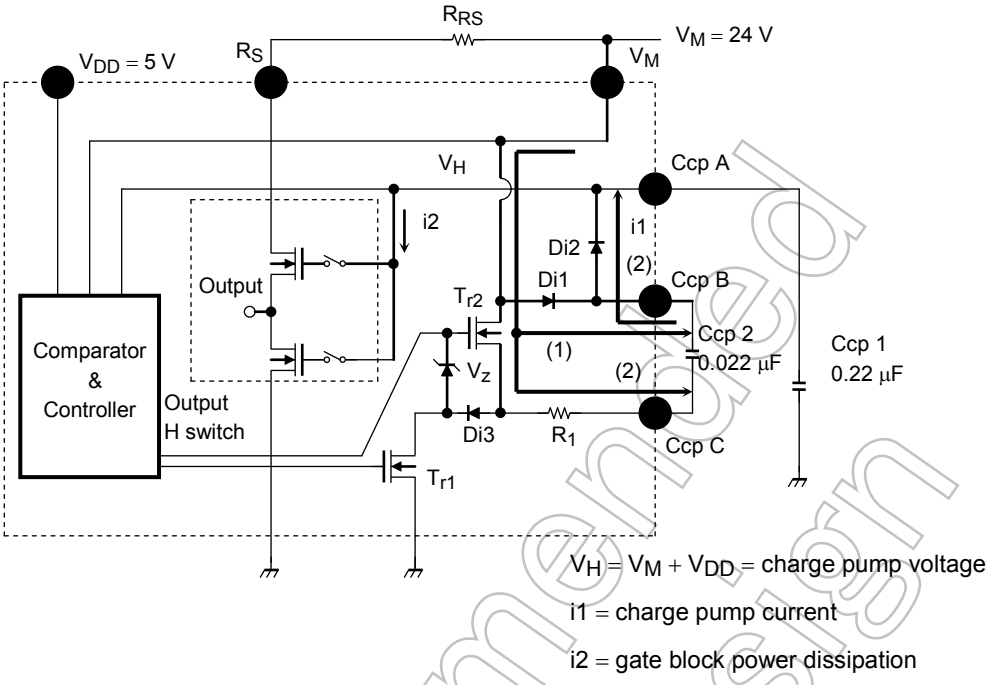
Note: $R_{th\ (j\text{-}a)}$: 8.5°C/W

Relationship between V_M and V_H (charge pump voltage)

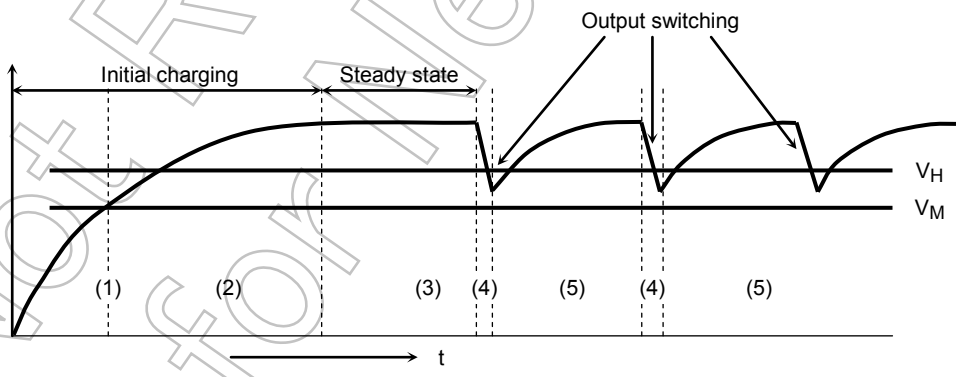


Note: V_{DD} = 5 V
Ccp 1 = 0.22 μF, Ccp 2 = 0.022 μF, f_{chop} = 150 kHz
(Be aware the temperature changes of capacitance of charge pump capacitor.)

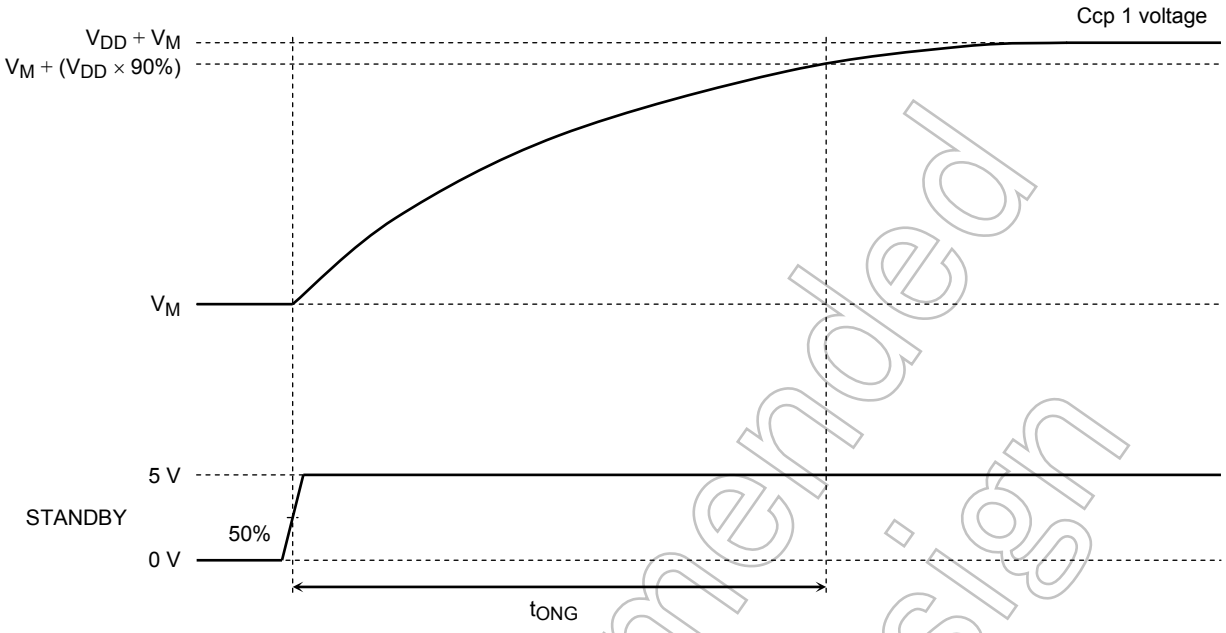
Operation of Charge Pump Circuit



- Initial charging
  - (1) When RESET is released, T_{r1} is turned ON and T_{r2} turned OFF. Ccp 2 is charged from V_M via Di1.
  - (2) T_{r1} is turned OFF, T_{r2} is turned ON, and Ccp 1 is charged from Ccp 2 via Di2.
  - (3) When the voltage difference between V_M and V_H (Ccp A pin voltage = charge pump voltage) reaches V_{DD} or higher, operation halts (Steady state).
- Actual operation
  - (4) Ccp 1 charge (i2) is used at f_{chop} switching and the V_H potential drops.
  - (5) Charges up by (1) and (2) above.



Charge Pump Rise Time



t_{ONG}:

Time taken for capacitor Ccp 2 (charging capacitor) to fill up Ccp 1 (storing capacitor) to $V_M + V_{DD}$ after a reset is released.

The internal IC cannot drive the gates correctly until the voltage of Ccp 1 reaches $V_M + V_{DD}$. Be sure to wait for t_{ONG} or longer before driving the motors.

Basically, the larger the Ccp 1 capacitance, the smaller the voltage fluctuation, though the initial charge up time is longer.

The smaller the Ccp 1 capacitance, the shorter the initial charge-up time but the voltage fluctuation is larger.

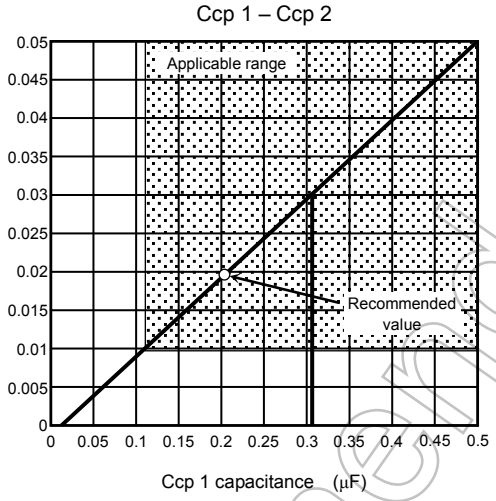
Depending on the combination of capacitors (especially with small capacitance), voltage may not be sufficiently boosted.

When the voltage does not increase sufficiently, output DMOS R_{ON} turns lower than the normal, and it raises the temperature.

Thus, use the capacitors under the capacitor combination conditions (Ccp 1 = 0.22 μF, Ccp 2 = 0.022 μF) recommended by Toshiba.

External Capacitor for Charge Pump

When driving the stepping motor with V_{DD} = 5 V, f_{chop} = 150 kHz, L = 10 mH under the conditions of V_M = 13 V and 1.5 A, the logical values for Ccp 1 and Ccp 2 are as shown in the graph below:



Choose Ccp 1 and Ccp 2 to be combined from the above applicable range. We recommend Ccp 1:Ccp 2 at 10:1 or more. (If our recommended values (Ccp1 = 0.22 μF, Ccp 2 = 0.022 μF) are used, the drive conditions in the specification sheet are satisfied. (There is no capacitor temperature characteristic as a condition.)

When setting the constants, make sure that the charge pump voltage is not below the specified value and set the constants with a margin (the larger Ccp 1 and Ccp 2, the more the margin).

Some capacitors exhibit a large change in capacitance according to the temperature. Make sure the above capacitance is obtained under the usage environment temperature.

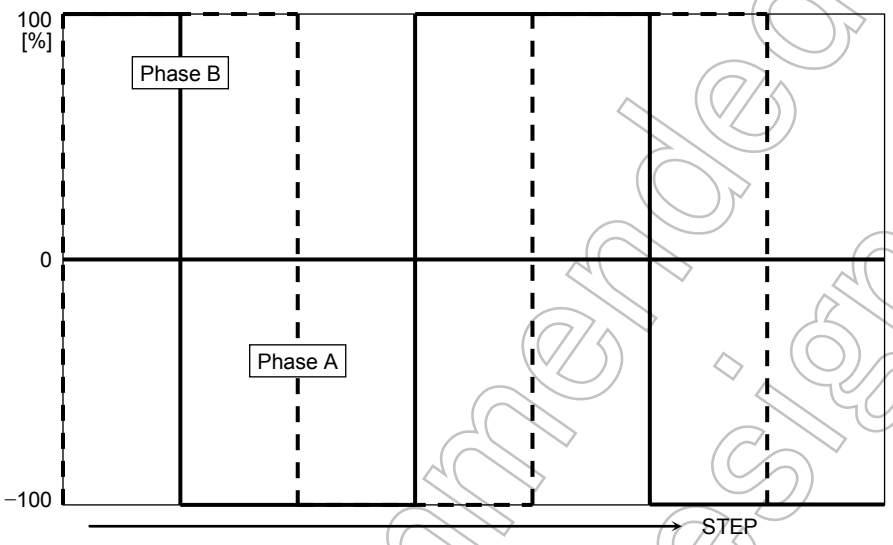
(1) Low Power Dissipation mode

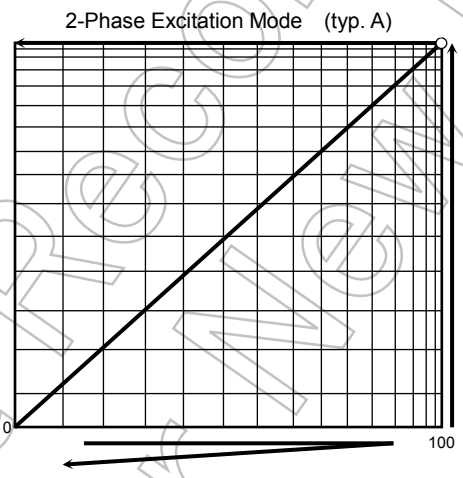
Low Power Dissipation mode turns off phases A and B, and also halts the charge pump.
Operation is the same as that when the $\overline{\text{STANDBY}}$ pin is set to Low.

(2) Motor Lock mode

Motor Lock mode turns phase B output only off with phase A off.
From reset, with IA = 0 and IB = 100%, the normal 4W1-2 phase operating current is output.
Use this mode when you want to hold (lock) the rotor at any desired value.

(3) 2-Phase Excitation mode

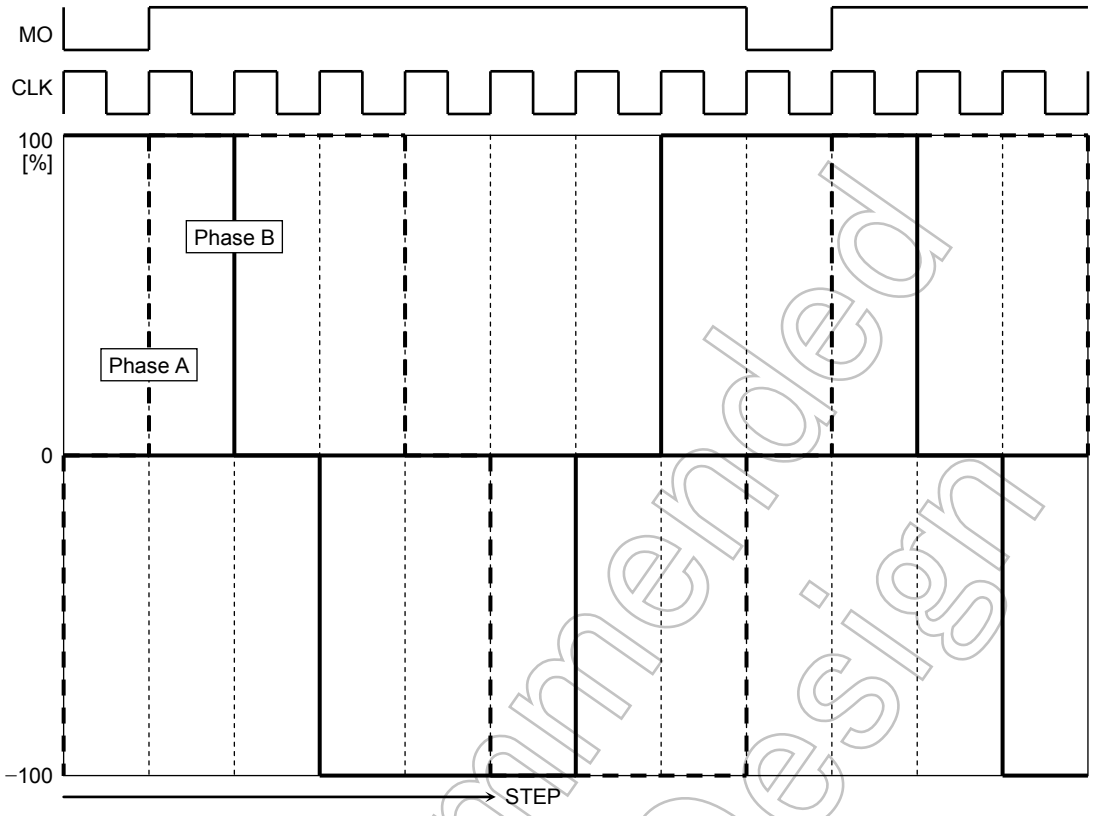


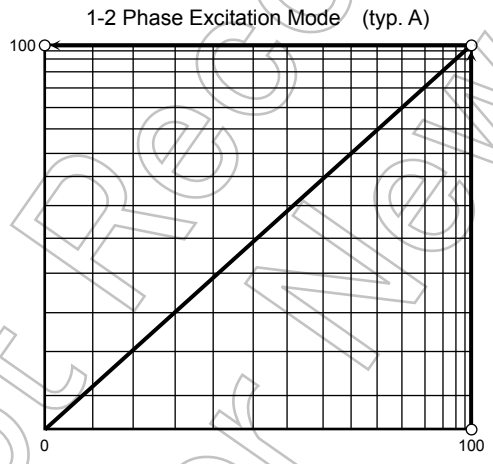


Electrical angle 360° = 4 CLKs

Note: 2-phase excitation has a large load change due to motor induced electromotive force. If a mode in which the current attenuation capability (current control capability) is small is used, current increase due to induced electromotive force may not be suppressed. In such a case, use a mode in which the mixed decay ratio is large.
We recommend 37.5% Mixed Decay mode as the initial value (general condition).

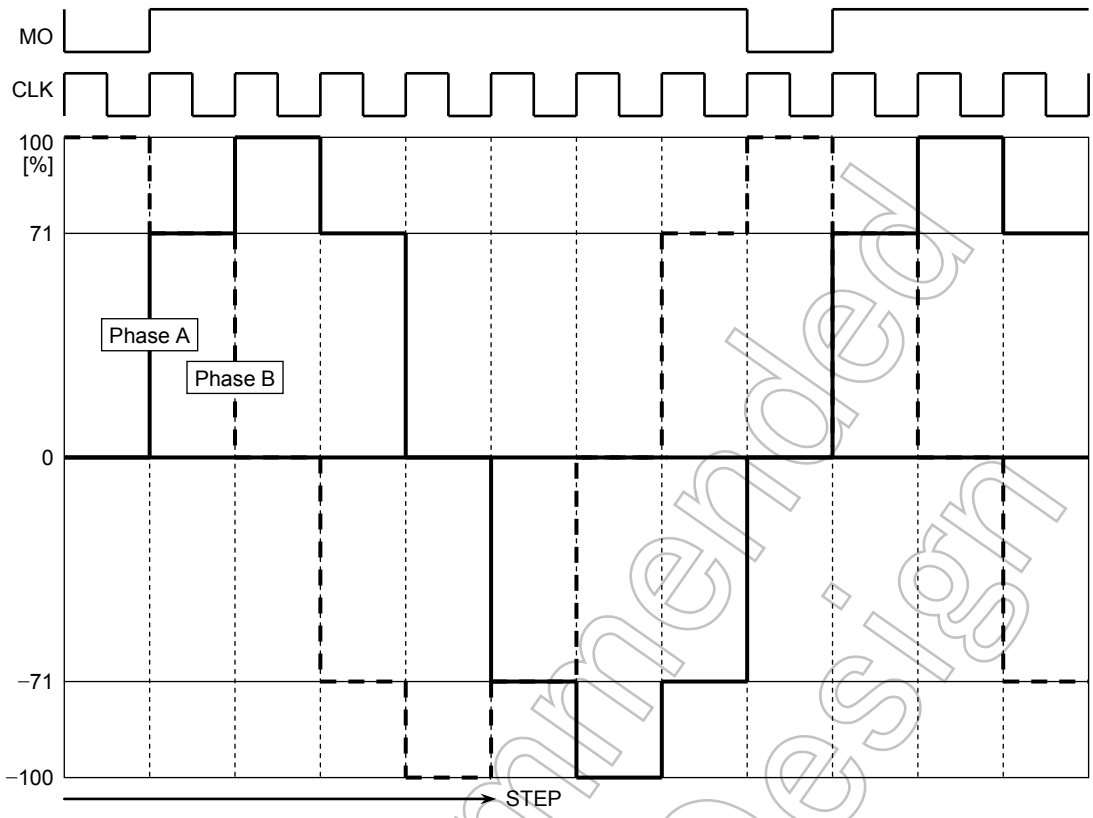
(4) 1-2 Phase Excitation mode (a)

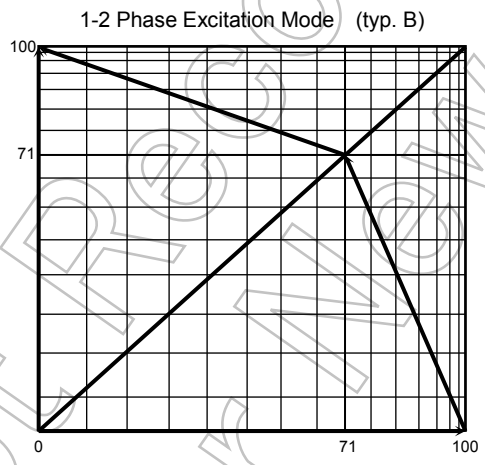




Electrical angle 360° = 8 CLK

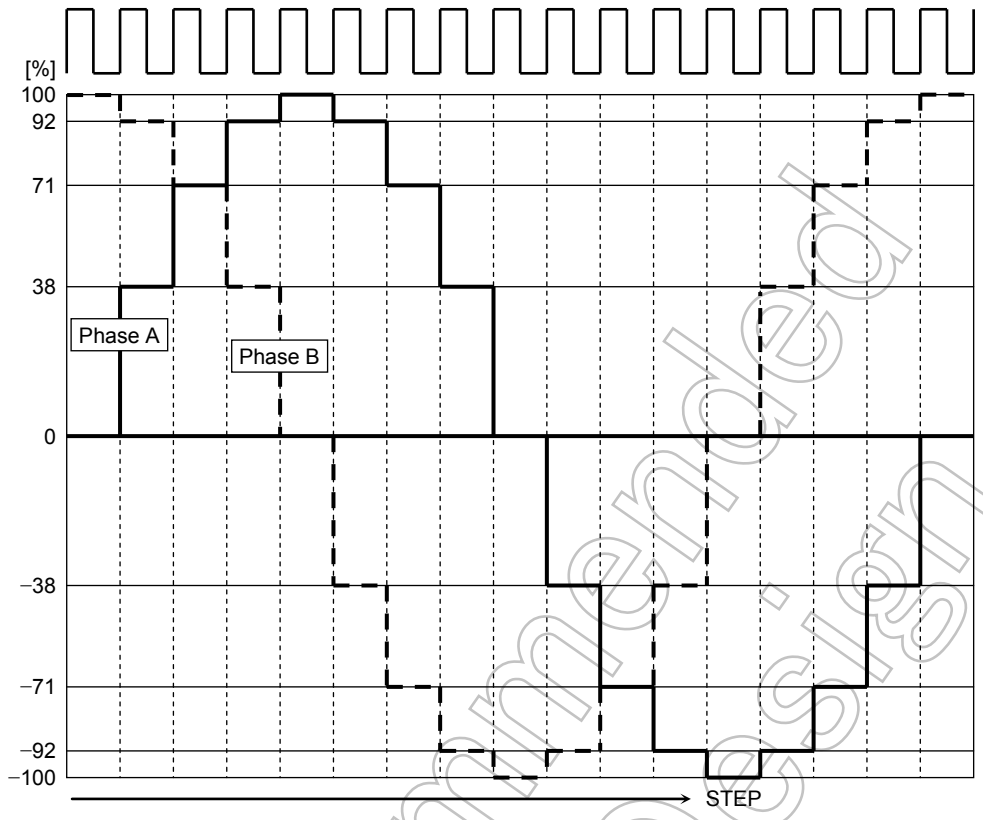
(5) 1-2 Phase Excitation mode (b)



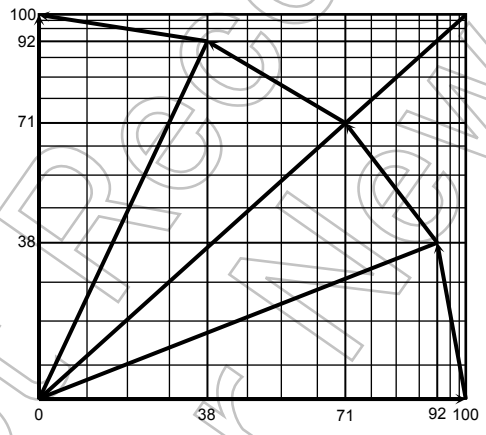


Electrical angle 360° = 8 CLK

(6) W1-2 Phase Excitation mode

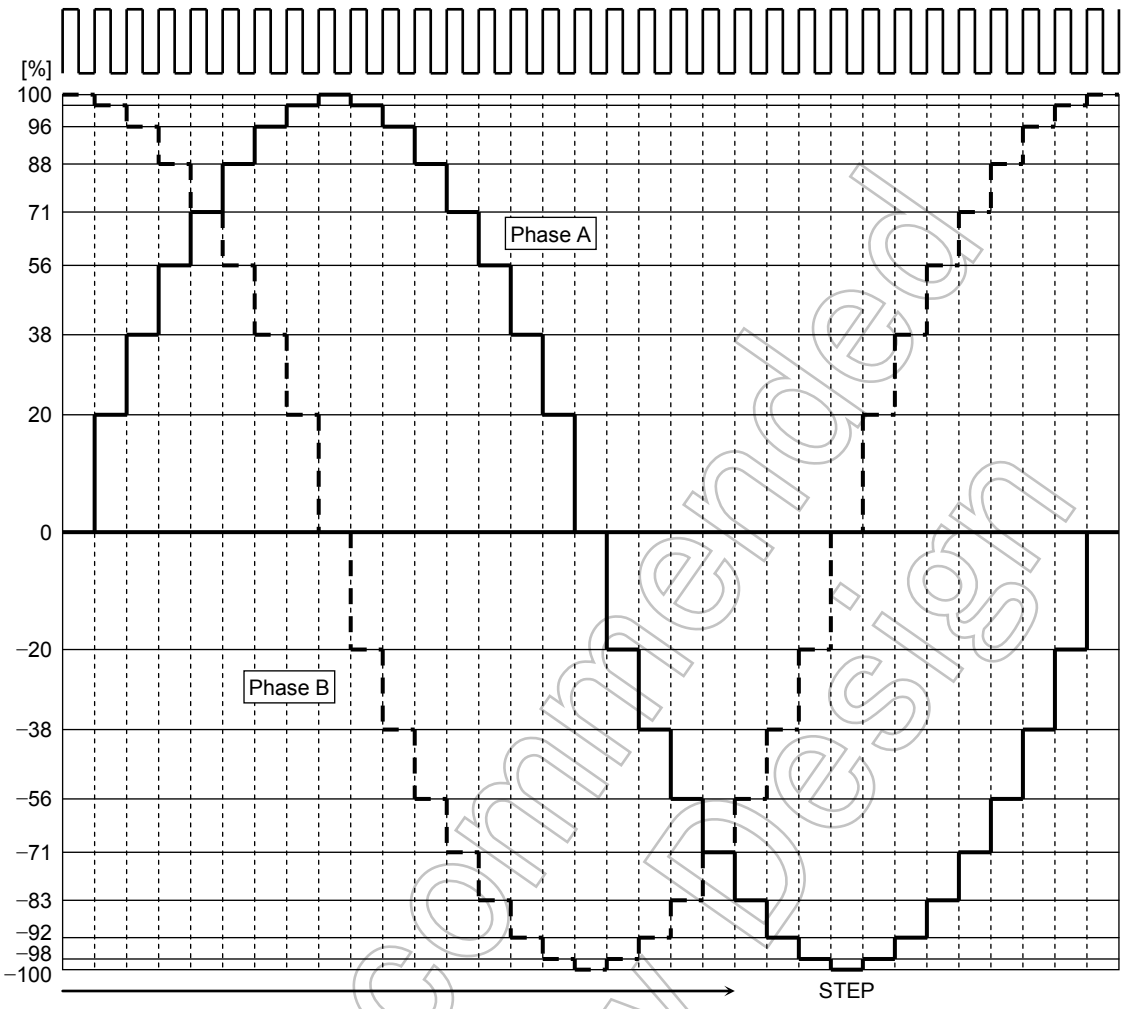


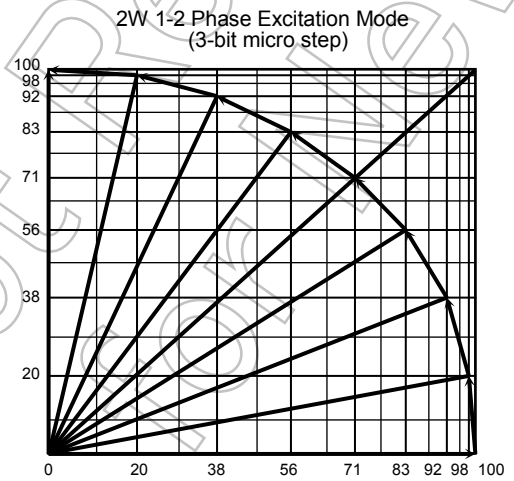
W1-2 Phase Excitation Mode
(2-bit micro step)



Electrical angle 360° = 16 CLK

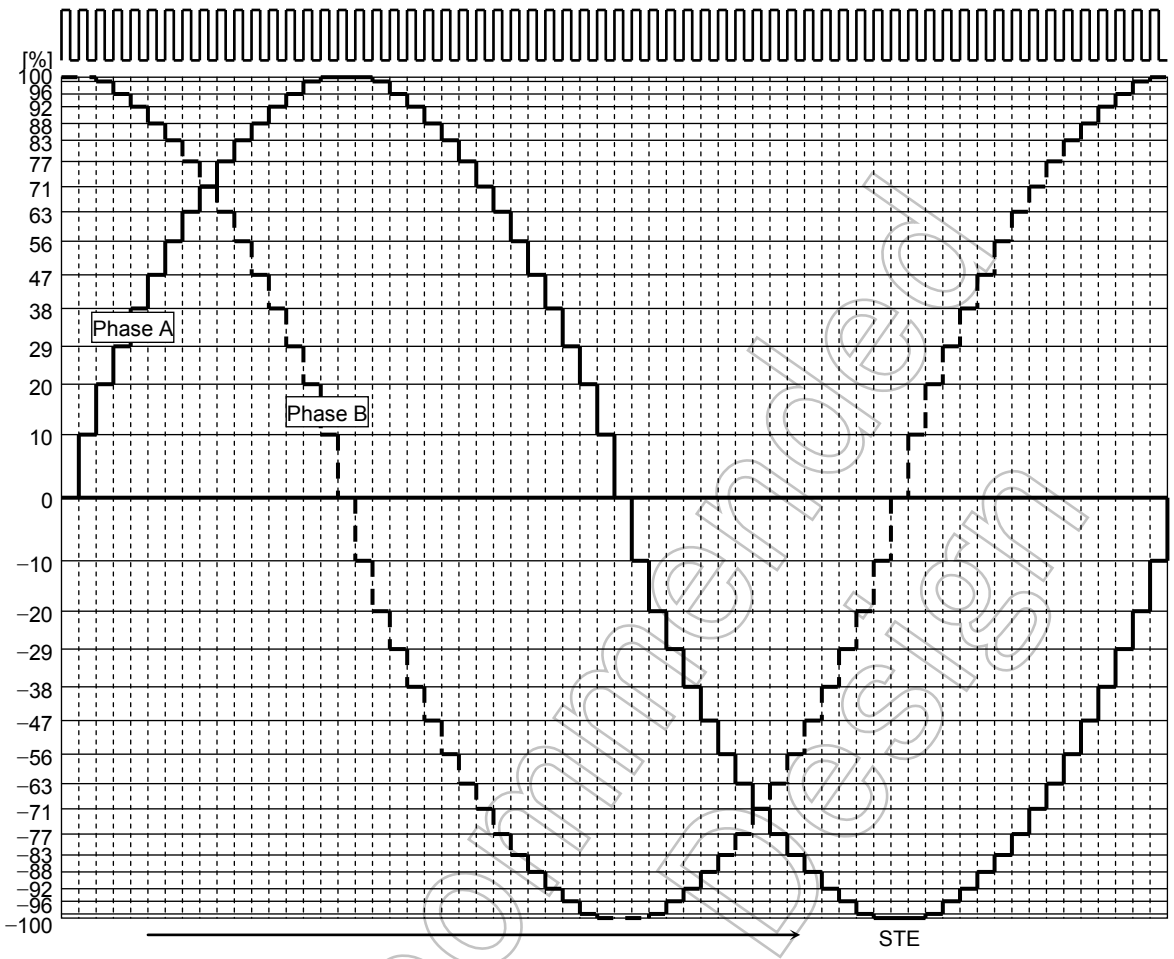
(7) 2W1-2 Phase Excitation mode





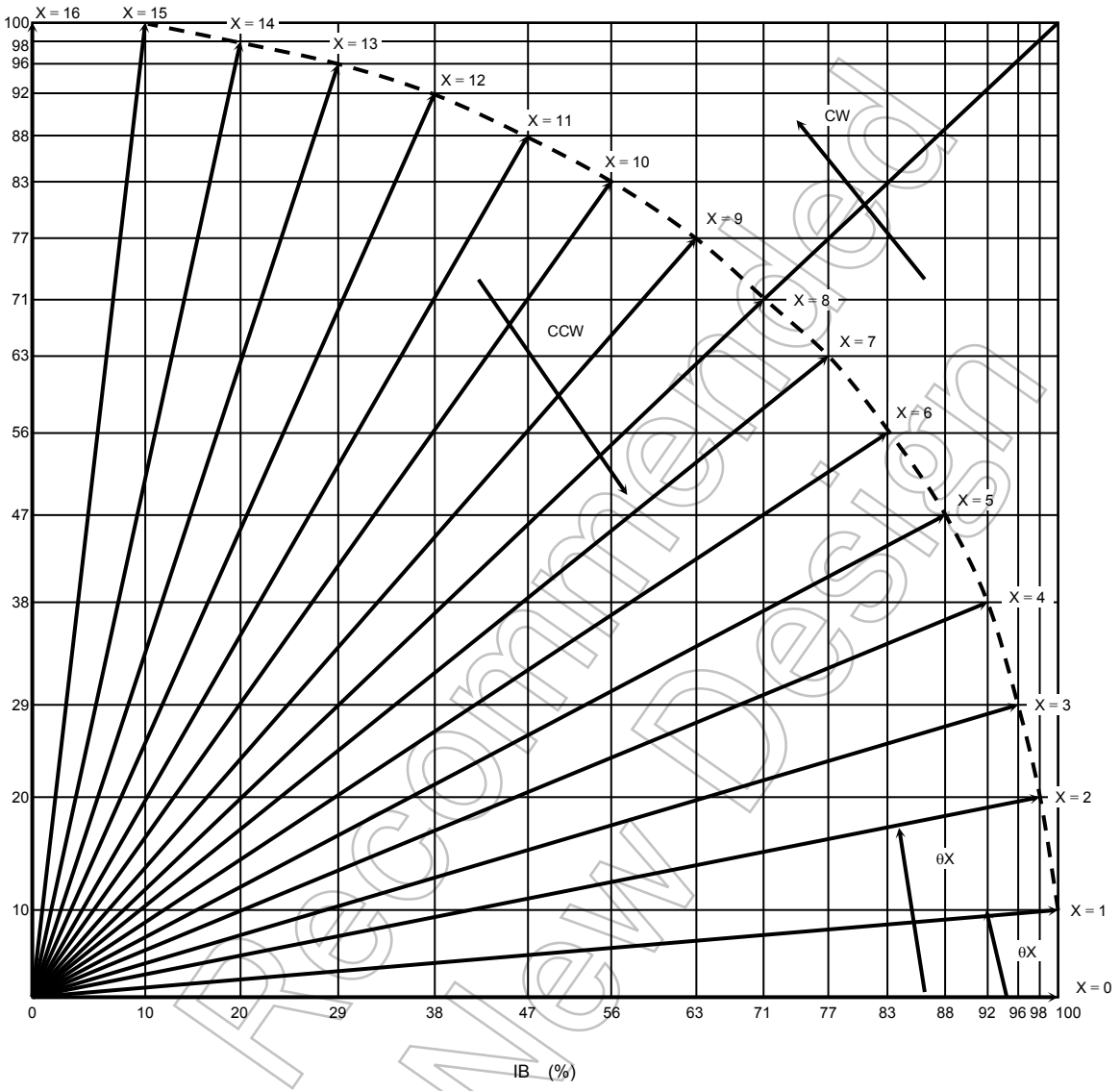
Electrical angle 360° = 32 CLK

(8) 4W1-2 Phase Excitation mode



Electrical angle 360° = 64 CLK

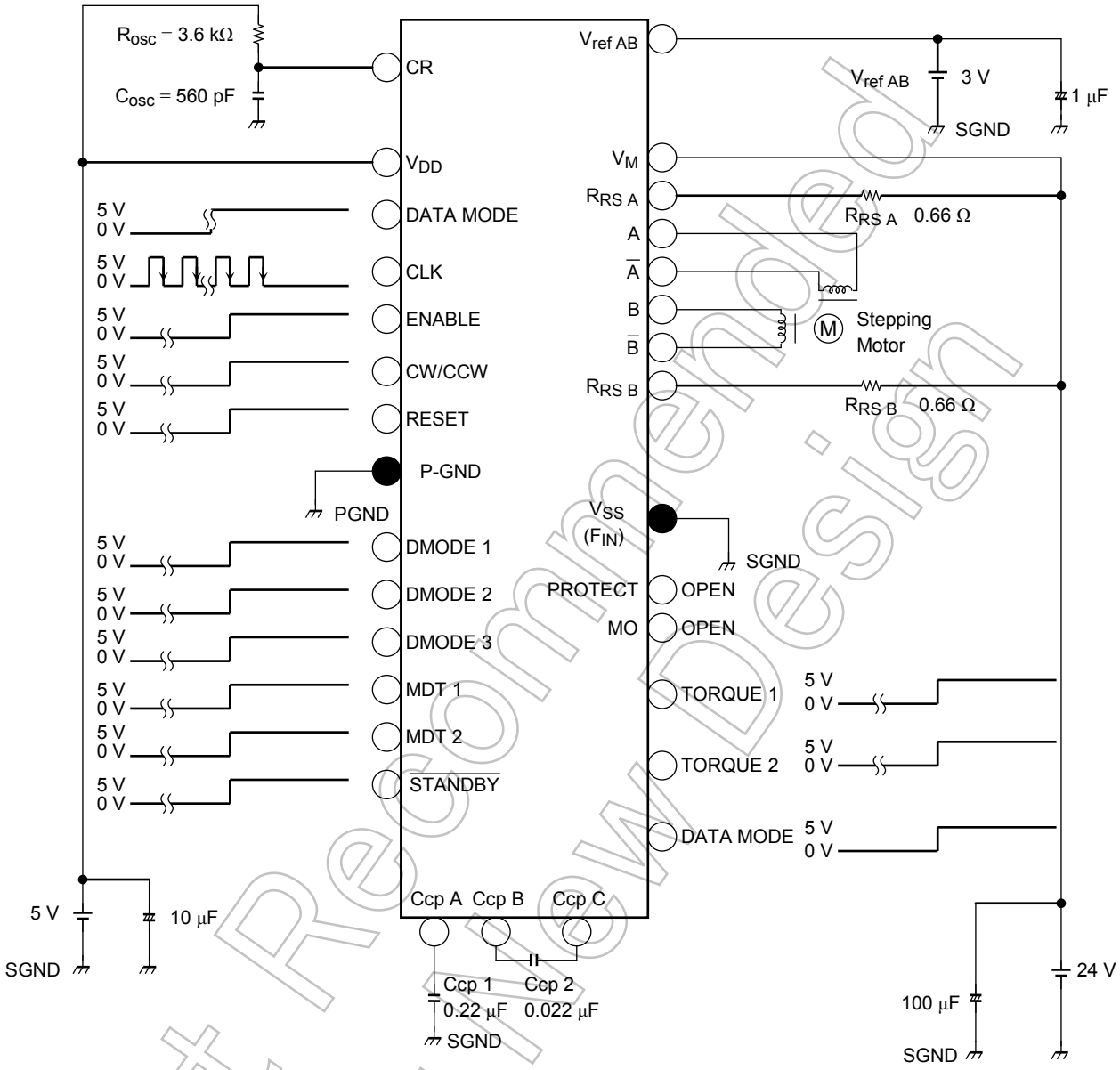
4-Bit Micro Step Output Current Vector Locus (Normalizing each step to 90°)



For input data, see the current function examples.

Application Circuit (example)

The values for the devices are all recommended values. For values under each input condition, see the above-mentioned recommended operating conditions.

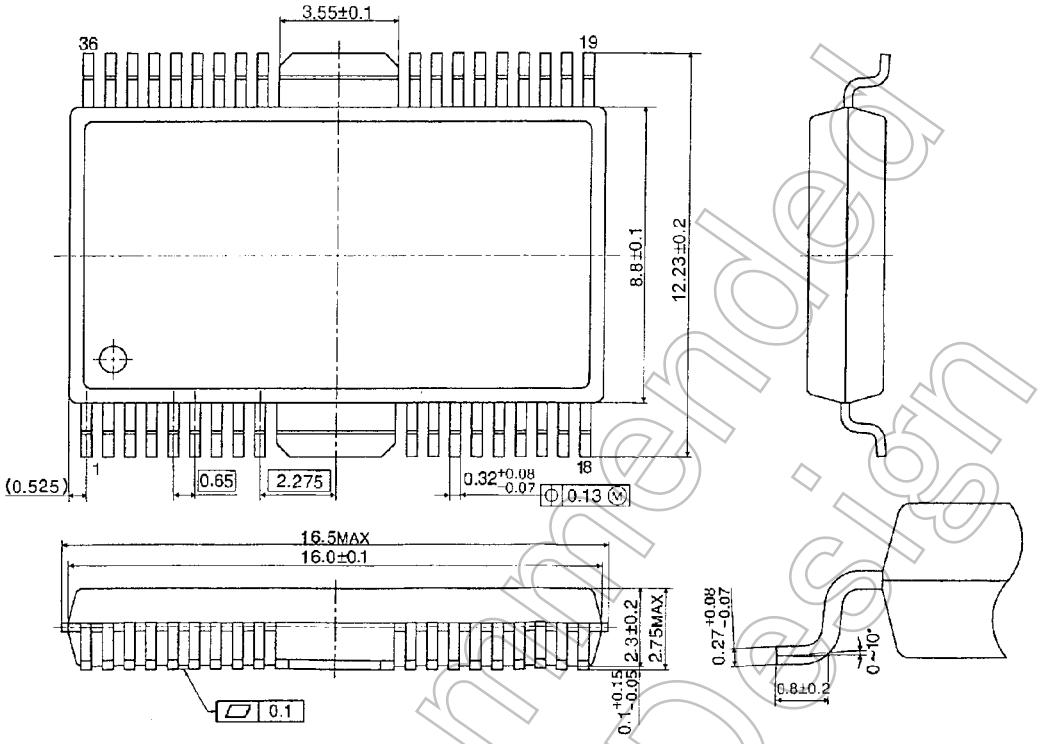


Note: Adding bypass capacitors is recommended.
Make sure that GND wiring has only one contact point, and to design the pattern that allows the heat radiation.
To control setting pins in each mode by SW, make sure to pull down or pull up them to avoid high impedance.
To input the data, see the section on the recommended input data. Please use DATA MODE fixed at the L level.

Careful attention should be paid to the layout of the output, VDD(VM) and GND traces, to avoid short circuits across output pins or to the power supply or ground. If such a short circuit occurs, the device may be permanently damaged.

Package Dimensions

HSOP36-P-450-0.65 Unit: mm



Weight: 0.79 g (typ.)

Notes on Contents

1. Block Diagrams

Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purposes.

2. Equivalent Circuits

The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

3. Timing Charts

Timing charts may be simplified for explanatory purposes.

4. Application Examples

The application examples provided in this data sheet are provided for reference only. Thorough evaluation and testing should be implemented when designing your application's mass production design.

In providing these application examples, Toshiba does not grant the use of any industrial property rights.

5. Test Circuits

Components in the test circuits are used only to obtain and confirm the device characteristics. These components and circuits are not guaranteed to prevent malfunction or failure from occurring in the application equipment.

IC Usage Considerations

Notes on handling of ICs

[1] The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings.
Exceeding the rating(s) may cause breakdown, damage or deterioration of the device, which may result in injury by explosion or combustion.

[2] Do not insert devices incorrectly or in the wrong orientation.
Make sure that the positive and negative terminals of power supplies are connected properly.
Otherwise, the current or power consumption may exceed the absolute maximum rating, and exceeding the rating(s) may cause breakdown, damage or deterioration of the device, which may result in injury by explosion or combustion.
In addition, do not use any device that has had current applied to it while inserted incorrectly or in the wrong orientation even once.

[3] Use an appropriate power supply fuse to ensure that a large current does not continuously flow in the event of over current and/or IC failure. The IC will fully break down when used under conditions that exceed its absolute maximum ratings, when the wiring is routed improperly or when an abnormal pulse noise occurs from the wiring or load, causing a large current to continuously flow. Such a breakdown can lead to smoke or ignition. To minimize the effects of a large current flow in the event of breakdown, fuse capacity, fusing time, insertion circuit location, and other such suitable settings are required.

[4] If your design includes an inductive load such as a motor coil, incorporate a protection circuit into the design to prevent device malfunction or breakdown caused by the current resulting from the inrush current at power ON or the negative current resulting from the back electromotive force at power OFF. IC breakdown may cause injury, smoke or ignition.
For ICs with built-in protection functions, use a stable power supply with. An unstable power supply may cause the protection function to not operate, causing IC breakdown. IC breakdown may cause injury, smoke or ignition.

[5] Carefully select power amp, regulator, or other external components (such as inputs and negative feedback capacitors) and load components (such as speakers).
If there is a large amount of leakage current such as input or negative feedback capacitors, the IC output DC voltage will increase. If this output voltage is connected to a speaker with low input withstand voltage, overcurrent or IC failure can cause smoke or ignition. (The over current can cause smoke or ignition from the IC itself.) In particular, please pay attention when using a Bridge Tied Load (BTL) connection type IC that inputs output DC voltage to a speaker directly.

Points to remember on handling of ICs

(1) Over current Protection Circuit
Over current protection circuits (referred to as current limiter circuits) do not necessarily protect ICs under all circumstances. If the Over current protection circuits operate against the over current, clear the over current status immediately.
Depending on the method of use and usage conditions, such as exceeding absolute maximum ratings can cause the over current protection circuit to not operate properly or IC breakdown before operation. In addition, depending on the method of use and usage conditions, if over current continues to flow for a long time after operation, the IC may generate heat resulting in breakdown.

(2) Thermal Shutdown Circuit
Thermal shutdown circuits do not necessarily protect ICs under all circumstances. If the thermal shutdown circuits operate against the over temperature, clear the heat generation status immediately.
Depending on the method of use and usage conditions, such as exceeding absolute maximum ratings can cause the thermal shutdown circuit to not operate properly or IC breakdown before operation.

(3) Heat Dissipation Design
In using an IC with large current flow such as a power amp, regulator or driver, please design the device so that heat is appropriately dissipated, not to exceed the specified junction temperature (Tj) at any time or under any condition. These ICs generate heat even during normal use. An inadequate IC heat dissipation design can lead to decrease in IC life, deterioration of IC characteristics or IC breakdown. In addition, please design the device taking into consideration the effect of IC heat dissipation on peripheral components.

(4) Back-EMF
When a motor rotates in the reverse direction, stops or slows down abruptly, a current flow back to the motor's power supply due to the effect of back-EMF. If the current sink capability of the power supply is small, the device's motor power supply and output pins might be exposed to conditions beyond maximum ratings. To avoid this problem, take the effect of back-EMF into consideration in your system design.

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