Wireless Power Consortium / Qi Compliant series

Wireless Power Receiver IC

BD57011GWL

General Description

BD57011GWL is stand-alone integrated IC for wireless power receiver. The device is composed fully synchronous rectifier circuit in low-impedance FETs, Qi compliant packet controller, Adjustable low-dropout, and open-drain output terminal to communicate the power transmitter by amplitude modulation.
BD57011GWL applies to 5W-power mobile application based on WPC ver. 1.1.

Features

- Low Impedance FET in rectifier
- High efficiency fully synchronous rectifier
- Maximum Input Voltage is 20V
- WPC / Qi Lower Power ver1.1 support
- Adjustable voltage at low-dropout
- Open-Drain output terminal for modulation
- TX-RX coil Position Gap alarm

Applications

WPC compliant Device
- Smart Phones
- Cell Phones
- Hand-held Mobile Devices

Typical Application Circuit

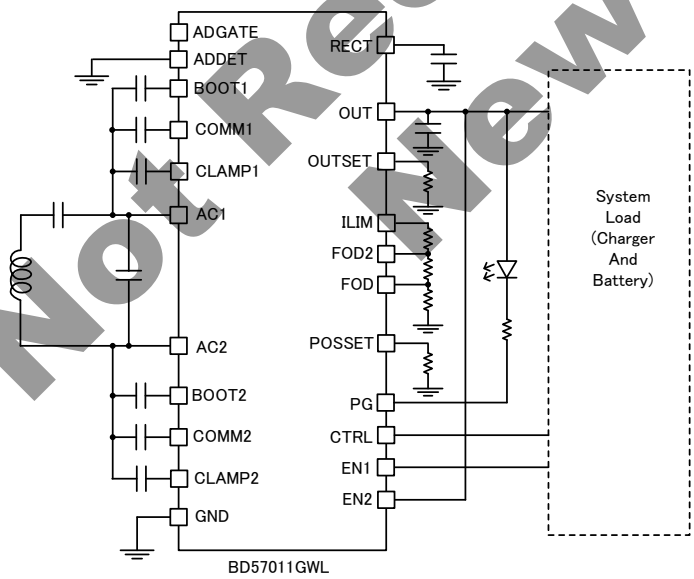


Figure 1. Typical application circuit

Key Specifications

- Variable Output Voltage: 4.3～5.3V(16steps)
- Maximum Input Voltage: 20[V] (Max.)
- Maximum Input/Output Current: 1.1 [A] (Max.)
- AC Input Frequency: 100-210 [kHz]
- Operating Temperature Range: -20°C to +85°C

Package

W(Typ) D(Typ) H(Max)



UCSP50L3C
3.36 ㎜ × 2.62 ㎜ × 0.57 ㎜
(7 x 6 array, 0.4mm pitch)

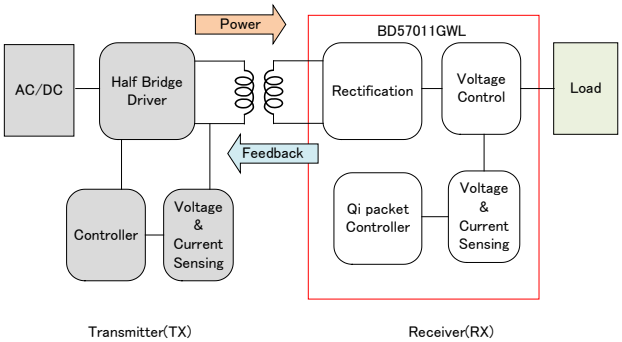


Figure 2. Product position in Wireless Power Supply System

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○Product structure：Silicon monolithic integrated circuit ○This product is not designed protection against radioactive rays

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Absolute Maximum Ratings

Parameter	Symbol	Limit	Unit
RECT,AC1,AC2,COMM1, COMM2,CLAMP1,CLAMP2 Voltage	VINOUT_H	-0.3 to 20	V
BOOT1,BOOT2 Voltage	VINOUT_H2	-0.3 to 26	V
BOOT1-AC1, BOOT2-AC2 Voltage	VBOOT_AC	-0.3 to 7	V
ADDET,ADGATE Voltage	VAD_MAX	-0.3 to 28	V
OUT, OUTSET, POSSET, ILIM, CTRL, EN1, EN2, PG Voltage	VINOUT_L	-0.3 to 7	V
FOD,FOD2 Voltage	VINOUT_L2	-0.3 to 3.6	V
Input/Output rating current	IMAX	1.5(Note 1)	A
PG terminal rating current	IMAX_PG	15	mA
Storage temperature range	Tstg	-55 to +150	°C
Power dissipation	Pd	1.38(Note 2)	W

(Note 1) Applied to AC1, AC2, RECT, GND with the proviso that all multi-terminal should connect to common pattern.
(Note 2) Derate by 11mW/°C when operating above Ta=25°C (when mounted in ROHM's standard board).
Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Recommended Operating Conditions

Parameter	Symbol	Limit	Unit
Rectified Voltage range	VRECT	0 to15	V
AC1,AC2 Input peak Voltage range	VAC1,VAC2	15	V
Capacitance between RECT-GND	CRECT	Min. 20	µF
Operating ambient temperature range	Ta	-20 to +85	°C

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Electrical Characteristics (Unless otherwise specified, Ta = 25 °C, VRECT = 5.0 V)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
Whole Chip						
Operating circuit current 1	IRECT1	-	28	40	mA	VRECT=5.0V, OUT off.
Operating circuit current 2	IRECT2	-	2.4	4.8	mA	VRECT=5.5V, OUT=5V set.
Quiescent current (wireless charging is disable)	IOUT	-	20	40	μA	VOUT=5.0V, RECT=0V
Protection Block						
RECT Under voltage lockout	RECT_UVLO	2.5	2.6	2.7	V	VRECT:0→5V
Hysteresis on UVLO	RECT_UVLOHYS	150	300	450	mV	VRECT:5→0V
RECT Over voltage lockout	RECT_OVLO	14.5	15	15.5	V	VRECT:10→18V
Hysteresis on OVLO	RECT_OVLOHYS	60	130	260	mV	VRECT:18→10V
OUTPUT Block						
Regulated Output Voltage	VOUT	4.93	5.0	5.07	V	Iload=100mA,RSET=27kΩ
OUT Load regulation	dVOUT	-	100	200	mV	Iload=0-500mA
PG Output Block						
Open Drain ability on PG pin	V_{PG}	-	300	500	mV	Isink=5mA
PG pin leak current	Ileak_PG	-	-	2	μA	V_{PG}=7V
ILIM / FOD block						
ILIM Source Current	I_{ILIM}	9.7	10	10.3	μA	RADJ=100kΩ
Highest value of resistance for ILIM setting	R_{ADJ}max	-	-	150	kΩ	
Maximum output current limit	I_{LOAD}max	-	-	1.5	A	Maximum ILIM deliver within 1ms.
FOD pin leak current	Ileak_FOD	-	-	2	μA	VFOD=2V
FOD2 pin leak current	Ileak_FOD2	-	-	2	μA	VFOD2=2V
COMM Block						
Comm1 and Comm2 ON Resistance	RON_COMM	-	2.8	4.2	Ω	
Driving frequency on COMM signal	f_{COMM}	1.92	2	2.08	kHz	
COMM pin leak current	Ileak_comm	-	-	2	μA	V_{COMM}=20V

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Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
CLAMP Block						
Clamp1 and Clamp2 ON Resistance	RON_CLAMP	-	3.8	5.7	Ω	
CLAMP pin leak current	Ileak_clamp	-	-	2	μA	V_{CLAMP}=20V
Adapter Detection Block						
Adapter Input detection threshold voltage	VADDET	3.4	3.6	3.8	V	Vaddet:0→5V
Adapter Input detection hysteresis voltage	VHYS_AD	200	400	600	mV	Vaddet:5→0V
Adapter Input Overvoltage detection voltage	VADDET_OV	6.6	6.8	7.0	V	Vaddet:5→7V
Adapter Input Overvoltage detection hysteresis voltage	VHYS_AD_OV	100	200	400	mV	Vaddet:7→5V
ADDET pin Input current	I_{ADGATE}	-	80	160	μA	V_{ADDET}=5V
EN1, EN2 and CTRL Input Block						
Input low threshold for EN1,EN2 and CTRL	VINL_EN	-	-	0.4	V	
Input high threshold for EN1,EN2 and CTRL	VINH_EN	1.3	-	-	V	
EN1,EN2 and CTRL pull down resistance	R_{EN}	100	200	400	kΩ	

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Typical Performance Cures

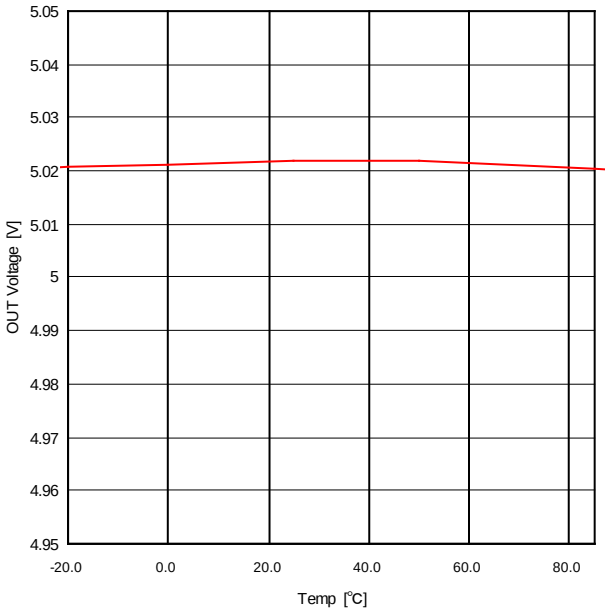


Figure 3. OUT Voltage [V] vs. Temp. [°C] (ILIM=27k Ω)

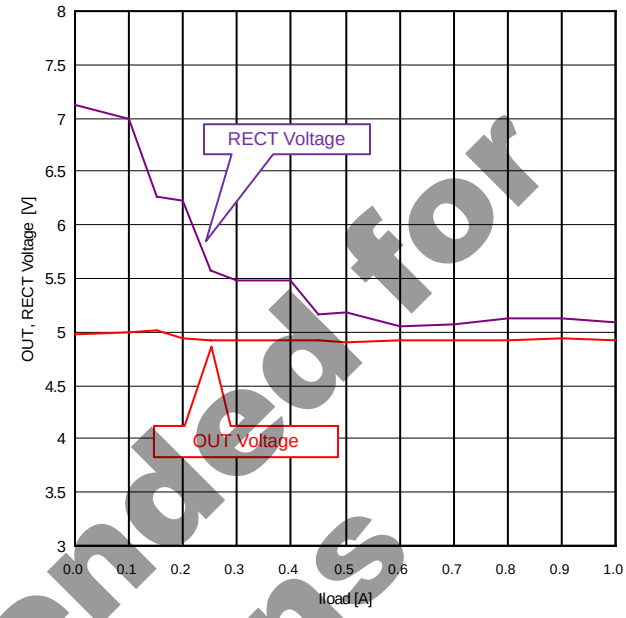


Figure 4. OUT Voltage [V] and RECT Voltage [V] vs. Iload [A] (ILIM=27k Ω)

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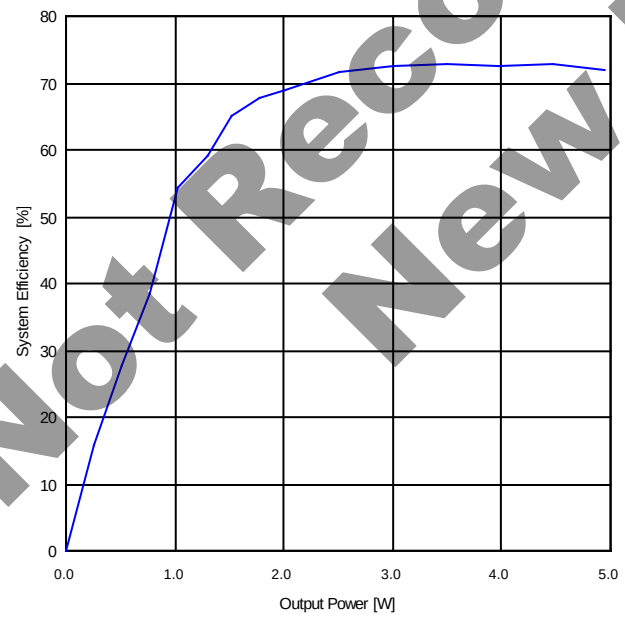


Figure 5. System Efficiency [%] vs. Output Power [W] (ILIM=27k Ω)

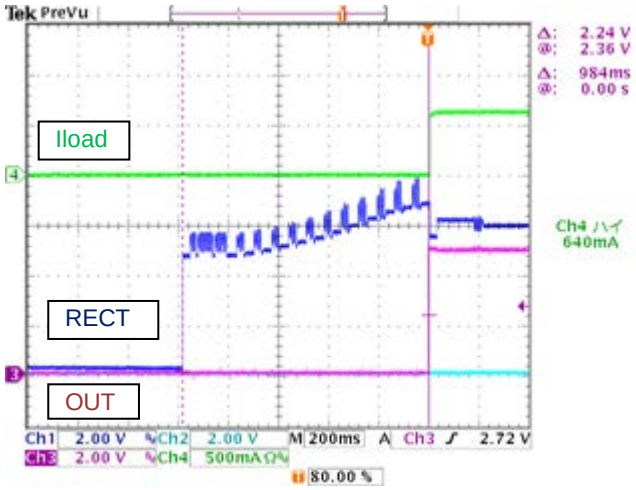


Figure 6. Startup Waveform (ILIM=27k Ω)

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Pin Configuration (Bottom View)

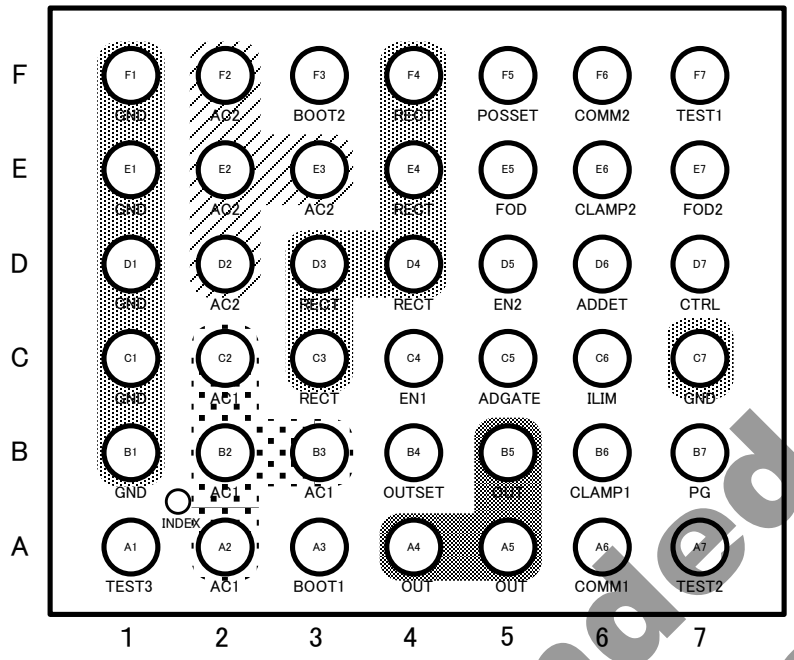


Figure 7. Pin configuration

F7:TEST1, A7:TEST2, A1:TES3 are private TEST terminals, these terminals deal with open.

Pin Description

Pin No.	Pin Name	I/O	Function
B1,C1,C7,D1,E1,F1	GND	-	Rectifier and Analog Ground
D2,E2,E3,F2	AC2	In	AC input2
A2,B2,B3,C2	AC1	In	AC input1
F3	BOOT2	Out	Bootstrap capacitor2 connect for driving FET
C3,D3,D4,E4,F4	RECT	Out	Rectifier Output
A3	BOOT1	Out	Bootstrap capacitor1 connect for driving FET
F5	POSSET	In/Out	Resistor connecting pin for the Position Gap alarm.
B4	OUTSET	In/Out	Resistor connecting pin for output voltage setting
A4,A5,B5	OUT	Out	Adjustable Output
D5	EN2	In	Input that decide to enable/disable wireless and wired charging
C4	EN1	In	
F6	COMM2	Out	Modulation Control Output2
E6	CLAMP2	Out	AC2 Clamp Protection
D6	ADDET	In	Adapter Voltage Detection
C5	ADGATE	Out	External Power Pass Gate Driver
B6	CLAMP1	Out	AC1 Clamp Protection
A6	COMM1	Out	Modulation Control Output1
E5	FOD	In	Foreign Object Detecting adjust pin1
E7	FOD2	In	Foreign Object Detecting adjust pin2
D7	CTRL	In	Input terminal to send End Power packet/ abnormal temperature or termination signal.
C6	ILIM	In/Out	Resistor connecting pin for the over current limit
B7	PG	Out	Open drain Output for know the output is enabled

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Block Diagram

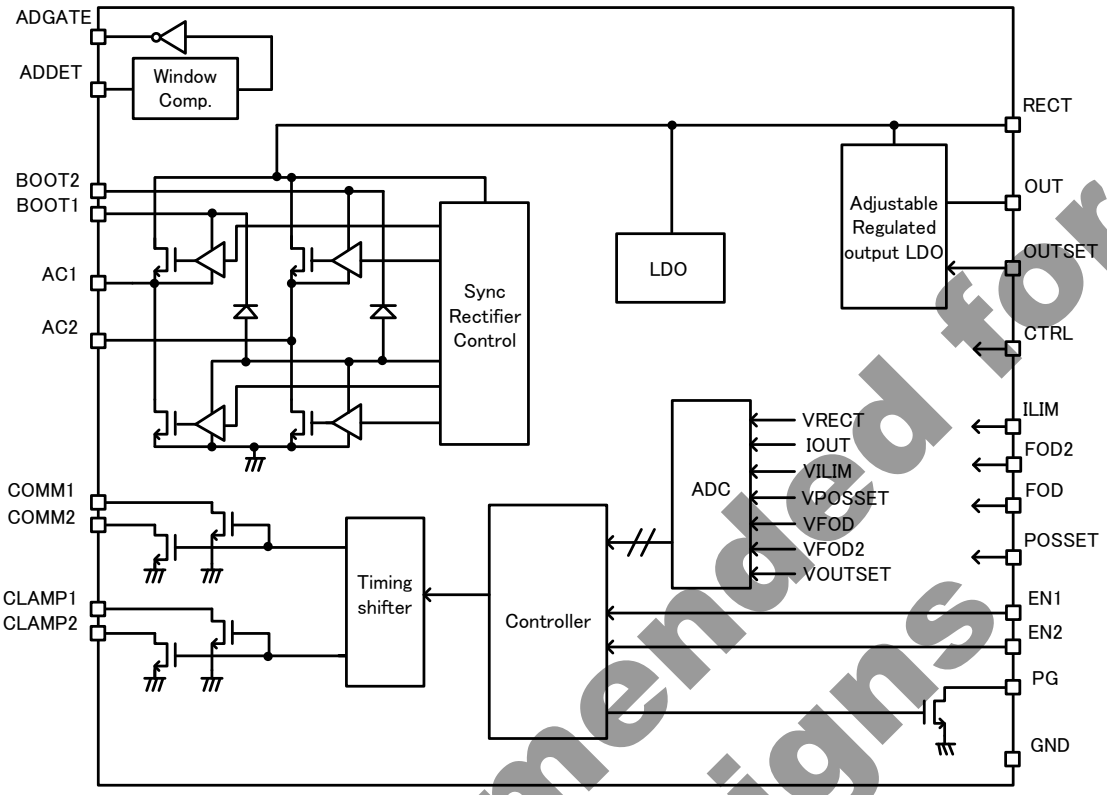


Figure 8. Block diagram

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Description of Block

1) Rectifier block

According to electromagnetic induction phenomena, electromotive force occurs in a secondary side coil in inputting AC signal into the both ends of a primary side (TX) coil. Full-wave rectification by switching operation is realized by detecting output current from the coil generated from the above-mentioned operation, making on/offf built-in FET connected to AC1 and AC2 terminal based on the detection signal, outputting current to RECT, and charging REC terminal external capacity.
Detecting a coil current to compare AC terminal voltage (FET Ron x Icoil) with GND level, it detects the timing set to 0 mA.
The on/off signal of built-in FET is generated based on this detection signal. The on/off timing of L side FET and H side FET was generated, and penetration current is prevented.

The bootstrap drive system which sets the H side-L side to Nch FET is adopted for high efficiency. Therefore, the capacitor for voltage maintenance is needed for BOOT1 (BOOT2) terminal to AC1 (AC2) terminal.

2) Low Drop Out (LDO) block

OUT terminal output voltage can be freely set up by external resistance. It assumes that system load (PMIC) including a charger is connected to an OUT terminal. In order to suppress heating on the whole set, it recommends carrying out an OUT setup near the full charge voltage of the Li-ion battery.

An error signal is returned to the TX side so that the input-and-output difference of RECT and OUT may become the minimum. An input-and-output difference is made small, so that load is large, and heating of IC simple substance is suppressed.
The relation between Iout and desired point (voltage which RECT terminal voltage converges) is as follows.

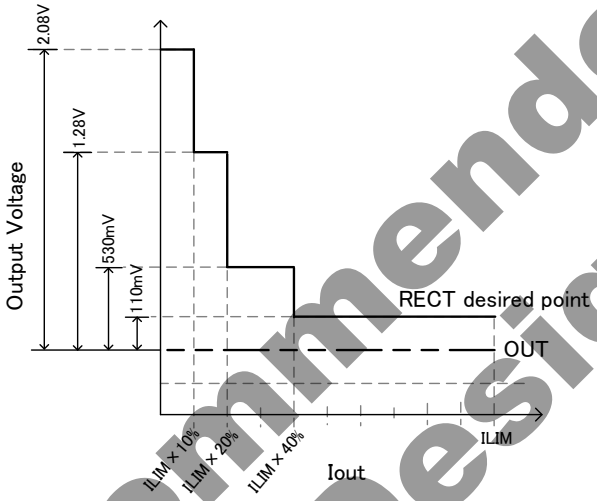


Figure 9. RECT desired point

Output voltage becomes settled uniquely in the resistance (E24 series) connected to an OUTSET terminal.
It can choose from the 16 following steps.

Step	OUT setting[V]	RSET[kΩ](E24)
0	4.30	180
1	4.35	120
2	4.40	91
3	4.45	75
4	4.50	62
5	4.55	56
6	4.60	47
7	4.65	43
8	4.70	39
9	4.75	36
10	4.80	33
11	4.90	30
12	5.00	27
13	5.10	24
14	5.20	22
15	5.30	20

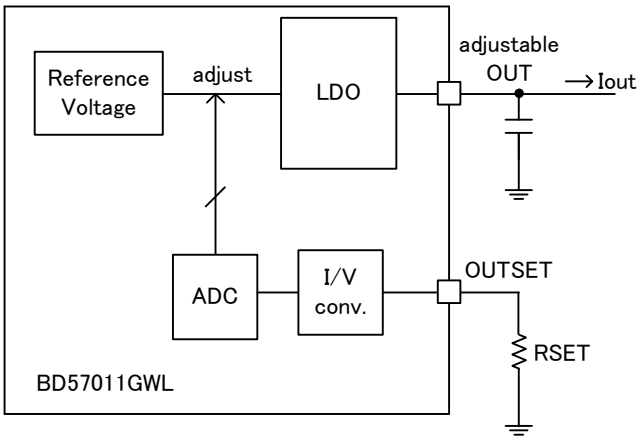


Figure 10. OUTSET circuit

An OUTSET terminal cannot be used by OPEN. Please be sure to use it, connecting resistance.
Moreover, you can't change OUTSET setting during operation.
You need to apply a load after OUT output due to OCP limitation.

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3) A/D Converter block

The Analog to Digital translation of the various analog signals which serve as a candidate for operation in the case of packet generation is carried out. The A/D converter has adopted successive approximation register.
This converter is completed inside IC and cannot be controlled from the outside.

4) Controller block

The packet based on Qi standard (ver1.1) of WPC (Wireless Power Consortium) is controlled.
The packet to support becomes as follows about an End Power Transfer packet(EPT).

End Power transfer			
value	**reason**	**support**	**condition**
0x00	Unknown	Sent	Adapter Input detection
0x01	Charge Complete	Sent	Charge Complete
0x02	Internal Fault	Sent	Internal abnormal temperature, ILIM abnormal setting, OUTSET abnormal setting
0x03	Over Temperature	Sent	External abnormal temperature
0x04	Over Voltage	Not Sent	-
0x05	Over Current	Not Sent	-
0x06	Battery Failure	Not Sent	-
0x07	Reconfiguer	Not Sent	-
0x08	No Response	Sent	No convergence to RECT desired point

5) Adapter detection block

BD57011GWL includes the detective function of the cable power supply of the 5V system.
If it detects that the ADDET terminal became more than 3.6V(typ.),since priority is given to an adapter(cable charge),wireless power supply will be stopped (End Power Transfer output),and an OUT output will be dropped firgt.
It checks after it that OUT has decended enough , and makes the PMOS opposite switch of an adapter line turn on(ADGATE:H →L).
The sequence of operation at the time of adapter detection is as follows.

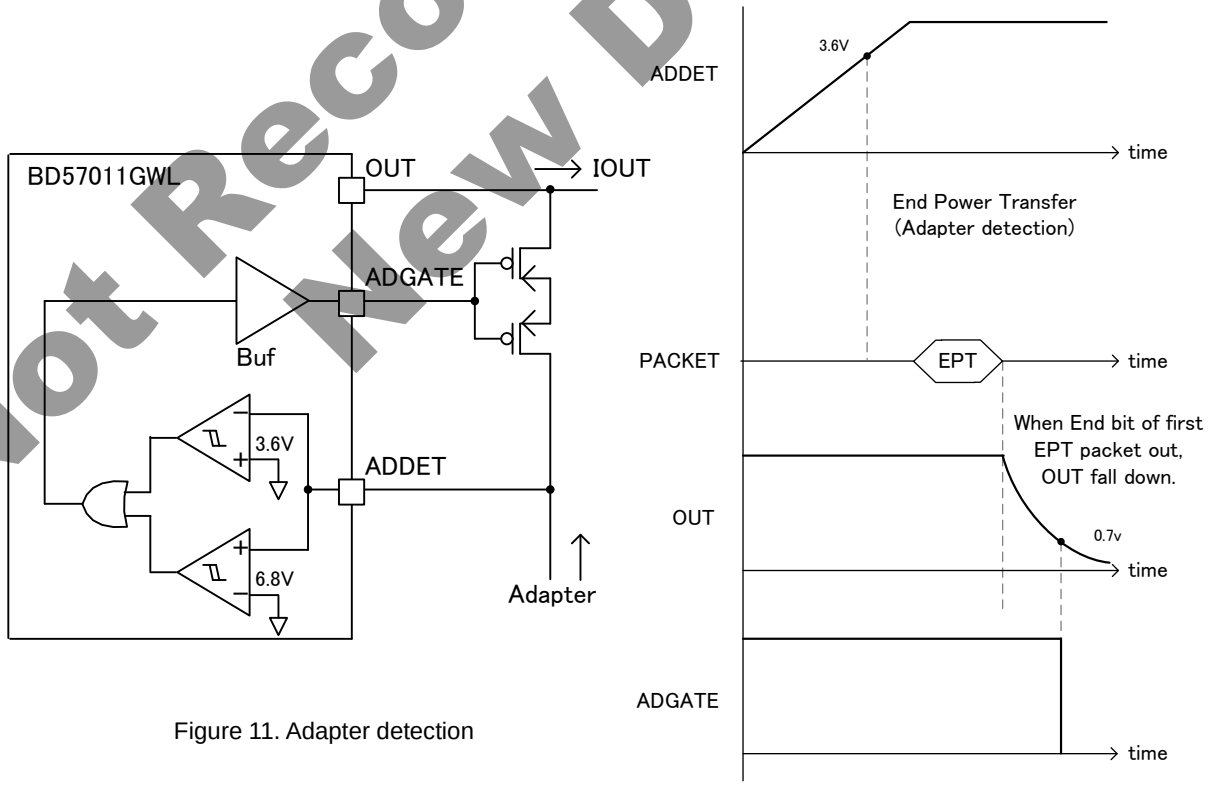


Figure 11. Adapter detection

If set to ADDET>6.8V, it will be in an OVP detection state and will carry out the instant stop of the PMOS of a power path regardless of the existence of wireless power supply.

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6) External control input (EN1, EN2, CTRL).

Active/non-active of wireless supply and wired (adapter) supply can be set up by EN1 and EN2.

It becomes the standard when (EN1=L,EN2=H) setting uses wireless charge, so both wireless power supply and adapter control are active. When both powers come, priority is given to adapter (wired power), wireless power is stopped according to the sequence explained in adapter detection block, and the electrical connection of the path from an adapter is carried out.

When EN1 turn to H, End Power Transfer (0x01: Charge Complete) packet outputs, so wireless power supply will be stopped.

It is as follows if these are summarized in a table.

EN1	EN2	Result
L	H	Both wireless power supply and adapter control are active. Priority is given to the supply from an adapter. That is, if an adapter input is carried out during wireless power supply, wireless power immediately stop and only an adapter carry out.
H	H	Both an adapter and wireless power supply are non-active. That is, in this mode, power is not supplied from OUT.

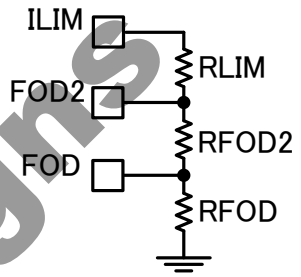
A CTRL terminal becomes an external temperature abnormal signal input.
Please input H signal to suspend wireless power supply system compulsorily by unusual generation of heat of a set, etc.
End Power Transfer (0x03:Over Temperature) is outputted.

7) **ILIM setup**

The current limit value of an OUT terminal can be set up by resistance connected to an ILIM terminal.
The relation between setting resistance and limit current (ILIM) becomes as the following formula.

$$I_{LIM} = RADJ \times 10^{-5}[A]$$

RADJ is total value of RLIM, RFOD2 and RFOD.
E.g. ILIM=1A setup at the time of RADJ=100kΩ.
If RADJ sets over 150kΩ (ILIM setting over 1.5A),
IC outputs EPT packet(internal fault).



$$RADJ = RLIM + RFOD2 + RFOD$$

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9) FOD adjust setting

In order to implement FOD (Foreign Object Detection) function that Qi ver1.1 make rules, it is necessary to compute received power strictly and to compare with the power transmitted power from the TX side. The FOD and FOD2 pin is used for the received power fine tuning. These parameters adjust a lost (e.g. LC loss) which is not understood inside IC.

The relation between received power (PPR) and FOD, FOD2 pin input voltage becomes as the following formula.

$$P_{PR} = \alpha \times f(RECT, IOUT) + \beta[W]$$

$$\alpha = 1 + \frac{VFOD2}{1.955mV} \times 0.004$$

$$\beta = \frac{VFOD}{1.955mV} \times 0.004 - 0.25[W]$$

α is a parameter for slope adjust, proportional to FOD2 voltage. β is a parameter for offset adjust, proportional to FOD voltage. A Function f(RECT, IOUT) is a value calculating in IC, nearly proportional to output power.
Setting example presents. It necessary to coordinated with RFOD, RFOD2 and ILIM setting resistor.
In the case of setting; ILIM=1A, α=1.2, β=0.1W, Solving the following simultaneous equations, the value of FOD setting resistors is obtained.

$$RADJ = RLIM + RFOD2 + RFOD$$

$$\frac{(\alpha - 1) \times 1.955mV}{0.004} = IILIM \times (RFOD2 + RFOD)$$

$$\frac{(\beta + 0.25) \times 1.955mV}{0.004} = IILIM \times RFOD$$

In this case, RFOD=6.9kΩ, RFOD2=10.2kΩ,RLIM=82.9kΩ.
The configuration discribed above is a reference value. Must be adjusted by the considering external factors(the presence or absence of the metal for absorbing the magnetic flux, such as a battery) and the surrounding environment of the coil material, the coil shape, and the distance to the Tx coil.

10) POSSET setting

The height of the RECT voltage at a start-up is judged, and position gap of the XY direction between TX coil and RX coil is detected. The threshold (Vth, pos) of whether to take out alarm with the resistance connected to a POSSET terminal can be decided. When RECT voltage is lower than Vth,pos, a pulse is outputted 5 times from PG terminal at the time of an OUT output.

The relation between setting resistance and detection threshold voltage(Vth,pos) becomes as the following formula.

$$Vth,pos = \frac{2.8 \times 10^5}{RPOS}[V]$$

RPOS is POSSET terminal connection resistance. E.g. Vth,pos=2.8V setup at the time of RPOS=100kΩ.
In the case of nullification for this function, set RPOS=120kΩ.

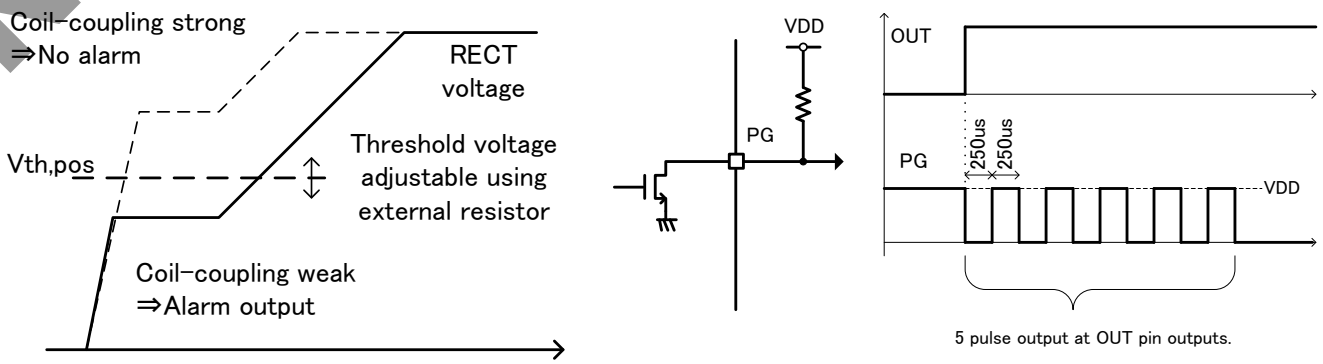


Figure 12. Position Gap alarm

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Application Example

1) Recommended Diagram

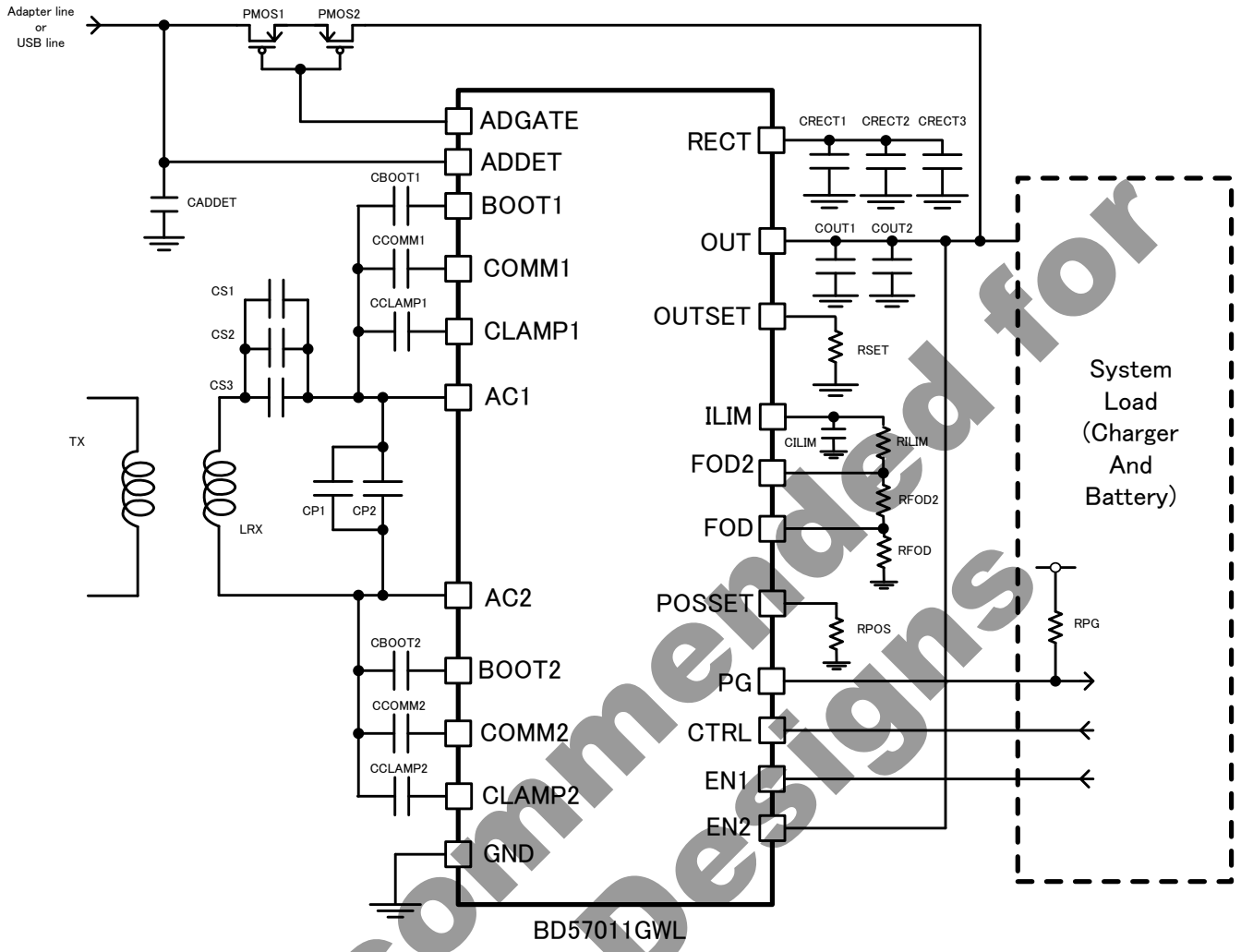


Figure 13. Typical application circuit

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2)Parts list

Part Name	Recommended Value	Unit	Recommended Part	Maker
LRX	12	uH	WR-482350-15M2-G	TDK Co., Ltd.
CS1	0.068	uF	GRM Series	MURATA Co., Ltd.
CS2	0.068	uF	GRM Series	MURATA Co., Ltd.
CS3	0.068	uF	GRM Series	MURATA Co., Ltd.
CP1	1500	pF	GRM Series	MURATA Co., Ltd.
CP2	680	pF	GRM Series	MURATA Co., Ltd.
CBOOT1, CBOOT2	0.01	uF	GRM Series	MURATA Co., Ltd.
CCOMM1, CCOMM2	0.033	uF	GRM Series	MURATA Co., Ltd.
CCLAMP1, CCLAMP2	0.47	uF	GRM Series	MURATA Co., Ltd.
CRECT1	0.1	uF	GRM Series	MURATA Co., Ltd.
CRECT2	10	uF	GRM Series	MURATA Co., Ltd.
CRECT3	10	uF	GRM Series	MURATA Co., Ltd.
COUT1	0.1	uF	GRM Series	MURATA Co., Ltd.
COUT2	2.2	uF	GRM Series	MURATA Co., Ltd.
CILIM	No Mount (dummy)	pF	-	-
CADDET	1.0	uF	GRM Series	MURATA Co., Ltd.
RSET	Refer to OUTSET setting	kΩ	MCR006	ROHM Co., Ltd.
RILIM	Refer to ILIM setting	kΩ	MCR006	ROHM Co., Ltd.
RFOD	Refer to FOD setting	kΩ	MCR006	ROHM Co., Ltd.
RFOD2	Refer to FOD setting	kΩ	MCR006	ROHM Co., Ltd.
RPOS	47 to 130	kΩ	MCR006	ROHM Co., Ltd.
PMOS1, PMOS2	Ron < 100mΩ	-	TT8J2TR	ROHM Co., Ltd.

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Timing Chart

Start up sequence

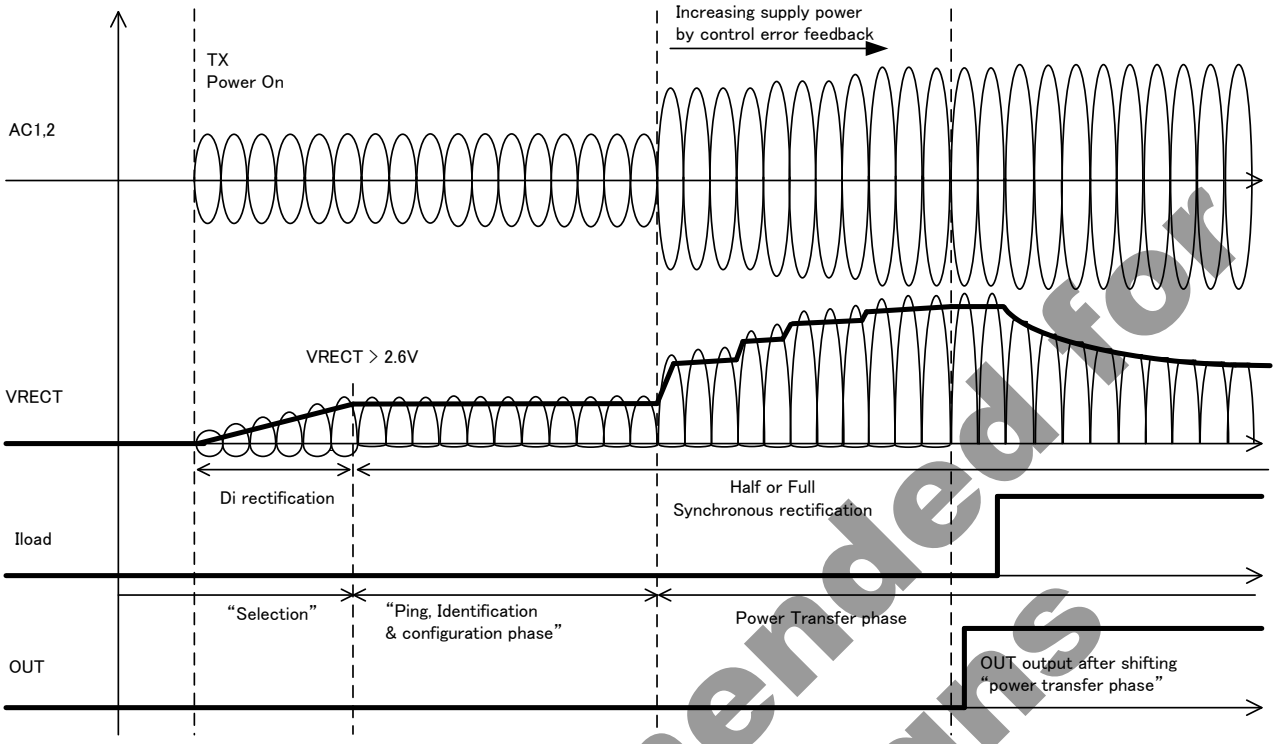
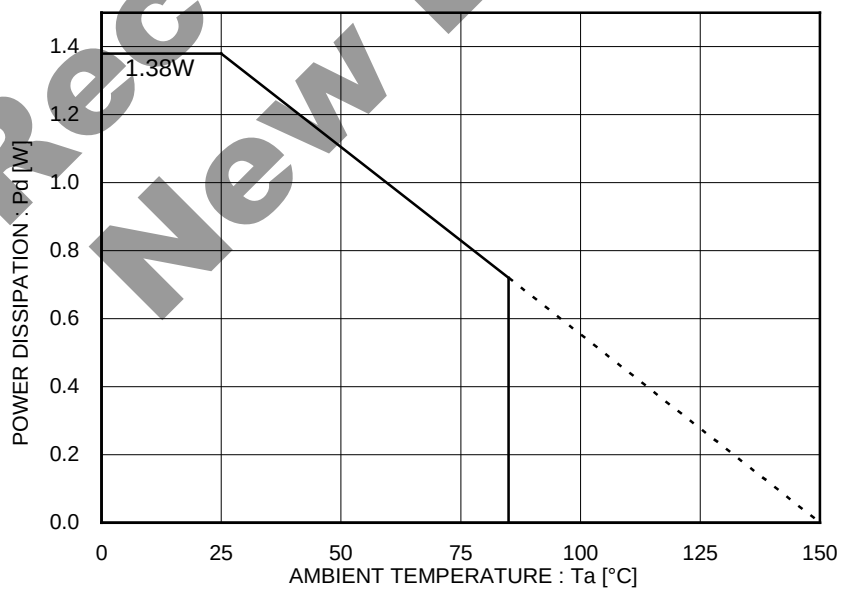


Figure 14. Start up sequence

Power Dissipation

(UCSP50L3C Package)

Use a thermal design that allows for a sufficient margin by taking into account the permissible power dissipation (Pd) in actual operating conditions.



* 54mm x 62mm x 1.6mm Glass Epoxy Board

Figure 15. Power Dissipation Curve (Pd-Ta Curve)

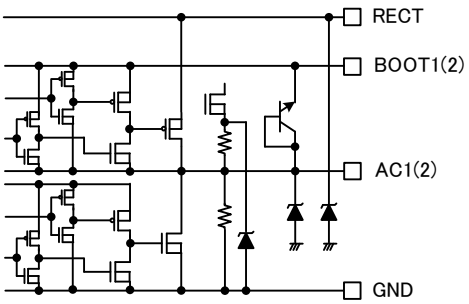
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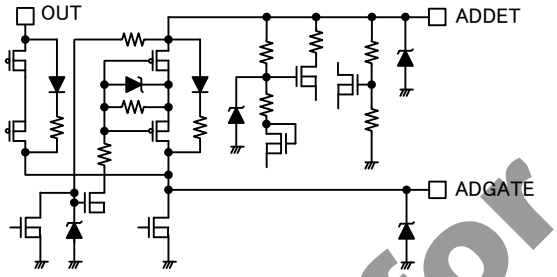
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I/O equivalence circuit

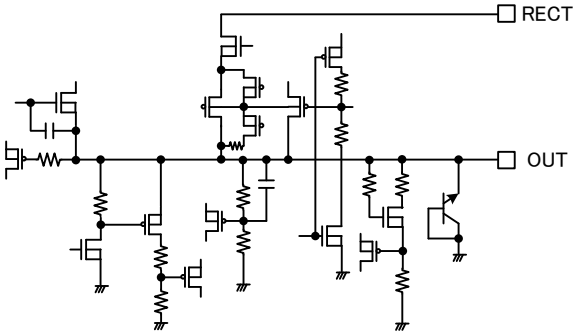
RECT, AC1(2), BOOT1(2), GND pin



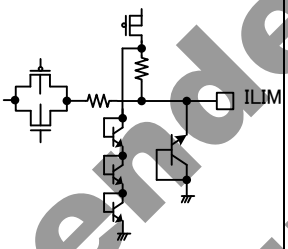
ADDET, ADGATE pin



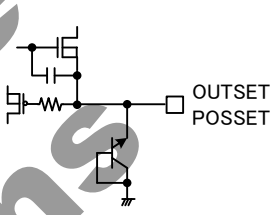
OUT pin



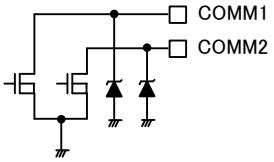
ILIM pin



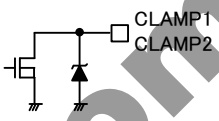
OUTSET,POSSET pin



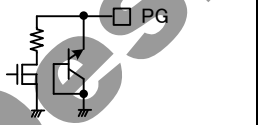
COMM1, COMM2 pin



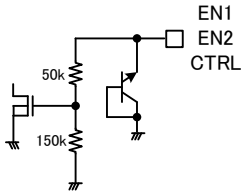
CLAMP1, CLAMP2 pin



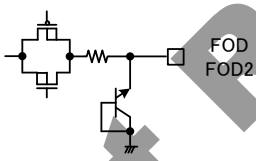
PG pin



EN1,EN2,CTRL pin



FOD, FOD2 pin



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Operation Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply terminals.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Thermal Consideration**
   Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. The absolute maximum rating of the Pd stated in this specification is when the IC is mounted on a 54mm x 62mm x 1.6mm glass epoxy board. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6. **Recommended Operating Conditions**
   These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. **Rush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. **Operation Under Strong Electromagnetic Field**
   Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. **Inter-pin Short and Mounting Errors**
    Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

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Operational Notes – continued

11. Unused Input Terminals

Input terminals of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input terminals should be connected to the power supply or ground line.

12. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

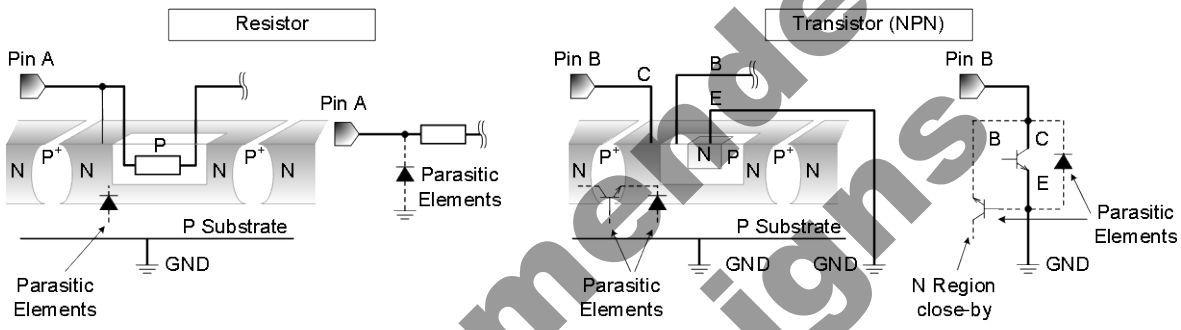


Figure 16. Example of monolithic IC structure

13. Ceramic Capacitor

When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

14. Thermal Shutdown Circuit(TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's power dissipation rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF all output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

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Status of this document
The English version of this document is formal specification. A customer may use this translation version only for a reference to help reading the formal version.
If there are any differences in translation version of this document formal version takes priority

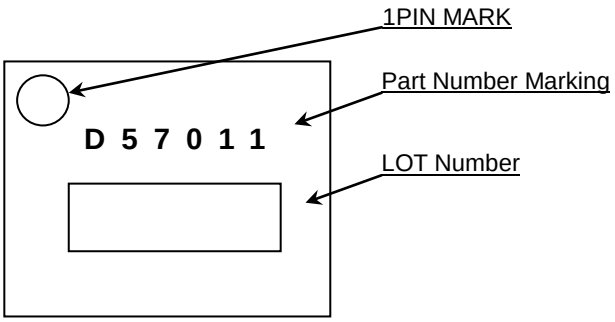
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Ordering Information

B D 5 7 0 1 1 G W L	-	E 2
Part Number		Package GWL: UCSP50L3C
		Packaging and forming specification E2: Embossed tape and reel

Marking Diagram



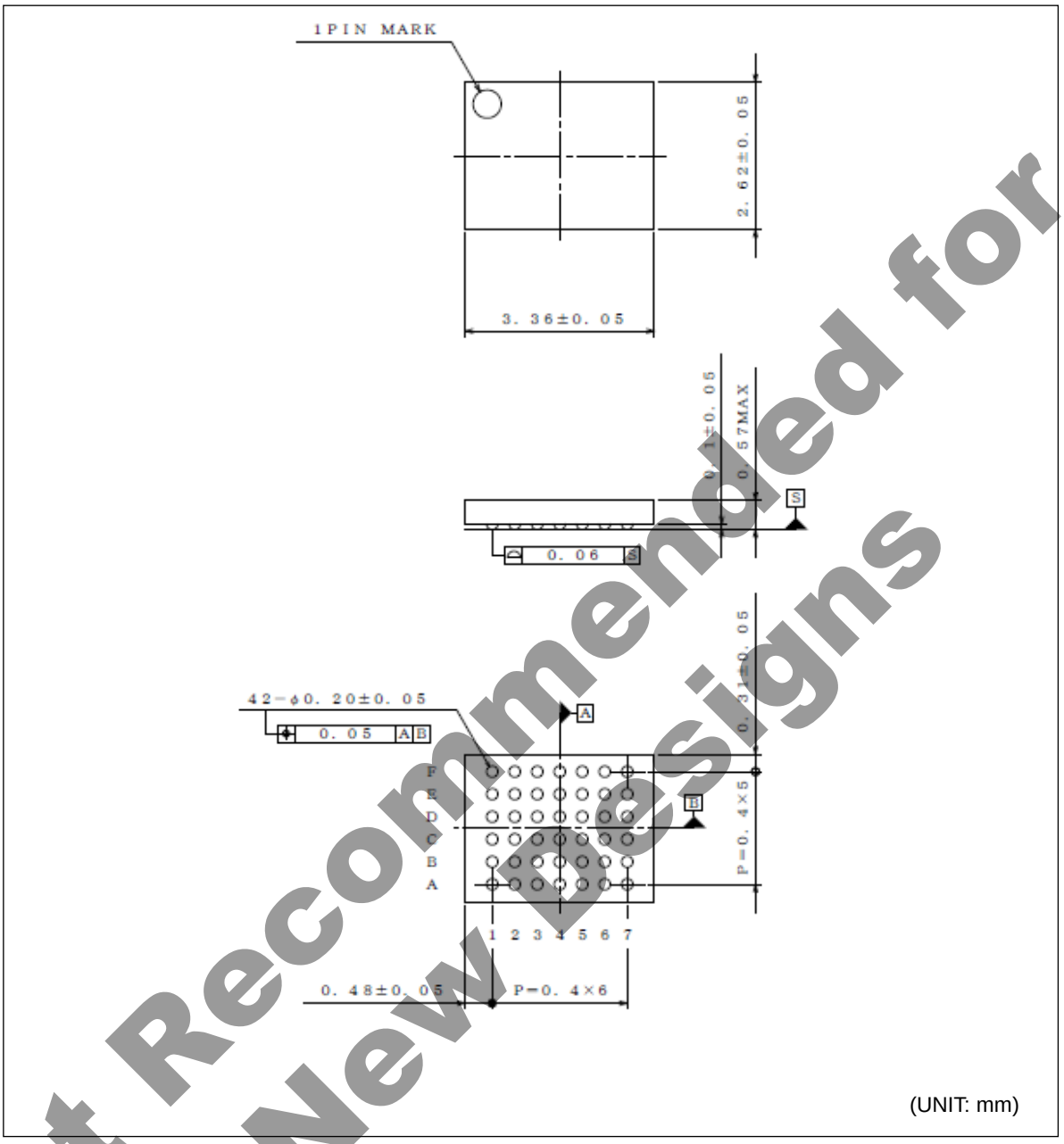
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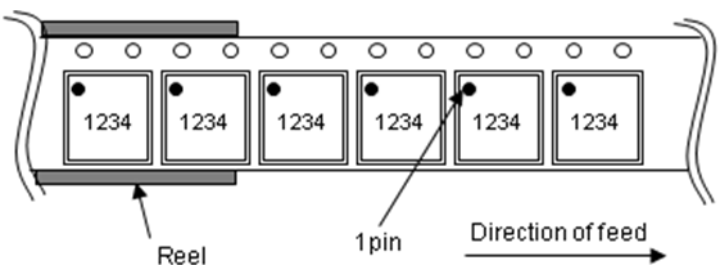
Physical Dimension Tape and Reel Information

Package Name	UCSP50L3C(BD57011GWL)



< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	2,500pcs
Direction of feed	E2 The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand



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Revision History

Date	Revision	Changes
29.Nov.2013	001	New Release
28.Aug.2014	001b	revision
10.Jun.2015	001c	Correct written error (P.6 an explanation for Pin configuration)
2.Jul.2015	002	Page. 5 Correct written error (Figure 4. X-axis name) Page. 6 Correct written error (an explanatory note for Pin Configuration) Page. 9 Correct written error (Figure 11. PMOS symbol, add X-axis name(time)) Page.11 “POSSET setting”: add an explanatory note about nullification Page.12 “Recommended Diagram”, “Parts list” modification(CFOD, CFOD2 delete) Page.13 “Start up sequence” modification(Iload timing, AC1 and AC2 waveform)

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(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

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   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

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   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation (Pd) depending on Ambient temperature (Ta). When used in sealed area, confirm the actual ambient temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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