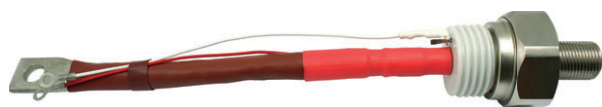


Phase Control Thyristors (Stud Version), 330 A


TO-118 (TO- 209AE)

FEATURES

- Center amplifying gate
- International standard case TO-118 (TO-209AE)
- Hermetic metal case with ceramic insulator
- Compression bonded encapsulation for heavy duty operations such as severe thermal cycling
- Designed and qualified for industrial level
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912


**RoHS
COMPLIANT**

PRIMARY CHARACTERISTICS

$I_{T(AV)}$	330 A
V_{DRM}/V_{RRM}	400 V, 800 V, 1200 V, 1400 V, 1600 V, 2000 V
V_{TM}	1.52 V
I_{GT}	200 mA
T_J	-40 °C to +125 °C
Package	TO-118 (TO-209AE)
Circuit configuration	Single SCR

TYPICAL APPLICATIONS

- DC motor controls
- Controlled DC power supplies
- AC controllers

MAJOR RATINGS AND CHARACTERISTICS

PARAMETER	TEST CONDITIONS	VALUES	UNITS
$I_{T(AV)}$		330	A
	T_C	75	°C
$I_{T(RMS)}$		520	A
I_{TSM}	50 Hz	9000	
	60 Hz	9420	
I^2t	50 Hz	405	kA ² s
	60 Hz	370	
V_{DRM}/V_{RRM}		400 to 2000	V
t_q	Typical	100	μs
T_J		-40 to +125	°C

ELECTRICAL SPECIFICATIONS

VOLTAGE RATINGS

TYPE NUMBER	VOLTAGE CODE	V_{DRM}/V_{RRM} , MAXIMUM REPETITIVE PEAK AND OFF-STATE VOLTAGE V	V_{RSM} , MAXIMUM NON-REPETITIVE PEAK VOLTAGE V	I_{DRM}/I_{RRM} MAXIMUM AT $T_J = T_J$ MAXIMUM mA
VS-ST330S	04	400	500	50
	08	800	900	
	12	1200	1300	
	14	1400	1500	
	16	1600	1700	
	20	2000	2100	



ABSOLUTE MAXIMUM RATINGS						
PARAMETER	SYMBOL	TEST CONDITIONS			VALUES	UNITS
Maximum average on-state current at case temperature	I _{T(AV)}	180° conduction, half sine wave			330	A
					75	°C
Maximum RMS on-state current	I _{T(RMS)}	DC at 75 °C case temperature			520	A
Maximum peak, one-cycle non-repetitive surge current	I _{TSM}	t = 10 ms	No voltage reapplied	Sinusoidal half wave, initial T _J = T _J maximum	9000	
		t = 8.3 ms			9420	
		t = 10 ms	100 % V _{RRM} reapplied		7570	
		t = 8.3 ms			7920	
Maximum I ² t for fusing	I ² t	t = 10 ms	No voltage reapplied		405	kA ² s
		t = 8.3 ms			370	
		t = 10 ms	100 % V _{RRM} reapplied		287	
		t = 8.3 ms			262	
Maximum I ² √t for fusing	I ² √t	t = 0.1 to 10 ms, no voltage reapplied			4050	kA ² √s
Low level value of threshold voltage	V _{T(TO)1}	(16.7 % × π × I _{T(AV)}) < I < π × I _{T(AV)} , T _J = T _J maximum			0.834	V
High level value of threshold voltage	V _{T(TO)2}	(I > π × I _{T(AV)}), T _J = T _J maximum			0.898	
Low level value of on-state slope resistance	r _{t1}	(16.7 % × π × I _{T(AV)}) < I < π × I _{T(AV)} , T _J = T _J maximum			0.687	mΩ
High level value of on-state slope resistance	r _{t2}	(I > π × I _{T(AV)}), T _J = T _J maximum			0.636	
Maximum on-state voltage	V _{TM}	I _{pk} = 1000 A, T _J = T _J maximum, t _p = 10 ms sine pulse			1.52	V
Maximum holding current	I _H	T _J = 25 °C, anode supply 12 V resistive load			600	mA
Typical latching current	I _L				1000	

SWITCHING				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum non-repetitive rate of rise of turned-on current	di/dt	Gate drive 20 V, 20 Ω, $t_r \leq 1$ μs $T_J = T_J$ maximum, anode voltage ≤ 80 % V_{DRM}	1000	A/μs
Typical delay time	t_d	Gate current A, $di_g/dt = 1$ A/μs $V_d = 0.67$ % V_{DRM} , $T_J = 25$ °C	1.0	μs
Typical turn-off time	t_q	$I_{TM} = 550$ A, $T_J = T_J$ maximum, $di/dt = 40$ A/μs, $V_R = 50$ V, $dV/dt = 20$ V/μs, gate 0 V 100 Ω, $t_p = 500$ μs	100	

BLOCKING				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum critical rate of rise of off-state voltage	dV/dt	$T_J = T_J$ maximum linear to 80 % rated V_{DRM}	500	V/μs
Maximum peak reverse and off-state leakage current	I_{RRM} , I_{DRM}	$T_J = T_J$ maximum, rated V_{DRM}/V_{RRM} applied	50	mA



TRIGGERING						
PARAMETER	SYMBOL	TEST CONDITIONS		VALUES		UNITS
				TYP.	MAX.	
Maximum peak gate power	P _{GM}	T _J = T _J maximum, t _p ≤ 5 ms		10.0		W
Maximum average gate power	P _{G(AV)}	T _J = T _J maximum, f = 50 Hz, d% = 50		2.0		
Maximum peak positive gate current	I _{GM}	T _J = T _J maximum, t _p ≤ 5 ms		3.0		A
Maximum peak positive gate voltage	+V _{GM}	T _J = T _J maximum, t _p ≤ 5 ms		20		V
Maximum peak negative gate voltage	-V _{GM}			5.0		
DC gate current required to trigger	I _{GT}	T _J = -40 °C	Maximum required gate trigger/ current/voltage are the lowest value which will trigger all units 12 V anode to cathode applied	200	-	mA
		T _J = 25 °C		100	200	
		T _J = 125 °C		50	-	
DC gate voltage required to trigger	V _{GT}	T _J = -40 °C		2.5	-	V
		T _J = 25 °C		1.8	3	
		T _J = 125 °C		1.1	-	
DC gate current not to trigger	I _{GD}	T _J = T _J maximum	Maximum gate current/voltage not to trigger is the maximum value which will not trigger any unit with rated V _{DRM} anode to cathode applied	10		mA
DC gate voltage not to trigger	V _{GD}			0.25		V

THERMAL AND MECHANICAL SPECIFICATIONS				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum operating junction temperature range	T_J		-40 to +125	°C
Maximum storage temperature range	T_{Stg}		-40 to +150	
Maximum thermal resistance, junction to case	R_{thJC}	DC operation	0.10	K/W
Maximum thermal resistance, case to heatsink	R_{thC-hs}	Mounting surface, smooth, flat and greased	0.03	
Mounting torque, ± 10 %		Non-lubricated threads	48.5 (425)	N · m (lbf · in)
Approximate weight			535	g
Case style		See dimension - link at the end of datasheet	TO-118 (TO-209AE)	

ΔR_{thJC} CONDUCTION				
CONDUCTION ANGLE	SINUSOIDAL CONDUCTION	RECTANGULAR CONDUCTION	TEST CONDITIONS	UNITS
180°	0.011	0.008	$T_J = T_J$ maximum	K/W
120°	0.013	0.014		
90°	0.017	0.018		
60°	0.025	0.026		
30°	0.041	0.042		

Note

- The table above shows the increment of thermal resistance R_{thJC} when devices operate at different conduction angles than DC

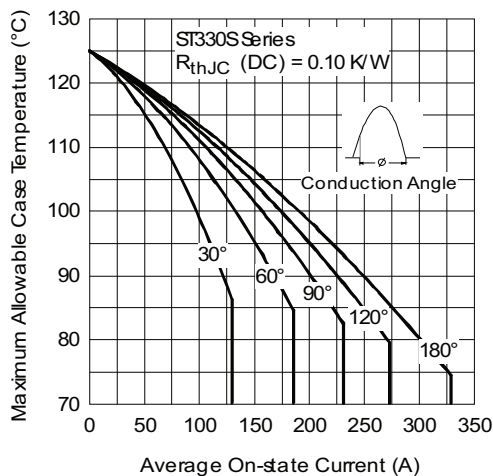


Fig. 1 - Current Ratings Characteristics

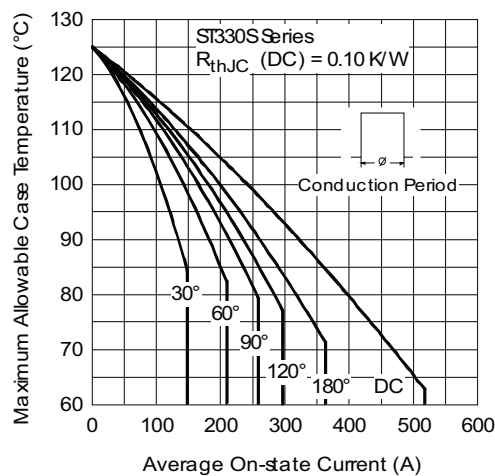


Fig. 2 - Current Ratings Characteristics

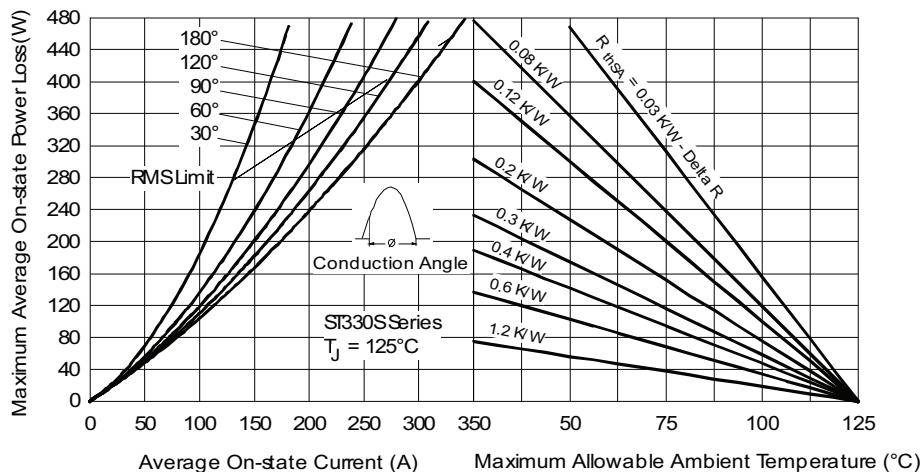


Fig. 3 - On-State Power Loss Characteristics

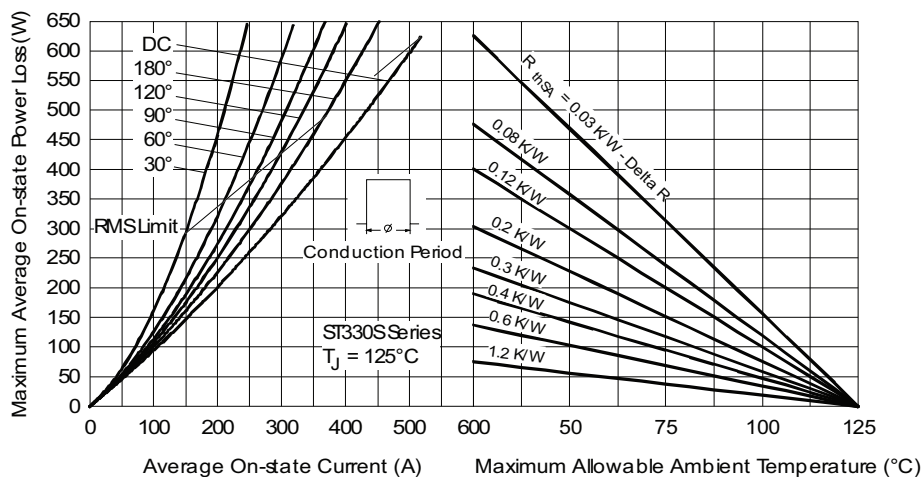


Fig. 4 - On-State Power Loss Characteristics

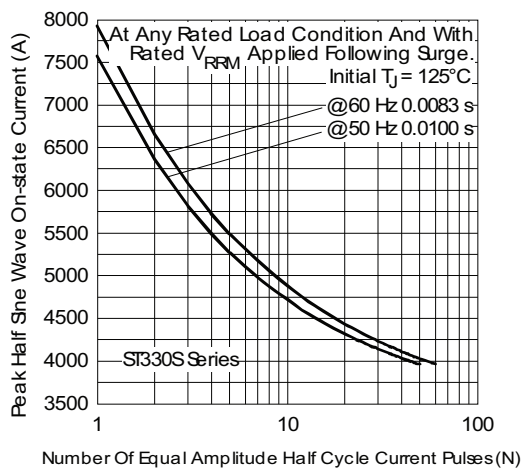


Fig. 5 - Maximum Non-Repetitive Surge Current

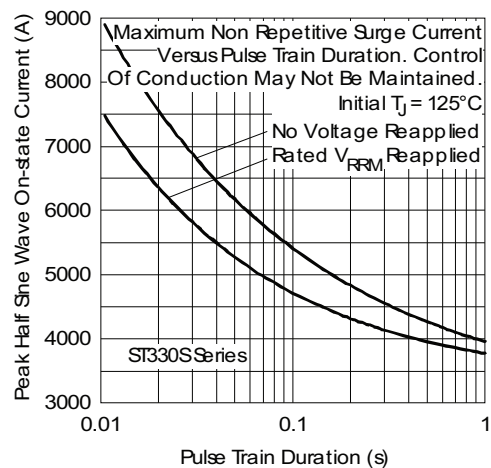


Fig. 6 - Maximum Non-Repetitive Surge Current

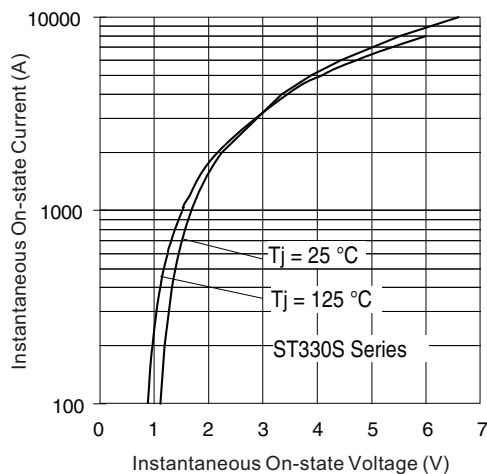
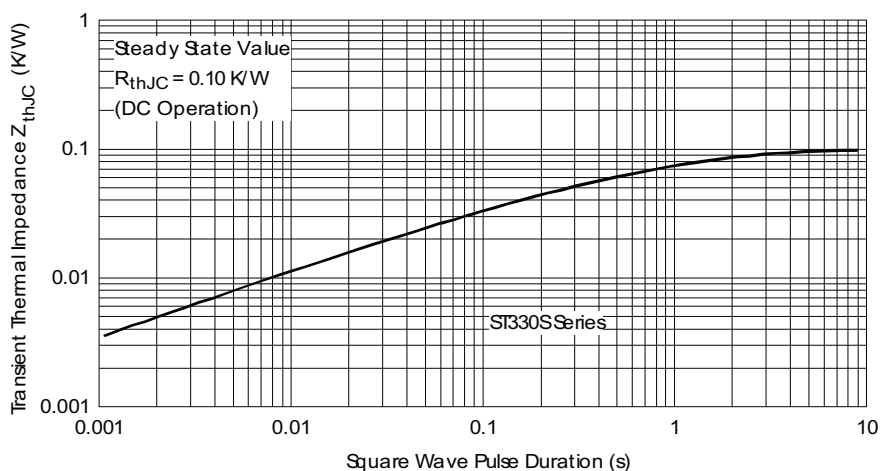


Fig. 7 - On-State Voltage Drop Characteristics


Fig. 8 - Thermal Impedance Z_{thJC} Characteristics

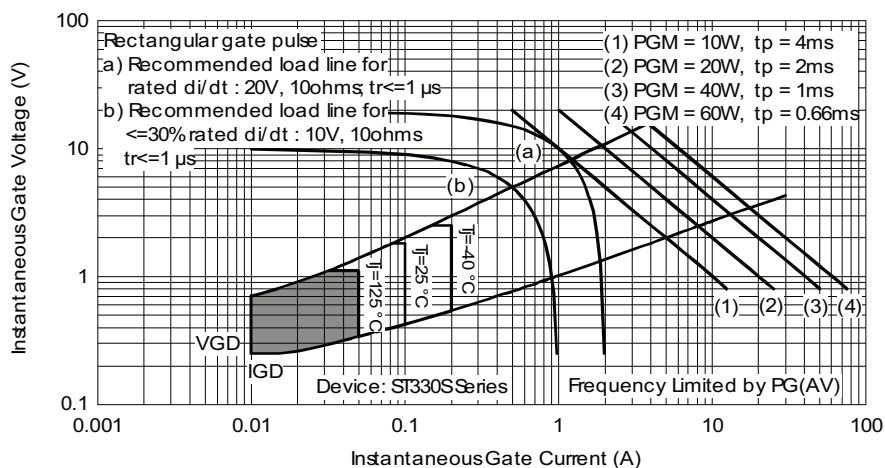


Fig. 9 - Gate Characteristics

ORDERING INFORMATION TABLE

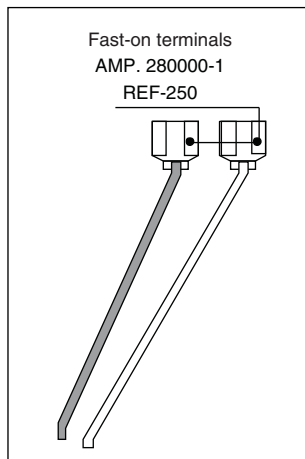
Device code	VS-	ST	33	0	S	16	P	0	PbF
	1	2	3	4	5	6	7	8	9
1	Vishay Semiconductors product								
2	Thyristor								
3	Essential part number								
4	0 = converter grade								
5	S = compression bonding stud								
6	Voltage code x 100 = V_{RRM} (see Voltage Ratings table)								
7	P = stud base 3/4"-16UNF-2A threads M = stud base metric threads (M24 x 1.5)								
8	0 = eyelet terminals (gate and auxiliary cathode leads) 1 = fast-on terminals (gate and auxiliary cathode leads)								
9	None = standard production PbF = lead (Pb)-free								

LINKS TO RELATED DOCUMENTS

Dimensions

www.vishay.com/doc?95080

DIMENSIONS in millimeters (inches)



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