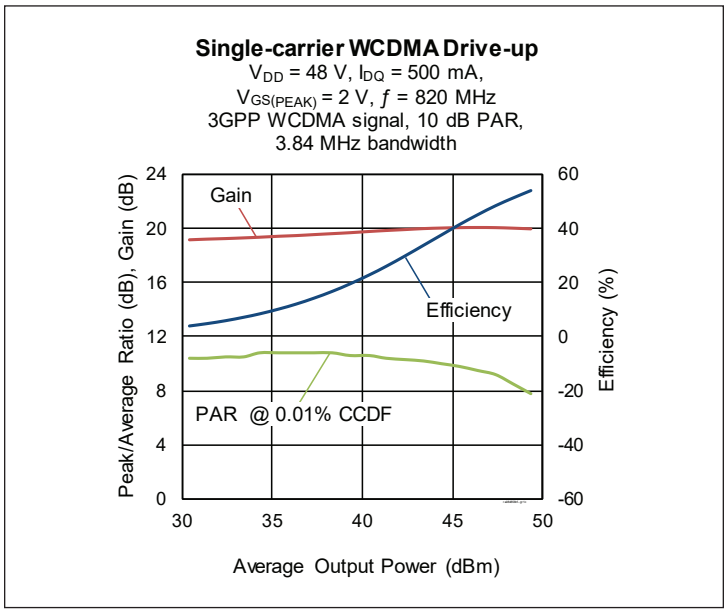
PTRA084858NF

Thermally-Enhanced High Power RF LDMOS FET
615 W, 48 V, 730 – 960 MHz

Description

The PTRA084858NF is a 615-watt LDMOS FET intended for use in multistandard cellular power amplifier applications in the 730 to 960 MHz frequency band. Features include input and output matching, high gain and a thermally-enhanced plastic overmold package for cool and reliable operation. Manufactured with an advanced LDMOS process, this device provides excellent thermal performance and superior reliability.

PTRA084858NF
Package PG-HBSOF-6-3



Features

- Broadband Input and output matching
- Asymmetric Doherty design
  - Main: P1dB = 211 W Typ
  - Peak: P1dB = 468 W Typ
- Typical pulsed CW performance: 10 µs pulse width, 10% duty cycle, 820 MHz, 48 V, Doherty fixture
  - Gain = 19.5 dB
  - Efficiency = 52%
  - Output power at P_{1dB} = 214 W
  - Output power at P_{3dB} = 615 W
- Capable of handling 10:1 VSWR @ 48 V, 87 W (CW) output power
- Integrated ESD protection
- Human Body Model Class 1C (per ANSI/ESDA/JEDEC JS-001)
- Pb-free and RoHS-compliant

RF Characteristics

Single-carrier WCDMA Specifications (tested in the Doherty test fixture)
V_{DD} = 48 V, I_{DQ} = 500 mA, $V_{GS(PEAK)}$ = 2 V, P_{OUT} = 87 W avg, f = 820 MHz
3GPP signal, channel bandwidth = 3.84 MHz, peak/average = 10 dB @ 0.01% CCDF

Characteristic	Symbol	Min	Typ	Max	Unit
Gain	G_{ps}	18.2	19	—	dB
Drain Efficiency	η_D	46	50	—	%
Adjacent Channel Power Ratio	ACPR	—	–36	–30	dBc
Output PAR @ 0.01% CCDF	OPAR	7	7.4	—	dB

All published data at T_{CASE} = 25°C unless otherwise indicated

ESD: Electrostatic discharge sensitive device—observe handling precautions!

RoHS compliant

Rev. 03, 2023-07-07

DC Characteristics

Characteristics		Conditions	Symbol	Min	Typ	Max	Unit
Drain-source Breakdown Voltage		V_{GS} = 0 V, I_{DS} = 10 mA	$V_{(BR)DSS}$	105	—	—	V
Drain Leakage Current		V_{DS} = 48 V, V_{GS} = 0 V	I_{DSS}	—	—	1	µA
		V_{DS} = 105 V, V_{GS} = 0 V		—	—	10	µA
Gate Leakage Current		V_{GS} = 10 V, V_{DS} = 0 V	I_{GSS}	—	—	1	µA
On-State Resistance	(main)	V_{GS} = 10 V, V_{DS} = 0.1 V	$R_{DS(on)}$	0.025	0.08	0.41	Ω
	(peak)	V_{GS} = 10 V, V_{DS} = 0.1 V	$R_{DS(on)}$	0.01	0.05	0.38	Ω
Operating Gate Voltage	(main)	V_{DS} = 48 V, I_{DQ} = 500 mA	V_{GS}	3.4	3.7	4	V
	(peak)	V_{DS} = 48 V, I_{DQ} = 500 mA	V_{GS}	—	2	—	V

Maximum Ratings

Parameter	Symbol	Value	Unit
Drain-source Voltage	V_{DSS}	105	V
Gate-source Voltage	V_{GS}	–6 to +12	V
Operating Voltage	V_{DD}	0 to +55	V
Junction Temperature	T_J	225	°C
Storage Temperature Range	T_{STG}	–65 to +150	°C

1. Operation above the maximum values listed here may cause permanent damage. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the component. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. For reliable continuous operation, the device should be operated within the operating voltage range (V_{DD}) specified above.
2. Parameters values can be affected by end application and product usage. Values may change over time.

Thermal Characteristics

Thermal resistance, junction to case (T_{CASE} = 70°C, f = 790 MHz)

Characteristics			Symbol	Value	Unit
Thermal Resistance	(main)	P_{DISS} = 56 W CW , 48 V, I_{DQ} = 500 mA	$R_{\theta JC}$	0.52	°C/W
	(peak)	P_{DISS} = 215 W CW , 48 V, V_{GS} = 2.0 V	$R_{\theta JC}$	0.23	°C/W

Moisture Sensitivity Level

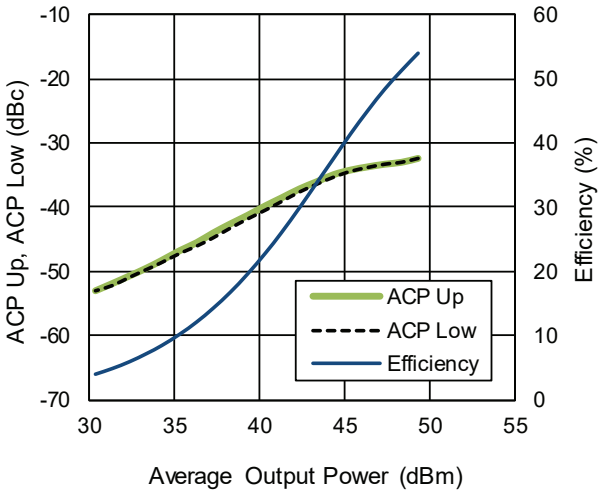
Level	Test Standard	Package Temperature	Unit
3	IPC/JEDEC J-STD-020	260	°C

Ordering Information

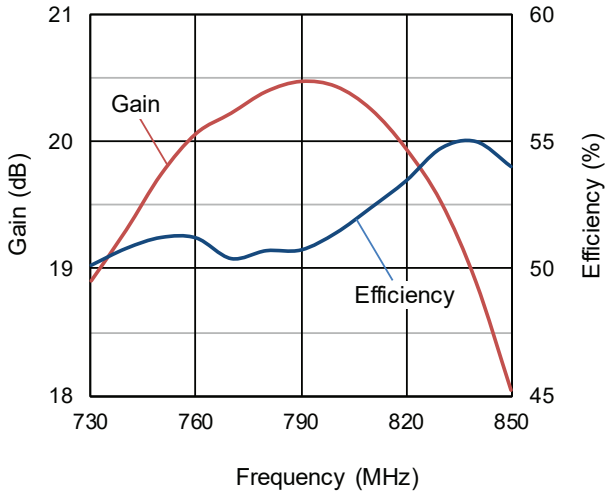
Type and Version	Order Code	Package	Shipping
PTRA084858NF V1 R5	PTRA084858NF-V1-R5	PG-HBSOF-6-3	Tape & Reel, 500 pcs

Typical Performance (data taken in the production test fixture)

Single-carrier WCDMA Drive-up
V_{DD} = 48 V, $I_{DQ(MAIN)}$ = 500 mA,
$V_{GS(PEAK)}$ = 2 V, f = 820 MHz
3GPP WCDMA signal,
10 dB PAR, 3.84 MHz bankdwidth



Single-carrier WCDMA Broadband Performance
V_{DD} = 48 V, I_{DQ} = 500 mA, $V_{GS(PEAK)}$ = 2.0 V
P_{OUT} = 49.4 dBm,
3GPP WCDMA signal, 10 dB PAR



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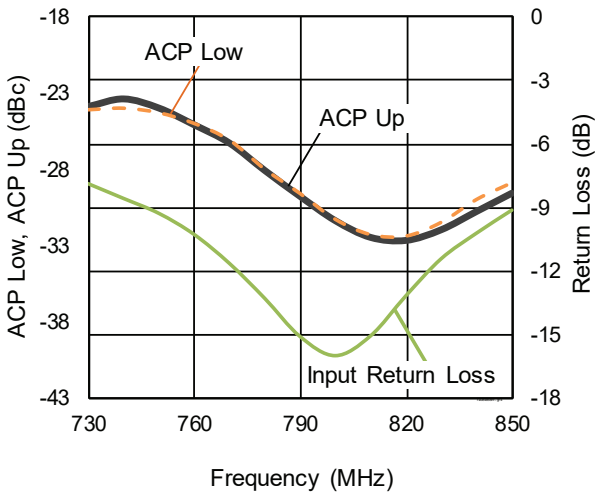
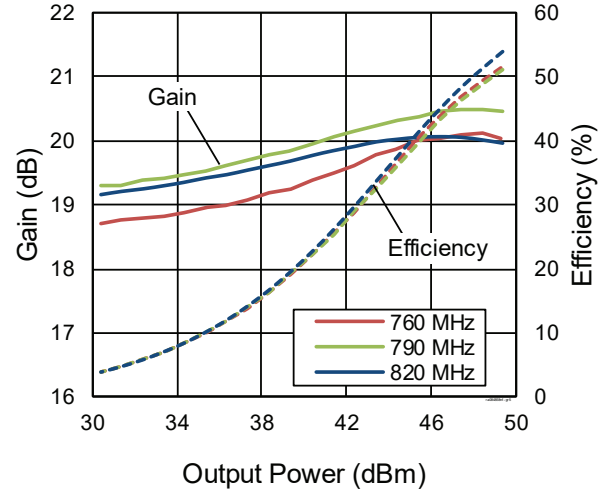
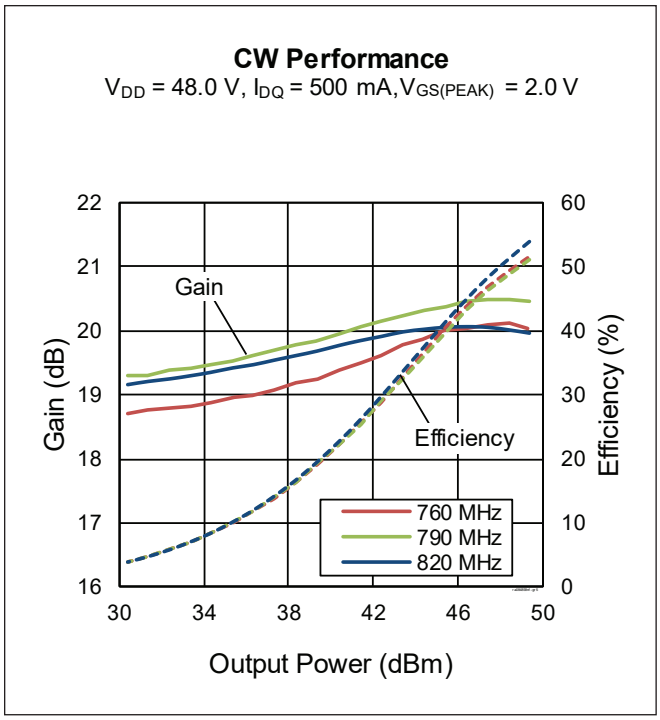
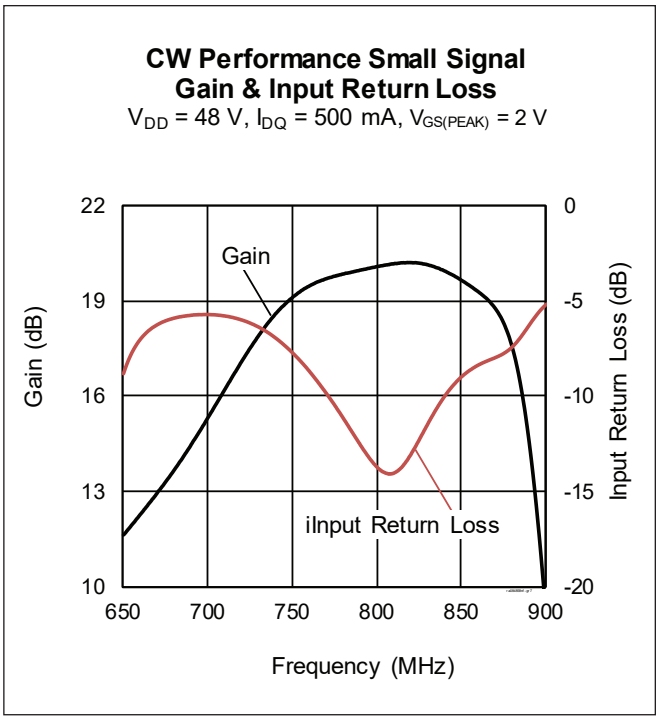


CW Performance
V_{DD} = 48.0 V, I_{DQ} = 500 mA, $V_{GS(PEAK)}$ = 2.0 V



Typical Performance (cont.)





Load Pull

Main side pulsed CW signal: 12 µsec, 10% duty cycle; 48 V, I_{DQ} = 400 mA, class AB

		P_{1dB}									
		Max Output Power					Max Drain Efficiency				
Freq [MHz]	Zs [Ω]	Zl [Ω]	Gain [dB]	P_{OUT} [dBm]	P_{OUT} [W]	η_D [%]	Zl [Ω]	Gain [dB]	P_{OUT} [dBm]	P_{OUT} [W]	η_D [%]
760	1.5 – j1.0	2.7 – j0.6	22.2	53.30	214	56.3	5.1 + j0.9	23.8	52.10	162	67.3
790	1.4 – j1.9	2.6 – j0.4	22.1	53.30	214	57.0	4.8 + j1.3	23.8	52.00	158	67.2
820	1.4 – j2.6	2.5 – j0.4	21.8	53.20	209	56.3	4.5 + j1.5	23.6	51.90	155	66.9

		P_{3dB}									
		Max Output Power					Max Drain Efficiency				
Freq [MHz]	Zs [Ω]	Zl [Ω]	Gain [dB]	P_{OUT} [dBm]	P_{OUT} [W]	η_D [%]	Zl [Ω]	Gain [dB]	P_{OUT} [dBm]	P_{OUT} [W]	η_D [%]
760	1.5 – j1.0	2.7 – j0.8	20.3	54.10	257	58.9	5.4 + j1.3	21.9	52.50	178	68.5
790	1.4 – j1.9	2.6 – j0.7	20.1	54.10	257	59.2	4.8 + j1.9	21.8	52.30	170	68.6
820	1.4 – j2.6	2.6 – j0.7	19.9	54.00	251	59.2	4.5 + j1.7	21.6	52.40	174	68.3

See next page for peak side load pull

Load Pull

Peak side pulsed CW signal: 12 µsec, 10% duty cycle; 48 V, $V_{GS(PEAK)}$ = 2 V, class C

		P_{1dB}									
		Max Output Power					Max Drain Efficiency				
Freq [MHz]	Zs [Ω]	Zl [Ω]	Gain [dB]	P_{OUT} [dBm]	P_{OUT} [W]	η_D [%]	Zl [Ω]	Gain [dB]	P_{OUT} [dBm]	P_{OUT} [W]	η_D [%]
760	0.7 – j1.8	1.1 + j0.1	17.7	56.50	447	61.5	1.1 + j1.3	18.6	53.90	245	75.2
790	0.7 – j2.2	1.1 + j0.1	17.3	56.50	447	61.2	1.1 + j1.3	18.2	54.00	251	74.5
820	0.8 – j2.5	1.0 + j0.2	17.5	56.70	468	64.8	1.0 + j1.3	18.3	54.30	269	77.3

		P_{3dB}									
		Max Output Power					Max Drain Efficiency				
Freq [MHz]	Zs [Ω]	Zl [Ω]	Gain [dB]	P_{OUT} [dBm]	P_{OUT} [W]	η_D [%]	Zl [Ω]	Gain [dB]	P_{OUT} [dBm]	P_{OUT} [W]	η_D [%]
760	0.7 – j1.8	1.1 + j0.0	15.6	57.20	525	62.7	1.1 + j1.3	16.6	54.60	288	74.5
790	0.7 – j2.2	1.1 + j0.0	15.2	57.20	525	62.4	1.1 + j1.3	16.3	54.80	302	74.7
820	0.8 – j2.5	1.1 + j0.2	15.4	57.30	537	65.4	1.0 + j1.3	16.3	54.80	302	77.0

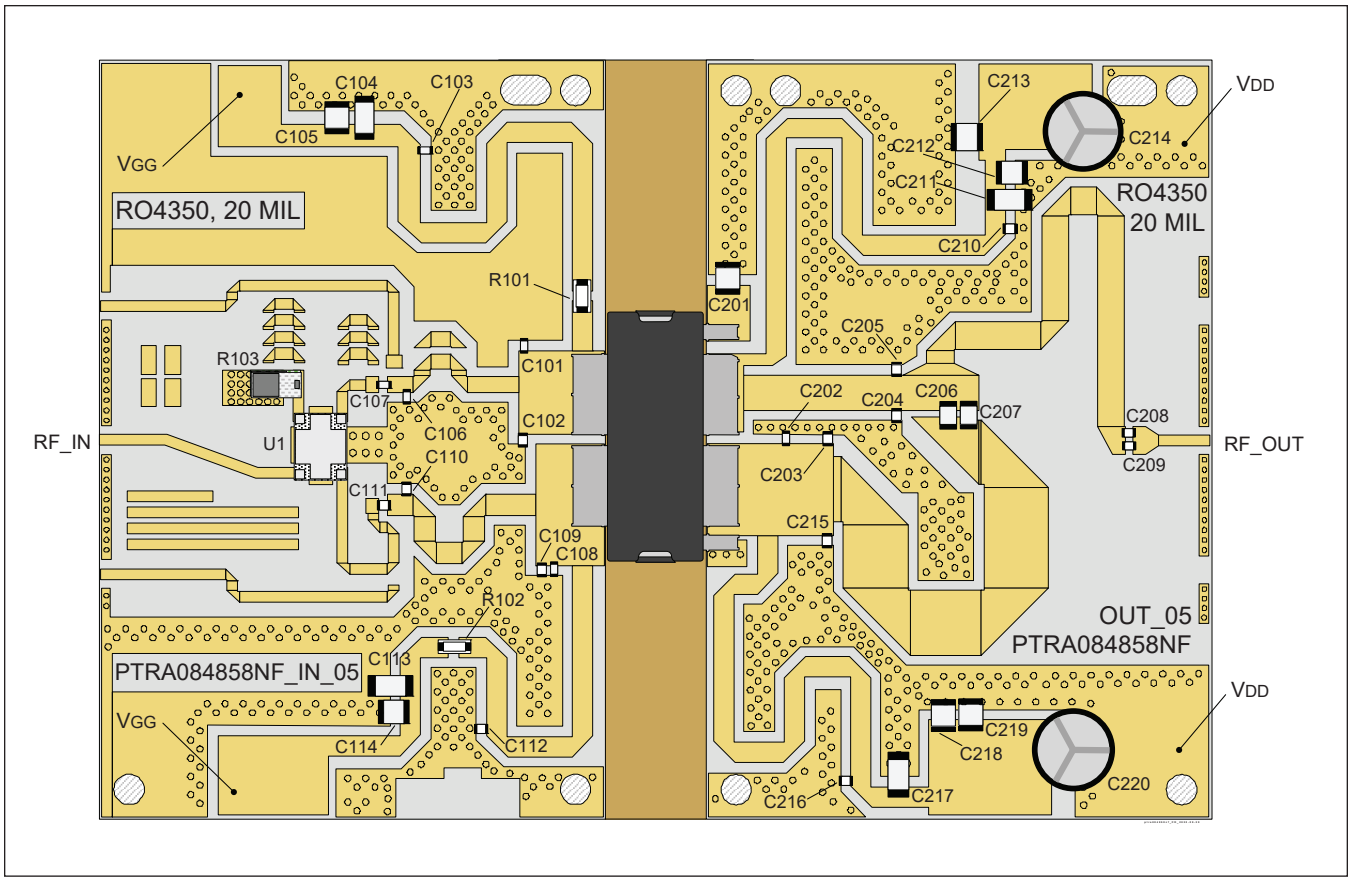
Reference Circuit, 760 – 820 MHz

Reference Circuit Assembly

DUT	PTRA084858NF
Test Fixture Part No.	LTA/PTRA084858NF-V1
PCB	Rogers 4350, 0.508 mm [0.020”] thick, 2 oz. copper, ε_r = 3.66

Reference Circuit continued next page

Reference Circuit, 760 – 820 MHz (cont.)



Reference circuit assembly diagram (not to scale)

Bias Sequencing

Bias ON

1. Ensure RF is turned off
2. Apply pinch-off voltage of 0 V to the gate
3. Apply nominal drain voltage
4. Bias gate to desired quiescent drain current
5. Apply RF

Bias OFF

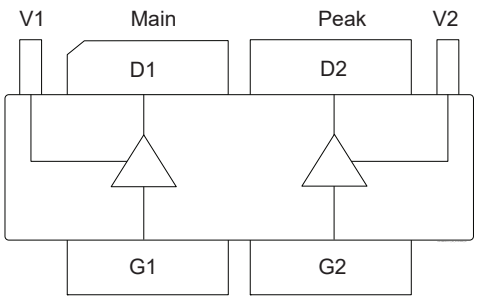
1. Turn RF off
2. Apply pinch-off voltage of 0 V to the gate
3. Turn off drain voltage
4. Turn off gate voltage

Reference Circuit, 760 – 820 MHz (cont.)

Components Table

Component	Description	Manufacturer	P/N
Input			
C101, C102	Capacitor, 18 pF	ATC	ATC600F180JT250XT
C103, C107, C111, C112	Capacitor, 100 pF	ATC	ATC600F101JT250XT
C104, C113	Capacitor, 1 µF	TDK Corporation	C4532X7R2A105M230KA
C105, C114	Capacitor, 10 µF, 100 V	Murata Electronics	GRM32EC72A106KE05L
C106	Capacitor, 10 pF	ATC	ATC600F100JT250XT
C108, C110	Capacitor, 5.6 pF	ATC	ATC600F5R6CT250XT
C109	Capacitor, 18 pF	ATC	ATC600F180JT250XT
R101	Resistor, 8.2 ohms	Panasonic Electronic Components	ERJ-8RQJ8R2V
R102	Resistor, 10 ohms	Panasonic Electronic Components	ERJ-8GEYJ100V
R103	Resistor, 50 ohms	Anaren	C16A50Z4
U1	Hybrid Coupler	RN2 Technolgies Co	CMX07Q01
Output			
C201, C212, C213, C218, C219	Capacitor, 10 µF, 100 V	Murata Electronics	GRM32EC72A106KE05L
C202	Capacitor, 18 pF	ATC	ATC600F180JT250XT
C203, C215	Capacitor, 12 pF	ATC	ATC600F120JT250XT
C204, C205	Capacitor, 6.8 pF	ATC	ATC600F6R8JT250XT
C206, C207	Capacitor, 47 pF	ATC	ATC100B470JW500XB
C208, C209, C210, C216	Capacitor, 100 pF	ATC	ATC600F101JT250XT
C211, C217	Capacitor, 1 µF	TDK Corporation	C4532X7R2A105M230KA
C214, C220	Capacitor, 100 µF	Panasonic Electronic Components	EEE-FP1V101A

Pinout Diagram (top view)



Pin	Description
D1	Drain Device 1 (Main)
D2	Drain Device 2 (Peak)
G1	Gate Device 1(Main)
G2	Gate Device 2 (Peak)
S	Source (flange)
V1, V2	Drain video decoupling, no DC Bias

Package Outline Specifications

Package PG-HBSOF-6-3

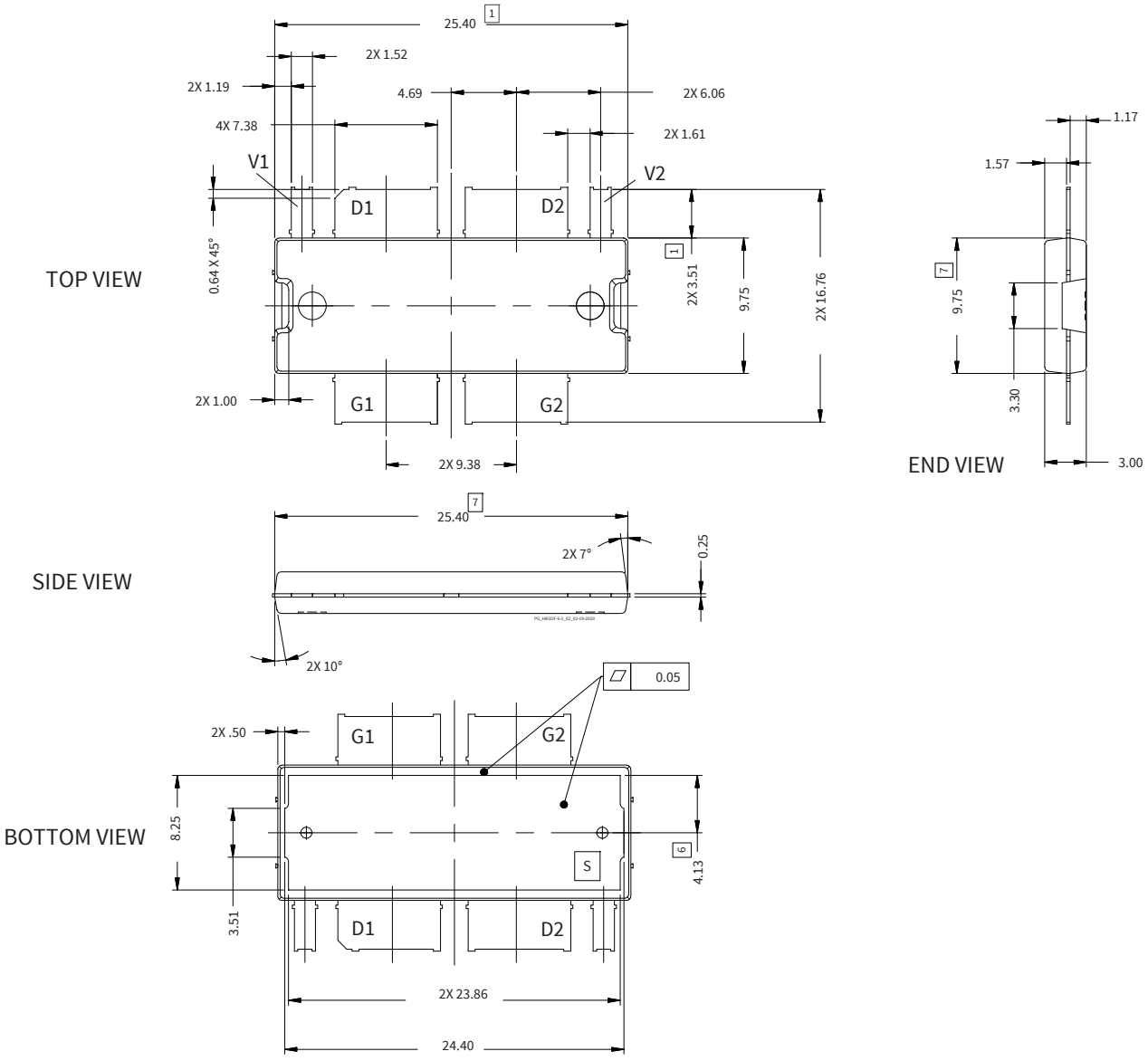


Diagram Notes–unless otherwise specified:

1. Mold/dam bar/metal protusion of 0.30 mm max per side not included.
2. Metal protrusion are connected to source and shall not exceed 0.10 mm max.
3. Fillets and radii: all radii are 0.3 mm max.
4. Interpret dimensions and tolerances per ISO 8015.
5. Dimensions are mm.
6. Exposed metal surface is tin-plated, may not be covered by mold compound.
7. Does not include mold/dam bar/metal protusion.
8. All tolerances ± 0.1 mm unless specified otherwise.
9. All metal surfaces pre-plated, except area of cut.
10. Lead thickness: 0.25 mm.
11. Pins: D1, D2 = drain; G1, G2 = gate; S = source; V1, V2 = drain video decoupling, not for DC bias.

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