System Lens Driver Series for Mobile Phone Cameras

# 2 wire serial interface Lens Driver for Voice Coil Motor ($I^2C$ BUS compatible)

**BH6455GUL**

No.12015EAT04

## ●General Description

The BH6455GUL motor driver provide 1 Constant -Current Driver 0.25ch bridge.
This lens driver is offered in an ultra-small functional lens system for use in an auto focus system using a Voice Coil motor.

## ●Features

- Ultra-small chip size package .
- Low ON-Resistance Power CMOS output.
- Built-in ±5% high-precision Constant-Voltage Driver (phase compensation capacitor-free design)
- Built-in UVLO (Under Voltage Locked Out: UVLO).
- Built-in TSD (Thermal Shut Down) circuit.
- Standby current consumption: 0μA Typ.
- 1.8V can be put into each control input terminal

## ●Applications

- Cell Phone
- Digital still camera
- Camera Modules
- Lens Auto focus
- Web Cameras

## ●Key Specifications

- ESD resistance (Human Body Model); 8000V
- Pch ON Resistance: 1.20Ω (Typ.)
- Nch ON Resistance: 0.40Ω (Typ.)
- Standby current consumption: 0μA (Typ.)
- Operating temperature range: -25℃ to +85℃

## ●Package(s)

| | W(Typ.) x D(Typ.) x H(Max.) |
|---|---|
| VCSP50L1 | 1.50mm x 1.00mm x 0.55mm |

## ●Typical Application Circuit

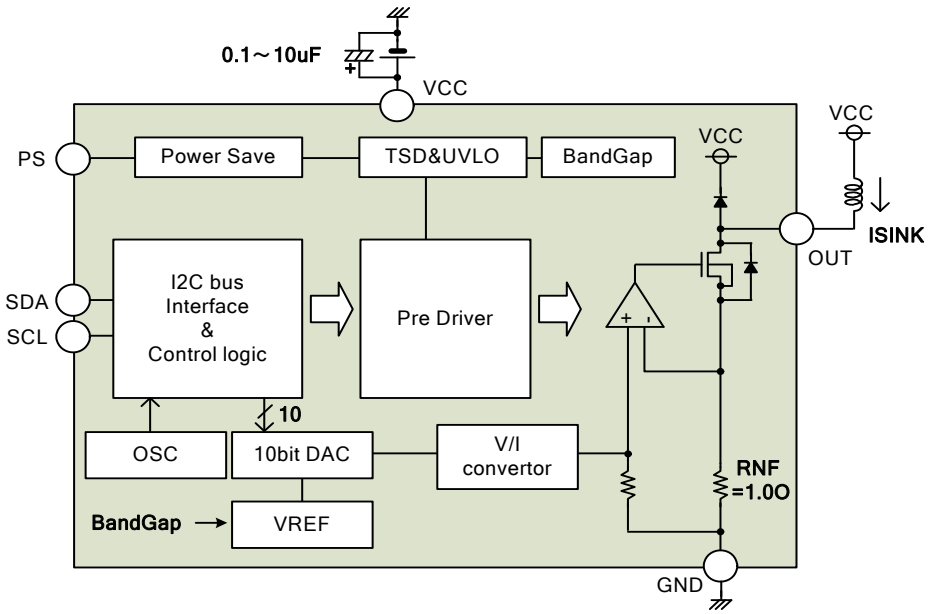



Fig.1 Block Diagram

○Product structure：Silicon monolithic integrated circuit ○This product is not designed protection against radioactive rays

## ●Absolute maximum ratings

| Parameter | Symbol | Limit | Unit |
|---|---|---|---|
| Power supply voltage | VCC | -0.5 to +5.5 | V |
| Output voltage[*1] | VOUT | -0.5 to +6.5 | V |
| Power save input voltage | VPS | -0.5～4.5 | V |
| Control input voltage[*2] | VIN | -0.5～4.5 | V |
| Power dissipation | Pd | 460[*3] | mW |
| Operating temperature range | Topr | -25 to +85 | °C |
| Junction temperature | Tjmax | 125 | °C |
| Storage temperature range | Tstg | -55 to +125 | °C |
| Output current | Iout | 200[*4] | mA |

[*1] VOUT is output pin (OUT).

[*2] VIN is I2C BUS input pin (SCL, SDA).

[*3] Reduced by 4.6 mW/°C over 25°C, when mounted on a glass epoxy board (50mm × 58mm × 1.75mm; 8 layers)

[*4] Must not exceed Pd, ASO, or Tjmax of 125°C.

## ●Operating Conditions (Ta= -25°C to +85°C)

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Power supply voltage | VCC | 2.3 | 3.0 | 4.8 | V |
| Power save input voltage | VPS | 0 | - | 3.6 | V |
| Control input voltage | VIN | 0 | - | 3.6 | V |
| I2C Bus Frequency | fCLK | - | - | 400 | kHz |
| Output current | Iout | - | - | 125[*5] | mA |

[*5] Must not exceed Pd, ASO.

## ●Package Outline

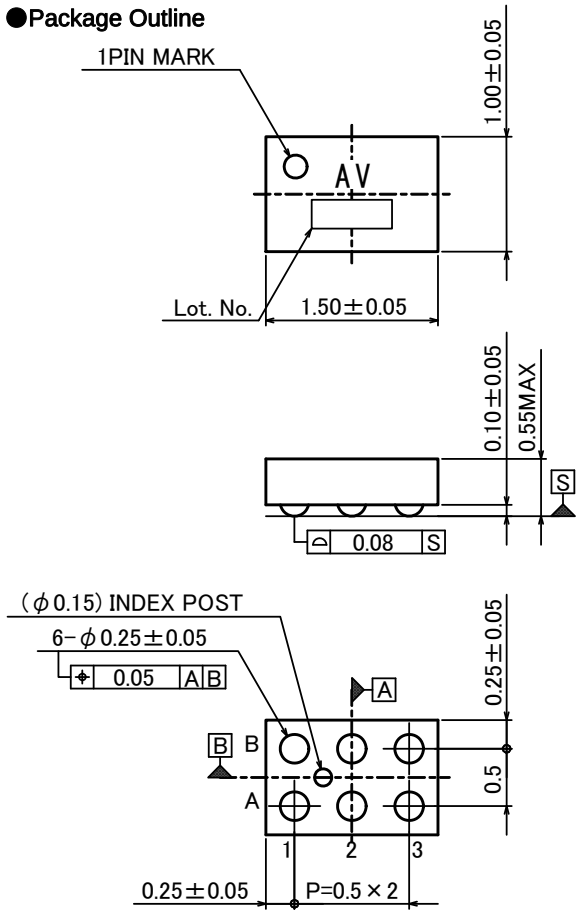



Fig.2 VCSP50L1 Package (Unit: mm)

## ●Pin Arrangement (Top View)

| | 1 | 2 | 3 |
|---|---|---|---|
| A | GND | VCC | PS |
| B | OUT | SDA | SCL |

Fig.3 Pin Arrangement (Top View)

● **Electrical Characteristics (Unless otherwise specified Ta=25°C, VCC=3.0V )**

| Parameter | Symbol | Limit | | | Unit | Conditions |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Overall | | | | | | |
| Circuit current during standby operation | ICCST | - | 0 | 5 | μA | PS=0V |
| Circuit current | ICC | - | 1.5 | 2.5 | mA | PS=3V, SCL=400kHz |
| Power save input | | | | | | |
| High level input voltage | VPSH | 1.5 | - | VPS | V | |
| Low level input voltage | VPSL | 0 | - | 0.5 | V | |
| High level input current | IPSH | 15 | 30 | 60 | μA | VPSH=3.0V, pull down resistance typ.100kΩ |
| Low level input current | IPSL | -1 | 0 | - | μA | VPSL=0V |
| Control input (SCL, SDA) | | | | | | |
| High level input voltage | VINH | 1.5 | - | VIN | V | |
| Low level input voltage | VINL | 0 | - | 0.5 | V | |
| Low level output voltage | VINOL | - | - | 0.4 | V | IIN=+3.0mA (SDA) |
| High level input current | IINH | -10 | - | 10 | μA | Input voltage=0.9×VIN |
| Low level input current | IINL | -10 | - | 10 | μA | Input voltage=0.1×VIN |
| OSC | | | | | | |
| Frequency | FOSC | 15 | 20 | 25 | kHz | |
| UVLO | | | | | | |
| UVLO voltage | VUVLO | 1.6 | - | 2.2 | V | |
| 10bit D/A converter(for setting limit voltage) | | | | | | |
| Resolution | DRES | - | 10 | - | Bits | Output current :125uA/LSB (reference) |
| Differential Nonlinearity | DDNL | -1 | - | 1 | LSB | DACcode = 0x07F to 0x3FF |
| Integral Nonlinearity | DINL | -4 | - | 4 | LSB | DACcode = 0x07F to 0x3FF |
| Constant-Current Driver block | | | | | | |
| Output current 1 | IO1 | 81 | 85 | 89 | mA | DACcode = 0x2C8 |
| Output current 2 | IO2 | 115 | 125 | 135 | mA | DACcode = 0x3FF |
| Zero code offset current | IOOFS | 0 | 1 | 5 | mA | DACcode = 0x000 |
| Output Voltage | VOUT | - | 150 | 200 | mV | Io = 100mA, RNF = 1Ω(typ) |
| Maximum applied voltage | VOMAX | - | - | VCC | V | |

## ●2 wire Serial Interface Register detail

**Write mode (R/W=0h)** Output from Master Output from Slave

| S | 0 | 0 | 0 | 1 | 1 | 0 | 0 | R/W | A | D17 | D16 | D15 | D14 | D13 | D12 | D11 | D10 | A | D27 | D26 | D25 | D24 | D23 | D22 | D21 | D20 | A | D37 | D36 | D35 | D34 | D33 | D32 | D31 | D30 | A | P |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| S | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | A | D17 | D16 | D15 | D14 | D13 | D12 | D11 | D10 | A | | | | | | | | | | | | | | | | | | |

**Read mode (R/W=1h)**

| S | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | A | D17 | D16 | D15 | D14 | D13 | D12 | D11 | D10 | A | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| S | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | A | D17 | D16 | D15 | D14 | D13 | D12 | D11 | D10 | A | D27 | D26 | D25 | D24 | D23 | D22 | D21 | D20 | A | D37 | D36 | D35 | D34 | D33 | D32 | D31 | D30 | nA | P |

S : start signal P : stop signal A : acknowledge nA : non acknowledge

## ●2 wire Serial Interface Action Timing Characteristics (Unless otherwise specified, $T_a$ = -25 to +85°C, VCC = 2.3 to 4.8V)

| Parameter | Symbol | FAST-MODE*6 | | | STANDARD-MODE*6 | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | Min. | Typ. | Max. | |
| SCL frequency | fSCL | - | - | 400 | - | - | 100 | kHz |
| Data clock high time | tHIGH | 0.6 | - | - | 4.0 | - | - | µs |
| Data clock low time | tLOW | 1.3 | - | - | 4.7 | - | - | µs |
| Start condition hold time | tHD:STA | 0.6 | - | - | 4.0 | - | - | µs |
| Start condition setup time | tSU:STA | 0.6 | - | - | 4.7 | - | - | µs |
| Data hold time | tHD:DAT | 0 | - | 0.9 | 0 | - | 3.45 | µs |
| Data setup time | tSU:DAT | 100 | - | - | 250 | - | - | ns |
| Stop condition setup time | tSU:STO | 0.6 | - | - | 4.0 | - | - | µs |
| BUS release time | tBUF | 1.3 | - | - | 4.7 | - | - | µs |
| Noise removal valid period | tI | 0 | - | 50 | 0 | - | 50 | ns |

*6 Standard-mode and Fast-mode 2-wire serial interface devices must be able to transmit or receive at that speed.
The maximum bit transfer rates of 100 kbit/s for Standard-mode devices and 400 kbit/s for Fast-mode devices
This transfer rates is provided the maximum transfer rates, for example it is able to drive 100 kbit/s of clocks with Fast-mode.

## ●2 wire Serial Interface Data timing

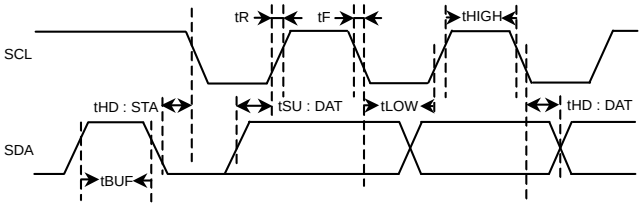



Fig.4 Serial data timing

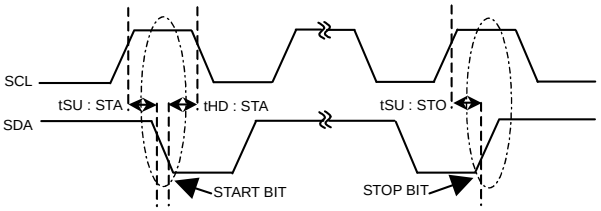



Fig.5 Start stop bit timing

| Register name | Setting item | Description |
|---|---|---|
| PS | Serial power save | '0' = Standby mode, '1' = Operating mode |
| EN | OUT pin status | '0' = Hi-impedance, '1' = Constant current sink. |
| M | Mode select signal | '0' = Direct mode, '1' = Step mode |
| W | Register address | '0' = DAC code setting, '1' = Step operation setting |
| F | Step operation flag | '0' = Finished, '1' = Running （Read only） |
| TD9～TD0 | Target position DAC | Target position DAC code. |
| CD9～CD0 | Current position DAC | Current position DAC code. (Read only) |
| R7～R0 | Step resolution | The width of step. (It is set by the unit of LSB of 10bit DAC.) |
| T7～T0 | Step time | The time interval of step. (It is set by the unit of 50µsec / LSB.) |
| - | Test bit | A low signal should be input to the Test bit at all times. |

●Register catalogue

Write mode (R/W=0)

| Bit | BIT Name | Function |
|---|---|---|
| D17 | PS | Serial power save |
| D16 | EN | OUT pin status |
| D15 | - | Don't care |
| D14 | - | Don't care |
| D13 | M | Mode select signal |
| D12 | W | Register address |

| W (Register address) : 0 | | |
|---|---|---|
| D11 | TD[9] | Target position DAC code setting[9] |
| D10 | TD[8] | Target position DAC code setting[8] |
| D27 | TD[7] | Target position DAC code setting[7] |
| D26 | TD[6] | Target position DAC code setting[6] |
| D25 | TD[5] | Target position DAC code setting[5] |
| D24 | TD[4] | Target position DAC code setting[4] |
| D23 | TD[3] | Target position DAC code setting[3] |
| D22 | TD[2] | Target position DAC code setting[2] |
| D21 | TD[1] | Target position DAC code setting[1] |
| D20 | TD[0] | Target position DAC code setting[0] |
| D37 | - | Don't care |
| D36 | - | Don't care |
| D35 | - | Don't care |
| D34 | - | Don't care |
| D33 | - | Don't care |
| D32 | - | Don't care |
| D31 | - | Don't care |
| D30 | - | Don't care |

| W (Register address) : 1 | | |
|---|---|---|
| D11 | - | Don't care |
| D10 | - | Don't care |
| D27 | R[7] | Step resolution setting[7] |
| D26 | R[6] | Step resolution setting[6] |
| D25 | R[5] | Step resolution setting[5] |
| D24 | R[4] | Step resolution setting[4] |
| D23 | R[3] | Step resolution setting[3] |
| D22 | R[2] | Step resolution setting[2] |
| D21 | R[1] | Step resolution setting[1] |
| D20 | R[0] | Step resolution setting[0] |
| D37 | T[7] | Step time setting[7] |
| D36 | T[6] | Step time setting[6] |
| D35 | T[5] | Step time setting[5] |
| D34 | T[4] | Step time setting[4] |
| D33 | T[3] | Step time setting[3] |
| D32 | T[2] | Step time setting[2] |
| D31 | T[1] | Step time setting[1] |
| D30 | T[0] | Step time setting[0] |

Read mode (R/W=1)

| Bit | BIT Name | Function |
|---|---|---|
| D17 | PS | Serial power save |
| D16 | EN | OUT pin status |
| D15 | - | Don't care |
| D14 | F | Step operation flag |
| D13 | M | Mode select signal |
| D12 | W | Register address |

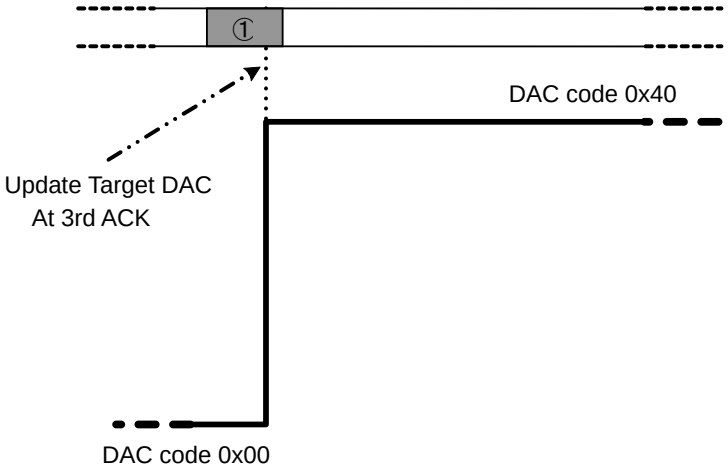
| W (Register address) : 0 | | |
|---|---|---|
| D11 | CD[9] | Current position DAC code |
| D10 | CD[8] | Current position DAC code |
| D27 | CD[7] | Current position DAC code |
| D26 | CD[6] | Current position DAC code |
| D25 | CD[5] | Current position DAC code |
| D24 | CD[4] | Current position DAC code |
| D23 | CD[3] | Current position DAC code |
| D22 | CD[2] | Current position DAC code |
| D21 | CD[1] | Current position DAC code |
| D20 | CD[0] | Current position DAC code |
| D37 | - | Don't care |
| D36 | - | Don't care |
| D35 | - | Don't care |
| D34 | - | Don't care |
| D33 | - | Don't care |
| D32 | - | Don't care |
| D31 | - | Don't care |
| D30 | - | Don't care |

| W (Register address) : 1 | | |
|---|---|---|
| D11 | - | Don't care |
| D10 | - | Don't care |
| D27 | R[7] | Step resolution[7] |
| D26 | R[6] | Step resolution[6] |
| D25 | R[5] | Step resolution[5] |
| D24 | R[4] | Step resolution[4] |
| D23 | R[3] | Step resolution[3] |
| D22 | R[2] | Step resolution[2] |
| D21 | R[1] | Step resolution[1] |
| D20 | R[0] | Step resolution[0] |
| D37 | T[7] | Step time[7] |
| D36 | T[6] | Step time[6] |
| D35 | T[5] | Step time[5] |
| D34 | T[4] | Step time[4] |
| D33 | T[3] | Step time[3] |
| D32 | T[2] | Step time[2] |
| D31 | T[1] | Step time[1] |
| D30 | T[0] | Step time[0] |

## ●Direct mode operation

During the Direct mode operation, setting of 10bit DAC_code will come effect to the Target position DAC at 3rd_ACK in the set 2 wire Serial communication, and the actuator will move.

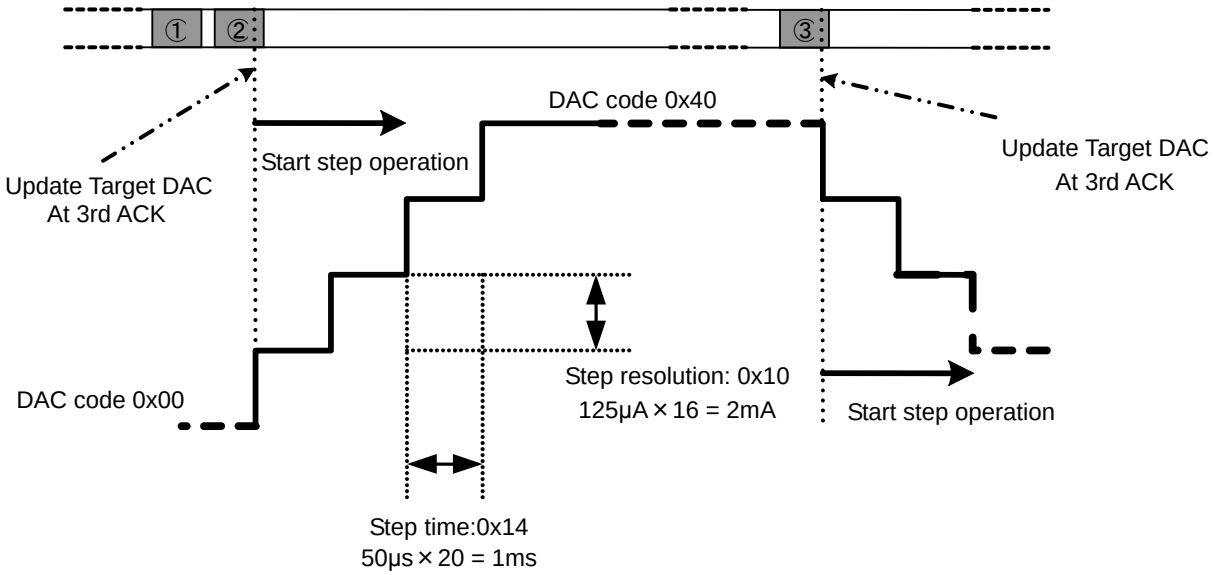
○ 2 wire Serial input serial data
① : 00011000_11xx0000_01000000_xxxxxxxx (DAC code setting)




## ●Step mode operation

When Target DAC and step mode are still at initial condition then you can use any operation.
Once you set the Target DAC, BH6455GUL will automatically start the step mode operation.
Therefore it is recommended to sell the step mode before changing the target DAC or the BH6455GUL will use the initial step mode condition

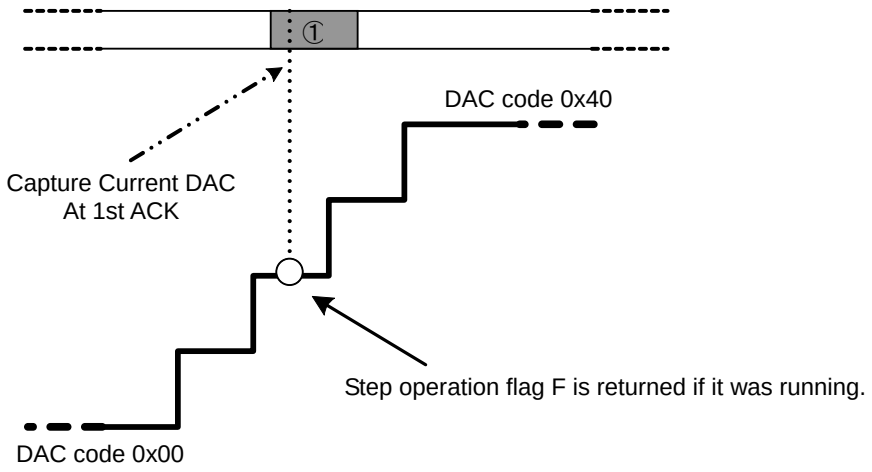
○ 2 wire Serial input serial data
① : 00011000_11xx11xx_00010000_00010100 (Step mode setting)
② : 00011000_11xx1000_01000000_xxxxxxxx (DAC code setting)
③ : 00011000_11xx1000_00000000_xxxxxxxx (DAC code setting)



## ●Interrupt read or write

In the case, if you read when it is running in step mode, it reply Current DAC code when it captures at 1st ACK, and step operation flag.

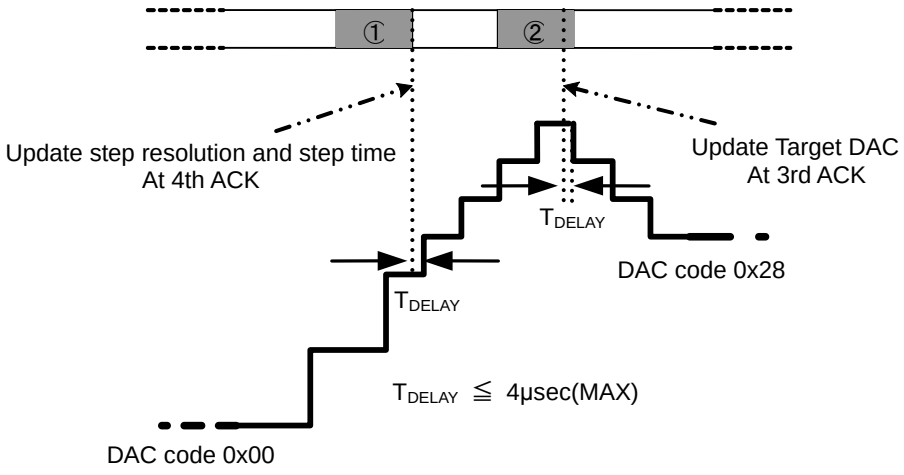
○ Read DAC code
when w = 0 initially
① : 00011001_11x11000_00100000_xxxxxxxx




○Write Step resolution, Step time and Target DAC code

If you write Target DAC when it is running instep mode, it just change Target DAC.
If you write Step mode setting when it is running in step mode, it reset step counter and restart step operation in the latest step mode settings.

① : 00011000_11xx11xx_00001000_00001010 (Step resolution 0x10 to 0x08 and step time 0x14 to 0x0A.)
② : 00011000_11xx1000_00101000_xxxxxxxx (Change target code 0x40 to 0x28.)



## ●I/O Peripheral Circuit

1) Pull up resistance of SDA terminal

SDA is NMOS open drain, so requires pull up resistance. As for this resistance value ($R_{PU}$), select an appropriate value to this resistance value from micro-controller $V_{IL}$, $I_L$, and $V_{OL}$ – $I_{OL}$ characteristics of this IC. If $R_{PU}$ is large, action frequency is limited. The smaller the $R_{PU}$, the larger the consumption current at action.

2) Maximum value of $R_{PU}$

The maximum value of $R_{PU}$ is determined by the following factors.

（Ⅰ）SDA rise time to be determined by the capacity (CBUS) of BUS line of $R_{PU}$ and SDA should be tR or below. And AC timing should be satisfied even when SDA rise time is late.

（Ⅱ）The BUS electric potential $V_1$ to be determined by input leak total (IL) of device connected to BUS at output of “H” to SDA BUS and RPU should sufficiently secure the input “H” level (VIH) of micro-controller and driver including recommended noise margin 0.2VCC.

$$VCC - I_L \times R_{PU} - 0.2 \times VCC \geqq V_{IH}$$

$$\therefore R_{PU} \leqq \frac{0.8 \times VCC - V_{IH}}{I_L} \quad \cdots\cdots ①$$

Example.) VCC = 3V, $I_L$=10μA, $V_{IH} = 0.7 \times VCC$

from ①

$$R_{PU} \leqq \frac{0.8 \times 3 - 0.7 \times 3}{10 \times 10^{-6}} = 30k\Omega$$

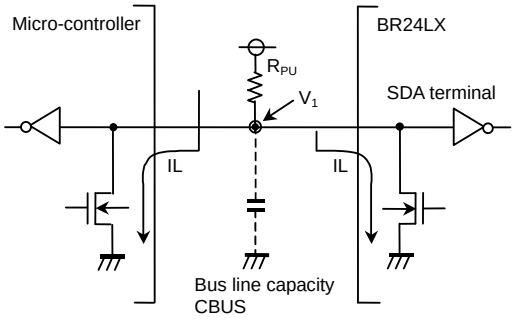



Fig.6 2 wire Serial Interface 1

3) Minimum value of $R_{PU}$

The minimum value of $R_{PU}$ is determined by the following factors.

（Ⅰ）When IC outputs LOW, it should be satisfied that $V_{OLMAX}$ = 0.4V, and $I_{OLMAX}$ = 3mA.

$$\frac{VCC - V_{OL}}{R_{PU}} \leqq I_{OL} \quad \cdots\cdots ②$$

（Ⅱ）$V_{OLMAX}$ = 0.4V should secure the input “L” level (VIL) of micro-controller and driver including recommended noise margin 0.1VCC.

$$V_{OLMAX} \leqq VIL - 0.1 \times VCC$$

Ex.) VCC = 3V, $V_{OL}$=0.4V, $I_{OL}$ = 3mA, micro-controller, driver $V_{IL} = 0.3 \times VCC$

$$R_{PU} \geqq \frac{3 - 0.4}{3 \times 10^{-3}} = 867[\Omega]$$

And $V_{OL}$ = 0.4[V], $V_{IL} = 0.3 \times 3 = 0.9$[V]

Therefore, the condition (Ⅱ) is satisfied.

4) Pull up resistance of SCL terminal

WHEN SCL control is made at CMOS output port, there is no need but in the case there is timing where SCL becomes “Hi-Z”, add a pull up resistance. As for the pull up resistance, one of several kΩ to several ten kΩ is recommended in consideration of drive performance of output port of micro-controller.

## ●Cautions on Micro-controller Connection

1) $R_s$

In the 2 wire Serial Interface, it is recommended that SDA port is of open drain input/output. However, when to use CMOS input / output of tri state to SDA port, inset a series resistance $R_s$ between the pull up resistance $R_{pu}$ and the SDA terminal of driver. This controls over current that occurs when PMOS of the micro-controller and NMOS of driver are turned ON simultaneously. $R_s$ also plays the role of protection of SDA terminal against surge. Therefore, even when SDA port is open drain input/output, $R_s$ can be used.

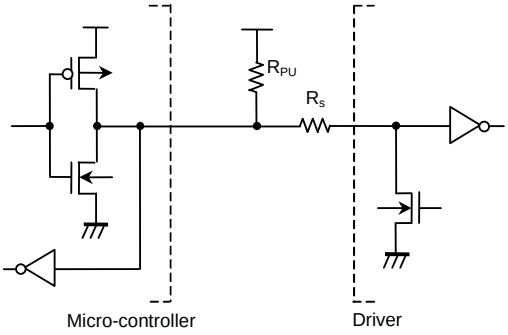
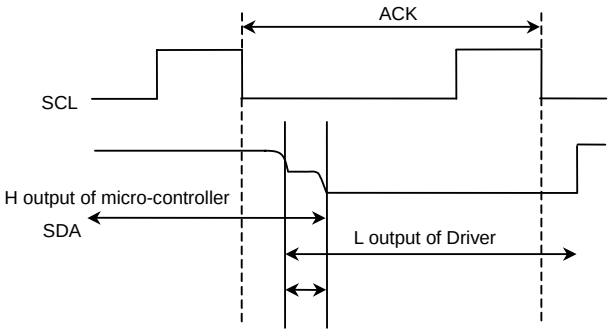



Fig.7 2 wire Serial Interface 2




Over current flows to SDA line by H output of micro-controller and L output of Driver

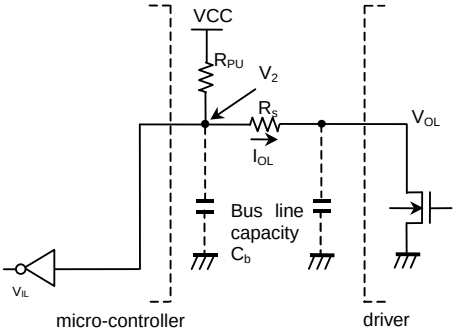
Fig.8 Input / Output collision timing

2) Maximum value of $R_s$

The maximum value of $R_s$ is determined by the following relations.

（Ⅰ）SDA rise time to be determined by the capacity ($C_b$) of BUS line of $R_{pu}$ and SDA should be tR or below. And AC timing should be satisfied even when SDA rise time is late.

（Ⅱ）The BUS electric potential $V_2$ to be determined by $R_{pu}$ and $R_s$ at the moment when driver outputs “L” to SDA BUS should sufficiently secure the input “L” level ($V_{IL}$) of micro-controller including recommended noise margin 0.1VCC.




$$\frac{(VCC-V_{OL})\times R_s}{R_{PU}+R_s} + V_{OL} + 0.1\times VCC \leqq V_{IL}$$

$$\therefore R_s \leqq \frac{V_{IL}-V_{OL}-0.1\times VCC}{1.1\times VCC-V_{IL}} \times R_{PU} \quad \cdots\cdot ③$$

Example) When VCC = 3V, $V_{IL} = 0.3\times VCC$, $V_{OL} = 0.4V$, $R_{PU} = 20k\Omega$, from ③

Fig.9 2 wire Serial Interface 3

$$R_s \leqq \frac{0.3\times 3 - 0.4 - 0.1\times 3}{1.1\times 3 - 0.3\times 3} \times 20\times 10^3 = 1.67[k\Omega]$$

3) Minimum value of $R_S$

The minimum value of $R_s$ is determined by over current at BUS collision. When over current flows, noises in power source line, and instantaneous power failure of power source may occur. When allowable over current is defined as I, the following relation must be satisfied. Determine the allowable current in consideration of impedance of power source line in set and so forth. Set the over current to driver 10mA or below.

$$\frac{VCC}{R_s} \leqq I \quad \cdots\cdot ④$$

Exampre) When VCC=3V, I=10mA, From ④

$$R_s \geqq \frac{3}{10\times 10^{-3}} = 300[\Omega]$$

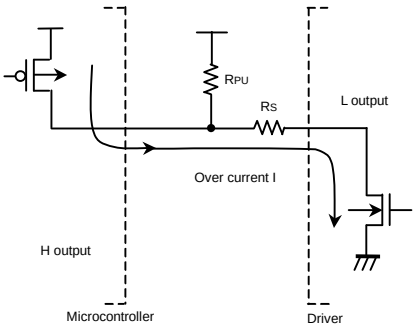



Fig.10 2 wire Serial Interface 4

## ●Operation Notes

1) Absolute maximum ratings

Use of the IC in excess of absolute maximum ratings, such as the applied voltage (VCC) or operating temperature range (Topr), may result in IC damage. Assumptions should not be made regarding the state of the IC (short mode or open mode) when such damage is suffered. A physical safety measure, such as a fuse, should be implemented when using the IC at times where the absolute maximum ratings may be exceeded.

2) Storage temperature range (Tstq)

As long as the IC is kept within this range, there should be no problems in the IC's performance. Conversely, extreme temperature changes may result in poor IC performance, even if the changes are within the above range.

3) Power supply and wiring

Be sure to connect the power terminals outside the IC. Do not leave them open. Because a return current is generated by a counter electromotive force of the motor, take necessary measures such as putting a Capacitor between the power source and the ground as a passageway for the regenerative current. Be sure to connect a Capacitor of proper capacitance (0.1μF to 10μF) between the power source and the ground at the foot of the IC, and ensure that there is no problem in properties of electrolytic Capacitors such as decrease in capacitance at low temperatures. When the connected power source does not have enough current absorbing capability, there is a possibility that the voltage of the power source line increases by the regenerative current an exceeds the absolute maximum rating of this product and the peripheral circuits.

Therefore, be sure to take physical safety measures such as putting a zener diode for a voltage clamp between the power source an the ground.

4) Ground terminal and wiring

The potential at GND terminals should be made the lowest under any operating conditions. Ensure that there are no terminals where the potentials are below the potential at GND terminals, including the transient phenomena. The motor ground terminals RNF and PGND, and the small signal ground terminal GND are not interconnected with one another inside the IC. It is recommended that you should isolate the large-current RNF pattern and PGND pattern from the small-signal GND pattern, and should establish a one-point grounding at a reference point of the set, to avoid fluctuation of small-signal G voltages caused by voltage changes due to pattern wire resistances and large currents. Also prevent the voltage variation of the ground wiring patterns of external components. Use short and thick power source and ground wirings to ensure low impedance.

5) Thermal design

Use a proper thermal design that allows for a sufficient margin of the power dissipation (Pd) at actual operating conditions.

6) Pin short and wrong direction assembly of the device

Use caution when positioning the IC for mounting on printed circuit boards. The IC may be damaged if there is any connection error or if positive and ground power supply terminals are reversed. The IC may also be damaged if pins are shorted together or are shorted to other circuit's power lines.

7) Avoiding strong magnetic field

Malfunction may occur if the IC is used around a strong magnetic field.

8) ASO

Ensure that the output transistors of the motor driver are not driven under excess conditions of the absolute maximum ratings and ASO.

9) TSD (Thermal Shut Down) circuit

If the junction temperature (Tjmax) reaches 150°C, the TSD circuit will operate, and the coil output circuit of the motor will open. There is a temperature hysterics of approximately 25°C. The TSD circuit is designed only to shut off the IC in order to prevent runaway thermal operating. It is not designed to protect the IC or guarantee its operation. The performance of the IC's characteristics is not guaranteed and it is recommended that the device is replaced after the TSD is activated.

10) Regarding the input pin of the IC

This monolithic IC contains $P^+$ isolation and P substrate layers between adjacent elements to keep them isolated. P-N junctions are formed at the intersection of these P layers with the N layers of other elements, creating a parasitic diode or transistor. For example, the relation between each potential is as follows:

When GND > Pin A, the P-N junction operates as a parasitic diode.

When GND > Pin B, the P-N junction operates as a parasitic diode and transistor.

Parasitic elements can occur inevitably in the structure of the IC. The operation of parasitic elements can result in mutual interference among circuits, operational faults, or physical damage. Accordingly, methods by which parasitic elements operate, such as applying a voltage that is lower than the GND (P substrate) voltage to an input pin, should not be used.

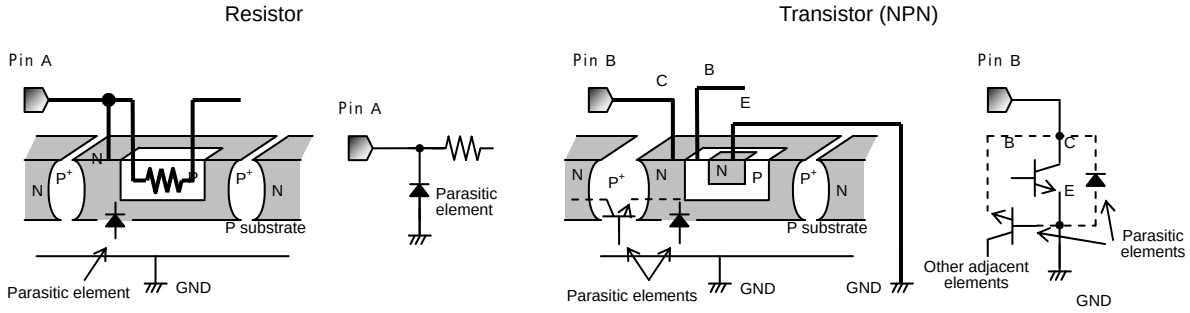



Fig.11 Example of Simple IC Architecture

## ●Ordering Information

| B H 6 4 5 5 G U L | E 2 |
|---|---|
| Part Number | Packaging and forming specification<br>E2: Embossed tape and reel |
| Package<br>VCSP50L1 | |

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(Note1) Medical Equipment Classification of the Specific Applications

| JAPAN | USA | EU | CHINA |
|---|---|---|---|
| CLASSⅢ | CLASSⅢ | CLASSⅡb | CLASSⅢ |
| CLASSⅣ | | CLASSⅢ | |

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   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

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   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including $Cl_2$, $H_2S$, $NH_3$, $SO_2$, and $NO_2$
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation (Pd) depending on Ambient temperature (Ta). When used in sealed area, confirm the actual ambient temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

## Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used; if flow soldering method is preferred, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

## Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

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## Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

## Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   - [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   - [b] the temperature or humidity exceeds those recommended by ROHM
   - [c] the Products are exposed to direct sunshine or condensation
   - [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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## Precaution for Disposition

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