# LDO Regulator - Ultra Low $I_q$

## 350 mA

# NCV8774C

The NCV8774C is a 350 mA LDO regulator. Its robustness allows NCV8774C to be used in severe automotive environments. Ultra low quiescent current as low as 17 μA typical makes it suitable for applications permanently connected to battery requiring ultra low quiescent current with or without load. This feature is especially critical when modules remain in active mode when ignition is off. The NCV8774C contains protection functions as current limit, thermal shutdown.

### Features

- Output Voltage Options: 3.3 V and 5 V
- Output Voltage Accuracy: ±2%
- Output Current up to 350 mA
- Ultra Low Quiescent Current: typ 17 μA
- Wide Input Voltage Operation Range: up to 40 V
- Protection Features
  - Current Limitation
  - Thermal Shutdown
- EMC Compliant
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Grade 1 Qualified and PPAP Capable
- These are Pb-Free Devices

### Typical Applications (For safety applications refer to Figure 29)

- Body Control Module
- Instruments and Clusters
- Occupant Protection and Comfort
- Powertrain

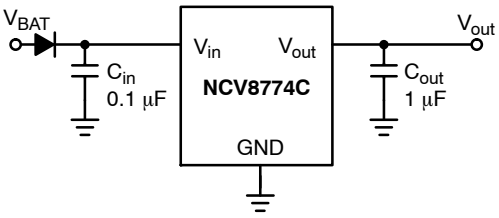
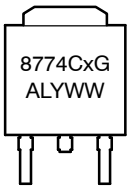



**Figure 1. Typical Application Schematic**



**DPAK-3**
**DT SUFFIX**
**CASE 369C**

**MARKING DIAGRAM**




| | |
|---|---|
| x | = Voltage Option |
| A | = Assembly Location |
| WL, L | = Wafer Lot |
| Y | = Year |
| WW | = Work Week |
| G | = Pb-Free Package |

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 12 of this data sheet.

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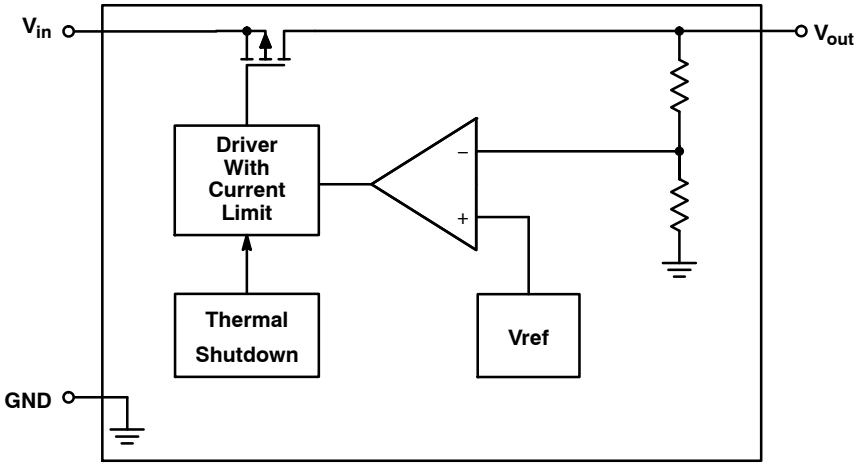
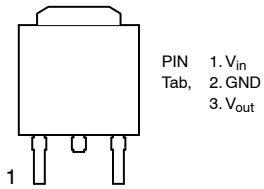



**Figure 2. Simplified Block Diagram**

## PIN CONNECTIONS




DPAK-3

**Figure 3. Pin Connections**

### PIN FUNCTION DESCRIPTION

| Pin No. | Pin Name | Description |
|---|---|---|
| 1 | $V_{in}$ | Positive Power Supply Input. Connect 0.1 μF capacitor to ground. |
| 2, TAB | GND | Power Supply Ground. |
| 3 | $V_{out}$ | Regulated Output Voltage. Connect 1 μF capacitor with ESR < 5 Ω to ground. |



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## ABSOLUTE MAXIMUM RATINGS

| Rating | | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|
| Input Voltage (Note 1) | DC | $V_{in}$ | −0.3 | 40 | V |
| Input Voltage (Note 2) | Load Dump − Suppressed | $U_S$* | − | 45 | V |
| Output Voltage | | $V_{out}$ | −0.3 | 7 | V |
| Junction Temperature | | $T_J$ | −40 | 150 | °C |
| Storage Temperature | | $T_{STG}$ | −55 | 150 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected. Operating the device outside its recommended conditions, but still within its maximum rated limits may not cause immediate damage. However, doing so can lead to reduced performance, unpredictable behavior, and potentially shorten the device's lifespan or reliability.

1. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
2. Load Dump Test B (with centralized load dump suppression) according to ISO16750-2 standard. Guaranteed by design. Not tested in production. Passed Class A according to ISO16750-1.

## ESD CAPABILITY (Note 3)

| Rating | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| ESD Capability, Human Body Model | $ESD_{HBM}$ | −4 | 4 | kV |
| ESD Capability, Charged Device Model | $ESD_{CDM}$ | −1 | 1 | kV |

3. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per AEC-Q100-002 (JS-001-2017)
   Field Induced Charge Device Model ESD characterization is not performed on plastic molded packages with body sizes smaller than 2 x 2 mm due to the inability of a small package body to acquire and retain enough charge to meet the minimum CDM discharge current waveform characteristic defined in JEDEC JS-002-2018

## LEAD SOLDERING TEMPERATURE AND MSL (Note 4)

| Rating | | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|
| Moisture Sensitivity Level | DPAK-3 | MSL | 1 | | − |

4. For more information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

## THERMAL CHARACTERISTICS

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Thermal Characteristics, DPAK-3 | | | °C/W |
| Thermal Resistance, Junction-to-Air (Note 5) | $R_{\theta JA}$ | 49 | |
| Thermal Reference, Junction-to-Case (Note 5) | $R_{\Psi JC}$ | 6.6 | |
| Thermal Resistance, Junction-to-Air (Note 6) | $R_{\theta JA}$ | 28 | |
| Thermal Reference, Junction-to-Case (Note 6) | $R_{\Psi JC}$ | 6.6 | |

5. Values based on 1s0p board with copper area of 645 $mm^2$ (or 1 $in^2$) of 1 oz copper thickness and FR4 PCB substrate. Single layer − according to JEDEC51.3.
6. Values based on 2s2p board with copper area of 645 $mm^2$ (or 1 $in^2$) of 1 oz copper thickness and FR4 PCB substrate. 4 layers − according to JEDEC51.7.

## RECOMMENDED OPERATING RANGE

| Rating | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Input Voltage (Note 7) | $V_{in}$ | 4.5 | 40 | V |
| Junction Temperature | $T_J$ | −40 | 150 | °C |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

7. Minimum $V_{in}$ = 4.5 V or ($V_{out}$ + $V_{DO}$), whichever is higher.



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**ELECTRICAL CHARACTERISTICS** $V_{in}$ = 13.5 V, $C_{in}$ = 0.1 μF, $C_{out}$ = 1 μF, Min and Max values are valid for temperature range −40 °C ≤ $T_J$ ≤ +150 °C unless noted otherwise and are guaranteed by test, design or statistical correlation. Typical values are referenced to $T_J$ = 25 °C. (Note 8)

| Parameter | Test Conditions | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **REGULATOR OUTPUT** | | | | | | |
| Output Voltage (Accuracy %) | | $V_{out}$ | | | | V |
| 3.3 V | $V_{in}$ = 4.5 V to 40 V, $I_{out}$ = 0.1 mA to 200 mA | | 3.234 | 3.3 | 3.366 | |
| | $V_{in}$ = 4.5 V to 16 V, $I_{out}$ = 0.1 mA to 350 mA | | 3.234 | 3.3 | 3.366 | |
| 5.0 V | $V_{in}$ = 5.45 V to 40 V, $I_{out}$ = 0.1 mA to 200 mA | | 4.9 | 5.0 | 5.1 | |
| | $V_{in}$ = 5.7 V to 16 V, $I_{out}$ = 0.1 mA to 350 mA | | 4.9 | 5.0 | 5.1 | |
| Output Voltage (Accuracy %) | | $V_{out}$ | | | | V |
| 3.3 V | $V_{in}$ = 4.5 V to 40 V, $I_{out}$ = 0 mA | | 3.234 | 3.3 | 3.366 | |
| 5.0 V | $V_{in}$ = 5.45 V to 40 V, $I_{out}$ = 0 mA | | 4.9 | 5.0 | 5.1 | |
| Line Regulation | | $Reg_{line}$ | −20 | 0 | 20 | mV |
| 3.3 V | $V_{in}$ = 4.5 V to 28 V, $I_{out}$ = 5 mA | | | | | |
| 5.0 V | $V_{in}$ = 6 V to 28 V, $I_{out}$ = 5 mA | | | | | |
| Load Regulation | $I_{out}$ = 0.1 mA to 350 mA | $Reg_{load}$ | −35 | 0 | 35 | mV |
| Dropout Voltage (Note 9) | | $V_{DO}$ | | | | mV |
| 5.0 V | $I_{out}$ = 200 mA | | – | 200 | 350 | |
| | $I_{out}$ = 350 mA | | – | 350 | 600 | |
| **QUIESCENT CURRENT** | | | | | | |
| Quiescent Current ($I_q$ = $I_{in}$ − $I_{out}$) | | $I_q$ | | | | μA |
| | $I_{out}$ = 0 mA, $T_J$ = 25 °C | | – | 17 | 21 | |
| | $I_{out}$ = 0 mA, $T_J$ ≤ 125 °C | | – | – | 23 | |
| | $I_{out}$ = 0.1 mA, $T_J$ = 25 °C | | – | 19 | 23 | |
| | $I_{out}$ = 0.1 mA, $T_J$ ≤ 125 °C | | – | – | 25 | |
| **CURRENT LIMIT PROTECTION** | | | | | | |
| Current Limit | $V_{out}$ = 0.96 x $V_{out_nom}$ | $I_{LIM}$ | 400 | – | 1100 | mA |
| Short Circuit Current Limit | $V_{out}$ = 0 V | $I_{SC}$ | 400 | – | 1100 | mA |
| **PSRR** | | | | | | |
| Power Supply Ripple Rejection (Note 10) | f = 100 Hz, 0.5 $V_{pp}$ | PSRR | – | 80 | – | dB |
| **THERMAL SHUTDOWN** | | | | | | |
| Thermal Shutdown Temperature (Note 10) | | $T_{SD}$ | 150 | 175 | 195 | °C |
| Thermal Shutdown Hysteresis (Note 10) | | $T_{SH}$ | – | 10 | – | °C |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

8. Performance guaranteed over the indicated operating temperature range by design and/or characterization tested at $T_A \approx T_J$. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.
9. Measured when output voltage falls 100 mV below the regulated voltage at $V_{in}$ = 13.5 V.
10. Values based on design and/or characterization.



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## TYPICAL CHARACTERISTICS

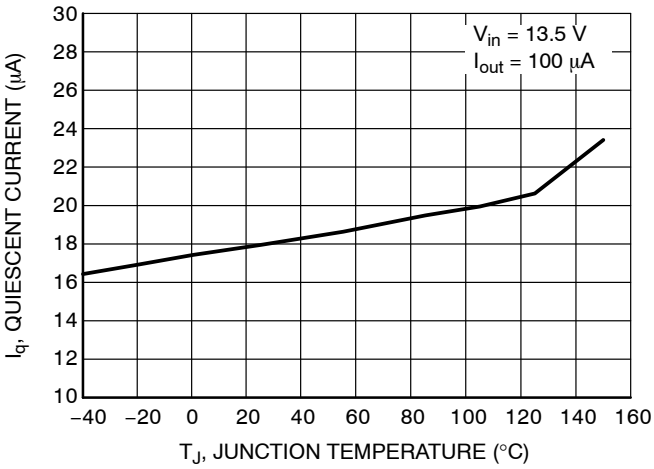



**Figure 4. Quiescent Current vs. Temperature**

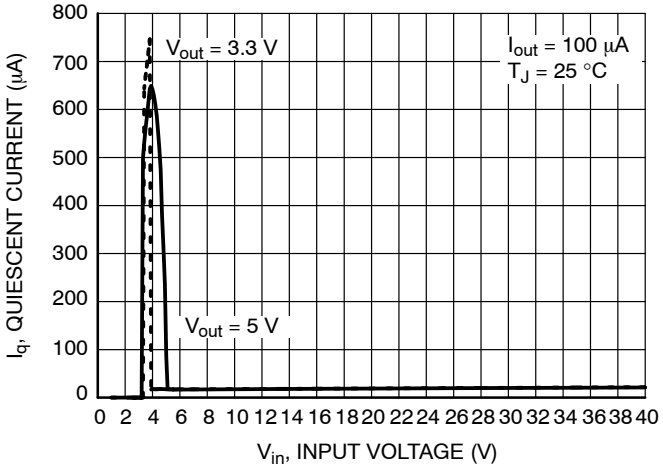



**Figure 5. Quiescent Current vs. Input Voltage**

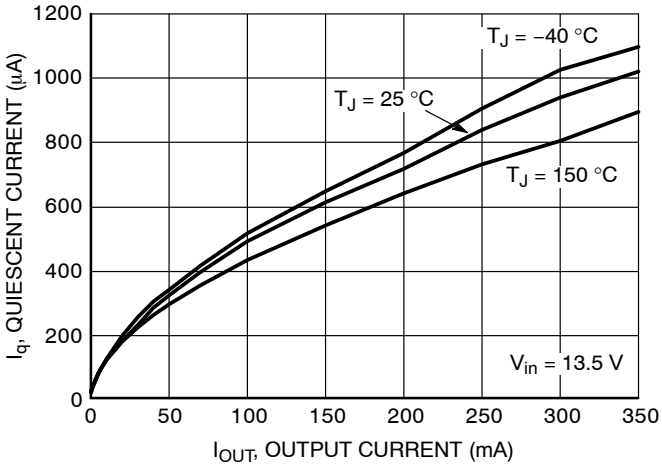



**Figure 6. Quiescent Current vs. Output Current**

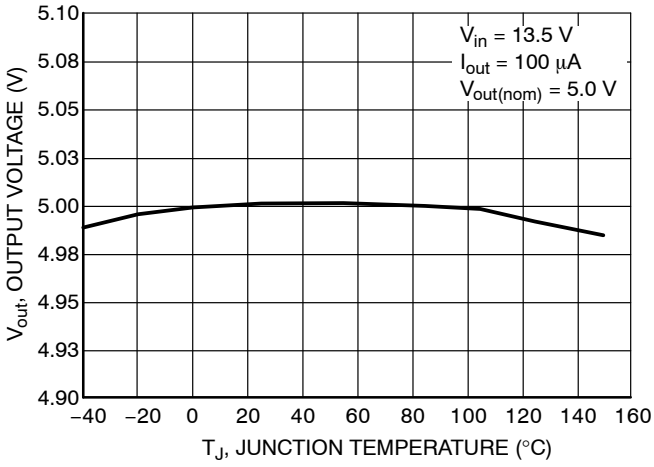



**Figure 7. Output Voltage vs. Temperature**

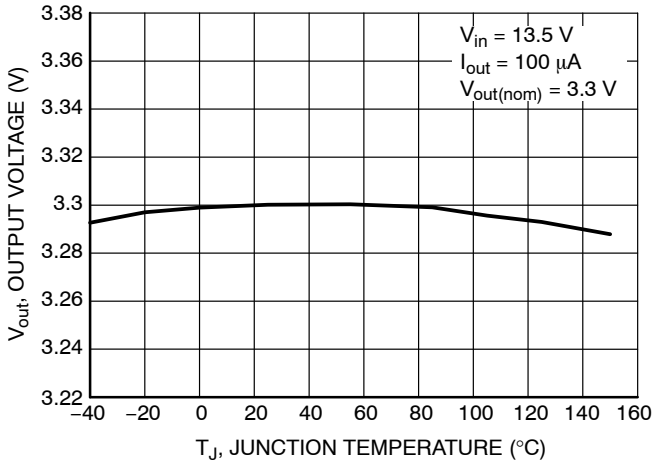



**Figure 8. Output Voltage vs. Temperature**



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## TYPICAL CHARACTERISTICS (continued)

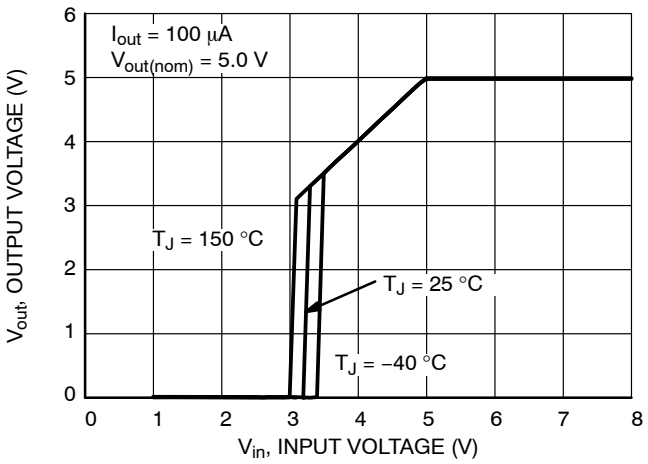



**Figure 9. Output Voltage vs. Input Voltage**

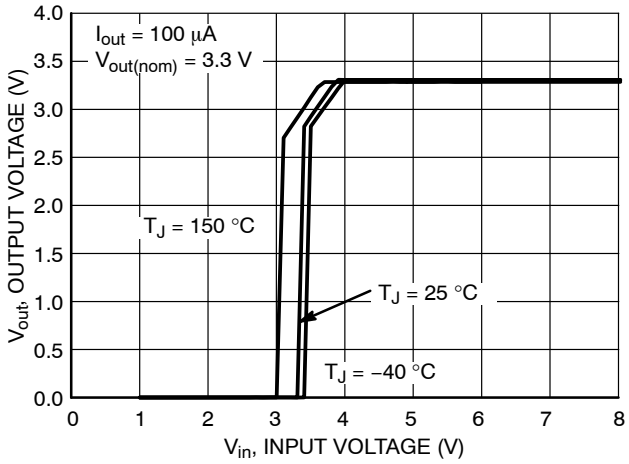



**Figure 10. Output Voltage vs. Input Voltage**

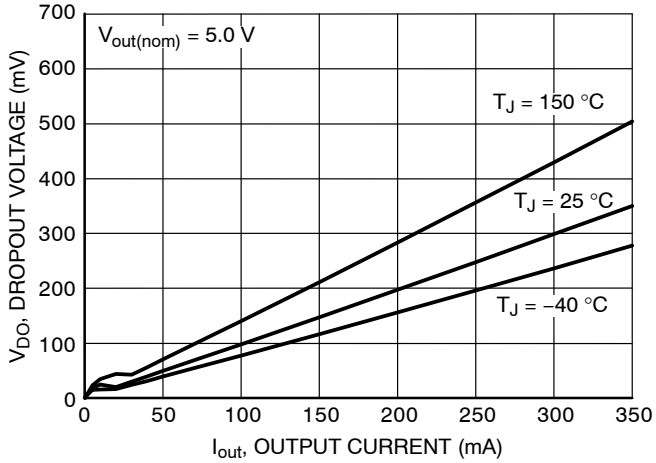



**Figure 11. Dropout vs. Output Current**

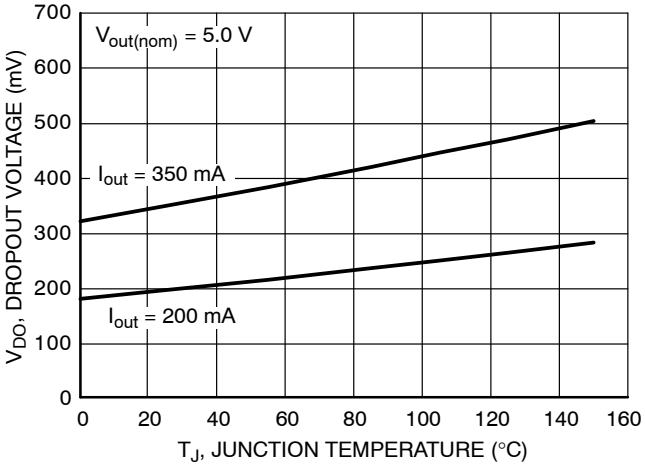



**Figure 12. Dropout vs. Temperature**



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## TYPICAL CHARACTERISTICS (continued)

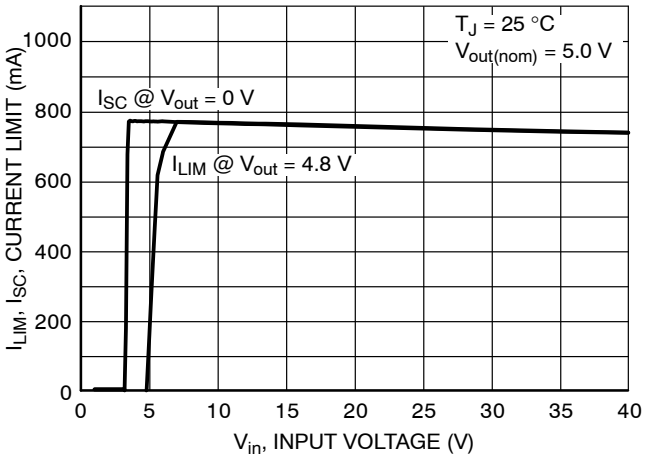



**Figure 13. Output Current Limit vs. Input Voltage**

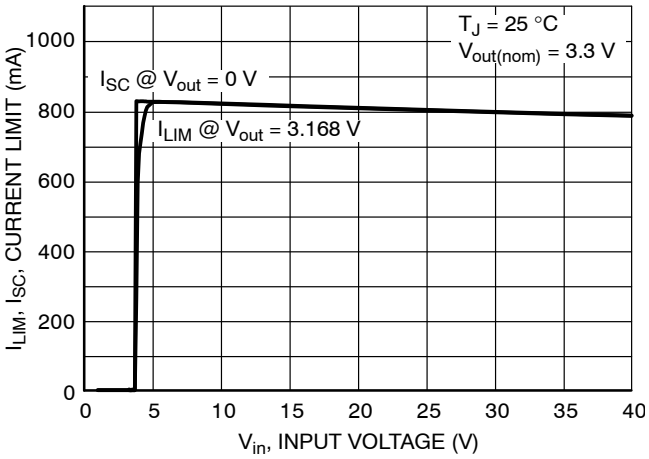



**Figure 14. Output Current Limit vs. Input Voltage**

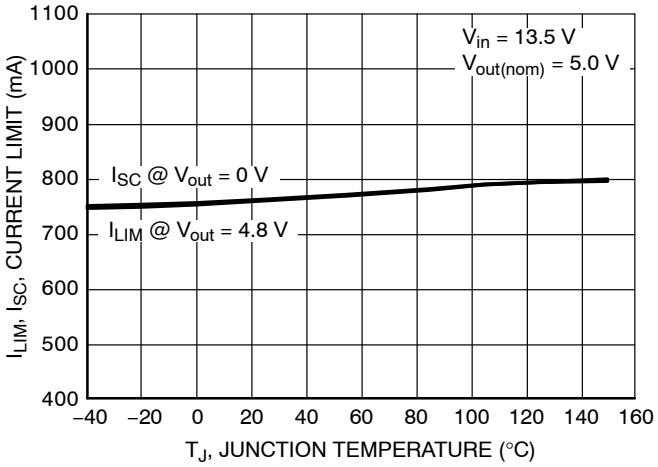



**Figure 15. Output Current Limit vs. Temperature**

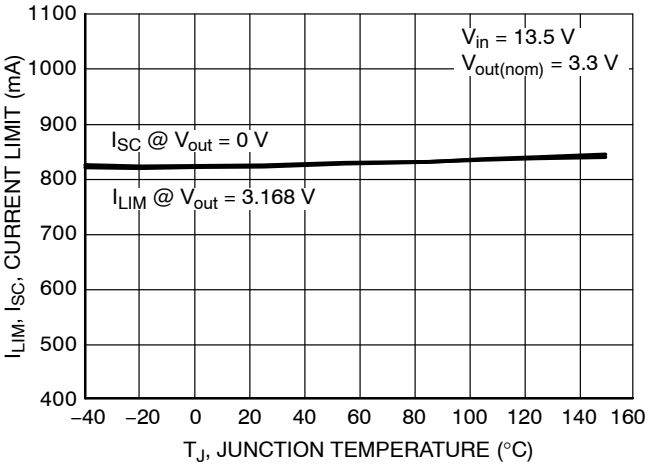



**Figure 16. Output Current Limit vs. Temperature**

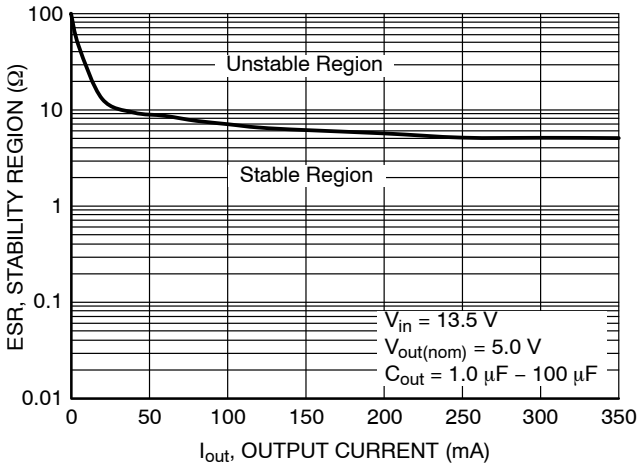



**Figure 17. $C_{out}$ ESR Stability Region vs. Output Current**

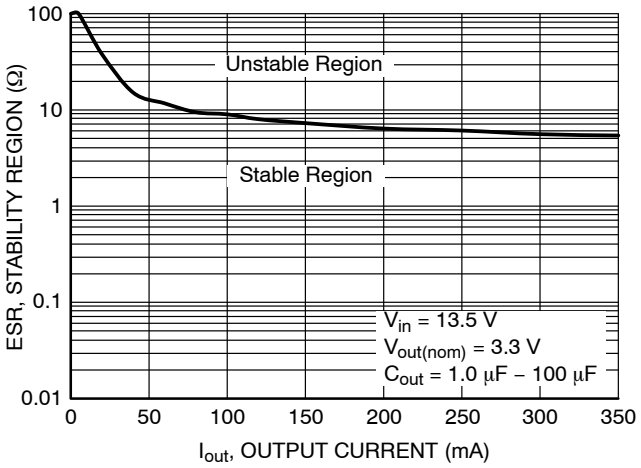



**Figure 18. $C_{out}$ ESR Stability Region vs. Output Current**



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## TYPICAL CHARACTERISTICS (continued)

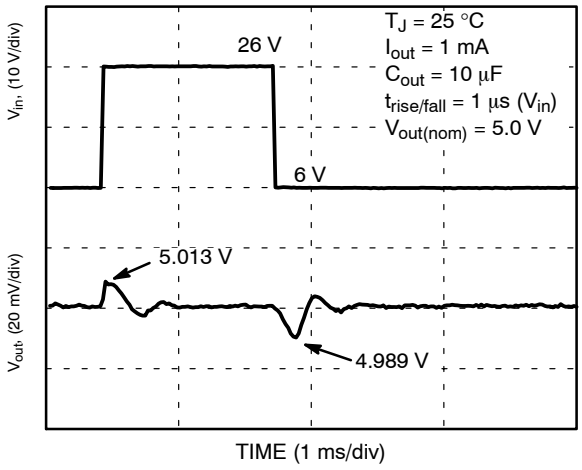



**Figure 19. Line Transients**

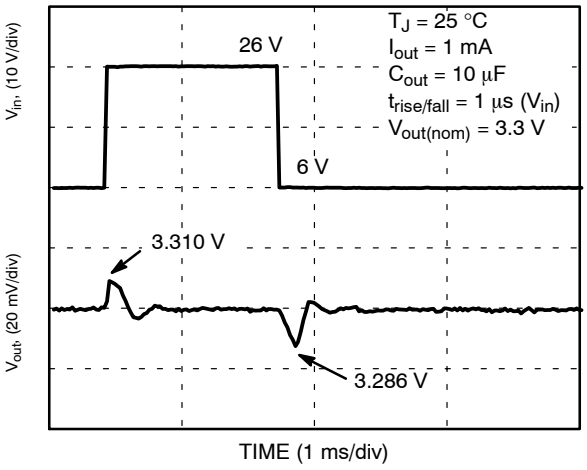



**Figure 20. Line Transients**

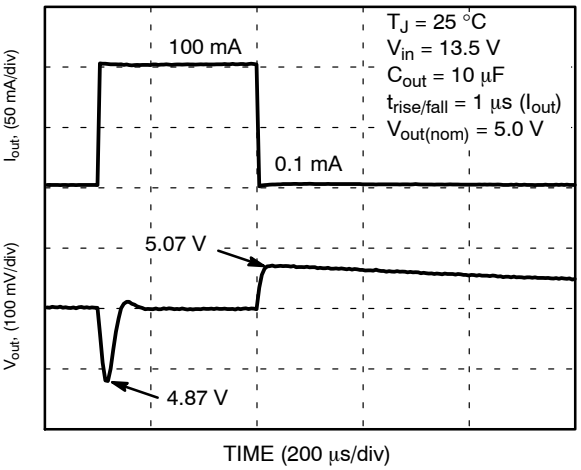



**Figure 21. Load Transients**

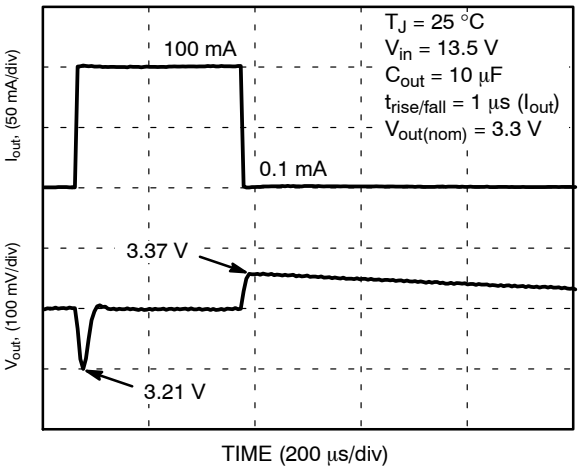



**Figure 22. Load Transients**

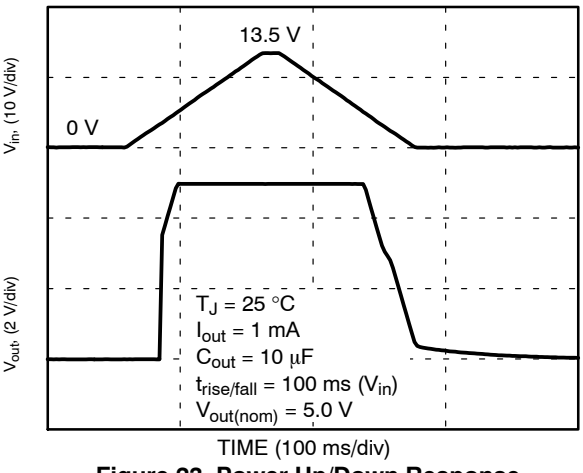



**Figure 23. Power Up/Down Response**

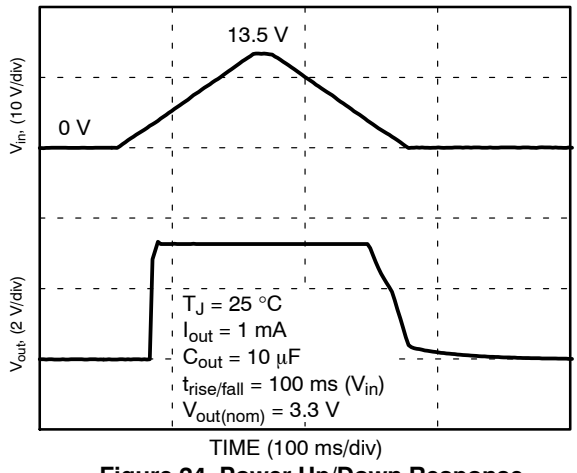



**Figure 24. Power Up/Down Response**



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## TYPICAL CHARACTERISTICS (continued)

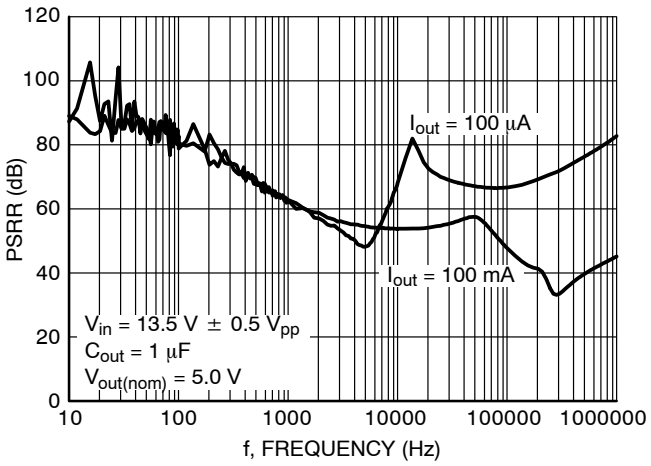



**Figure 25. PSRR vs. Frequency**

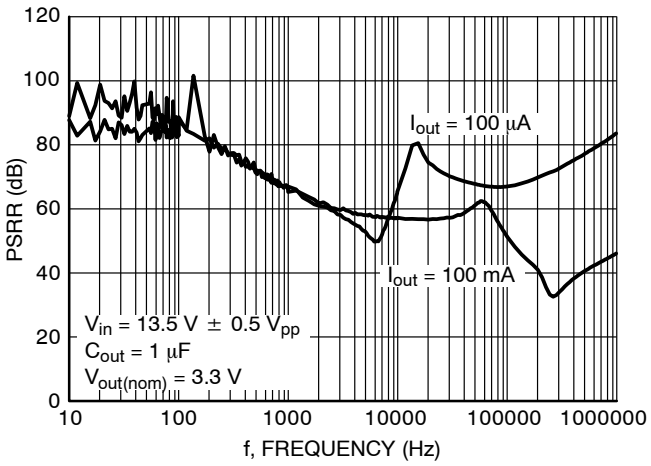



**Figure 26. PSRR vs. Frequency**

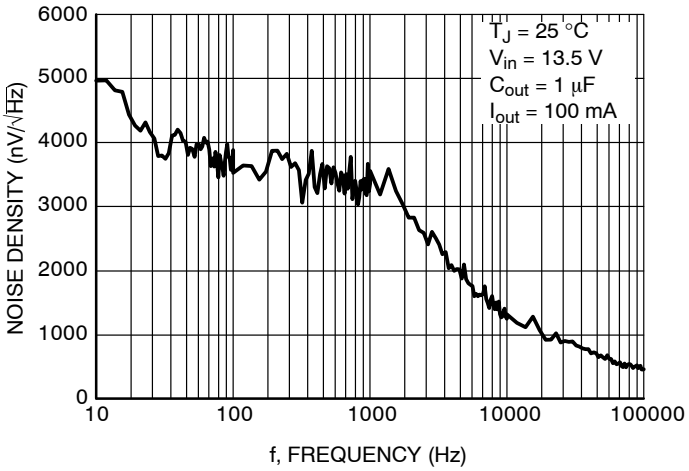



**Figure 27. Noise vs. Frequency**



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## DEFINITIONS

### General

All measurements are performed using short pulse low duty cycle techniques to maintain junction temperature as close as possible to ambient temperature.

### Output voltage

The output voltage parameter is defined for specific temperature, input voltage and output current values or specified over Line, Load and Temperature ranges.

### Line Regulation

The change in output voltage for a change in input voltage measured for specific output current over operating ambient temperature range.

### Load Regulation

The change in output voltage for a change in output current measured for specific input voltage over operating ambient temperature range.

### Dropout Voltage

The input to output differential at which the regulator output no longer maintains regulation against further reductions in input voltage. It is measured when the output drops 100 mV below its nominal value. The junction temperature, load current, and minimum input supply requirements affect the dropout level.

### Quiescent and Disable Currents

Quiescent Current ($I_q$) is the difference between the input current (measured through the LDO input pin) and the output load current.

### Current Limit and Short Circuit Current Limit

Current Limit is value of output current by which output voltage drops below 96% of its nominal value. Short Circuit Current Limit is output current value measured with output of the regulator shorted to ground.

### PSRR

Power Supply Rejection Ratio is defined as ratio of output voltage and input voltage ripple. It is measured in decibels (dB).

### Line Transient Response

Typical output voltage overshoot and undershoot response when the input voltage is excited with a given slope.

### Load Transient Response

Typical output voltage overshoot and undershoot response when the output current is excited with a given slope between low-load and high-load conditions.

### Thermal Protection

Internal thermal shutdown circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. When activated at typically 175 °C, the regulator turns off. This feature is provided to prevent failures from accidental overheating.

### Maximum Package Power Dissipation

The power dissipation level is maximum allowed power dissipation for particular package or power dissipation at which the junction temperature reaches its maximum operating value, whichever is lower.



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## APPLICATIONS INFORMATION

The NCV8774C regulator is self-protected with internal thermal shutdown and internal current limit. Typical characteristics are shown in Figures 4 to 27.

### Input Decoupling ($C_{in}$)

A ceramic or tantalum 0.1 μF capacitor is recommended and should be connected close to the NCV8774C package. Higher capacitance and lower ESR will improve the overall line and load transient response.

If extremely fast input voltage transients are expected then appropriate input filter must be used in order to decrease rising and/or falling edges below 4 V/μs for proper operation. The filter can be composed of several capacitors in parallel.

### Output Decoupling ($C_{out}$)

The NCV8774C is a stable component and does not require a minimum Equivalent Series Resistance (ESR) for the output capacitor. Stability region of ESR vs Output Current is shown in Figures 17 to 18. The minimum output decoupling value is 1 μF and can be augmented to fulfill stringent load transient requirements. The regulator works with ceramic chip capacitors as well as tantalum devices. Larger values improve noise rejection and load regulation transient response.

### Thermal Considerations

As power in the NCV8774C increases, it might become necessary to provide some thermal relief. The maximum power dissipation supported by the device is dependent upon board design and layout. Mounting pad configuration on the PCB, the board material, and the ambient temperature affect the rate of junction temperature rise for the part. When the NCV8774C has good thermal conductivity through the PCB, the junction temperature will be relatively low with high power applications. The maximum dissipation the NCV8774C can handle is given by:

$$P_{D(max)} = \frac{\left[T_{J(max)} - T_A\right]}{R_{\theta JA}} \qquad \text{(eq. 1)}$$

Since $T_J$ is not recommended to exceed 150 °C, then the NCV8774C soldered on 645 mm$^2$, 1 oz copper area, FR4 can dissipate up to 2.53 W for 1s0p PCB board and 4.49 W for 2s2p PCB board when the ambient temperature ($T_A$) is 25 °C. See Figure 28 for $R_{\theta JA}$ versus PCB area. The power dissipated by the NCV8774C can be calculated from the following equations:

$$P_D = V_{in}(I_q@I_{out}) + I_{out}(V_{in} - V_{out}) \qquad \text{(eq. 2)}$$

or

$$V_{in(max)} = \frac{P_{D(max)} + (V_{out} \times I_{out})}{I_{out} + I_q} \qquad \text{(eq. 3)}$$

NOTE: Items containing $I_q$ can be neglected if $I_{out} >> I_q$.

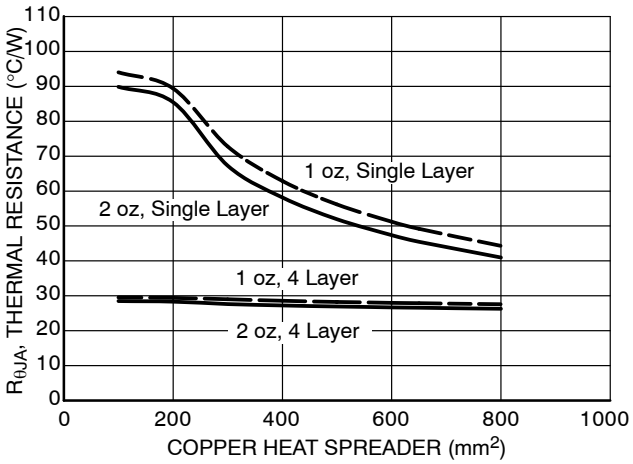



**Figure 28. Thermal Resistance vs. PCB Copper Area**

### Hints

$V_{in}$ and GND printed circuit board traces should be as wide as possible. When the impedance of these traces is high, there is a chance to pick up noise or cause the regulator to malfunction. Place external components, especially the output capacitor, as close as possible to the NCV8774C and make traces as short as possible. The NCV8774C is not developed in compliance with ISO26262 standard. If application is safety critical then the below application example diagram shown in Figure 29 can be used.

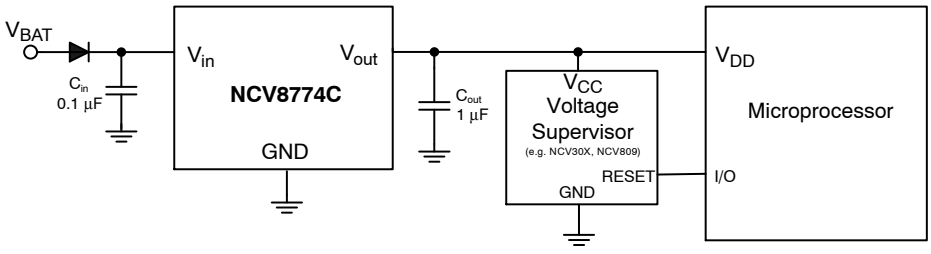



**Figure 29. NCV8774C Application Diagram**



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## ORDERING INFORMATION

| Device | Output Voltage | Marking | Package | Shipping† |
|---|---|---|---|---|
| NCV8774CDT50RKG | 5.0 V | 8774C5G | DPAK-3 (Pb-Free) | 2500 / Tape & Reel |
| NCV8774CDT33RKG | 3.3 V | 8774C3G | DPAK-3 (Pb-Free) | 2500 / Tape & Reel |

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



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## REVISION HISTORY

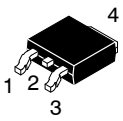
| Revision | Description of Changes | Date |
|---|---|---|
| 3 | Document rebranded to **onsemi** format. | 2/17/2026 |

This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.



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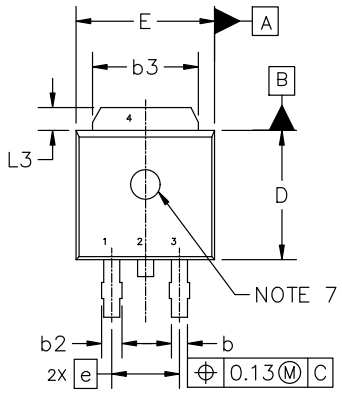
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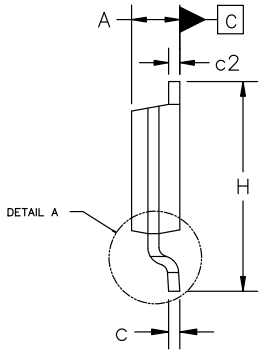

**DPAK−3 6.10x6.54x2.28, 2.29P**
CASE 369C
ISSUE K

DATE 14 MAY 2026

**SCALE 1:1**

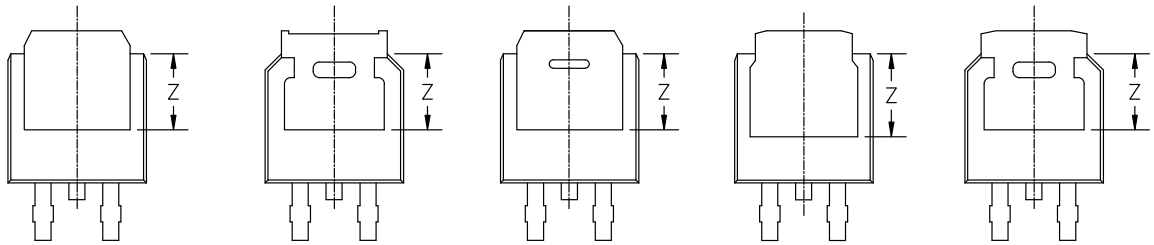



TOP VIEW




SIDE VIEW

| MILLIMETERS | | | |
|---|---|---|---|
| DIM | MIN | NOM | MAX |
| A | 2.18 | 2.28 | 2.38 |
| A1 | 0.00 | −−− | 0.13 |
| b | 0.63 | 0.76 | 0.89 |
| b2 | 0.72 | 0.93 | 1.14 |
| b3 | 4.57 | 5.02 | 5.46 |
| c | 0.46 | 0.54 | 0.61 |
| c2 | 0.46 | 0.54 | 0.61 |
| D | 5.97 | 6.10 | 6.22 |
| E | 6.35 | 6.54 | 6.73 |
| e | 2.29 BSC | | |
| H | 9.40 | 9.91 | 10.41 |
| L | 1.40 | 1.59 | 1.78 |
| L1 | 2.90 REF | | |
| L2 | 0.51 BSC | | |
| L3 | 0.89 | −−− | 1.27 |
| L4 | −−− | −−− | 1.01 |
| Z | 3.93 | −−− | −−− |

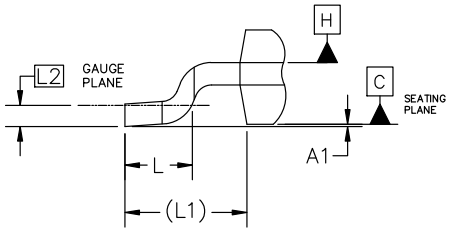



BOTTOM VIEW

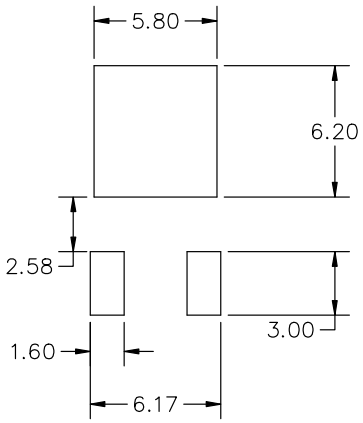
ALTERNATE CONSTRUCTIONS

NOTES:

1. DIMENSIONING AND TOLERANCING ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3, AND Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. OPTIONAL MOLD FEATURE.




DETAIL A
ROTATED 90° CW




RECOMMENDED MOUNTING FOOTPRINT*

*FOR ADDITIONAL INFORMATION ON OUR PB−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

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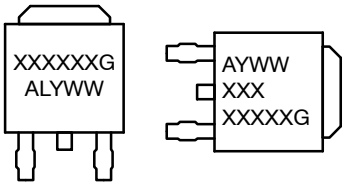


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**DPAK−3 6.10x6.54x2.28, 2.29P**
CASE 369C
ISSUE K

DATE 13 MAY 2026

## GENERIC MARKING DIAGRAM*




**IC** **Discrete**

| | |
|---|---|
| XXXXXX | = Device Code |
| A | = Assembly Location |
| L | = Wafer Lot |
| Y | = Year |
| WW | = Work Week |
| G | = Pb−Free Package |

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

STYLE 4:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 5:
PIN 1. GATE
2. ANODE
3. CATHODE
4. ANODE

STYLE 6:
PIN 1. MT1
2. MT2
3. GATE
4. MT2

STYLE 7:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 8:
PIN 1. N/C
2. CATHODE
3. ANODE
4. CATHODE

STYLE 9:
PIN 1. ANODE
2. CATHODE
3. RESISTOR ADJUST
4. CATHODE

STYLE 10:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. ANODE




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