Radiation Hardened NPN Silicon Low Power Transistor

2N2484_UA_UB_UBC

Product Overview

Devices:

- 2N2484
- 2N2484UA
- 2N2484UB
- 2N2484UBC [1]

Qualified Levels:

- JANSE – 30K Rads (Si)[2]
- JANSK – 50K Rads (Si)[2]
- JANSU – 100K Rads (Si)[2]
- JANSM – 3K Rads (Si)
- JANSD – 10K Rads (Si)
- JANSP – 30K Rads (Si)
- JANSL – 50K Rads (Si)
- JANSR – 100K Rads (Si)
- JANSF – 300K Rads (Si)

Notes:

1. Available to JANS quality level only
2. Low dose rate 10 mRad/s

Figure 1. TO-18 (TO-206AA) 2N2484

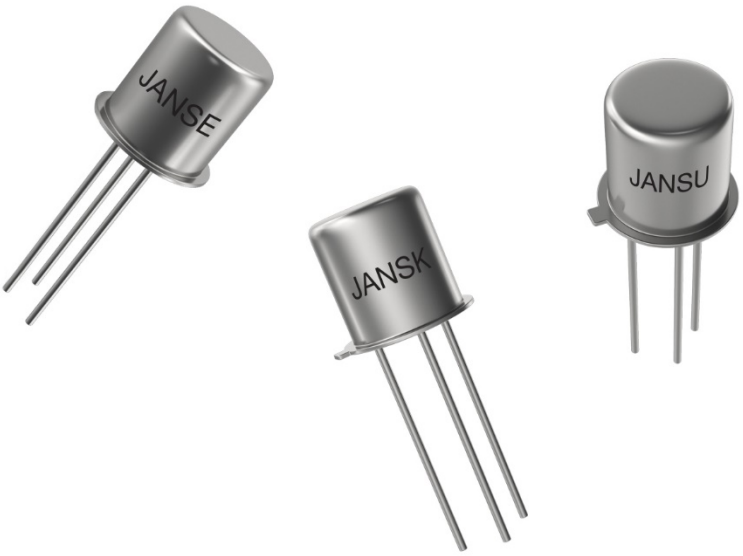


Figure 2. 2N2484UA

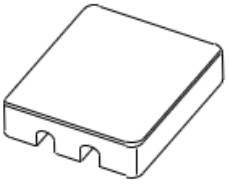
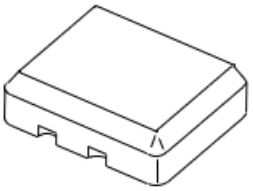


Figure 3. 2N2484UB, UBC (UBC = Ceramic Lid Version)



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1. Maximum Ratings

Table 1-1. Maximum Ratings at 25 °C Unless Otherwise Noted

Parameters / Test Conditions	Symbol	Value	Unit
Collector-Emitter voltage	V_{CEO}	60	Vdc
Collector-Base voltage	V_{CBO}	60	Vdc
Emitter-Base voltage	V_{EBO}	6.0	Vdc
Collector current	I_C	50	mAdc
Total power dissipation at T_A = +25 °C[1]	P_T	360	mW
Operating and storage junction temperature range	T_J, T_{stg}	–65 to +200	°C

Note:

1. See 19500/376 for Thermal Performance Curves.

1.1 Thermal Characteristics

Table 1-2. Thermal Characteristics

Parameters / Test Conditions	Symbol	Value	Unit
Thermal resistance, ambient-to-case 2N2484 2N2484UA 2N2484UB, UBC	$R_{\theta JA}$	 325 275 350	°C/W

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2. Electrical Characteristics

Table 2-1. Electrical Characteristics at 25 °C Unless Otherwise Stated

Parameters / Test Conditions	Symbol	Min.	Max.	Unit
Off Characteristics				
Collector-Emitter breakdown voltage I_C = 10 mAdc	$V_{(BR)CEO}$	60	—	Vdc
Collector-Emitter cutoff current V_{CE} = 45 Vdc	I_{CES}	—	5.0	ηAdc
Collector-Base cutoff current V_{CB} = 45 Vdc V_{CB} = 60 Vdc	I_{CBO}	—	5.0 10	ηAdc μAdc
Collector-Emitter cutoff current V_{CE} = 5.0 Vdc	I_{CEO}	—	2.0	ηAdc
Emitter-Base cutoff current V_{EB} = 5.0 Vdc V_{EB} = 6.0 Vdc	I_{EBO}	—	2.0 10	ηAdc μAdc
On Characteristics[1]				
Forward-Current transfer ratio I_C = 1.0 μAdc, V_{CE} = 5.0 Vdc I_C = 10 μAdc, V_{CE} = 5.0 Vdc I_C = 100 μAdc, V_{CE} = 5.0 Vdc I_C = 500 μAdc, V_{CE} = 5.0 Vdc I_C = 1.0 mAdc, V_{CE} = 5.0 Vdc I_C = 10 mAdc, V_{CE} = 5.0 Vdc	h_{FE}	45 200 225 250 250 225	— 500 675 800 800 800	—
Collector-Emitter saturation voltage I_C = 1.0 mAdc, I_B = 100 μAdc	$V_{CE(sat)}$	—	0.3	Vdc
Base-Emitter voltage V_{CE} = 5.0 Vdc, I_C = 100 μAdc	$V_{BE(ON)}$	0.5	0.7	Vdc

Note:

1. Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2.0%

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3. Dynamic Characteristics

Table 3-1. Dynamic Characteristics

Parameters / Test Conditions	Symbol	Min.	Max.	Unit
Forward current transfer ratio I_C = 50 µAdc, V_{CE} = 5.0 Vdc, f = 5.0 MHz I_C = 500 µAdc, V_{CE} = 5.0 Vdc, f = 30 MHz	$\lvert h_{fe} \rvert$	3.0 2.0	— 0.7	—
Open circuit output admittance I_C = 1.0 mAdc, V_{CE} = 5.0 Vdc, f = 1.0 kHz	h_{oe}	—	40	µmhos
Open circuit reverse-voltage transfer ratio I_C = 1.0 mAdc, V_{CE} = 5.0 Vdc, f = 1.0 kHz	h_{re}	—	8.0×10^{-4}	—
Input impedance I_C = 1.0 mAdc, V_{CE} = 5.0 Vdc, f = 1.0 kHz	h_{je}	3.5	24	kΩ
Small-Signal short-circuit forward current transfer ratio I_C = 1.0 mAdc, V_{CE} = 5.0 Vdc, f = 1.0 kHz	h_{fe}	250	900	—
Output capacitance V_{CB} = 5.0 Vdc, I_E = 0, 100 kHz ≤ f ≤ 1.0 MHz	C_{obo}	—	5.0	pF
Input capacitance V_{EB} = 0.5 Vdc, I_C = 0, 100 kHz ≤ f ≤ 1.0 MHz	C_{ibo}	—	6.0	pF

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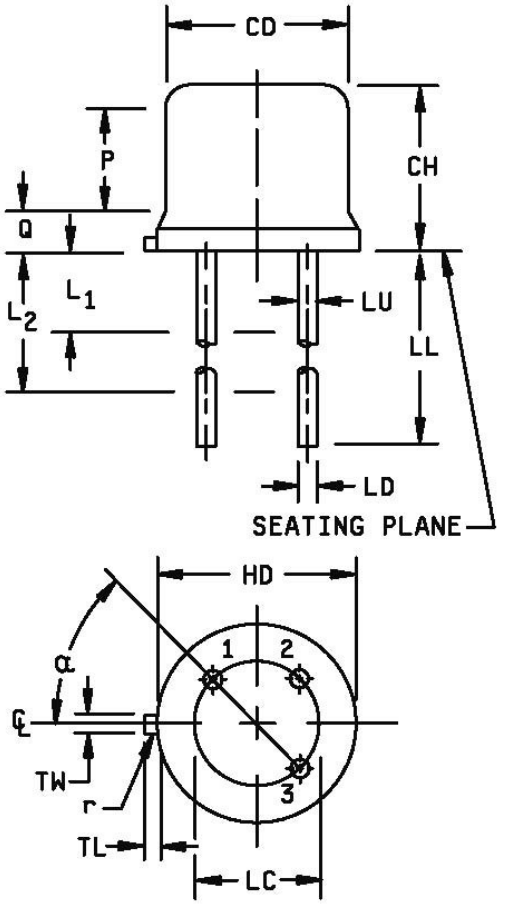
4. Package Dimensions

Figure 4-1. Physical Dimensions (similar to TO-18)



Symbol	Dimensions				Notes
	Inches		Millimeters		
	Min.	Max.	Min.	Max.	
CD	0.178	0.195	4.52	4.95	—
CH	0.170	0.210	4.32	5.33	—
HD	0.209	0.230	5.31	5.84	—
LC	0.100 TP		2.54 TP		6
LD	0.016	0.021	0.41	0.53	7, 8
LL	0.500	0.750	12.70	19.05	7, 8
LU	0.016	0.019	0.41	0.48	7, 8
L1	—	0.050	—	1.27	7, 8
L2	0.250	—	6.35	—	7, 8
P	0.100	—	2.54	—	—
Q	—	0.040	—	1.02	5
TL	0.028	0.048	0.71	1.22	3, 4

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Symbol	Dimensions				Notes
	Inches		Millimeters		
	Min.	Max.	Min.	Max.	
TW	0.036	0.046	0.91	1.17	3
r	—	0.010	—	0.25	10
α	45° TP		45° TP		6

Notes:

1. Dimension are in inches.
2. Millimeters are given for general information only.
3. Beyond r (radius) maximum, TW shall be held for a minimum length of 0.011 inch (0.28 mm).
4. Dimension TL measured from maximum HD.
5. Body contour optional within zone defined by HD, CD, and Q.
6. Leads at gauge plane 0.054 +0.001 –0.000 inch (1.37 +0.03 –0.00 mm) below seating plane shall be within 0.007 inch (0.18 mm) radius of true position (TP) at maximum material condition (MMC) relative to tab at MMC.
7. Dimension LU applies between L1 and L2. Dimension LD applies between L2 and LL minimum. Diameter is uncontrolled in L1 and beyond LL minimum.
8. All three leads
9. The collector shall be internally connected to the case.
10. Dimension r (radius) applies to both inside corners of tab.
11. In accordance with ASME Y14.5M, diameters are equivalent to φx symbology.
12. Lead 1 = emitter, lead 2 = base, lead 3 = collector

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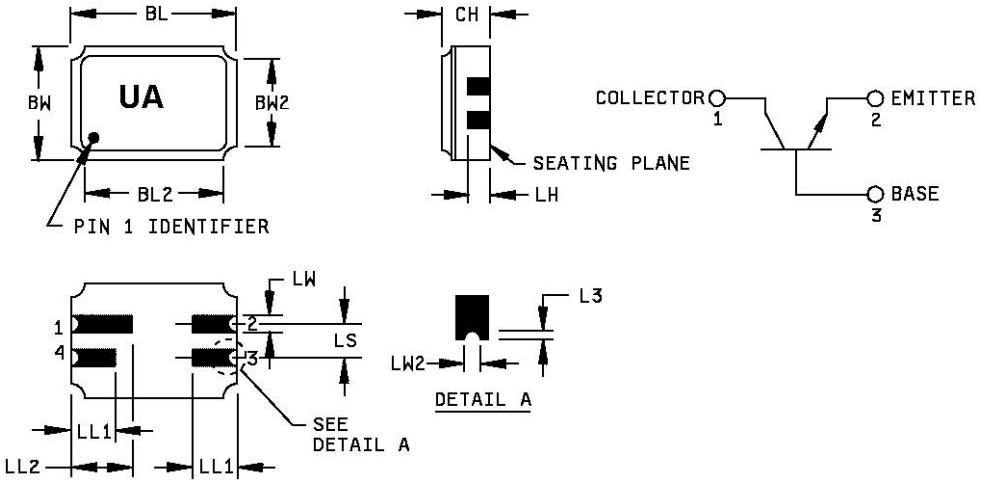
Figure 4-2. Physical dimensions, Surface Mount (2N2484UA)



Symbol	Dimensions				Notes
	Inches		Millimeters		
	Min.	Max.	Min.	Max.	
BL	0.215	0.225	5.46	5.71	—
BL2	—	0.225	—	5.71	—
BW	0.145	0.155	3.68	3.94	—
BW2	—	0.155	—	3.94	—
CH	0.061	0.075	1.55	1.91	3
L3	0.003	0.007	0.08	0.18	5
LH	0.029	0.042	0.74	1.07	—
LL1	0.032	0.048	0.81	1.22	—
LL2	0.072	0.088	1.83	2.24	—
LS	0.045	0.055	1.14	1.39	—
LW	0.022	0.028	0.56	0.71	—
LW2	0.006	0.022	0.15	0.56	5

Pin No.	1	2	3	4
Transistor	Collector	Emitter	Base	N/C

Notes:

1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Dimension CH controls the overall package thickness. When a window lid is used, dimension CH must increase by a minimum of 0.010 inch (0.254 mm) and a maximum of 0.040 inch (1.020 mm).
4. The corner shape (square, notch, radius) may vary at the manufacturer's option, from that shown on the drawing.
5. Dimensions LW2 minimum and L3 minimum and the appropriate castellation length define an unobstructed three-dimensional space traversing all of the ceramic layers in which a castellation was designed. (Castellations are required on the bottom two layers, optional on the top ceramic

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layer.) Dimension LW2 maximum and L3 maximum define the maximum width and depth of the castellation at any point on its surface. Measurement of these dimensions may be made prior to solder dipping.

6. The co-planarity deviation of all terminal contact points, as defined by the device seating plane, shall not exceed 0.006 inch (0.15 mm) for solder dipped leadless chip carriers.
7. In accordance with ASME Y14.5M, diameters are equivalent to φx symbology.

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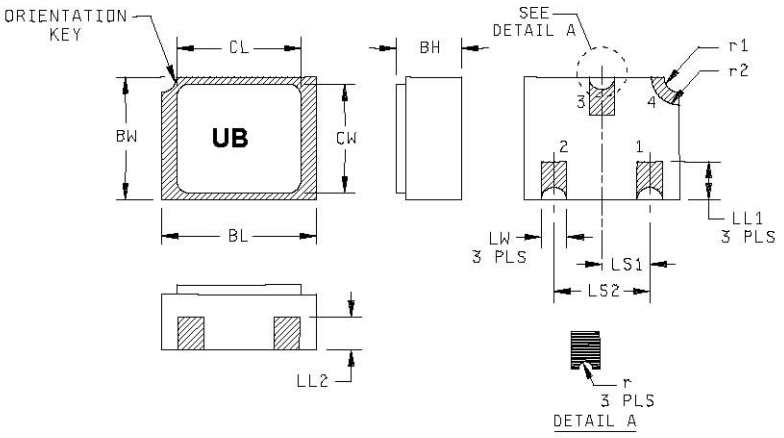
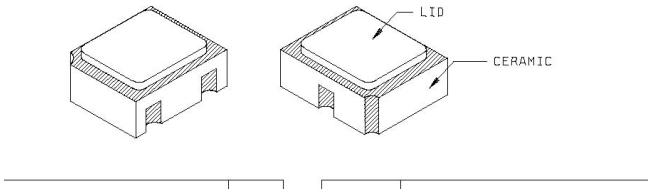
Figure 4-3. Physical Dimensions, Surface Mount (2N2484UB)





Symbol	Dimensions				Symbol	Dimensions			
	Inches		Millimeters			Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
BH	0.046	0.056	1.17	1.42	LS1	0.036	0.040	0.91	1.02
BL	0.115	0.128	2.92	3.25	LS2	0.071	0.079	1.80	2.01
BW	0.085	0.108	2.16	2.74	LW	0.016	0.024	0.41	0.61
CL	—	0.128	—	3.25	r	—	0.008	—	0.203
CW	—	0.108	—	2.74	r1	—	0.012	—	0.305
LL1	0.022	0.038	0.56	0.97	r2	—	0.022	—	0.559
LL2	0.017	0.035	0.43	0.89					

Notes:

1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Hatched areas on package denote metallized areas.
4. Pad 1 = Base, Pad 2 = Emitter, Pad 3 = Collector, Pad 4 = Shielding connected to the lid
5. In accordance with ASME Y14.5M, diameters are equivalent to φx symbology.

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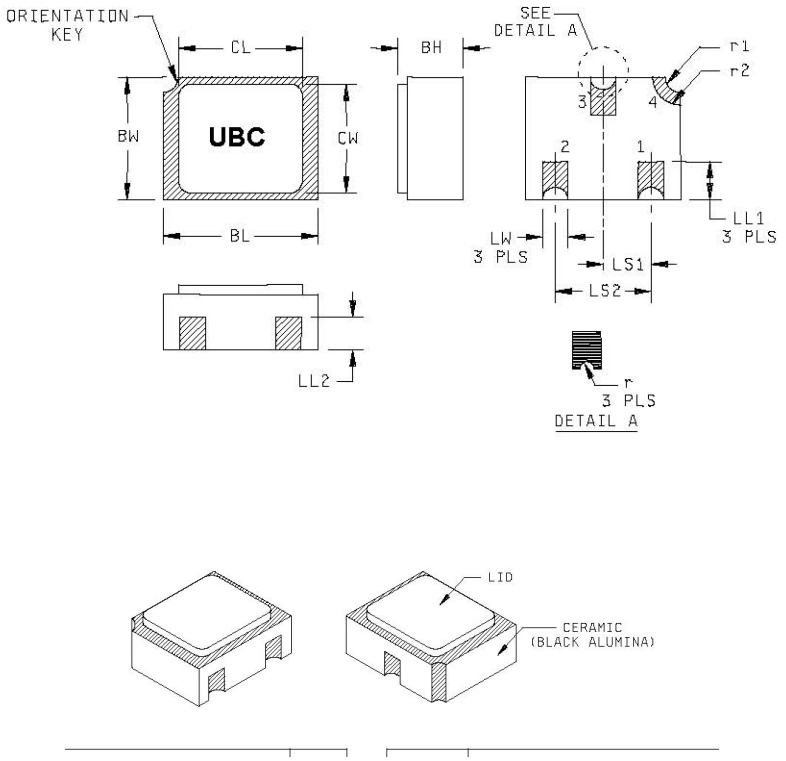
Figure 4-4. Physical Dimensions, Surface Mount (2N2484UBC)



Symbol	Dimensions				Symbol	Dimensions			
	Inches		Millimeters			Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
BH	0.046	0.071	1.17	1.80	LS1	0.036	0.040	0.91	1.02
BL	0.115	0.128	2.92	3.25	LS2	0.071	0.079	1.80	2.01
BW	0.085	0.108	2.16	2.74	LW	0.016	0.024	0.41	0.61
CL	—	0.128	—	3.25	r	—	0.008	—	0.203
CW	—	0.108	—	2.74	r1	—	0.012	—	0.305
LL1	0.022	0.038	0.56	0.97	r2	—	0.022	—	0.559
LL2	0.017	0.035	0.43	0.89					

Notes:

1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Pad 1 = Base, Pad 2 = Emitter, Pad 3 = Collector, Pad 4 = connected to the lid braze ring
4. In accordance with ASME Y14.5M, diameters are equivalent to φx symbology.

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5. Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Revision	Date	Description
A	06/2024	Document was converted to Microchip template. Previous Microsemi literature number T4-LDS-780778 was replaced with DS00005470A.

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