Lead-free Green

PI7C9X113SL

PCI Express-to-PCI Bridge

Datasheet

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Revision 7

A Product Line of Diodes Incorporated

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REVISION HISTORY

DATE	REVISION	DESCRIPTION
05/27/2009	0.1	Preliminary Datasheet
09/15/2009	0.2	Updated Section 6.3 (I/O Limit Register – Offset 1Ch, Interrupt Line Register – Offset 3Ch, Arbiter Enable Register – Offset 48h, Memory ReadSmart Range Control Register – Offset 58h, Upstream Memory Read/Write Control Register – Offset 68h, XPIP Configuration Register 1 – Offset D0h) Updated Section 12 IEEE 1149.1 Compatible JTAG Controller (Removed TRST_L) Updated Table 14-2 DC Electrical Characteristics (VDDA)
07/26/2010	0.3	Updated Section 2 Pin Definitions (Pin 22 to NC) Updated Section 6.3 PCI Configuration Registers (Offset 40h, 44h, 6Ch, A4h, D0h, D4h) Updated VDDC and VDDA voltage to 1.1V (Section 2.7, Table 14-2) Updated Temperature Support Range from Extended Commercial to Industrial
01/14/2011	0.3g	Updated DC Spec Parameters
08/19/2011	1.0	Updated Figure 15-1 Package outline drawing Datasheet Released
09/7/2011	1.1	Updated VDDC and VDDA voltage to 1.0V (Section 2.7, Table 14-2)
05/27/2013	1.2	Remove Figure 8-2 Topology of internal clock generator and internal clock buffering – external feedback mode Remove Figure 8-4 Topology of external clock generator and internal clock buffering – external feedback mode Updated VDDC and VDDA voltage to 1.15V (retroactive notice in January 2016)
07/24/2014	1.3	Remove NC and pin 22 from Section 2.6 and added pin 22 to Section 2.7 under pin name VSS
04/21/2016	1.4	Updated Section 2.5 JTAG Boundary Scan Signals
01/23/2017	1.5	Updated Logo Updated Section 2.7 Power and Ground Pins Updated Section 2.8 Pin Assignments Updated Section 14.1 Absolute Maximum Ratings Updated Section 14.2 DC Specifications Added Section 14.4 Operating Ambient Temperature Added Table 14-4 PCI Express Interface - Differential Transmitter (TX) Output Characteristics Added Table 14-5 PCI Express Interface - Differential Receiver (RX) Input Characteristics
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04/09/2020	4	Updated Section 14 Power Sequencing Added Section 14.2 Power-Off Sequence
01/18/2021	5	Updated Section 14 Power Sequencing Updated Section 2.2 PCI Express Signals
03/24/2025	6	Not Recommended for New Design
01/20/2026	7	Remove the NRND Updated Package Outline Drawing

PREFACE

The datasheet of PI7C9X113SL will be enhanced periodically when updated information is available. The technical information in this datasheet is subject to change without notice. This document describes the functionalities of PI7C9X113SL (PCI Express Bridge) and provides technical information for designers to design their hardware using PI7C9X113SL.

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TABLE OF CONTENTS

1 INTRODUCTION 10

1.1 INDUSTRY SPECIFICATION COMPLIANCE 10
1.2 GENERAL FEATURES 10
1.3 PCI EXPRESS FEATURES 11
1.4 PCI FEATURES 11

2 PIN DEFINITIONS 12

2.1 SIGNAL TYPES 12
2.2 PCI EXPRESS SIGNALS 12
2.3 PCI SIGNALS 12
2.4 MODE SELECT AND STRAPPING SIGNALS 14
2.5 JTAG BOUNDARY SCAN SIGNALS 14
2.6 MISCELLANEOUS SIGNALS 14
2.7 POWER AND GROUND PINS 14
2.8 PIN ASSIGNMENTS 16

3 MODE SELECTION AND PIN STRAPPING 17

3.1 FUNCTIONAL MODE SELECTION 17
3.2 PIN STRAPPING 17

4 TRANSPARENT AND FORWARD BRIDGING 18

4.1 TRANSPARENT MODE 18
4.2 FORWARD BRDIGE 18

5 PCI EXPRESS FUNCTIONAL OVERVIEW 20

5.1 TLP STRUCTURE 20
5.2 VIRTUAL ISOCHRONOUS OPERATION 20

6 CONFIGURATION REGISTER ACCESS 21

6.1 CONFIGURATION REGISTER MAP 21
6.2 PCI EXPRESS EXTENDED CAPABILITY REGISTER MAP 23
6.3 PCI CONFIGURATION REGISTERS 24

6.3.1 VENDOR ID – OFFSET 00h 25
6.3.2 DEVICE ID – OFFSET 00h 25
6.3.3 COMMAND REGISTER – OFFSET 04h 25
6.3.4 PRIMARY STATUS REGISTER – OFFSET 04h 26
6.3.5 REVISION ID REGISTER – OFFSET 08h 26
6.3.6 CLASS CODE REGISTER – OFFSET 08h 26
6.3.7 CACHE LINE SIZE REGISTER – OFFSET 0Ch 27
6.3.8 PRIMARY LATENCY TIMER REGISTER – OFFSET 0Ch 27
6.3.9 HEADER TYPE REGISTER – OFFSET 0Ch 27
6.3.10 RESERVED REGISTERS – OFFSET 10h TO 17h 27
6.3.11 PRIMARY BUS NUMBER REGISTER – OFFSET 18h 28
6.3.12 SECONDARY BUS NUMBER REGISTER – OFFSET 18h 28
6.3.13 SUBORDINATE BUS NUMBER REGISTER – OFFSET 18h 28
6.3.14 SECONDARY LATENCY TIME REGISTER – OFFSET 18h 28

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6.3.15 I/O BASE REGISTER – OFFSET 1Ch 28
6.3.16 I/O LIMIT REGISTER – OFFSET 1Ch 28
6.3.17 SECONDARY STATUS REGISTER – OFFSET 1Ch 28
6.3.18 MEMORY BASE REGISTER – OFFSET 20h 29
6.3.19 MEMORY LIMIT REGISTER – OFFSET 20h 29
6.3.20 PREFETCHABLE MEMORY BASE REGISTER – OFFSET 24h 29
6.3.21 PREFETCHABLE MEMORY LIMIT REGISTER – OFFSET 24h 30
6.3.22 PREFETCHABLE BASE UPPER 32-BIT REGISTER – OFFSET 28h 30
6.3.23 PREFETCHABLE LIMIT UPPER 32-BIT REGISTER – OFFSET 2Ch 30
6.3.24 I/O BASE UPPER 16-BIT REGISTER – OFFSET 30h 30
6.3.25 I/O LIMIT UPPER 16-BIT REGISTER – OFFSET 30h 30
6.3.26 CAPABILITY POINTER – OFFSET 34h 30
6.3.27 EXPANSION ROM BASE ADDRESS REGISTER – OFFSET 38h 30
6.3.28 INTERRUPT LINE REGISTER – OFFSET 3Ch 31
6.3.29 INTERRUPT PIN REGISTER – OFFSET 3Ch 31
6.3.30 BRIDGE CONTROL REGISTER – OFFSET 3Ch 31
6.3.31 PCI DATA PREFETCHING CONTROL REGISTER – OFFSET 40h 32
6.3.32 CHIP CONTROL 0 REGISTER – OFFSET 40h 33
6.3.33 RESERVED REGISTER – OFFSET 44h 34
6.3.34 ARBITER ENABLE REGISTER – OFFSET 48h 34
6.3.35 ARBITER MODE REGISTER – OFFSET 48h 35
6.3.36 ARBITER PRIORITY REGISTER – OFFSET 48h 35
6.3.37 RESERVED REGISTERS – OFFSET 4Ch 36
6.3.38 MEMORY READSMART BASE LOWER 32-Bit REGISTER 1 – OFFSET 50h 36
6.3.39 MEMORY READSMART BASE UPPER 32-Bit REGISTER 1 – OFFSET 54h 36
6.3.40 MEMORY READSMART RANGE CONTROL REGISTER 1 – OFFSET 58h 36
6.3.41 MEMORY READSMART BASE LOWER 32-Bit REGISTER 2 – OFFSET 5Ch 36
6.3.42 MEMORY READSMART BASE UPPER 32-Bit REGISTER 2 – OFFSET 60h 37
6.3.43 MEMORY READSMART RANGE SIZE REGISTER 2 – OFFSET 64h 37
6.3.44 UPSTREAM MEMORY READ/WRITE CONTROL REGISTER – OFFSET 68h 37
6.3.45 PHY TRANSMIT/RECEIVE CONTROL REGISTER – OFFSET 6Ch 38
6.3.46 EEPROM AUTOLOAD CONTROL/STATUS REGISTER – OFFSET 70h 39
6.3.47 RESERVED REGISTER – OFFSET 74h 39
6.3.48 GPIO DATA AND CONTROL REGISTER – OFFSET 78h 39
6.3.49 RESERVED REGISTER – OFFSET 7Ch 40
6.3.50 PCI-X CAPABILITY ID REGISTER – OFFSET 80h 40
6.3.51 NEXT CAPABILITY POINTER REGISTER – OFFSET 80h 40
6.3.52 PCI-X SECONDARY STATUS REGISTER – OFFSET 80h 40
6.3.53 PCI-X BRIDGE STATUS REGISTER – OFFSET 84h 40
6.3.54 UPSTREAM SPLIT TRANSACTION REGISTER – OFFSET 88h 41
6.3.55 DOWNSTREAM SPLIT TRANSACTION REGISTER – OFFSET 8Ch 42
6.3.56 POWER MANAGEMENT ID REGISTER – OFFSET 90h 42
6.3.57 NEXT CAPABILITY POINTER REGISTER – OFFSET 90h 42
6.3.58 POWER MANAGEMENT CAPABILITY REGISTER – OFFSET 90h 42
6.3.59 POWER MANAGEMENT CONTROL AND STATUS REGISTER – OFFSET 94h 43
6.3.60 PCI-TO-PCI SUPPORT EXTENSION REGISTER – OFFSET 94h 44
6.3.61 SUBTRACTIVE DECODING PCI-TO-PCI BRIDGE ENABLE – OFFSET 98h 44
6.3.62 RESERVED REGISTERS – OFFSET 9Ch 44
6.3.63 CAPABILITY ID REGISTER – OFFSET A0h 44
6.3.64 NEXT POINTER REGISTER – OFFSET A0h 44
6.3.65 SLOT NUMBER REGISTER – OFFSET A0h 44
6.3.66 CHASSIS NUMBER REGISTER – OFFSET A0h 45
6.3.67 SECONDARY CLOCK AND CLKRUN CONTROL REGISTER – OFFSET A4h 45
6.3.68 XPIP CONFIGURATION REGISTER 3 – OFFSET A4h 46

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6.3.69 CAPABILITY ID REGISTER – OFFSET A8h 46
6.3.70 NEXT POINTER REGISTER – OFFSET A8h 46
6.3.71 RESERVED REGISTER – OFFSET A8h 46
6.3.72 SUBSYSTEM VENDOR ID REGISTER – OFFSET ACh 46
6.3.73 SUBSYSTEM ID REGISTER – OFFSET ACh 46
6.3.74 PCI EXPRESS CAPABILITY ID REGISTER – OFFSET B0h 47
6.3.75 NEXT CAPABILITY POINTER REGISTER – OFFSET B0h 47
6.3.76 PCI EXPRESS CAPABILITY REGISTER – OFFSET B0h 47
6.3.77 DEVICE CAPABILITY REGISTER – OFFSET B4h 47
6.3.78 DEVICE CONTROL REGISTER – OFFSET B8h 48
6.3.79 DEVICE STATUS REGISTER – OFFSET B8h 49
6.3.80 LINK CAPABILITY REGISTER – OFFSET BCh 49
6.3.81 LINK CONTROL REGISTER – OFFSET C0h 50
6.3.82 LINK STATUS REGISTER – OFFSET C0h 50
6.3.83 RESERVED REGISTER – OFFSET C4 – C8h 51
6.3.84 XPIP CONFIGURATION REGISTER 0 – OFFSET CCh 51
6.3.85 XPIP CONFIGURATION REGISTER 1 – OFFSET D0h 51
6.3.86 XPIP CONFIGURATION REGISTER 2 – OFFSET D4h 51
6.3.87 CAPABILITY ID REGISTER – OFFSET D8h 51
6.3.88 NEXT POINTER REGISTER – OFFSET D8h 52
6.3.89 VPD REGISTER – OFFSET D8h 52
6.3.90 VPD DATA REGISTER – OFFSET DCh 52
6.3.91 EXTENDED CONFIGURATION ACCESS ADDRESS REGISTER – OFFSET E0h 52
6.3.92 EXTENDED CONFIGURATION ACCESS DATA REGISTER – OFFSET E4h 52
6.3.93 RESERVED REGISTERS – OFFSET E8h – ECh 52
6.3.94 MESSAGE SIGNALED INTERRUPTS ID REGISTER – F0h 52
6.3.95 NEXT CAPABILITIES POINTER REGISTER – F0h 53
6.3.96 MESSAGE CONTROL REGISTER – OFFSET F0h 53
6.3.97 MESSAGE ADDRESS REGISTER – OFFSET F4h 53
6.3.98 MESSAGE UPPER ADDRESS REGISTER – OFFSET F8h 53
6.3.99 MESSAGE DATA REGISTER – OFFSET FCh 53
6.3.100 ADVANCE ERROR REPORTING CAPABILITY ID REGISTER – OFFSET 100h 53
6.3.101 ADVANCE ERROR REPORTING CAPABILITY VERSION REGISTER – OFFSET 100h 54
6.3.102 NEXT CAPABILITY OFFSET REGISTER – OFFSET 100h 54
6.3.103 UNCORRECTABLE ERROR STATUS REGISTER – OFFSET 104h 54
6.3.104 UNCORRECTABLE ERROR MASK REGISTER – OFFSET 108h 54
6.3.105 UNCORRECTABLE ERROR SEVERITY REGISTER – OFFSET 10Ch 54
6.3.106 CORRECTABLE ERROR STATUS REGISTER – OFFSET 110h 55
6.3.107 CORRECTABLE ERROR MASK REGISTER – OFFSET 114h 55
6.3.108 ADVANCED ERROR CAPABILITIES AND CONTROL REGISTER – OFFSET 118h 55
6.3.109 HEADER LOG REGISTER 1 – OFFSET 11Ch 56
6.3.110 HEADER LOG REGISTER 2 – OFFSET 120h 56
6.3.111 HEADER LOG REGISTER 3 – OFFSET 124h 56
6.3.112 HEADER LOG REGISTER 4 – OFFSET 128h 56
6.3.113 SECONDARY UNCORRECTABLE ERROR STATUS REGISTER – OFFSET 12Ch 56
6.3.114 SECONDARY UNCORRECTABLE ERROR MASK REGISTER – OFFSET 130h 57
6.3.115 SECONDARY UNCORRECTABLE ERROR SEVERITY REGISTER – OFFSET 134h 57
6.3.116 SECONDARY ERROR CAPABILITY AND CONTROL REGISTER – OFFSET 138h 58
6.3.117 SECONDARY HEADER LOG REGISTER – OFFSET 13Ch – 148h 58
6.3.118 RESERVED REGISTER – OFFSET 14Ch 58
6.3.119 VC CAPABILITY ID REGISTER – OFFSET 150h 58
6.3.120 VC CAPABILITY VERSION REGISTER – OFFSET 150h 58
6.3.121 NEXT CAPABILITY OFFSET REGISTER – OFFSET 150h 58
6.3.122 PORT VC CAPABILITY REGISTER 1 – OFFSET 154h 58

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6.3.123 PORT VC CAPABILITY REGISTER 2 – OFFSET 158h 59
6.3.124 PORT VC CONTROL REGISTER – OFFSET 15Ch 59
6.3.125 PORT VC STATUS REGISTER – OFFSET 15Ch 59
6.3.126 VC0 RESOURCE CAPABILITY REGISTER – OFFSET 160h 59
6.3.127 VC0 RESOURCE CONTROL REGISTER – OFFSET 164h 59
6.3.128 VC0 RESOURCE STATUS REGISTER – OFFSET 168h 59
6.3.129 RESERVED REGISTERS – OFFSET 16Ch – 2FCh 60
6.3.130 EXTENDED GPIO DATA AND CONTROL REGISTER – OFFSET 300h 60
6.3.131 EXTENDED GPI/GPO DATA AND CONTROL REGISTER – OFFSET 304h 60
6.3.132 RESERVED REGISTERS – OFFSET 308h – 30Ch 60
6.3.133 REPLAY AND ACKNOWLEDGE LATENCY TIMERS – OFFSET 310h 60
6.3.134 RESERVED REGISTERS – OFFSET 314h – FFCh 60

7 GPIO PINS AND SM BUS ADDRESS 61

8 CLOCK SCHEME 62

9 INTERRUPTS 66

10 EEPROM (I2C) INTERFACE AND SYSTEM MANAGEMENT BUS 67

10.1 EEPROM (I2C) INTERFACE 67
10.2 SYSTEM MANAGEMENT BUS 67
10.3 EEPROM AUTOLOAD CONFIGURATION 67

11 RESET SCHEME 69

12 IEEE 1149.1 COMPATIBLE JTAG CONTROLLER 70

12.1 INSTRUCTION REGISTER 70
12.2 BYPASS REGISTER 70
12.3 DEVICE ID REGISTER 70
12.4 BOUNDARY SCAN REGISTER 71
12.5 JTAG BOUNDARY SCAN REGISTER ORDER 71

13 POWER MANAGEMENT 72

14 POWER SEQUENCING 73

14.1 INITIAL POWER-UP (G3 TO L0) 74
14.2 POWER-OFF SEQUENCE 75

15 ELECTRICAL AND TIMING SPECIFICATIONS 76

15.1 ABSOLUTE MAXIMUM RATINGS 76
15.2 DC SPECIFICATIONS 76
15.3 AC SPECIFICATIONS 77
15.4 OPERATING AMBIENT TEMPERATURE 78

16 PACKAGE INFORMATION 79

17 ORDERING INFORMATION 80

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TABLE OF FIGURES

FIGURE 1-1 PI7C9X113SL TOPOLOGY 10
FIGURE 4-1 FORWARD BRIDGE MODE 19
FIGURE 8-1 TOPOLOGY OF INTERNAL CLOCK GENERATOR AND INTERNAL CLOCK BUFFERING – INTERNAL FEEDBACK MODE 63
FIGURE 8-2 TOPOLOGY OF INTERNAL CLOCK GENERATOR AND INTERNAL CLOCK BUFFERING – EXTERNAL FEEDBACK MODE 63
FIGURE 8-3 TOPOLOGY OF EXTERNAL CLOCK GENERATOR AND INTERNAL CLOCK BUFFERING – INTERNAL FEEDBACK MODE 64
FIGURE 8-4 TOPOLOGY OF EXTERNAL CLOCK GENERATOR AND INTERNAL CLOCK BUFFERING – EXTERNAL FEEDBACK MODE 64
FIGURE 8-5 TOPOLOGY OF EXTERNAL CLOCK GENERATOR AND EXTERNAL CLOCK BUFFERING 65
FIGURE 14-1 TIMING SEQUENCE WITH UNDETERMINED I/O STATE 73
FIGURE 14-2 RECOMMENDED POWER SEQUENCE 73
FIGURE 14-3 INITIAL POWER-UP 74
FIGURE 15-1 PCI SIGNAL TIMING CONDITIONS 77
FIGURE 16-1 PACKAGE OUTLINE DRAWING 79
FIGURE 16-2 PART MARKING 79

LIST OF TABLES

TABLE 2-1 PIN ASSIGNMENTS 16
TABLE 3-1 MODE SELECTION 17
TABLE 3-2 PIN STRAPPING FOR CLOCK POWER MANAGEMENT 17
TABLE 5-1 TLP FORMAT 20
TABLE 6-1 CONFIGURATION REGISTER MAP (00H – FFH) 21
TABLE 6-2 PCI EXPRESS EXTENDED CAPABILITY REGISTER MAP (100H – FFFH) 24
TABLE 7-1 SM BUS DEVICE ID STRAPPING 61
TABLE 8-1 FREQUENCY OF PCI CLKOUT WITH INTERNAL CLOCK SOURCE: 62
TABLE 9-1 PCI INTERRUPT TO PCIE INTERRUPT MESSAGE MAPPING IN FORWARD BRIDGE MODE 66
TABLE 12-1 INSTRUCTION REGISTER CODES 70
TABLE 12-2 JTAG DEVICE ID REGISTER 70
TABLE 14-1 POWER SEQUENCING AND RESET SIGNAL TIMINGS 74
TABLE 15-1 ABSOLUTE MAXIMUM RATINGS 76
TABLE 15-2 DC ELECTRICAL CHARACTERISTICS 76
TABLE 15-3 PCI BUS TIMING PARAMETERS 77
TABLE 15-4 PCI EXPRESS INTERFACE - DIFFERENTIAL TRANSMITTER (TX) OUTPUT CHARACTERISTICS 77
TABLE 15-5 PCI EXPRESS INTERFACE - DIFFERENTIAL RECEIVER (RX) INPUT CHARACTERISTICS 78
TABLE 15-6 OPERATING AMBIENT TEMPERATURE 78

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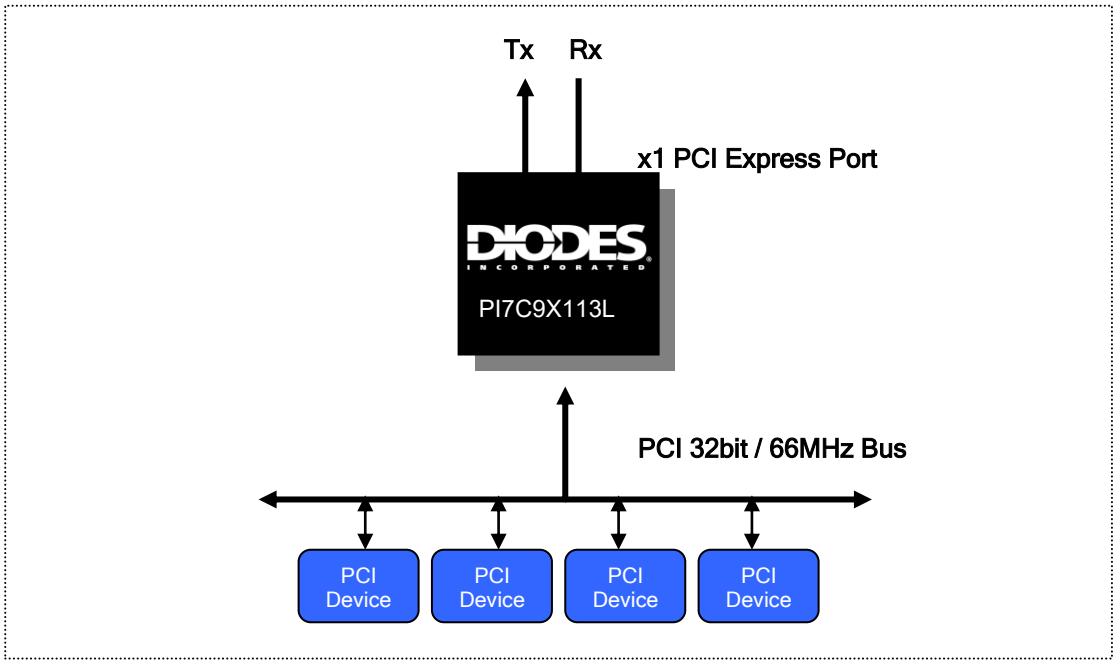
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1 INTRODUCTION

PI7C9X113SL is a PCIe-to-PCI/PCI-X bridge. PI7C9X113SL is compliant with the *PCI Express Base Specification,* Revision 1.1, the *PCI Express Card Electromechanical Specification*, Revision 1.1, the *PCI Local Bus Specification,* Revision 3.0 and *PCI Express to PCI/PCI-X Bridge Specification*, Revision 1.0. PI7C9X113SL supports transparent mode operation and forward bridging. PI7C9X113SL has an x1 PCI Express upstream port and a 32-bit PCI downstream port. The 32-bit PCI downstream port is 66MHz capable (see Figure 1-1). PI7C9X113SL configuration registers are backward compatible with existing PCI bridge software and firmware. No modification of PCI bridge software and firmware is needed for the original operation.

Figure 1-1 PI7C9X113SL Topology



1.1 INDUSTRY SPECIFICATION COMPLIANCE

- Compliant with PCI Express Base Specification, Revision 1.1
- Compliant with PCI Express to PCI/PCI-X Bridge Specification, Revision 1.0
- Compliant with PCI Express Card Electromechanical Specification, Revision 1.1
- Compliant with PCI-to-PCI Bridge Architecture Specification, Revision 1.2
- Compliant with PCI Local Bus Specification, Revision 3.0
- Compliant with PCI SHPC and Subsystem Specification, Revision 1.0
- Compliant with PCI Mobile Design Guide, Version 1.1
- Compliant with PCI Bus PM Interface Specification, Revision 1.2
- Compliant with System Management (SM) Bus, Version 2.0
- Compliant with Advanced Configuration and Power Interface Specification (ACPI), Revision 2.0b

1.2 GENERAL FEATURES

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- Forward bridging (PCI Express as primary bus, PCI as secondary bus)
- x1 PCI Express interface (2.5Gb/s data rate)
- 32-bit PCI interface capable of 66MHz
- GPIO support (4 bi-directional pins). When external arbiter is used, 3 additional GPI (input) and GPO (output) pins
- Power Management (including ACPI, PCI_PM, CLKRUN_L and CLKREQ_L,)
- Transparent mode support
- Subtractive Decoding PCI-to-PCI bridge to support legacy device
- Masquerade support (user-defined vendor, device, revision, subsystem device, and subsystem vendor ID)
- EEPROM (I2C) Interface
- SM Bus Interface
- 10k byte buffer: 2K byte buffer for downstream memory read, 4K bytes for upstream memory read, and 2K byte buffer for memory write in both directions
- Auxiliary powers (VAUX, VDDAUX, VDDCAUX) support
- Power consumption less than 350 mW in typical condition
- Industrial temperature range (-40C to 85C)
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. “Green” Device (Note 3)
- For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative.
  https://www.diodes.com/quality/product-definitions/

1.3 PCI EXPRESS FEATURES

- Physical Layer interface (x1 link with 2.5Gb/s data rate)
- Virtual Isochronous support (upstream TC1-7 generation, downstream TC1-7 mapping)
- CRC (16-bit), LCRC (32-bit)
- ECRC and advanced error reporting
- Lane polarity toggle
- ASPM support
- WAKE_L support
- Maximum payload size to 512 bytes
- CLKREQ_L support to disable Refclk at L1 and L2 state

1.4 PCI FEATURES

- Provides two level arbitration support for four PCI Bus masters
- 3.3V PCI signaling with 5V I/O tolerance
- PME_L support
- LOCK support
- 16-bit address decode for VGA
- Subsystem Vendor and Subsystem Device IDs support
- PCI INT interrupt or MSI Function support
- Adaptive fragmentation support for memory write
- Internal clock generator for PCI bus
- CLKRUN_L support to stop the PCI clock

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated’s definitions of Halogen- and Antimony-free, "Green" and Lead-free.
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2 PIN DEFINITIONS

2.1 SIGNAL TYPES

TYPE OF SIGNAL	- DESCRIPTIONS
B	**Bi-directional**
I	**Input**
IU	**Input with pull-up**
ID	**Input with pull-down**
IOD	**Bi-directional with open drain output**
OD	**Open drain output**
O	**Output**
P	**Power**
G	**Ground**

"_L" in signal name indicates Active LOW signal

2.2 PCI EXPRESS SIGNALS

NAME	PIN ASSIGNMENT	TYPE	DESCRIPTION
REFCLKP REFCLKN	13, 12	I	**Reference Clock Inputs:** Connect to external 100MHz differential clock. These signals require AC coupled with 0.1uF capacitors.
RP RN	21, 20	I	**PCI Express Data Inputs:** Differential data receiver input signals
TP TN	17, 16	O	**PCI Express Data Outputs:** Differential data transmitter output signals
PERST_L	29	I	**PCI Express Fundamental Reset (Active LOW):** PI7C9X113SL The device uses this signal reset to initialize the internal state machines.

2.3 PCI SIGNALS

NAME	PIN ASSIGNMENT	TYPE	DESCRIPTION
AD [31:0]	125, 126, 124, 121, 122, 120, 119, 117, 113, 111, 110, 109, 108, 106, 103, 104, 90, 88, 86, 85, 83, 80, 79, 78, 75, 74, 71, 70, 68, 69, 67, 64	B	**Address / Data:** Multiplexed address and data bus. Address phase is aligned with first clock of FRAME_L assertion. Data phase is aligned with IRDY_L or TRDY_L assertion. Data is transferred on rising edges of CLKOUT[0] when both IRDY_L and TRDY_L are asserted. During bus idle (both FRAME_L and IRDY_L are de-asserted), PI7C9X113SL drives AD to a valid logic level when arbiter is parking to PI7C9X113SL on PCI bus.
CBE_L[3:0]	116, 99, 89, 76	B	**Command / Byte Enables (Active LOW):** Multiplexed command at address phase and byte enable at data phase. During address phase, the initiator drives commands on CBE [3:0] signals to start the transaction. If the command is a write transaction, the initiator will drive the byte enables during data phase. Otherwise, the target will drive the byte enables during data phase. During bus idle, PI7C9X113SL drives CBE [3:0] signals to a valid logic level when arbiter is parking to PI7C9X113SL on PCI bus.
PAR	94	B	**Parity Bit:** Parity bit is an even parity (i.e. even number of 1's), which generates based on the values of AD [31:0], CBE [3:0]. If PI7C9X113SL is an initiator with a write transaction, PI7C9X113SL will tri-state PAR. If PI7C9X113SL is a target and a write transaction, PI7C9X113SL will drive PAR one clock after the address or data phase. If PI7C9X113SL is a target and a read transaction, PI7C9X113SL will drive PAR one clock after the address phase and tri-state PAR during data phases. PAR is tri-stated one cycle after the AD lines are tri-stated. During bus idle, PI7C9X113SL drives PAR to a valid logic level when arbiter is parking to PI7C9X113SL on PCI bus.
FRAME_L	63	B	**FRAME (Active LOW):** Driven by the initiator of a transaction to indicate the beginning and duration an access. The de-assertion of FRAME_L indicates the final data phase signaled by the initiator in burst transfers. Before being tri-stated, it is driven to a de-asserted state for one cycle.
IRDY_L	97	B	**IRDY (Active LOW):** Driven by the initiator of a transaction to indicate its ability to complete current data phase on the primary side. Once asserted in a data phase, it is not de-asserted until the end of the data phase. Before tri-stated, it is driven to a de-asserted state for one cycle.

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NAME	PIN ASSIGNMENT	TYPE	DESCRIPTION
TRDY_L	100	B	**TRDY (Active LOW):** Driven by the target of a transaction to indicate its ability to complete current data phase on the primary side. Once asserted in a data phase, it is not de-asserted until the end of the data phase. Before tri-stated, it is driven to a de-asserted state for one cycle.
DEVSEL_L	98	B	**Device Select (Active LOW):** Asserted by the target indicating that the device is accepting the transaction. As a master, PI7C9X113SL waits for the assertion of this signal within 5 cycles of FRAME_L assertion; otherwise, terminate with master abort. Before tri-stated, it is driven to a de-asserted state for one cycle.
STOP_L	96	B	**STOP (Active LOW):** Asserted by the target indicating that the target is requesting the initiator to stop the current transaction. Before tri-stated, it is driven to a de-asserted state for one cycle.
LOCK_L	93	B	**LOCK (Active LOW):** Asserted by the initiator for multiple transactions to complete. PI7C9X113SL does not support any upstream LOCK transaction.
PERR_L	92	B	**Parity Error (Active LOW):** Asserted when a data parity error is detected for data received on the PCI bus interface. Before being tri-stated, it is driven to a de-asserted state for one cycle.
SERR_L	61	IOD	**System Error (Active LOW):** Can be driven LOW by any device to indicate a system error condition. If SERR control is enabled, PI7C9X113SL will drive this pin on: ▪ Address parity error ▪ Posted write data parity error on target bus ▪ Master abort during posted write transaction ▪ Target abort during posted write transaction ▪ Posted write transaction discarded ▪ Delayed write request discarded ▪ Delayed read request discarded ▪ Delayed transaction master timeout ▪ Errors reported from PCI Express port (advanced error reporting) in transparent mode. This signal is an open drain buffer that requires an external pull-up resistor for proper operation.
REQ_L [3:0]	33, 34, 32, 31	I	**Request (Active LOW):** REQ_L's are asserted by bus master devices to request for transactions on the PCI bus. The master devices de-assert REQ_Ls for at least 2 PCI clock cycles before asserting them again. If external arbiter is selected, REQ_L [0] will be the bus grant input to PI7C9X113SL. Also, REQ_L [3:1] will become the GPI [2:0]. When powered up, if both REQ_L[2] and REQ_L[3] and pulled low (Active LOW) and stay low in normal operation, the PI7C9X113SL will change the function of CLKOUT[3] to CLKRUN_L and CLKOUT[2] to CLKREQ_L, respectively.
GNT_L [3:0]	41, 39, 40, 37	O	**Grant (Active LOW):** PI7C9X113SL asserts GNT_Ls to release PCI bus control to bus master devices. During idle and all GNT_Ls are de-asserted and arbiter is parking to PI7C9X113SL, PI7C9X113SL will drive AD, CBE, and PAR to valid logic levels. If external arbiter is selected, GNT_L [0] will be the bus request from PI7C9X113SL to external arbiter. Also, GNT_L [3:1] will become the GPO [2:0].
CLKOUT [3:0]	49, 54, 56, 59	B	**PCI Clock Outputs:** PCI clock outputs are derived from the CLKIN and provide clocking signals to external PCI Devices. In external feedback mode, CLKOUT[0] becomes an input for feedback clock and CLKOUT[1:3] remain as clock outputs to provide clock signals to external PCI Devices. Please see Chapter 8 for further information.
M66EN	102	I	**66MHz Enable:** This input is used to specify if Bridge is capable of running at 66MHz. For 66MHz operation on the PCI bus, this signal should be pulled "HIGH". For 33MHz operation on the PCI bus, this signal should be pulled LOW.
RESET_L	46	O	**RESET_L (Active LOW):** When RESET_L active, all PCI signals should be asynchronously tri-stated.
INTA_L INTB_L INTC_L INTD_L	36, 43, 57, 60	I	**Interrupt:** Signals are asserted to request an interrupt. After asserted, it can be cleared by the device driver. INTA_L, INTB_L, INTC_L, INTD_L signals are inputs and asynchronous to the clock in the forward mode.
CLKIN	44	I	**PCI Clock Input:** PCI Clock Input Signal connects to an external clock source. The PCI Clock Outputs CLKOUT [3:0] pins are derived from CLKIN Input.

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2.4 MODE SELECT AND STRAPPING SIGNALS

NAME	PIN ASSIGNMENT	TYPE	DESCRIPTION
TM0	128	ID	**Mode Select 0:** Mode Selection Pin to select EEPROM or SM Bus. TM0=0 for EEPROM (I2C) support and TM0=1 for SM Bus support. TM0 is a strapping pin. See Table 3-1 mode selection and Table 3-2 for strapping control.
TM1	23	ID	**Mode Select 1:** Mode Selection Pin for normal operation. Set TM1=0 for normal operation. TM1=1 is reserved. TM1 is a strapping pin. See Table 3-1 mode selection and Table 3-2 for strapping control.

2.5 JTAG BOUNDARY SCAN SIGNALS

NAME	PIN ASSIGNMENT	TYPE	DESCRIPTION
TCK	26	IU	**Test Clock:** TCK is the test clock to synchronize the state information and data on the PCI bus side of PI7C9X113SL during boundary scan operation. At normal operation mode, this pin should be left open(NC).
TMS	24	IU	**Test Mode Select:** TMS controls the state of the Test Access Port (TAP) controller. At normal operation mode, this pin should be pulled low through a 1K-Ohm pull-down resistor.
TDO	27	O	**Test Data Output:** TDO is the test data output and connects to the end of the JTAG scan chain. At normal operation mode, this pin should be left open(NC).
TDI	28	IU	**Test Data Input:** TDI is the test data input and connects to the beginning of the JTAG scan chain. It allows the test instructions and data to be serially shifted into the PCI side of PI7C9X113SL. At normal operation mode, this pin should be left open(NC).

2.6 MISCELLANEOUS SIGNALS

NAME	PIN ASSIGNMENT	TYPE	DESCRIPTION
GPIO [3:0]	47, 48, 51, 52	B	**General Purpose I/O Data Pins:** The 4 general-purpose signals are programmable as either input-only or bi-directional signals by writing the GPIO output enable control register in the configuration space.
SMBCLK / SCL	3	B	**SMBUS / EEPROM Clock Pin:** When EEPROM (I2C) interface is selected (TM0=0), this pin is an output of SCL clock and connected to EEPROM clock input. When SMBUS interface is selected (TM0=1), this pin is an input for the clock of SMBUS.
SMBDATA / SDA	5	B/IOD	**SMBUS / EEPROM Data Pin:** Data Interface Pin to EERPOM or SMBUS. When EEPROM (I2C) interface is selected (TM0=0), this pin is a bi-directional signal. When SMBUS interface is selected (TM0=1), this pin is an open drain signal.
PME_L	1	I	**Power Management Event Pin:** Power Management Event Signal is asserted to request a change in the device or link power state.
WAKE_L	4	O	**Wakeup Signal (Active LOW):** This signal is asserted when PME_L pin is asserted and the link is in the L2 state
REXTP, REXTN	8, 9	I	**External Precision Resistor:** Connect an external resistor (1.43K Ohm +/- 1%) to provide a reference to both the bias currents and impedance calibration circuitry.

2.7 POWER AND GROUND PINS

NAME	PIN ASSIGNMENT	TYPE	DESCRIPTION
VDDA	15, 18	P	**Analog Voltage Supply for PCI Express Interface:** Connect to the 1.1V-1.2V Power Supply.
VDDA33	10		**High Voltage Supply for PCI Express Interface:** Connect to the 3.3V Power Supply.
VDDC	30, 35, 45, 53, 62, 73, 81, 95, 105, 114, 127	P	**Core Supply Voltage:** Connect to the 1.1V-1.2V Power Supply.
VDDCAUX	7	P	**Auxiliary Core Supply Voltage:** Connect to the 1.1V-1.2V Power Supply.
VD33	25, 38, 50, 55, 58, 66 72, 77, 82, 87, 91, 101, 107, 112, 118, 123	P	**I/O Supply Voltage for PCI Interface:** Connect to the 3.3V Power Supply for PCI I/O Buffers.

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NAME	PIN ASSIGNMENT	TYPE	DESCRIPTION
VAUX	2	P	**Auxiliary I/O Supply Voltage for PCI interface:** Connect to the 3.3V Power Supply.
VSS	6, 11, 14, 19, 22, 42, 65, 84, 115, 129	P	**Ground:** Connect to Ground.

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2.8 PIN ASSIGNMENTS

Table 2-1 Pin Assignments

PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME
1	PME_L	34	REQ_L[2]	67	AD[1]	100	TRDY_L
2	VAUX	35	VDDC	68	AD[3]	101	VD33
3	SMBCLK / SCL	36	INTA_L	69	AD[2]	102	M66EN
4	WAKE_L	37	GNT_L[0]	70	AD[4]	103	AD[17]
5	SMBDAT / SDA	38	VD33	71	AD[5]	104	AD[16]
6	VSS	39	GNT_L[2]	72	VD33	105	VDDC
7	VDDCAUX	40	GNT_L[1]	73	VDDC	106	AD[18]
8	REXTP	41	GNT_L[3]	74	AD[6]	107	VD33
9	REXTN	42	VSS	75	AD[7]	108	AD[19]
10	VDDA33	43	INTB_L	76	CBE[0]	109	AD[20]
11	VSS	44	CLKIN	77	VD33	110	AD[21]
12	REFCLKN	45	VDDC	78	AD[8]	111	AD[22]
13	REFCLKP	46	RESET_L	79	AD[9]	112	VD33
14	VSS	47	GPIO[3]	80	AD[10]	113	AD[23]
15	VDDA	48	GPIO[2]	81	VDDC	114	VDDC
16	TN	49	CLKOUT[3]	82	VD33	115	VSS
17	TP	50	VD33	83	AD[11]	116	CBE[3]
18	VDDA	51	GPIO[1]	84	VSS	117	AD[24]
19	VSS	52	GPIO[0]	85	AD[12]	118	VD33
20	RN	53	VDDC	86	AD[13]	119	AD[25]
21	RP	54	CLKOUT[2]	87	VD33	120	AD[26]
22	VSS	55	VD33	88	AD[14]	121	AD[28]
23	TM1	56	CLKOUT[1]	89	CBE[1]	122	AD[27]
24	TMS	57	INTC_L	90	AD[15]	123	VD33
25	VD33	58	VD33	91	VD33	124	AD[29]
26	TCK	59	CLKOUT[0]	92	PERR_L	125	AD[31]
27	TDO	60	INTD_L	93	LOCK_L	126	AD[30]
28	TDI	61	SERR_L	94	PAR	127	VDDC
29	PERST_L	62	VDDC	95	VDDC	128	TM0
30	VDDC	63	FRAME_L	96	STOP_L	129	E_PAD
31	REQ_L[0]	64	AD[0]	97	IRDY_L		
32	REQ_L[1]	65	VSS	98	DEVSEL_L		
33	REQ_L[3]	66	VD33	99	CBE[2]		

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3 MODE SELECTION AND PIN STRAPPING

3.1 FUNCTIONAL MODE SELECTION

PI7C9X113SL uses TM1 and TM0 pins to select different modes of operations. These input signals are required to be stable during normal operation. One of the four combinations of normal operation can be selected by setting the logic values for the three mode select pins. For example, if the logic values are low for both two (TM1 and TM0) pins, the normal operation will have EEPROM (I2C) support with internal arbiter. The designated operation with respect to the values of the TM1 and TM0 pins are defined on Table 3-1:

Table 3-1 Mode Selection

TM1 Strapped	TM0 Strapped	Functional Mode
0	0	EEPROM (I2C) support
0	1	SM Bus support

3.2 PIN STRAPPING

If TM1 is strapped to low, PI7C9X113SL uses REQ_L[3:2] as the strapping pins at the PCIe PERST_L de-assertion to enable Clock Power Management feature.

Table 3-2 Pin Strapping for Clock Power Management

TM1 Strapped	REQ_L[3:2] Strapped	Test Functions
0	2'b0	Clock Power Management is enabled, only two PCI devices supported. CLKOUT[2] is used as CLKREQ_L CLKOUT[3] is used as CLKRUN_L

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4 TRANSPARENT AND FORWARD BRIDGING

4.1 TRANSPARENT MODE

In transparent bridge mode, base class code of PI7C9X113SL is set to be 06h (bridge device). The sub-class code is set to be 04h (PCI-to-PCI bridge). Programming interface is set to either 00h or 01h. If this interface is set to 00h, subtractive decoding is not supported. If it is set to 01h, legacy support is enabled and subtractive decoding is supported.

When Subtractive Decoding PCI-to-PCI bridge is enabled by setting the legacy bit (bit 0 of offset 98h), all cycles (Memory/IO) are forwarded to downstream PCI devices. However, the Type-1 configuration cycle still should be checked for the bus number in order to be forwarded to PCI bus. The PCI-X/PCIe capability is not included in the Capability List and all PCI-X/PCIe capability registers and Extended Configuration registers are treated as reserved registers. As a result, all Write accesses are completed normally but data is discarded, and all Read accesses are returned with data value of 0.

When PCI bus Subtractive Decoding Enable bit (bit 1 of 98h) is set, the device performs subtractive decode at PCI bus when the cycle is outside the range (negative decoding is used).

PI7C9X113SL has type-1 configuration header. These configuration registers are the same as traditional transparent PCI-to-PCI Bridge. In fact, it is backward compatible to the software that supporting traditional transparent PCI-to-PCI bridges. Configuration registers can be accessed from several different ways. For PCI Express access, PCI Express configuration transaction is in forward bridge mode. For I2C access, I2C bus protocol is used with EEPROM selected (TM0=0). For SM bus access, SM bus protocol is used with SM bus selected (TM0=1).

4.2 FORWARD BRDIGE

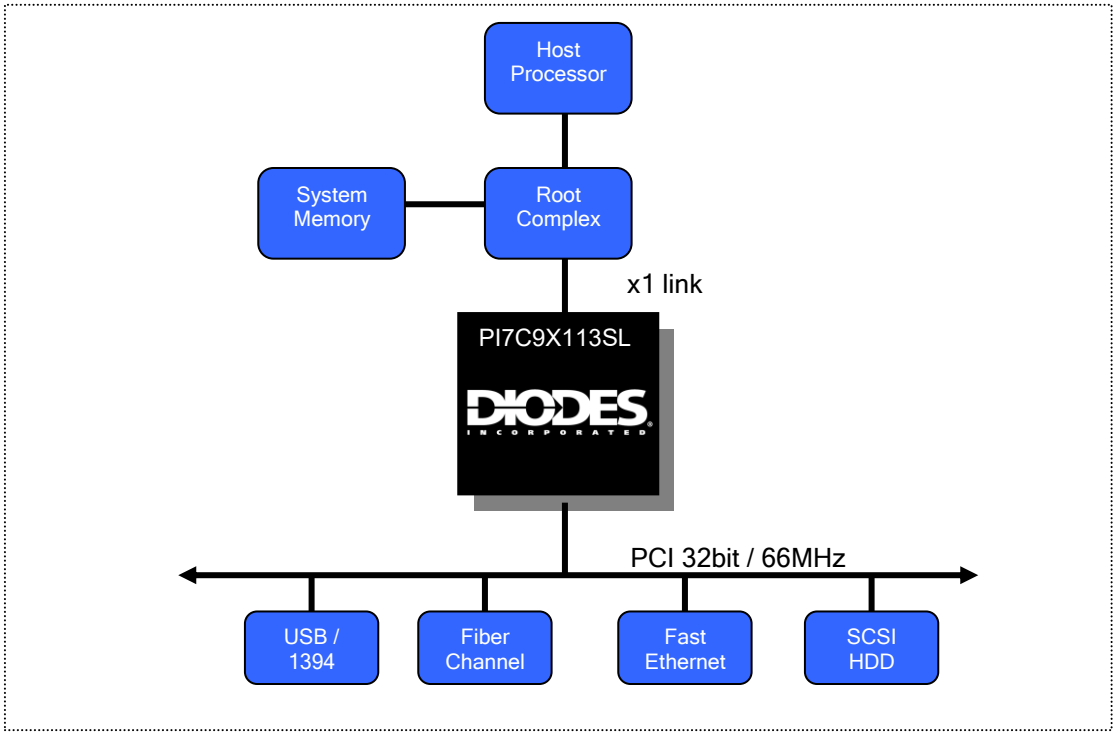
PI7C9X113SL supports forward mode of bridging. In forward bridging mode, its PCI Express interface is connected to a root complex and its PCI bus interface is connected to PCI devices.

PCI based systems and peripherals are ubiquitous in the I/O interconnect technology market today. It will be a tremendous effort to convert existing PCI based products to be used in PCI Express systems. PI7C9X113SL provides a solution to bridge existing PCI based products to the latest PCI Express technology.

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Figure 4-1 Forward Bridge Mode



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5 PCI EXPRESS FUNCTIONAL OVERVIEW

5.1 TLP STRUCTURE

PCI Express TLP (Transaction Layer Packet) Structure is comprised of format, type, traffic class, attributes, TLP digest, TLP poison, and length of data payload.

There are four TLP formats defined in PI7C9X113SL based on the states of FMT [1] and FMT [0] as shown on Table 5-1 .

Table 5-1 TLP Format

FMT [1]	FMT [0]	TLP Format
0	0	3 double word, without data
0	1	4 double word, without data
1	0	3 double word, with data
1	1	4 double word, with data

Data payload of PI7C9X113SL can range from 4 (1DW) to 512 (128DW) bytes. PI7C9X113SL supports three TLP routing mechanisms. They are comprised of Address, ID, and Implicit routings. Address routing is being used for Memory and IO requests. ID based (bus, device, function numbers) routing is being used for configuration requests. Implicit routing is being used for message routing. There are two message groups (baseline and advanced switching). The baseline message group contains INTx interrupt signaling, power management, error signaling, locked transaction support, slot power limit support, vendor defined messages, hot-plug signaling. The other is advanced switching support message group. The advanced switching support message contains data packet and signal packet messages. Advanced switching is beyond the scope of PI7C9X113SL implementation.

The r [2:0] values of the "type" field will determine the destination of the message to be routed. All baseline messages must use the default traffic class zero (TC0).

5.2 VIRTUAL ISOCHRONOUS OPERATION

This section provides a summary of Virtual Isochronous Operation supported by PI7C9X113SL. Virtual Isochronous support is disabled by default. Virtual Isochronous feature can be turned on with setting bit [26] of offset 40h to one. Control bits are designated for selecting which traffic class (TC1-7) to be used for upstream (PCI -to-PCI Express). PI7C9X113SL accepts only TC0 packets of configuration, IO, and message packets for downstream (PCI Express-to-PCI). If configuration, IO and message packets have traffic class other than TC0, PI7C9X113SL will treat them as malformed packets. PI7C9X113SL maps all downstream memory packets from PCI Express to PCI transactions regardless the virtual Isochronous operation is enabled or not.

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6 CONFIGURATION REGISTER ACCESS

PI7C9X113SL supports Type-0 and Type-1 configuration space headers and Capability ID of 01h (PCI power management) to 10h (PCI Express capability structure).

PI7C9X113SL supports PCI Express capabilities register structure with capability version set to 1h (bit [3:0] of offset 02h).

6.1 CONFIGURATION REGISTER MAP

PI7C9X113SL supports capability pointer with PCI power management (ID=01h), PCI bridge sub-system vendor ID (ID=0Dh), PCI Express (ID=10h), and message signaled interrupt (ID=05h).

Table 6-1 Configuration Register Map (00h – FFh)

Primary Bus Configuration Access or Secondary Bus Configuration Access	PCI Configuration Register Name (type1)	EEPROM (I2C) Access	SM Bus Access
01h - 00h	Vendor ID	Yes1	Yes2
03h – 02h	Device ID	Yes1	Yes2
05h – 04h	Command Register	Yes	Yes
07h – 06h	Primary Status Register	Yes	Yes
0Bh – 08h	Class Code and Revision ID	Yes1	Yes2
0Ch	Cacheline Size Register	Yes	Yes
0Dh	Primary Latency Timer	Yes	Yes
0Eh	Header Type Register	Yes	Yes
0Fh	Reserved	-	-
17h – 10h	Reserved	-	-
18h	Primary Bus Number Register	Yes	Yes
19h	Secondary Bus Number Register	Yes	Yes
1Ah	Subordinate Bus Number Register	Yes	Yes
1Bh	Secondary Latency Timer	Yes	Yes
1Ch	I/O Base Register	Yes	Yes
1Dh	I/O Limit Register	Yes	Yes
1Fh – 1Eh	Secondary Status Register	Yes	Yes
21h – 20h	Memory Base Register	Yes	Yes
23h – 22h	Memory Limit Register	Yes	Yes
25h – 24h	Prefetchable Memory Base Register	Yes	Yes
27h – 26h	Prefetchable Memory Limit Register	Yes	Yes
2Bh – 28h	Prefetchable Memory Base Upper 32-bit Register	Yes	Yes
2Dh – 2Ch	Prefetchable Memory Limit Upper 32-bit Register	Yes	Yes
2Fh – 2Eh	Prefetchable Memory Limit Upper 32-bit Register	Yes	Yes
31h – 30h	I/O Base Upper 16-bit	Yes	Yes

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Primary Bus Configuration Access or Secondary Bus Configuration Access	PCI Configuration Register Name (type1)	EEPROM (I2C) Access	SM Bus Access
	Register		
33h – 32h	I/O Limit Upper 16-bit Register	Yes	Yes
34h	Capability Pointer	Yes	Yes
37h – 35h	Reserved	No	Yes
3Bh – 38h	Reserved	No	Yes
3Ch	Interrupt Line	Yes	Yes
3Dh	Interrupt Pin	Yes	Yes
3Fh – 3Eh	Bridge Control	Yes	Yes
41h – 40h	PCI Data Prefetching Control	Yes	Yes
43h – 42h	Chip Control 0	Yes	Yes
47h – 44h	Reserved	-	-
4Bh – 48h	Arbiter Mode, Enable, Priority	-	-
4Fh – 4Ch	Reserved	-	-
53h – 50h	Memory Readsmart Base Lower 32-Bit Register 1	Yes	Yes
57h – 54h	Memory Readsmart Base Upper 32-Bit Register 1	Yes	Yes
5Bh – 58h	Memory Readsmart Range Control Register 1	Yes	Yes
5Fh – 5Ch	Memory Readsmart Memory Base Lower 32-Bit Register 2	Yes	Yes
63h – 60h	Memory Readsmart Base Upper 32-Bit Register 2	Yes	Yes
67h – 64h	Memory Readsmart Range Size Register 2	Yes	Yes
6Ah – 68h	Reserved	Yes	Yes
6Bh	Upstream Memory Read/Write Control	Yes	Yes
6Fh – 6Ch	PHY TX/RX Control	Yes	Yes
73h – 70h	EEPROM (I2C) Control and Status Register	No	Yes
77h – 74h	Reserved	-	-
7Bh – 78h	GPIO Data and Control	Yes	Yes
7Ch – 7Ch	Reserved	-	-
83h – 80h	PCI-X Capability	Yes	Yes
87h – 84h	PCI-X Bridge Status	Yes	Yes
8Bh – 88h	Upstream Split Transaction	Yes	Yes
8Fh – 8Ch	Downstream Split Transaction	Yes	Yes
93h – 90h	Power Management Capability	Yes	Yes
97h – 94h	Power Management Control and Status	Yes	Yes
98h	Subtractive Decoding PCI-to-PCI Bridge Enable	Yes	Yes
9Bh – 99h	Reserved	-	-
9Fh – 9Ch	Reserved	-	-
A3h – A0h	Slot ID Capability	Yes	Yes

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Primary Bus Configuration Access or Secondary Bus Configuration Access	PCI Configuration Register Name (type1)	EEPROM (I2C) Access	SM Bus Access
A5h – A4h	Secondary Clock and CLKRUN Control	Yes	Yes
A6h	XPIP Configuration Register 3		
A7h	Reserved	Yes	Yes
A9h – A8h	Subsystem ID and Subsystem Vendor ID Capability	Yes	Yes
ABh – AAh	Reserved		
AFh – ACh	Subsystem ID and Subsystem Vendor ID	Yes	Yes
B3h – B0h	PCI Express Capability	Yes	Yes
B7h – B4h	Device Capability	Yes	Yes
BBh – B8h	Device Control and Status	Yes	Yes
BFh – BCh	Link Capability	Yes	Yes
C3h – C0h	Link Control and Status	Yes	Yes
CBh – C4h	Reserved	-	-
CFh – CCh	XPIP Configuration Register 0	Yes	Yes
D3h – D0h	XPIP Configuration Register 1	Yes	Yes
D6h – D4h	XPIP Configuration Register 2	Yes	Yes
D7h	Reserved	-	-
DBh – D8h	VPD Capability Register	Yes	Yes
DFh – DCh	VPD Data Register	Yes3	Yes
E3h – E0h	Extended Config Access Address	Yes	Yes
E7h – E4h	Extended Config Access Data	Yes	Yes
EBh – E8h	Reserved	-	-
EFh – ECh	Reserved	-	-
F3h – F0h	MSI Capability Register	Yes	Yes
F7h – F4h	Message Address	Yes	Yes
FBh – F8h	Message Upper Address	Yes	Yes
FFh – FCh	Message Data	Yes	Yes

Note 1: When masquerade is enabled, it is pre-loadable.
Note 2: Read access only.
Note 3: The VPD data is read/write through I2C during VPD operation.

6.2 PCI EXPRESS EXTENDED CAPABILITY REGISTER MAP

PI7C9X113SL also supports PCI Express Extended Capabilities with from 257-byte to 4096-byte space. The offset range is from 100h to FFFh. The offset 100h is defined for Advance Error Reporting (ID=0001h). The offset 150h is defined for Virtual Channel (ID=0002h).

When Subtractive Decoding PCI-to-PCI bridge is enabled, the PCI-X/PCIe capability is not included in the Capability List and all PCI-X/PCIe capability registers and Extended Configuration registers are treated as reserved registers.

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Table 6-2 PCI Express Extended Capability Register Map (100h – FFFh)

Primary Bus Configuration Access or Secondary Bus Configuration Access	Transparent Mode (type1)	EEPROM (I2C) Access	SM Bus Access
103h – 100h	Advanced Error Reporting (AER) Capability	Yes	Yes2
107h – 104h	Uncorrectable Error Status	No	Yes
10Bh – 108h	Uncorrectable Error Mask	Yes	Yes
10Fh – 10Ch	Uncorrectable Severity	No	Yes
113h – 110h	Correctable Error Status	No	Yes
117h – 114h	Correctable Error Mask	No	Yes
11Bh – 118h	AER Capabilities and Control	No	Yes
12Bh – 11Ch	Header Log Registers	No	Yes
12Fh – 12Ch	Secondary Uncorrectable Error Status	No	Yes
133h – 130h	Secondary Uncorrectable Error Mask	No	Yes
137h – 134h	Secondary Uncorrectable Severity	No	Yes
13Bh – 138h	Secondary AER Capability and Control	No	Yes
14Bh – 13Ch	Secondary Header Log Register	No	Yes
14Fh – 14Ch	Reserved	No	Yes
153h – 150h	VC Capability	No	Yes
157h – 154h	Port VC Capability 1	No	Yes
15Bh – 158h	Port VC Capability 2	No	Yes
15Fh – 15Ch	Port VC Status and Control	No	Yes
163h – 160h	VC0 Resource Capability	No	Yes
167h – 164h	VC0 Resource Control	No	Yes
16Bh – 168h	VC0 Resource Status	No	Yes
2FFh – 16Ch	Reserved	No	No
303h – 300h	Extended GPIO Data and Control	No	Yes
307h – 304h	Extended GPI/GPO Data and Control	No	Yes
30Fh – 308h	Reserved	No	No
310h	Replay and Acknowledge Latency Timer	Yes	Yes
FFFh – 314h	Reserved	No	No

Note 5: Read access only.

6.3 PCI CONFIGURATION REGISTERS

The following section describes the configuration space when the device is in transparent mode. The descriptions for different register type are listed as follow:

Register Type	Descriptions
RO	Read Only
ROS	Read Only and Sticky

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Register Type	Descriptions
RW	Read/Write
RWC	Read/Write "1" to clear
RWS	Read/Write and Sticky
RWCS	Read/Write "1" to clear and Sticky

6.3.1 VENDOR ID – OFFSET 00h

BIT	FUNCTION	TYPE	DESCRIPTION
15:0	Vendor ID	RO	Identifies Pericom as the vendor of this device. Returns 12D8h when read.

6.3.2 DEVICE ID – OFFSET 00h

BIT	FUNCTION	TYPE	DESCRIPTION
31:16	Device ID	RO	Identifies this device as the PI7C9X113SL. Returns E113 when read.

6.3.3 COMMAND REGISTER – OFFSET 04h

BIT	FUNCTION	TYPE	DESCRIPTION
0	I/O Space Enable	RW	0: Ignore I/O transactions on the primary interface 1: Enable response to memory transactions on the primary interface Reset to 0
1	Memory Space Enable	RW	0: Ignore memory read transactions on the primary interface 1: Enable memory read transactions on the primary interface Reset to 0
2	Bus Master Enable	RW	0: Do not initiate memory or I/O transactions on the primary interface and disable response to memory and I/O transactions on the secondary interface 1: Enable the bridge to operate as a master on the primary interfaces for memory and I/O transactions forwarded from the secondary interface. Reset to 0
3	Special Cycle Enable	RO	0: PI7C9X113SL does not respond as a target to Special Cycle transactions, so this bit is defined as Read-Only and must return 0 when read Reset to 0
4	Memory Write and Invalidate Enable	RO	0: PI7C9X113SL does not originate a Memory Write and Invalidate transaction. Implements this bit as Read-Only and returns 0 when read (unless forwarding a transaction for another master). Reset to 0
5	VGA Palette Snoop Enable	RO	VGA Palette Snoop Enable is not supported. Reset to 0
6	Parity Error Response Enable	RW	0: May ignore any parity error that is detected and take its normal action 1: This bit if set, enables the setting of Master Data Parity Error bit in the Status Register when poisoned TLP received or parity error is detected and takes its normal action Reset to 0
7	Wait Cycle Control	RO	Wait Cycle Control is not supported. Reset to 0
8	SERR_L Enable Bit	RW	0: Disable 1: Enable PI7C9X113SL in forward bridge mode to report non-fatal or fatal error message to the Root Complex. Reset to 0
9	Fast Back-to-Back Enable	RO	Fast Back-to-back Enable is not supported Reset to 0

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BIT	FUNCTION	TYPE	DESCRIPTION
10	Interrupt Disable	RW	0: INTA_L can be asserted on PCI interface 1: Prevent INTA_L from being asserted on PCI interface Reset to 0
15:11	Reserved	RO	Reset to 00000

6.3.4 PRIMARY STATUS REGISTER – OFFSET 04h

BIT	FUNCTION	TYPE	DESCRIPTION
19:16	Reserved	RO	Reset to 0000
20	Capability List Capable	RO	0: PI7C9X113SL does not support the capability list 1: PI7C9X113SL supports the capability list (offset 34h in the pointer to the data structure) Reset to 1
21	66MHz Capable	RO	1: 66MHz capable Reset to 0
22	Reserved	RO	Reset to 0
23	Fast Back-to-Back Capable	RO	1: Enable fast back-to-back transactions Reset to 0
24	Master Data Parity Error Detected	RWC	This bit is set if its Parity Error Enable bit is set and either of the conditions occurs on the primary: • Receives a completion marked poisoned • Poisons a write request Reset to 0
26:25	DEVSEL_L Timing (medium decode)	RO	DEVSEL_L Timing is not supported. Reset to 00
27	Signaled Target Abort	RWC	This bit is set when PI7C9X113SL completes a request using completer abort status on the primary Reset to 0
28	Received Target Abort	RWC	This bit is set when PI7C9X113SL receives a completion with completer abort completion status on the primary Reset to 0
29	Received Master Abort	RWC	This bit is set when PI7C9X113SL receives a completion with Unsupported Request Completion Status on the primary Reset to 0
30	Signaled System Error	RWC	This bit is set when PI7C9X113SL sends an ERR_FATAL or ERR_NON_FATAL message on the primary Reset to 0
31	Detected Parity Error	RWC	This bit is set when poisoned TLP is detected on the primary Reset to 0

6.3.5 REVISION ID REGISTER – OFFSET 08h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Revision ID	RO	Reset to 00000000h

6.3.6 CLASS CODE REGISTER – OFFSET 08h

BIT	FUNCTION	TYPE	DESCRIPTION
15:8	Programming Interface	RO	00000000: Subtractive decoding of PCI-PCI bridge is not supported 00000001: Subtractive decoding of PCI-PCI bridge is supported

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BIT	FUNCTION	TYPE	DESCRIPTION
			RO as 00000000 when legacy bit (bit 0 of offset 98h) is clear, and 00000001 when legacy bit is set.
23:16	Sub-Class Code	RO	Sub-Class Code 00000100: PCI-to-PCI bridge Reset to 00000100
31:24	Base Class Code	RO	Base class code 00000110: Bridge Device Reset to 00000110

6.3.7 CACHE LINE SIZE REGISTER – OFFSET 0Ch

BIT	FUNCTION	TYPE	DESCRIPTION
1:0	Reserved	RO	Bit [1:0] not supported Reset to 00
2	Cache Line Size	RW	1: Cache line size = 4 double words Reset to 0
3	Cache Line Size	RW	1: Cache line size = 8 double words Reset to 0
4	Cache Line Size	RW	1: Cache line size = 16 double words Reset to 0
5	Cache Line Size	RW	1: Cache line size = 32 double words Reset to 0
7:6	Reserved	RO	Bit [7:6] not supported Reset to 00

6.3.8 PRIMARY LATENCY TIMER REGISTER – OFFSET 0Ch

BIT	FUNCTION	TYPE	DESCRIPTION
15:8	Primary Latency Timer	RO	8 bits of primary latency timer in PCI bus Reset to 00h

6.3.9 HEADER TYPE REGISTER – OFFSET 0Ch

BIT	FUNCTION	TYPE	DESCRIPTION
22:16	PCI-to-PCI Bridge Configuration	RO	PCI-to-PCI bridge configuration (10 – 3Fh) Reset to 0000001
23	Single Function Device	RO	0: Indicates single function device 1: Indicates multiple function device Reset to 0
31:24	BIST	RO	Reset to 00h

6.3.10 RESERVED REGISTERS – OFFSET 10h TO 17h

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6.3.11 PRIMARY BUS NUMBER REGISTER – OFFSET 18h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Primary Bus Number	RW	Reset to 00h

6.3.12 SECONDARY BUS NUMBER REGISTER – OFFSET 18h

BIT	FUNCTION	TYPE	DESCRIPTION
15:8	Secondary Bus Number	RW	Reset to 00h

6.3.13 SUBORDINATE BUS NUMBER REGISTER – OFFSET 18h

BIT	FUNCTION	TYPE	DESCRIPTION
23:16	Subordinate Bus Number	RW	Reset to 00h

6.3.14 SECONDARY LATENCY TIME REGISTER – OFFSET 18h

BIT	FUNCTION	TYPE	DESCRIPTION
31:24	Secondary Latency Timer	RW	Reset to 40h

6.3.15 I/O BASE REGISTER – OFFSET 1Ch

BIT	FUNCTION	TYPE	DESCRIPTION
1:0	32-bit I/O Addressing Support	RO	01: Indicates PI7C9X113SL supports 32-bit I/O addressing Reset to 01
3:2	Reserved	RO	Reset to 00
7:4	I/O Base	RW	Indicates the I/O base (0000_0000h) Reset to 0000

6.3.16 I/O LIMIT REGISTER – OFFSET 1Ch

BIT	FUNCTION	TYPE	DESCRIPTION
9:8	32-bit I/O Addressing Support	RO	01: Indicates PI7C9X113SL supports 32-bit I/O addressing Reset to 01
11:10	Reserved	RO	Reset to 00
15:12	I/O Limit	RW	Indicates the I/O Limit (0000_0FFFh) Reset to 0000

6.3.17 SECONDARY STATUS REGISTER – OFFSET 1Ch

BIT	FUNCTION	TYPE	DESCRIPTION
20:16	Reserved	RO	Reset to 00000
21	66MHz Capable	RO	Indicates PI7C9X113SL is 66MHz capable Reset to 1
22	Reserved	RO	Reset to 0
23	Fast Back-to-Back Capable	RO	1: Indicates PI7C9X113SL supports Fast Back-to-Back Capable Reset to 1

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BIT	FUNCTION	TYPE	DESCRIPTION
24	Master Data Parity Error Detected	RWC	This bit is set if its parity error enable bit is set and either of the conditions occur on the primary: • Detected parity error when receiving data or split response for read • Observes S_PERR_L asserted when sending data or receiving split response for write • Receives a split completion message indicating data parity error occurred for non-posted write Reset to 0
26:25	DEVSEL_L Timing (medium decoding)	RO	01: medium DEVSEL_L decoding Reset to 01
27	Signaled Target Abort	RWC	This bit is set when PI7C9X113SL signals target abort on the secondary interface. Reset to 0
28	Received Target Abort	RWC	This bit is set when PI7C9X113SL detects target abort on the secondary interface. Reset to 0
29	Received Master Abort	RWC	This bit is set when PI7C9X113SL detects master abort on the secondary interface. Reset to 0
30	Received System Error	RWC	This bit is set when PI7C9X113SL detects SERR_L assertion on the secondary interface. Reset to 0
31	Detected Parity Error	RWC	This bit is set when PI7C9X113SL detects address or data parity error on the secondary interface. Reset to 0

6.3.18 MEMORY BASE REGISTER – OFFSET 20h

BIT	FUNCTION	TYPE	DESCRIPTION
3:0	Reserved	RO	Reset to 0000
15:4	Memory Base	RW	Memory Base (00000000h) Reset to 000h

6.3.19 MEMORY LIMIT REGISTER – OFFSET 20h

BIT	FUNCTION	TYPE	DESCRIPTION
19:16	Reserved	RO	Reset to 0000
31:20	Memory Limit	RW	Memory Limit (000FFFFFh) Reset to 000h

6.3.20 PREFETCHABLE MEMORY BASE REGISTER – OFFSET 24h

BIT	FUNCTION	TYPE	DESCRIPTION
3:0	64-bit Addressing Support	RO	0001: Indicates PI7C9X113SL supports 64-bit addressing Reset to 0001
15:4	Prefetchable Memory Base	RW	Prefetchable Memory Base (00000000h) Reset to 000h

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6.3.21 PREFETCHABLE MEMORY LIMIT REGISTER – OFFSET 24h

BIT	FUNCTION	TYPE	DESCRIPTION
19:16	64-bit Addressing Support	RO	0001: Indicates PI7C9X113SL supports 64-bit addressing Reset to 0001
31:20	Prefetchable Memory Limit	RW	Prefetchable Memory Limit (000FFFFFh) Reset to 000h

6.3.22 PREFETCHABLE BASE UPPER 32-BIT REGISTER – OFFSET 28h

BIT	FUNCTION	TYPE	DESCRIPTION
31:0	Prefetchable Base Upper 32-bit	RW	Bit [63:32] of prefetchable base Reset to 00000000h

6.3.23 PREFETCHABLE LIMIT UPPER 32-BIT REGISTER – OFFSET 2Ch

BIT	FUNCTION	TYPE	DESCRIPTION
31:0	Prefetchable Limit Upper 32-bit	RW	Bit [63:32] of prefetchable limit Reset to 00000000h

6.3.24 I/O BASE UPPER 16-BIT REGISTER – OFFSET 30h

BIT	FUNCTION	TYPE	DESCRIPTION
15:0	I/O Base Upper 16-bit	RW	Bit [31:16] of I/O Base Reset to 0000h

6.3.25 I/O LIMIT UPPER 16-BIT REGISTER – OFFSET 30h

BIT	FUNCTION	TYPE	DESCRIPTION
31:16	I/O Limit Upper 16-bit	RW	Bit [31:16] of I/O Limit Reset to 0000h

6.3.26 CAPABILITY POINTER – OFFSET 34h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Capability Pointer	RO	Capability pointer Reset to 80h (RO as 90h in Legacy Mode to by pass PCI-X capability)
31:8	Reserved	RO	Reset to 0

6.3.27 EXPANSION ROM BASE ADDRESS REGISTER – OFFSET 38h

BIT	FUNCTION	TYPE	DESCRIPTION
31:0	Expansion ROM Base Address	RO	Expansion ROM is not supported. Reset to 00000000h

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6.3.28 INTERRUPT LINE REGISTER – OFFSET 3Ch

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Interrupt Line	RW	For initialization code to program to tell which input of the interrupt controller the PI7C9X113SL's INTA_L in connected to. Reset to 00h

6.3.29 INTERRUPT PIN REGISTER – OFFSET 3Ch

BIT	FUNCTION	TYPE	DESCRIPTION
15:8	Interrupt Pin	RO	Designates interrupt pin, INTA_L, is used Reset to 01h

6.3.30 BRIDGE CONTROL REGISTER – OFFSET 3Ch

BIT	FUNCTION	TYPE	DESCRIPTION
16	Parity Error Response Enable	RW	0: Ignore parity errors on the secondary 1: Enable parity error detection on secondary Controls the response to uncorrectable address attribute and data errors on the secondary Reset to 0
17	SERR_L Enable	RW	0: Disable the forwarding of SERR_L to ERR_FATAL and ERR_NONFATAL 1: Enable the forwarding of SERR_L to ERR_FATAL and ERR_NONFATAL Reset to 0
18	ISA Enable	RW	0: Forward downstream all I/O addresses in the address range defined by the I/O Base and Limit registers 1: Forward upstream all I/O addresses in the address range defined by the I/O Base and Limit registers that are in the first 64KB of PCI I/O address space (top 768 bytes of each 1KB block) Reset to 0
19	VGA Enable	RW	0: Do not forward VGA compatible memory and I/O addresses from the primary to secondary, unless they are enabled for forwarding by the defined I/O and memory address ranges 1: Forward VGA compatible memory and I/O addresses from the primary and secondary (if the I/O enable and memory enable bits are set), independent of the ISA enable bit Reset to 0
20	VGA 16-bit Decode	RW	0: Execute 10-bit address decodes on VGA I/O accesses 1: Execute 16-bit address decode on VGA I/O accesses Reset to 0
21	Master Abort Mode	RW	0: Do not report master aborts (return FFFFFFFFh on reads and discards data on write) 1: Report master abort by signaling target abort if possible or by the assertion of SERR_L (if enabled). Reset to 0
22	Secondary Interface Reset	RW	0: Do not force the assertion of RESET_L on secondary PCI bus 1: Force the assertion of RESET_L on secondary PCI bus Reset to 0
23	Fast Back-to-Back Enable	RO	Fast back-to-back is not supported Reset to 0

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BIT	FUNCTION	TYPE	DESCRIPTION
24	Primary Master Timeout	RW	0: Primary discard timer counts 2^{15} PCI clock cycles 1: Primary discard timer counts 2^{10} PCI clock cycles This bit is ignored by the PI7C9X113SL Reset to 0
25	Secondary Master Timeout	RW	0: Secondary discard timer counts 2^{15} PCI clock cycles 1: Secondary discard timer counts 2^{10} PCI clock cycles Reset to 0
26	Master Timeout Status	RWC	This bit is set when the discard timer expires and a delayed completion is discarded at the PCI interface Reset to 0
27	Discard Timer SERR_L Enable	RW	This bit is set to enable to generate ERR_NONFATAL or ERR_FATAL as a result of the expiration of the discard timer on the PCI interface. Reset to 0
31:28	Reserved	RO	Reset to 0000

6.3.31 PCI DATA PREFETCHING CONTROL REGISTER – OFFSET 40h

BIT	FUNCTION	TYPE	DESCRIPTION
0	Secondary Internal Arbiter's PARK Function	RW	0: Park to the last master 1: Park to PI7C9X113SL secondary port Reset to 0
1	Memory Read Prefetching Dynamic Control Disable	RW	0: Enable memory read prefetching dynamic control for PCI to PCIe read 1: Disable memory read prefetching dynamic control for PCI to PCIe read Reset to 0
2	Completion Data Prediction Control Disable	RW	0: Enable completion data prediction for PCI to PCIe read. 1: Disable completion data prediction Reset to 0
3	CFG Type0-to-Type1 Conversion Enable	RW	0: CFG Type0-to-Type1 conversion is disabled. 1: CFG Type0-to-Type1 conversion is enabled if the AD[31:28] is all 1s. PI7C9X113SL will ignore the AD[0] and always treats the cfg transaction as type 1, other AD bit (except AD[31:28], AD[0]) must meet the Type 1 format Reset to 0
5:4	PCI Read Multiple Prefetch Mode	RW	00: One cache line prefetch if memory read multiple address is in prefetchable range at the PCI interfac 01: Full prefetch if address is in prefetchable range at PCI interface, and the PI7C9X113SL will keep remaining data after it disconnects the external master during burst read with read multiple command until the discard timer expires 10: Full prefetch if address is in prefetchable range at PCI interface 11: Full prefetch if address is in prefetchable range at PCI interface and the PI7C9X113SL will keep remaining data after the read multiple is terminated either by an external master or by the PI7C9X113SL, until the discard time expires Reset to 10

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BIT	FUNCTION	TYPE	DESCRIPTION
7:6	PCI Read Line Prefetch Mode	RW	00: Once cache line prefetch if memory read address is in prefetchable range at PCI interface 01: Full prefetch if address is in prefetchable range at PCI interface and the PI7C9X113SL will keep remaining data after it is disconnected by an external master during burst read with read line command, until discard timer expires 10: Full prefetch if memory read line address is in prefetchable range at PCI interface 11: Full prefetch if address is in prefetchable range at PCI interface and the PI7C9X113SL will keep remaining data after the read line is terminated either by an external master or by the PI7C9X113SL, until the discard timer expires Reset to 00
9:8	PCI Read Prefetch Mode	RW	00: One cache line prefetch if memory read address is in prefetchable range at PCI interface 01: Reserved 10: Full prefetch if memory read address is in prefetchable range at PCI interface 11: Disconnect on the first DWORD Reset to 00
10	PCI Special Delayed Read Mode Enable	RW	0: Retry any master at PCI bus that repeats its transaction with command code changes. 1: Allows any master at PCI bus to change memory command code (MR, MRL, MRM) after it has received a retry. The PI7C9X113SL will complete the memory read transaction and return data back to the master if the address and byte enables are the same. Reset to 0
11	Optional Malformed Packet checking Enable	RW	0: Optional Malformed Packet checking is disabled 1: Optional Malformed Packet checking is enabled Reset to 0
14:12	Maximum Memory Read Byte Count	RW	Maximum byte count is used by the PI7C9X113SL when generating memory read requests on the PCIe link in response to a memory read initiated on the PCI bus and bit [9:8], bit [7:6], and bit [5:4] are set to “full prefetch”. 000: 512 bytes (default) 001: 128 bytes 010: 256 bytes 011: 512 bytes 100: 1024 bytes 101: 2048 bytes 110: 4096 bytes 111: 512 bytes Reset to 000

6.3.32 CHIP CONTROL 0 REGISTER – OFFSET 40h

BIT	FUNCTION	TYPE	DESCRIPTION
15	Flow Control Update Control	RW	0: Flow control is updated for every two credits available 1: Flow control is updated for every on credit available Reset to 0
16	PCI Retry Counter Status	RWC	0: The PCI retry counter has not expired since the last reset 1: The PCI retry counter has expired since the last reset Reset to 0

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BIT	FUNCTION	TYPE	DESCRIPTION
18:17	PCI Retry Counter Control	RW	00: No expiration limit 01: Allow 256 retries before expiration 10: Allow 64K retries before expiration 11: Allow 2G retries before expiration Reset to 00
19	PCI Discard Timer Disable	RW	0: Enable the PCI discard timer in conjunction with bit [24] or bit [25] of offset 3Ch (bridge control register) 1: Disable the PCI discard timer in conjunction with bit [24] or bit [25] of offset 3Ch (bridge control register) Reset to 0
20	PCI Discard Timer Short Duration	RW	0: Use bit [25] offset 3Ch to indicate how many PCI clocks should be allowed before the PCI discard timer expires 1: 64 PCI clocks allowed before the PCI discard timer expires Reset to 0
22:21	Configuration Request Retry Timer Counter Value Control	RW	00: Timer expires at 25us 01: Timer expires at 0.5ms 10: Timer expires at 5ms 11: Timer expires at 25ms Reset to 01
23	Delayed Transaction Order Control	RW	0: Enable out-of-order capability between delayed transactions 1: Disable out-of-order capability between delayed transactions Reset to 0
25:24	Completion Timer Counter Value Control	RW	00: Timer expires at 50us 01: Timer expires at 10ms 10: Timer expires at 50ms 11: Timer disabled Reset to 01
26	Isochronous Traffic Support Enable	RW	0: All memory transactions from PCI to PCIe will be mapped to TC0 1: All memory transactions from PCI to PCIe will be mapped to Traffic Class defined in bit [29:27] of offset 40h. Reset to 0
29:27	Traffic Class Used For Isochronous Traffic	RW	Reset to 001
30	Power Saving Mode Enable	RW	0: Disable the power saving mode; 1: Enable the power saving mode. The internal clock for MAC/DLL/TLP and PCI logic is disabled at L1s and L1 state. Reset to 1
31	Power Saving Mode Enable at ASPM L0s	RW	0: Disables the power saving mode at ASPM L0s 1: Enables the power saving mode at ASPM L0s Reset to 1

6.3.33 RESERVED REGISTER – OFFSET 44h

BIT	FUNCTION	TYPE	DESCRIPTION
31:0	Reserved	RO	Reset to 00000000h

6.3.34 ARBITER ENABLE REGISTER – OFFSET 48h

BIT	FUNCTION	TYPE	DESCRIPTION
0	Enable Arbiter 0	RW	0: Disable arbitration for internal PI7C9X113SL request 1: Enable arbitration for internal PI7C9X113SL request Reset to 1

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BIT	FUNCTION	TYPE	DESCRIPTION
1	Enable Arbiter 1	RW	0: Disable arbitration for master 1 1: Enable arbitration for master 1 Reset to 1
2	Enable Arbiter 2	RW	0: Disable arbitration for master 2 1: Enable arbitration for master 2 Reset to 1
3	Enable Arbiter 3	RW	0: Disable arbitration for master 3 1: Enable arbitration for master 3 Reset to 1
4	Enable Arbiter 4	RW	0: Disable arbitration for master 4 1: Enable arbitration for master 4 Reset to 1
8:5	Reserved	RO	Reset to 0h

6.3.35 ARBITER MODE REGISTER – OFFSET 48h

BIT	FUNCTION	TYPE	DESCRIPTION
9	External Arbiter Bit	RW	0: Enable internal arbiter 1: Use external arbiter and disable internal arbiter Reset to 0
10	Broken Master Timeout Enable	RW	0: Broken master timeout disable 1: This bit enables the internal arbiter to count 16 PCI bus cycles while waiting for FRAME_L to become active when a device's PCI bus GNT is active and the PCI bus is idle. If the broken master timeout expires, the PCI bus GNT for the device is de-asserted. Reset to 0
11	Broken Master Refresh Enable	RW	0: A broken master will be ignored forever after de-asserting its REQ_L for at least 1 clock 1: Refresh broken master state after all the other masters have been served once Reset to 0
19:12	Arbiter Fairness Counter	RW	08h: These bits are the initialization value of a counter used by the internal arbiter. It controls the number of PCI bus cycles that the arbiter holds a device's PCI bus GNT active after detecting a PCI bus REQ_L from another device. The counter is reloaded whenever a new PCI bus GNT is asserted. For every new PCI bus GNT, the counter is armed to decrement when it detects the new fall of FRAME_L. If the arbiter fairness counter is set to 00h, the arbiter will not remove a device's PCI bus GNT until the device has de-asserted its PCI bus REQ. Reset to 08h
20	GNT_L Output Toggling Enable	RW	0: GNT_L not de-asserted after granted master assert FRAME_L 1: GNT_L de-asserts for 1 clock after 2 clocks of the granted master asserting FRAME_L Reset to 0
21	Reserved	RO	Reset to 0

6.3.36 ARBITER PRIORITY REGISTER – OFFSET 48h

BIT	FUNCTION	TYPE	DESCRIPTION
22	Arbiter Priority 0	RW	0: Low priority request to internal PI7C9X113SL 1: High priority request to internal PI7C9X113SL Reset to 1

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BIT	FUNCTION	TYPE	DESCRIPTION
23	Arbiter Priority 1	RW	0: Low priority request to master 1 1: High priority request to master 1 Reset to 0
24	Arbiter Priority 2	RW	0: Low priority request to master 2 1: High priority request to master 2 Reset to 0
25	Arbiter Priority 3	RW	0: Low priority request to master 3 1: High priority request to master 3 Reset to 0
26	Arbiter Priority 4	RW	0: Low priority request to master 4 1: High priority request to master 4 Reset to 0
31:27	Reserved	RO	Reset to 00h

6.3.37 RESERVED REGISTERS – OFFSET 4Ch

6.3.38 MEMORY READSMART BASE LOWER 32-Bit REGISTER 1 – OFFSET 50h

BIT	FUNCTION	TYPE	DESCRIPTION
31:0	Memory Readsmart Base Lower 32-bit Register 1	RW	Memory Readsmart Base Address 1 in conjunction with Memory Readsmart Base Lower 32-bit register 1 and Memory Readsmart Range Size register 1, defines address range 1 in which PCI memory read are allowed (or not allowed) to use the Readsmart mode which is controlled by bit [7:4] of 40h. Reset to 00000000h

6.3.39 MEMORY READSMART BASE UPPER 32-Bit REGISTER 1 – OFFSET 54h

BIT	FUNCTION	TYPE	DESCRIPTION
31:0	Memory Readsmart Base Upper 32-bit register 1	RW	Bit[63:32] of Memory Readsmart Base Address 1 Reset to 00000000h

6.3.40 MEMORY READSMART RANGE CONTROL REGISTER 1 – OFFSET 58h

BIT	FUNCTION	TYPE	DESCRIPTION
0	Memory Readsmart Range Control	RW	Memory Readsmart Range Control register 0: any PCI memory read with address falling in the range are not allowed to use Readsmart mode. 1: only PCI memory read with address falling in the range are allowed to use Readsmart mode. Reset to 0
31:1	Memory Readsmart Range Address 1	RW	Define the size of the range 1, maximum 4G byte with granuity of 2 bytes Reset to 00000000h

6.3.41 MEMORY READSMART BASE LOWER 32-Bit REGISTER 2 – OFFSET 5Ch

BIT	FUNCTION	TYPE	DESCRIPTION
31:0	Readsmart Memory Base Lower 32-bit Register 2	RW	Memory Readsmart Base Address 1 in conjunction with Memory Readsmart Base Lower 32-bit register 2 and Memory Readsmart Range Size register 2, defines address range 1 in which PCI memory read are allowed (or not allowed) to use the Readsmart mode which is controlled by bit [7:4] of 40h.

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BIT	FUNCTION	TYPE	DESCRIPTION
			Reset to 00000000h

6.3.42 MEMORY READSMART BASE UPPER 32-Bit REGISTER 2 – OFFSET 60h

BIT	FUNCTION	TYPE	DESCRIPTION
31:0	Memory Readsmart Base Upper 32-bit register 2	RW	Bit[63:32] of Memory Readsmart Base Address 2 Reset to 00000000h

6.3.43 MEMORY READSMART RANGE SIZE REGISTER 2 – OFFSET 64h

BIT	FUNCTION	TYPE	DESCRIPTION
31:0	Memory Readsmart Range Size register 2	RW	Memory Readsmart Range Address 2 defines the size of the range 2, maximum 4G byte Reset to 00000000h

6.3.44 UPSTREAM MEMORY READ/WRITE CONTROL REGISTER – OFFSET 68h

BIT	FUNCTION	TYPE	DESCRIPTION
26:0	Reserved	RO	Reset to 0
29:27	Upstream Memory Read Request Transmitting Control	RW	Control when to transmit a second memory read request to PCIe link before receiving Completion data for the previous request which is from the same read channel. 000: Do not send 2nd request until receiving all completion data for the previous request. 001: Do not send 2nd request until 1 ADQ data left unrecived for the previous request. 010: Do not send 2nd request until 2 ADQ data left unrecived for the previous request. 011: Do not send 2nd request until 4 ADQ data left unrecived for the previous request. 1xx: Do not send 2nd request until 8 ADQ data left unrecived for the previous request. Reset to 7h
31:30	Memory Write Fragment Control	RW	Upstream Memory Write Fragment Control 00: Fragment at 32-byte boundary 01: Fragment at 64-byte boundary 1x: Fragment at 128-byte boundary Reset to 10

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6.3.45 PHY TRANSMIT/RECEIVE CONTROL REGISTER – OFFSET 6Ch

BIT	FUNCTION	TYPE	DESCRIPTION
2:0	Timing Threshold	RW	Timing threshold before sampling receiver detection circuit 000: 1.0us 001: 2.0us 010: 4.0us(default) 011: 5.0us 100: 10.0us 101: 20.0us 110: 40.0us 111: 50.0us Reset to 2h
6:3	Receiver Equalization Stage Enable (2.5G)	RW	xxx1: Enable stage 0 xx1x: Enable stage 1 x1xx: Enable stage 2 Reset to 2h
7	Clock and Data Recovery (CDR) Second Order Loop Enable	RW	Reset to 0
9:8	Set CDR Second Order Loop Gain	RW	Reset to 2h
11:10	Receiver Signal Detect Level Select	RW	Reset to 1h
13:12	Threshold Of Clock Recovery Filter	RW	Reset to 3h
14	De-Emphasis Offset Drive Level to the Lane Driver in Transmit Margin Mode Enable	RW	Reset to 0
15	De-Emphasis Offset Drive Level to the Lane Driver in Normal Mode Enable	RW	Reset to 0
16	Base Offset Drive Level to the Lane Driver in Normal Mode Enable	RW	Reset to 0
17	Base Offset Drive Level to the Lane Driver in Transmit Margin Mode Enable	RW	Reset to 0
22:18	De-Emphasis -3.5db of Transmit De-Emphasis Base	RW	Reset to 0Dh
27:23	De-Emphasis -3.5db of Transmit Level Base	RW	Reset to 13h
30:28	Transmitter Main Output Voltage Drive Level	RW	Set Transmitter main output voltage drive levels based on Drive Margin setting: 000: Nominal 001: Margin 1 case 010: Margin 2 case 011: Margin 3 case 100: Margin 4 case Other: Reserved Reset to 0h
31	Reserved	RO	Reset to 0

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6.3.46 EEPROM AUTOLOAD CONTROL/STATUS REGISTER – OFFSET 70h

BIT	FUNCTION	TYPE	DESCRIPTION
0	Initiate EEPROM Read or Write Cycle	RW	This bit will be reset to 0 after the EEPROM operation is finished. 0: EEPROM AUTOLOAD disabled 0 -> 1: Starts the EEPROM Read or Write cycle Reset to 0
1	Control Command for EEPROM	RW	0: Read 1: Write Reset to 0
2	EEPROM Error	RO	0: EEPROM acknowledge is always received during the EEPROM cycle 1: EEPROM acknowledge is not received during EEPROM cycle Reset to 0
3	EPROM Autoload Complete Status	RO	0: EEPROM autoload is not successfully completed 1: EEPROM autoload is successfully completed Reset to 0
5:4	EEPROM Clock Frequency Control	RW	Where PCLK is 256MHz 00: PCLK / 8192 01: PCLK / 4096 10: PCLK / 2048 11: PCLK / 256 Reset to 00
6	EEPROM Autoload Control	RW	0: Enable EEPROM autoload 1: Disable EEPROM autoload Reset to 0
7	Fast EEPROM Autoload Control	RW	=0: normal speed of EEPROM autoload =1: speeds up EEPROM autoload by 8 times Reset to 1
8	EEPROM Autoload Status	RO	0: EEPROM autoload is not on going 1: EEPROM autoload is on going Reset to 0
15:9	EEPROM Word Address	RW	EEPROM word address for EEPROM cycle Reset to 0000000
31:16	EEPROM Data	RW	EEPROM data to be written into the EEPROM or received from the EEPROM after read cycle has completed Reset to 0000h

6.3.47 RESERVED REGISTER – OFFSET 74h

6.3.48 GPIO DATA AND CONTROL REGISTER – OFFSET 78h

BIT	FUNCTION	TYPE	DESCRIPTION
11:0	Reserved	RO	Reset to 000h
15:12	GPIO Output Write-1-to-Clear	RW	Reset to 0h
19:16	GPIO Output Write-1-to-Set	RW	Reset to 0h
23:20	GPIO Output Enable Write-1-to-Clear	RW	Reset to 0h
27:24	GPIO Output Enable Write-1-to-Set	RW	Reset to 0h
31:28	GPIO Input Data Register	RO	Reset to 0h

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6.3.49 RESERVED REGISTER – OFFSET 7Ch

6.3.50 PCI-X CAPABILITY ID REGISTER – OFFSET 80h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	PCI-X Capability ID	RO	PCI-X Capability ID Reset to 07h

6.3.51 NEXT CAPABILITY POINTER REGISTER – OFFSET 80h

BIT	FUNCTION	TYPE	DESCRIPTION
15:8	Next Capability Pointer	RO	Point to power management Reset to 90h

6.3.52 PCI-X SECONDARY STATUS REGISTER – OFFSET 80h

BIT	FUNCTION	TYPE	DESCRIPTION
16	64-bit Device on Secondary Bus Interface	RO	64-bit is not supported Reset to 0
17	133MHz Capable	RO	133MHz capable on secondary interface. Reset to 0
18	Split Completion Discarded	RO	Split Completion Discarded Reset to 0
19	Unexpected Split Completion	RWC	0: No unexpected split completion has been received. 1: An unexpected split completion has been received with the request ID equaled to the bridge's secondary port number, device number 00h, and function number 0 on the bridge secondary interface. Reset to 0
20	Split Completion Overrun	RO	Reset to 0
21	Split Request Delayed	RO	0: The bridge has not delayed a split request. 1: The bridge has delayed a split request because the bridge cannot forward a transaction to secondary port due to not enough room within the limit specified in the split transaction commitment limit field in the downstream split transaction control register. Reset to 0
24:22	Secondary Clock Frequency	RO	000: Conventional PCI mode (minimum clock period not applicable) 001: 66MHz (minimum clock period is 15ns) 010: 100 to 133MHz (minimum clock period is 7.5ns) 011: Reserved 1xx: Reserved Reset to 000
31:25	Reserved	RO	Reset to 0000000

6.3.53 PCI-X BRIDGE STATUS REGISTER – OFFSET 84h

BIT	FUNCTION	TYPE	DESCRIPTION
2:0	Function Number	RO	Function Number; the function number (AD[10:8] of a type-0 configuration transaction) to which the bridge responds. Reset to 000

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BIT	FUNCTION	TYPE	DESCRIPTION
7:3	Device Number	RO	Device Number; the device number (AD[15:11] of a type-0 configuration transaction) is assigned to the bridge by the connection of system hardware. Each time the bridge is addressed by a configuration write transaction, the bridge updates this register with the contents of AD[15:11] of the address phase of the configuration transaction, regardless of which register in the bridge is addressed by the transaction. The bridge is addressed by a configuration write transaction if all of the following are true: • The transaction uses a configuration write command. • IDSEL is asserted during the address phase. • AD[1:0] are 00 (type-0 configuration transaction). • AD[10:8] of the configuration address contain the appropriate function number. Reset to 11111
15:8	Bus Number	RO	Bus Number; It is an additional address from which the contents of the primary bus number register on type-1 configuration space header is read. The bridge uses the bus number, device number, and function number fields to create the completer ID when responding with a split completion to a read of an internal bridge register. These fields are also used for cases when one interface is in conventional PCI mode and the other is in PCIX mode. Reset to 11111111
16	64-bit Device on Primary Bus Interface	RO	64-bit device. Reset to 0
17	133MHz Capable	RO	133MHz capable on primary interface. Reset to 0
18	Split Completion Discarded	RO	Reset to 0
19	Unexpected Split Completion	RWC	0: No unexpected split completion has been received. 1: An unexpected split completion has been received with the request ID equaled to the bridge's primary port number, device number, and function number on the bridge primary interface. Reset to 0
20	Split Completion Overrun	RO	Reset to 0
21	Split Request Delayed	RWC	When this bit is set to 1, a split request is delayed because PI7C9X113SL is not able to forward the split request transaction to its primary bus due to insufficient room within the limit specified in the split transaction commitment limit field of the downstream split transaction control register Reset to 0
31:22	Reserved	RO	Reset to 0000000000

6.3.54 UPSTREAM SPLIT TRANSACTION REGISTER – OFFSET 88h

BIT	FUNCTION	TYPE	DESCRIPTION
15:0	Upstream Split Transaction Capability	RO	Upstream Split Transaction Capability specifies the size of the buffer (in the unit of ADQs) to store split completions for memory read. It applies to the requesters on the secondary bus in addressing the completers on the primary bus. The 0010h value shows that the buffer has 16 ADQs or 2K bytes storage Reset to 0010h

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BIT	FUNCTION	TYPE	DESCRIPTION
31:16	Upstream Split Transaction Commitment Limit	RW	Upstream Split Transaction Commitment Limit indicates the cumulative sequence size of the commitment limit in units of ADQs. This field can be programmed to any value or equal to the content of the split capability field. For example, if the limit is set to FFFFh, PI7C9X113SL is allowed to forward all split requests of any size regardless of the amount of buffer space available. If the limit is set to 0100h or greater will cause the bridge to forward accepted split requests of any size regardless of the amount of buffer space available. The split transaction commitment limit is set to 0010h that is the same value as the split transaction capability. Reset to 0010h

6.3.55 DOWNSTREAM SPLIT TRANSACTION REGISTER – OFFSET 8Ch

BIT	FUNCTION	TYPE	DESCRIPTION
15:0	Downstream Split Transaction Capability	RO	Downstream Split Transaction Capability specifies the size of the buffer (in the unit of ADQs) to store split completions for memory read. It applies to the requesters on the primary bus in addressing the completers on the secondary bus. The 0010h value shows that the buffer has 16 ADQs or 2K bytes storage Reset to 0010h
31:16	Downstream Split Transaction Commitment Limit	RW	Downstream Split Transaction Commitment Limit indicates the cumulative sequence size of the commitment limit in units of ADQs. This field can be programmed to any value or equal to the content of the split capability field. For example, if the limit is set to FFFFh, PI7C9X113SL is allowed to forward all split requests of any size regardless of the amount of buffer space available. If the limit is set to 0100h or greater will cause the bridge to forward accepted split requests of any size regardless of the amount of buffer space available. The split transaction commitment limit is set to 0010h that is the same value as the split transaction capability. Reset to 0010h

6.3.56 POWER MANAGEMENT ID REGISTER – OFFSET 90h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Power Management ID	RO	Power Management ID Register Reset to 01h

6.3.57 NEXT CAPABILITY POINTER REGISTER – OFFSET 90h

BIT	FUNCTION	TYPE	DESCRIPTION
15:8	Next Pointer	RO	Next pointer (point to Subsystem ID and Subsystem Vendor ID) Reset to A8h

6.3.58 POWER MANAGEMENT CAPABILITY REGISTER – OFFSET 90h

BIT	FUNCTION	TYPE	DESCRIPTION
18:16	Version Number	RO	Version number that complies with revision 1.2 of the PCI Power Management Interface specification. Reset to 011
19	PME Clock	RO	PME clock is not required for PME_L generation Reset to 0
20	Reserved	RO	Reset to 0

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BIT	FUNCTION	TYPE	DESCRIPTION
21	Device Specific Initialization (DSI)	RO	DSI – no special initialization of this function beyond the standard PCI configuration header is required following transition to the D0 un-initialized state Reset to 0
24:22	AUX Current	RO	000: 0mA 001: 55mA 010: 100mA 011: 160mA 100: 220mA 101: 270mA 110: 320mA 111: 375mA Reset to 001
25	D1 Power Management	RO	D1 power management is not supported Reset to 0
26	D2 Power Management	RO	D2 power management is not supported Reset to 0
31:27	PME_L Support	RO	PME_L is supported in D3 cold, D3 hot, and D0 states. Reset to 11001

6.3.59 POWER MANAGEMENT CONTROL AND STATUS REGISTER – OFFSET 94h

BIT	FUNCTION	TYPE	DESCRIPTION
1:0	Power State	RW	Power State is used to determine the current power state of PI7C9X113SL. If a non-implemented state is written to this register, PI7C9X113SL will ignore the write data. When present state is D3 and changing to D0 state by programming this register, the power state change causes a device reset without activating the RESET_L of PCI bus interface 00: D0 state 01: D1 state not implemented 10: D2 state not implemented 11: D3 state Reset to 00
2	Reserved	RO	Reset to 0
3	No Soft Reset	RO	0: Internal reset occurs at D3hot->D0 1: No internal reset occurs and configuration registers are preserved at D3hot->D0 Reset to 1
7:4	Reserved	RO	Reset to 0h
8	PME Enable	RWS	0: PME_L assertion is disabled 1: PME_L assertion is enabled Reset to 0
12:9	Data Select	RO	Data register is not implemented Reset to 0000
14:13	Data Scale	RO	Data register is not implemented Reset to 00
15	PME Status	RWCS	PME_L is supported Reset to 0

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6.3.60 PCI-TO-PCI SUPPORT EXTENSION REGISTER – OFFSET 94h

BIT	FUNCTION	TYPE	DESCRIPTION
21:16	Reserved	RO	Reset to 000000
22	B2/B3 Support	RO	0: B2 / B3 is not support for D3hot Reset to 0
23	PCI Bus Power/Clock Control Enable	RO	0: PCI Bus Power/Clock is disabled Reset to 0
31:24	Data Register	RO	Data register is not implemented Reset to 00h

6.3.61 SUBTRACTIVE DECODING PCI-TO-PCI BRIDGE ENABLE – OFFSET 98h

BIT	FUNCTION	TYPE	DESCRIPTION
0	Subtractive Decoding PCI-to-PCI Bridge Enable	RW	0: 1: PI7C9X113SL's class code is 060401h, and the bridge forwards all cycles (Memory/IO) to downstream PCI devices. All PCI-X/PCIe Capability registers and Extended Configuration registers are treated as reserved registers: Write access is completed normally but data is discarded. Read accesses is returned with data value of 0. Reset to 0
1	PCI Bus Subtractive Decoding Enable	RW	0: PI7C9X113SL does not perform Subtractive Decoding at PCI Bus 1: PI7C9X113SL performs Subtractive Decoding at PCI Bus Reset to 0
31:3	Reserved	RO	Reset to 0

6.3.62 RESERVED REGISTERS – OFFSET 9Ch

6.3.63 CAPABILITY ID REGISTER – OFFSET A0h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Capability ID	RO	Capability ID for Slot Identification. SI is off by default but can be turned on through EEPROM interface Reset to 04h

6.3.64 NEXT POINTER REGISTER – OFFSET A0h

BIT	FUNCTION	TYPE	DESCRIPTION
15:8	Next Pointer	RO	Next pointer – points to PCI Express capabilities register Reset to B0h

6.3.65 SLOT NUMBER REGISTER – OFFSET A0h

BIT	FUNCTION	TYPE	DESCRIPTION
20:16	Expansion Slot Number	RW	Expansion slot number Reset to 00000
21	First In Chassis	RW	First in chassis Reset to 0
23:22	Reserved	RO	Reset to 00

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6.3.66 CHASSIS NUMBER REGISTER – OFFSET A0h

BIT	FUNCTION	TYPE	DESCRIPTION
31:24	Chassis Number	RW	Chassis number Reset to 00h

6.3.67 SECONDARY CLOCK AND CLKRUN CONTROL REGISTER – OFFSET A4h

BIT	FUNCTION	TYPE	DESCRIPTION
1:0	S_CLKOUT0 Enable	RW	S_CLKOUT0 should be always enabled in order to feed the internal secondary interface logic, unless there is external clock input feeding to the pin. 00: enable S_CLKOUT0 01: enable S_CLKOUT0 10: enable S_CLKOUT0 11: disable S_CLKOUT0 and driven LOW Reset to 00
3:2	S_CLKOUT1 Enable	RW	S_CLKOUT (Slot 1) Enable 00: enable S_CLKOUT1 01: enable S_CLKOUT1 10: enable S_CLKOUT1 11: disable S_CLKOUT1 and driven LOW Reset to 00
5:4	S_CLKOUT2 Enable	RW	S_CLKOUT (Slot 2) Enable 00: enable S_CLKOUT2 01: enable S_CLKOUT2 10: enable S_CLKOUT2 11: disable S_CLKOUT2 and driven LOW Reset to 00
7:6	S_CLKOUT3 Enable	RW	S_CLKOUT (Slot 3) Enable 00: enable S_CLKOUT3 01: enable S_CLKOUT3 10: enable S_CLKOUT3 11: disable S_CLKOUT3 and driven LOW Reset to 00
12:8	Reserved	RO	Reset to 0
13	Secondary Clock Stop Status	RO	Secondary clock stop status 0: secondary clock not stopped 1: secondary clock stopped Reset to 0
14	Secondary Clkrun Protocol Enable	RO / RW	0: disable protocol 1: enable protocol The bit is RO as 0 when Clock Power Management feature is disabled, or it is RW (default 1) when Clock Power Management feature is enabled by strapping REQ_L[3:2] to both low at deassertion of RESET_L

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BIT	FUNCTION	TYPE	DESCRIPTION
15	Clkrun Mode	RO / RW	0: Stop the secondary clock only when bridge is at D3hot state 1: Stop the secondary clock whenever the secondary bus is idle and there are no requests from the primary bus The bit is RO when Clock Power Management feature is disabled, or it is RW when Clock Power Management feature is enabled by strapping REQ_L[3:2] to both low at deassertion of RESET_L Reset to 0

6.3.68 XPIP CONFIGURATION REGISTER 3 – OFFSET A4h

BIT	FUNCTION	TYPE	DESCRIPTION
16	ASPM L0s Enable Control	RW	0: bridge may enter ASPM L0s regardless if Receiver is Electrical Idle 1: bridge may enter ASPM L0s only if Receiver is Electrical Idle Reset to 1
18:17	Scrambling Control	RW	Reset to 00
20:19	L0 Enter L1 Timer Control	RW	Reset to 01
31:21	Reserved	RO	Reset to 00

6.3.69 CAPABILITY ID REGISTER – OFFSET A8h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Capability ID	RO	Capability ID for subsystem ID and subsystem vendor ID Reset to 0Dh

6.3.70 NEXT POINTER REGISTER – OFFSET A8h

BIT	FUNCTION	TYPE	DESCRIPTION
15:8	Next Item Pointer	RO	Next item pointer (point to PCI Express Capability by default but can be programmed to A0h if Slot Identification Capability is enabled) Reset to B0h (RO as F0h in Legacy Mode to bypass PCIe capability)

6.3.71 RESERVED REGISTER – OFFSET A8h

BIT	FUNCTION	TYPE	DESCRIPTION
31:16	Reserved	RO	Reset to 0000h

6.3.72 SUBSYSTEM VENDOR ID REGISTER – OFFSET ACh

BIT	FUNCTION	TYPE	DESCRIPTION
15:0	Subsystem Vendor ID	RO	Subsystem vendor ID identifies the particular add-in card or subsystem Reset to 00h

6.3.73 SUBSYSTEM ID REGISTER – OFFSET ACh

BIT	FUNCTION	TYPE	DESCRIPTION
31:16	Subsystem ID	RO	Subsystem ID identifies the particular add-in card or subsystem Reset to 00h

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6.3.74 PCI EXPRESS CAPABILITY ID REGISTER – OFFSET B0h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	PCI Express Capability ID	RO	PCI Express capability ID Reset to 10h

6.3.75 NEXT CAPABILITY POINTER REGISTER – OFFSET B0h

BIT	FUNCTION	TYPE	DESCRIPTION
15:8	Next Item Pointer	RO	Next Capabilities Pointer Register Reset to F0h

6.3.76 PCI EXPRESS CAPABILITY REGISTER – OFFSET B0h

BIT	FUNCTION	TYPE	DESCRIPTION
19:16	Capability Version	RO	Reset to 1h
23:20	Device / Port Type	RO	0000: PCI Express endpoint device 0001: Legacy PCI Express endpoint device 0100: Root port of PCI Express root complex 0101: Upstream port of PCI Express switch 0110: Downstream port of PCI Express switch 0111: PCI Express to PCI bridge 1000: PCI to PCI Express bridge Others: Reserved Reset to 7h
24	Slot Implemented	RO	Reset to 0
29:25	Interrupt Message Number	RO	Reset to 0h
31:30	Reserved	RO	Reset to 0

6.3.77 DEVICE CAPABILITY REGISTER – OFFSET B4h

BIT	FUNCTION	TYPE	DESCRIPTION
2:0	Maximum Payload Size	RO	000: 128 bytes 001: 256 bytes 010: 512 bytes 011: 1024 bytes 100: 2048 bytes 101: 4096 bytes 110: reserved 111: reserved Reset to 2h
4:3	Phantom Functions	RO	Phantom functions is not supported Reset to 00
5	8-bit Tag Field	RO	8-bit tag field supported Reset to 1
8:6	Endpoint L0's Latency	RO	Endpoint L0's acceptable latency 000: less than 64 ns 001: 64 – 128 ns 010: 128 – 256 ns 011: 256 – 512 ns 100: 512 ns – 1 us 101: 1 – 2 us 110: 2 – 4 us 111: more than 4 us Reset to 000

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BIT	FUNCTION	TYPE	DESCRIPTION
11:9	Endpoint L1's Latency	RO	Endpoint L1's acceptable latency 000: less than 1 us 001: 1 – 2 us 010: 2 – 4 us 011: 4 – 8 us 100: 8 – 16 us 101: 16 – 32 us 110: 32 – 64 us 111: more than 64 us Reset to 000
12	Attention Button Present	RO	Reset to 0
13	Attention Indicator Present	RO	Reset to 0
14	Power Indicator Present	RO	Reset to 0
15	Role-Based Error Reporting	RO	1: Role-Based Error Reporting is supported by the bridge. Reset to 1
17:16	Reserved	RO	Reset to 000
25:18	Captured Slot Power Limit Value	RO	These bits are set by the Set_Slot_Power_Limit message Reset to 00h
27:26	Captured Slot Power Limit Scale	RO	This value is set by the Set_Slot_Power_Limit message Reset to 00
31:28	Reserved	RO	Reset to 0h

6.3.78 DEVICE CONTROL REGISTER – OFFSET B8h

BIT	FUNCTION	TYPE	DESCRIPTION
0	Correctable Error Reporting Enable	RW	Reset to 0h
1	Non-Fatal Error Reporting Enable	RW	Reset to 0h
2	Fatal Error Reporting Enable	RW	Reset to 0h
3	Unsupported Request Reporting Enable	RW	Reset to 0h
4	Relaxed Ordering Enable	RO	Relaxed Ordering is not supported Reset to 0h
7:5	Max Payload Size	RW	This field sets the maximum TLP payload size for the PI7C9X113SL 000: 128 bytes 001: 256 bytes 010: 512 bytes 011:1024 bytes 100: 2048 bytes 101: 4096 bytes 110: reserved 111: reserved Reset to 000
8	Extended Tag Field Enable	RW	Reset to 0
9	Phantom Functions Enable	RO	Phantom functions is not supported Reset to 0
10	Auxiliary Power PM Enable	RO	Auxiliary power PM is not supported Reset to 0
11	No Snoop Enable	RO	Bridge never sets the No Snoop attribute in the transaction it initiates Reset to 0

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BIT	FUNCTION	TYPE	DESCRIPTION
14:12	Maximum Read Request Size	RW	This field sets the maximum Read Request Size for the device as a requester 000: 128 bytes 001: 256 bytes 010: 512 bytes 011: 1024 bytes 100: 2048 bytes 101: 4096 bytes 110: reserved 111: reserved Reset to 2h
15	Configuration Retry Enable	RW	Reset to 0

6.3.79 DEVICE STATUS REGISTER – OFFSET B8h

BIT	FUNCTION	TYPE	DESCRIPTION
16	Correctable Error Detected	RWC	Reset to 0
17	Non-Fatal Error Detected	RWC	Reset to 0
18	Fatal Error Detected	RWC	Reset to 0
19	Unsupported Request Detected	RWC	Reset to 0
20	AUX Power Detected	RO	Reset to 1
21	Transaction Pending	RO	0: No transaction is pending on transaction layer interface 1: Transaction is pending on transaction layer interface Reset to 0
31:22	Reserved	RO	Reset to 0000000000

6.3.80 LINK CAPABILITY REGISTER – OFFSET BCh

BIT	FUNCTION	TYPE	DESCRIPTION
3:0	Maximum Link Speed	RO	Indicates the maximum speed of the Express link 0001: 2.5Gb/s link Reset to 1
9:4	Maximum Link Width	RO	Indicates the maximum width of the Express link (x1 at reset) 000000: reserved 000001: x1 000010: x2 000100: x4 001000: x8 001100: x12 010000: x16 100000: x32 Reset to 01/04h
11:10	ASPM Support	RO	This field indicates the level of Active State Power Management Support 00: reserved 01: L0's entry supported 10: reserved 11: L0's and L1's supported Reset to 11
14:12	L0's Exit Latency	RO	Reset to 3h
17:15	L1's Exit Latency	RO	The bits are RO as 0h when Clock Power Management feature is disabled, or RO as 6h when Clock Power Management feature is enabled by strapping REQ_L[3:2] to both low at deassertion of RESET_L. Reset to 0/6h

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BIT	FUNCTION	TYPE	DESCRIPTION
18	Clock Power Management Capable	RO	The bit is RO as 0 when Clock Power Management feature is disabled, or RO as 1 when Clock Power Management feature is enabled by strapping REQ_L[3:2] to both low at deassertion of RESET_L. Reset to 0/1
19	Reserved	RO	Reset to 0
20	Data Link Layer Link Active Reporting Capable	RO	Reset to 0
23:21	Reserved	RO	Reset to 0h
31:24	Port Number	RO	Reset to 00h

6.3.81 LINK CONTROL REGISTER – OFFSET C0h

BIT	FUNCTION	TYPE	DESCRIPTION
1:0	ASPM Control	RW	This field controls the level of ASPM supported on the Express link 00: disabled 01: L0's entry enabled 10: L1's entry enabled 11: L0's and L1's entry enabled Reset to 00
2	Reserved	RO	Reset to 0
3	Read Completion Boundary (RCB)	RO	Read completion boundary is not supported Reset to 0
4	Link Disable	RO	Reset to 0
5	Retrain Link	RO	Reset to 0
6	Common Clock Configuration	RW	Reset to 0
7	Extended Sync	RW	Reset to 0
8	Enable Clock Power Management	RO / RW	The bit is RO when Clock Power Management feature is disabled, or RW when Clock Power Management feature is enabled by strapping REQ_L[3:2] to both low at deassertion of RESET_L Reset to 0
15:9	Reserved	RO	Reset to 00h

6.3.82 LINK STATUS REGISTER – OFFSET C0h

BIT	FUNCTION	TYPE	DESCRIPTION
19:16	Link Speed	RO	This field indicates the negotiated speed of the Express link 001: 2.5Gb/s link Reset to 1h
25:20	Negotiated Link Width	RO	000000: reserved 000001: x1 000010: x2 000100: x4 001000: x8 001100: x12 010000: x16 100000: x32 Reset to 000001
26	Link Train Error	RO	Reset to 0
27	Link Training	RO	Reset to 0
28	Slot Clock Configuration	RO	Reset to 1
29	Data Link Layer Link Active	RO	0: Indicates the Data Link Active state 1: Indicates the Data Link Non-Active state Reset to 0

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BIT	FUNCTION	TYPE	DESCRIPTION
31:30	Reserved	RO	Reset to 0

6.3.83 RESERVED REGISTER – OFFSET C4 – C8h

6.3.84 XPIP CONFIGURATION REGISTER 0 – OFFSET CCh

BIT	FUNCTION	TYPE	DESCRIPTION
0	Hot Reset Enable	RW	Reset to 0
1	Loopback Function Enable	RW	Reset to 0
2	Cross Link Function Enable	RW	Reset to 0
3	Software Direct to Configuration State when in LTSSM state	RW	Reset to 0
4	Internal Selection for Debug Mode	RW	Reset to 0
7:5	Negotiate Lane Number of Times	RW	Reset to 3h
12:8	TS1 Number Counter	RW	Reset to 10h
14:13	Transmit N_FTS Number Control	RW	Reset to 0h
15	Compliance Pattern Parity Control	RW	Reset to 0
31:16	LTSSM Enter L1 Timer Default Value	RW	Reset to 0400h

6.3.85 XPIP CONFIGURATION REGISTER 1 – OFFSET D0h

BIT	FUNCTION	TYPE	DESCRIPTION
15:0	L0s Lifetime Timer	RW	Reset to 0800h
31:16	L1 Lifetime Timer	RW	Reset to 0400h

6.3.86 XPIP CONFIGURATION REGISTER 2 – OFFSET D4h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	CDR Recovery Time (in the number of FTS order sets)	RW	A Fast Training Sequence order set composes of one K28.5 (COM) Symbol and three K28.1 Symbols. Reset to 54h
14:8	L0's Exit to L0 Latency	RW	Reset to 2h
15	RXP/RXN Polarity Inversion Enable	RW	Reset to 1
22:16	L1 Exit to L0 Latency	RW	Reset to 19h
23	Power Down Wait Time	RW	Power management always waits a fixed time and then enters power down mode. Reset to 1
31:24	Reserved	RO	Reset to 0h

6.3.87 CAPABILITY ID REGISTER – OFFSET D8h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Capability ID for VPD Register	RO	Reset to 03h

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6.3.88 NEXT POINTER REGISTER – OFFSET D8h

BIT	FUNCTION	TYPE	DESCRIPTION
15:8	Next Pointer	RO	Next pointer (F0h, points to MSI capabilities) Reset to F0h

6.3.89 VPD REGISTER – OFFSET D8h

BIT	FUNCTION	TYPE	DESCRIPTION
17:16	Reserved	RO	Reset to 0
23:18	VPD Address for Read/Write Cycle	RW	Reset to 0
30:24	Reserved	RO	Reset to 0
31	VPD Operation	RW	0: Generate a read cycle from the EEPROM at the VPD address specified in bits [7:2] of offset D8h. This bit remains at '0' until EEPROM cycle is finished, after which the bit is then set to '1'. Data for reads is available at register ECh. 1: Generate a write cycle to the EEPROM at the VPD address specified in bits [7:2] of offset D8h. This bit remains at '1' until EEPROM cycle is finished, after which it is then cleared to '0'. Reset to 0

6.3.90 VPD DATA REGISTER – OFFSET DCh

BIT	FUNCTION	TYPE	DESCRIPTION
31:0	VPD Data	RW	VPD Data (EEPROM data [address + 0x40]) The least significant byte of this register corresponds to the byte of VPD at the address specified by the VPD address register. The data read form or written to this register uses the normal PCI byte transfer capabilities. Reset to 0

6.3.91 EXTENDED CONFIGURATION ACCESS ADDRESS REGISTER – OFFSET E0h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Register Number	RW	Reset to 00h
11:8	Extended Register Number	RW	Reset to 0h
30:12	Reserved	RO	Reset to 0

6.3.92 EXTENDED CONFIGURATION ACCESS DATA REGISTER – OFFSET E4h

BIT	FUNCTION	TYPE	DESCRIPTION
31:0	Extended Configuration Access Data	RW	Access to this register will access the internal configuration registers indexed by bit [11:0] at offset E0h Reset to 0

6.3.93 RESERVED REGISTERS – OFFSET E8h – ECh

6.3.94 MESSAGE SIGNALED INTERRUPTS ID REGISTER – F0h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Capability ID for MSI Registers	RO	Reset to 05h

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6.3.95 NEXT CAPABILITIES POINTER REGISTER – F0h

BIT	FUNCTION	TYPE	DESCRIPTION
15:8	Next Pointer	RO	Next pointer (00h indicates the end of capabilities) Reset to 00h

6.3.96 MESSAGE CONTROL REGISTER – OFFSET F0h

BIT	FUNCTION	TYPE	DESCRIPTION
16	MSI Enable	RW	0: Disable MSI and default to INTx for interrupt 1: Enable MSI for interrupt service and ignore INTx interrupt pins Reset to 0
19:17	Multiple Message Capable	RO	000: 1 message requested 001: 2 messages requested 010: 4 messages requested 011: 8 messages requested 100: 16 messages requested 101: 32 messages requested 110: reserved 111: reserved Reset to 000
22:20	Multiple Message Enable	RW	000: 1 message requested 001: 2 messages requested 010: 4 messages requested 011: 8 messages requested 100: 16 messages requested 101: 32 messages requested 110: reserved 111: reserved Reset to 000
23	64-bit Address Capable	RO	Reset to 1
31:24	Reserved	RO	Reset to 00h

6.3.97 MESSAGE ADDRESS REGISTER – OFFSET F4h

BIT	FUNCTION	TYPE	DESCRIPTION
1:0	Reserved	RO	Reset to 00
31:2	System Specified Message Address	RW	Reset to 00000000h

6.3.98 MESSAGE UPPER ADDRESS REGISTER – OFFSET F8h

BIT	FUNCTION	TYPE	DESCRIPTION
31:0	System Specified Message Upper Address	RW	Reset to 00000000h

6.3.99 MESSAGE DATA REGISTER – OFFSET FCh

BIT	FUNCTION	TYPE	DESCRIPTION
15:0	System Specified Message Data	RW	Reset to 0000h
31:16	Reserved	RO	Reset to 0000h

6.3.100 ADVANCE ERROR REPORTING CAPABILITY ID REGISTER – OFFSET 100h

BIT	FUNCTION	TYPE	DESCRIPTION
15:0	Advance Error Reporting Capability ID	RO	Reset to 0001h

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6.3.101 ADVANCE ERROR REPORTING CAPABILITY VERSION REGISTER – OFFSET 100h

BIT	FUNCTION	TYPE	DESCRIPTION
19:16	Advance Error Reporting Capability Version	RO	Reset to 1h

6.3.102 NEXT CAPABILITY OFFSET REGISTER – OFFSET 100h

BIT	FUNCTION	TYPE	DESCRIPTION
31:20	Next Capability Offset	RO	Next capability offset (150h points to VC capability) Reset to 150h

6.3.103 UNCORRECTABLE ERROR STATUS REGISTER – OFFSET 104h

BIT	FUNCTION	TYPE	DESCRIPTION
0	Training Error Status	RWCS	Reset to 0
3:1	Reserved	RO	Reset to 0
4	Data Link Protocol Error Status	RWCS	Reset to 0
11:5	Reserved	RO	Reset to 0
12	Poisoned TLP Status	RWCS	Reset to 0
13	Flow Control Protocol Error Status	RWCS	Reset to 0
14	Completion Timeout Status	RWCS	Reset to 0
15	Completer Abort Status	RWCS	Reset to 0
16	Unexpected Completion Status	RWCS	Reset to 0
17	Receiver Overflow Status	RWCS	Reset to 0
18	Malformed TLP Status	RWCS	Reset to 0
19	ECRC Error Status	RWCS	Reset to 0
20	Unsupported Request Error Status	RWCS	Reset to 0
31:21	Reserved	RO	Reset to 0

6.3.104 UNCORRECTABLE ERROR MASK REGISTER – OFFSET 108h

BIT	FUNCTION	TYPE	DESCRIPTION
0	Training Error Mast	RWS	Reset to 0
3:1	Reserved	RO	Reset to 0
4	Data Link Protocol Error Mask	RWS	Reset to 0
11:5	Reserved	RO	Reset to 0
12	Poisoned TLP Mask	RWS	Reset to 0
13	Flow Control Protocol Error Mask	RWS	Reset to 0
14	Completion Timeout Mask	RWS	Reset to 0
15	Completion Abort Mask	RWS	Reset to 0
16	Unexpected Completion Mask	RWS	Reset to 0
17	Receiver Overflow Mask	RWS	Reset to 0
18	Malformed TLP Mask	RWS	Reset to 0
19	ECRC Error Mask	RWS	Reset to 0
20	Unsupported Request Error Mask	RWS	Reset to 0
31:21	Reserved	RO	Reset to 0

6.3.105 UNCORRECTABLE ERROR SEVERITY REGISTER – OFFSET 10Ch

BIT	FUNCTION	TYPE	DESCRIPTION
0	Training Error Severity	RWS	Reset to 1

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BIT	FUNCTION	TYPE	DESCRIPTION
3:1	Reserved	RO	Reset to 0
4	Data Link Protocol Error Severity	RWS	Reset to 1
11:5	Reserved	RO	Reset to 0
12	Poisoned TLP Severity	RWS	Reset to 0
13	Flow Control Protocol Error Severity	RWS	Reset to 1
14	Completion Timeout Severity	RWS	Reset to 0
15	Completer Abort Severity	RWS	Reset to 0
16	Unexpected Completion Severity	RWS	Reset to 0
17	Receiver Overflow Severity	RWS	Reset to 1
18	Malformed TLP Severity	RWS	Reset to 1
19	ECRC Error Severity	RWS	Reset to 0
20	Unsupported Request Error Severity	RWS	Reset to 0
31:21	Reserved	RO	Reset to 0

6.3.106 CORRECTABLE ERROR STATUS REGISTER – OFFSET 110h

BIT	FUNCTION	TYPE	DESCRIPTION
0	Receiver Error Status	RWCS	Reset to 0
5:1	Reserved	RO	Reset to 0
6	Bad TLP Status	RWCS	Reset to 0
7	Bad DLLP Status	RWCS	Reset to 0
8	REPLAY_NUM Rollover Status	RWCS	Reset to 0
11:9	Reserved	RO	Reset to 0
12	Replay Timer Timeout Status	RWCS	Reset to 0
13	Advisory Non-Fatal Error Status	RWCS	Reset to 0
31:14	Reserved	RO	Reset to 0

6.3.107 CORRECTABLE ERROR MASK REGISTER – OFFSET 114h

BIT	FUNCTION	TYPE	DESCRIPTION
0	Receiver Error Mask	RWS	Reset to 0
5:1	Reserved	RO	Reset to 0
6	Bad TLP Mask	RWS	Reset to 0
7	Bad DLLP Mask	RWS	Reset to 0
8	REPLAY_NUM Rollover Mask	RWS	Reset to 0
11:9	Reserved	RO	Reset to 0
12	Replay Timer Timeout Mask	RWS	Reset to 0
13	Advisory Non-Fatal Error Mask	RWS	This bit is set by default to be compatible with software that does not comprehend Role-Based Error Reporting Reset to 1
31:14	Reserved	RO	Reset to 0

6.3.108 ADVANCED ERROR CAPABILITIES AND CONTROL REGISTER – OFFSET 118h

BIT	FUNCTION	TYPE	DESCRIPTION
4:0	First Error Pointer	ROS	Reset to 0h
5	ECRC Generation Capable	RO	Reset to 1
6	ECRC Generation Enable	RWS	Reset to 0
7	ECRC Check Capable	RO	Reset to 1
8	ECRC Check Enable	RWS	Reset to 0
31:9	Reserved	RO	Reset to 0

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6.3.109 HEADER LOG REGISTER 1 – OFFSET 11Ch

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Header Byte 3	ROS	Reset to 0
15:8	Header Byte 2	ROS	Reset to 0
23:16	Header Byte 1	ROS	Reset to 0
31:24	Header Byte 0	ROS	Reset to 0

6.3.110 HEADER LOG REGISTER 2 – OFFSET 120h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Header Byte 7	ROS	Reset to 0
15:8	Header Byte 6	ROS	Reset to 0
23:16	Header Byte 5	ROS	Reset to 0
31:24	Header Byte 4	ROS	Reset to 0

6.3.111 HEADER LOG REGISTER 3 – OFFSET 124h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Header Byte 11	ROS	Reset to 0
15:8	Header Byte 10	ROS	Reset to 0
23:16	Header Byte 9	ROS	Reset to 0
31:24	Header Byte 8	ROS	Reset to 0

6.3.112 HEADER LOG REGISTER 4 – OFFSET 128h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Header Byte 15	ROS	Reset to 0
15:8	Header Byte 14	ROS	Reset to 0
23:16	Header Byte 13	ROS	Reset to 0
31:24	Header Byte 12	ROS	Reset to 0

6.3.113 SECONDARY UNCORRECTABLE ERROR STATUS REGISTER – OFFSET 12Ch

BIT	FUNCTION	TYPE	DESCRIPTION
0	Target Abort on Split Completion Status	RWCS	Reset to 0
1	Master Abort on Split Completion Status	RWCS	Reset to 0
2	Received Target Abort Status	RWCS	Reset to 0
3	Received Master Abort Status	RWCS	Reset to 0
4	Reserved	RO	Reset to 0
5	Unexpected Split Completion Error Status	RWCS	Reset to 0
6	Uncorrectable Split Completion Message Data Error Status	RWCS	Reset to 0
7	Uncorrectable Data Error Status	RWCS	Reset to 0
8	Uncorrectable Attribute Error Status	RWCS	Reset to 0
9	Uncorrectable Address Error Status	RWCS	Reset to 0
10	Delayed Transaction Discard Timer Expired Status	RWCS	Reset to 0
11	PERR_L Assertion Detected Status	RWCS	Reset to 0
12	SERR_L Assertion Detected Status	RWCS	Reset to 0

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BIT	FUNCTION	TYPE	DESCRIPTION
13	Internal Bridge Error Status	RWCS	Reset to 0
31:14	Reserved	RO	Reset to 0

6.3.114 SECONDARY UNCORRECTABLE ERROR MASK REGISTER – OFFSET 130h

BIT	FUNCTION	TYPE	DESCRIPTION
0	Target Abort on Split Completion Mask	RWS	Reset to 0
1	Master Abort on Split Completion Mask	RWS	Reset to 0
2	Received Target Abort Mask	RWS	Reset to 0
3	Received Master Abort Mask	RWS	Reset to 1
4	Reserved	RO	Reset to 0
5	Unexpected Split Completion Error Mask	RWS	Reset to 1
6	Uncorrectable Split Completion Message Data Error Mask	RWS	Reset to 0
7	Uncorrectable Data Error Mask	RWS	Reset to 1
8	Uncorrectable Attribute Error Mask	RWS	Reset to 1
9	Uncorrectable Address Error Mask	RWS	Reset to 1
10	Delayed Transaction Discard Timer Expired Mask	RWS	Reset to 1
11	PERR_L Assertion Detected Mask	RWS	Reset to 0
12	SERR_L Assertion Detected Mask	RWS	Reset to 1
13	Internal Bridge Error Mask	RWS	Reset to 0
31:14	Reserved	RO	Reset to 0

6.3.115 SECONDARY UNCORRECTABLE ERROR SEVERITY REGISTER – OFFSET 134h

BIT	FUNCTION	TYPE	DESCRIPTION
0	Target Abort on Split Completion Severity	RWS	Reset to 0
1	Master Abort on Split Completion Severity	RWS	Reset to 0
2	Received Target Abort Severity	RWS	Reset to 0
3	Received Master Abort Severity	RWS	Reset to 0
4	Reserved	RO	Reset to 0
5	Unexpected Split Completion Error Severity	RWS	Reset to 0
6	Uncorrectable Split Completion Message Data Error Severity	RWS	Reset to 1
7	Uncorrectable Data Error Severity	RWS	Reset to 0
8	Uncorrectable Attribute Error Severity	RWS	Reset to 1
9	Uncorrectable Address Error Severity	RWS	Reset to 1
10	Delayed Transaction Discard Timer Expired Severity	RWS	Reset to 0
11	PERR_L Assertion Detected Severity	RWS	Reset to 0
12	SERR_L Assertion Detected Severity	RWS	Reset to 1

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BIT	FUNCTION	TYPE	DESCRIPTION
13	Internal Bridge Error Severity	RWS	Reset to 0
31:14	Reserved	RO	Reset to 0

6.3.116 SECONDARY ERROR CAPABILITY AND CONTROL REGISTER – OFFSET 138h

BIT	FUNCTION	TYPE	DESCRIPTION
4:0	Secondary First Error Pointer	ROS	Reset to 0
31:5	Reserved	RO	Reset to 0

6.3.117 SECONDARY HEADER LOG REGISTER – OFFSET 13Ch – 148h

BIT	FUNCTION	TYPE	DESCRIPTION
35:0	Transaction Attribute	ROS	Transaction attribute, CBE [3:0] and AD [31:0] during attribute phase Reset to 0
39:36	Transaction Command Lower	ROS	Transaction command lower, CBE [3:0] during first address phase Reset to 0
43:40	Transaction Command Upper	ROS	Transaction command upper, CBE [3:0] during second address phase of DAC transaction Reset to 0
63:44	Reserved	ROS	Reset to 0
95:64	Transaction Address	ROS	Transaction address, AD [31:0] during first address phase Reset to 0
127:96	Transaction Address	ROS	Transaction address, AD [31:0] during second address phase of DAC transaction Reset to 0

6.3.118 RESERVED REGISTER – OFFSET 14Ch

6.3.119 VC CAPABILITY ID REGISTER – OFFSET 150h

BIT	FUNCTION	TYPE	DESCRIPTION
15:0	VC Capability ID	RO	Reset to 0002h

6.3.120 VC CAPABILITY VERSION REGISTER – OFFSET 150h

BIT	FUNCTION	TYPE	DESCRIPTION
19:16	VC Capability Version	RO	Reset to 0001

6.3.121 NEXT CAPABILITY OFFSET REGISTER – OFFSET 150h

BIT	FUNCTION	TYPE	DESCRIPTION
31:20	Next Capability Offset	RO	Next capability offset – the end of capabilities Reset to 0

6.3.122 PORT VC CAPABILITY REGISTER 1 – OFFSET 154h

BIT	FUNCTION	TYPE	DESCRIPTION
2:0	Extended VC Count	RO	Reset to 0
3	Reserved	RO	Reset to 0
6:4	Low Priority Extended VC Count	RO	Reset to 0

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BIT	FUNCTION	TYPE	DESCRIPTION
7	Reserved	RO	Reset to 0
9:8	Reference Clock	RO	Reset to 0
11:10	Port Arbitration Table Entry Size	RO	Reset to 0
31:12	Reserved	RO	Reset to 0

6.3.123 PORT VC CAPABILITY REGISTER 2 – OFFSET 158h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	VC Arbitration Capability	RO	Reset to 0
23:8	Reserved	RO	Reset to 0
31:24	VC Arbitration Table Offset	RO	Reset to 0

6.3.124 PORT VC CONTROL REGISTER – OFFSET 15Ch

BIT	FUNCTION	TYPE	DESCRIPTION
0	Load VC Arbitration Table	RO	Reset to 0
3:1	VC Arbitration Select	RO	Reset to 0
15:4	Reserved	RO	Reset to 0

6.3.125 PORT VC STATUS REGISTER – OFFSET 15Ch

BIT	FUNCTION	TYPE	DESCRIPTION
16	VC Arbitration Table Status	RO	Reset to 0
31:17	Reserved	RO	Reset to 0

6.3.126 VC0 RESOURCE CAPABILITY REGISTER – OFFSET 160h

BIT	FUNCTION	TYPE	DESCRIPTION
7:0	Port Arbitration Capability	RO	Reset to 0
13:8	Reserved	RO	Reset to 0
14	Advanced Packet Switching	RO	Reset to 0
15	Reject Snoop Transactions	RO	Reset to0
22:16	Maximum Time Slots	RO	Reset to 0
23	Reserved	RO	Reset to 0
31:24	Port Arbitration Table Offset	RO	Reset to 0

6.3.127 VC0 RESOURCE CONTROL REGISTER – OFFSET 164h

BIT	FUNCTION	TYPE	DESCRIPTION
0	TC / VC Map	RO	For TC0 Reset to 1
7:1	TC / VC Map	RW	For TC7 to TC1 Reset to 7Fh
15:8	Reserved	RO	Reset to 0
16	Load Port Arbitration Table	RO	Reset to 0
19:17	Port Arbitration Select	RO	Reset to 0
23:20	Reserved	RO	Reset to 0
26:24	VC ID	RO	Reset to 0
30:27	Reserved	RO	Reset to 0
31	VC Enable	RO	Reset to 1

6.3.128 VC0 RESOURCE STATUS REGISTER – OFFSET 168h

BIT	FUNCTION	TYPE	DESCRIPTION
0	Port Arbitration Table 1	RO	Reset to 0
1	VC0 Negotiation Pending	RO	Reset to 0
31:2	Reserved	RO	Reset to 0

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6.3.129 RESERVED REGISTERS – OFFSET 16Ch – 2FCh

6.3.130 EXTENDED GPIO DATA AND CONTROL REGISTER – OFFSET 300h

BIT	FUNCTION	TYPE	DESCRIPTION
2:0	Extended GPIO Output Write-1-to-Clear	RW	Reset to 0
5:3	Extended GPIO Output Write-1-to-Set	RW	Reset to 0
8:6	Extended GPIO Output Enable Write-1-to-Clear	RW	Reset to 0
11:9	Extended GPIO Output Enable Write-1-to-Set	RW	Reset to 0
14:12	Extended GPIO Input Data Register	RO	Reset to 0
31:15	Reserved	RO	Reset to 0

6.3.131 EXTENDED GPI/GPO DATA AND CONTROL REGISTER – OFFSET 304h

BIT	FUNCTION	TYPE	DESCRIPTION
2:0	Extended GPO Output Write-1-to-Clear	RW	GPI/GPO Data and Control Register is only valid when external arbiter is used. Reset to 0
5:3	Extended GPO Output Write-1-to-Set	RW	Reset to 0
7:6	Reserved	RO	Reset to 0
10:8	Extended GPO Output Enable Write-1-to-Clear	RW	Reset to 0
13:11	Extended GPO Output Enable Write-1-to-Set	RW	Reset to 0
15:14	Reserved	RO	Reset to 0
18:16	Extended GPI Input Data Register	RO	Reset to 0
31:19	Reserved	RO	Reset to 0

6.3.132 RESERVED REGISTERS – OFFSET 308h – 30Ch

6.3.133 REPLAY AND ACKNOWLEDGE LATENCY TIMERS – OFFSET 310h

BIT	FUNCTION	TYPE	DESCRIPTION
11:0	Replay Timer	RW	Replay Timer Reset to 115h
12	Replay Timer Enable	RW	Replay Timer Enable Reset to 0
15:13	Reserved	RO	Reset to 0
29:16	Acknowledge Latency Timer	RW	Acknowledge Latency Timer Reset to CDh
30	Acknowledge Latency Timer Enable	RW	Acknowledge Latency Timer Enable Reset to 0
31	Reserved	RO	Reset to 0

6.3.134 RESERVED REGISTERS – OFFSET 314h – FFCh

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7 GPIO PINS AND SM BUS ADDRESS

GPIO[3:0] are defined for SMBUS device ID if TM0=1.

GPIO[3:0] can be further defined to serve other functions in the further generations.

With 128QFP package, additional three GPI and three GPO pins can be used when external arbiter is selected, and REQ_L[3:1] and GNT_L[3:1] will be mapped to GPI[2:0] and GPO[2:0] respectively.

The address-strapping table of SMBUS with GPIO [3:0] pins is defined in the following table:

Table 7-1 SM Bus Device ID Strapping

SM Bus Address Bit	SM Bus device ID
Address bit [7]	= 1
Address bit [6]	= 1
Address bit [5]	= 0
Address bit [4]	= GPIO [3]
Address bit [3]	= GPIO [2]
Address bit [2]	= GPIO [1]
Address bit [1]	= GPIO [0]

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8 CLOCK SCHEME

PCI Express Interface:
PI7C9X113SL requires 100MHz differential clock inputs through the pins of REFCLKP and REFCLKN.

PCI Interface:
PI7C9X113SL generates four clock outputs, from either external clock input (1MHz to 66MHz) at CLKIN or internal clock generator:

PI7C9X113SL can use configuration control to enable or disable the secondary clock output: CLKOUT[3:0].

PI7C9X113SL used either internally feedbacked clock from CLKOUT[0] or external clock input applied at CLKOUT[0], for internal secondary interface logic.

For using internal clock source, the internal clock generator needs to be enabled with CLKIN driven high or low. CLKIN and M66EN signals become the selection for PCI Frequency at 50MHz/25MHz or 66MHz/33MHz.

Table 8-1 Frequency of PCI CLKOUT with Internal Clock Source:

CLKIN	M66EN	PCI Clock
0	0	33MHz
0	1	66MHz
1	0	25MHz
1	1	50MHz

The PI7C9X113SL PCI Clock Outputs, CLKOUT [3:0], can be enabled or disabled through the configuration register.

PI7C9X113SL supports three different implementations of PCI clock.

- Internal clock generator, and internal clock buffering.
  - Internal feedback
  - External feedback
- External clock source, and internal clock buffering.
  - Internal feedback
  - External feedback
- External clock source, and external clock buffering.

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Figure 8-1 Topology of Internal Clock Generator and Internal Clock Buffering – Internal Feedback Mode

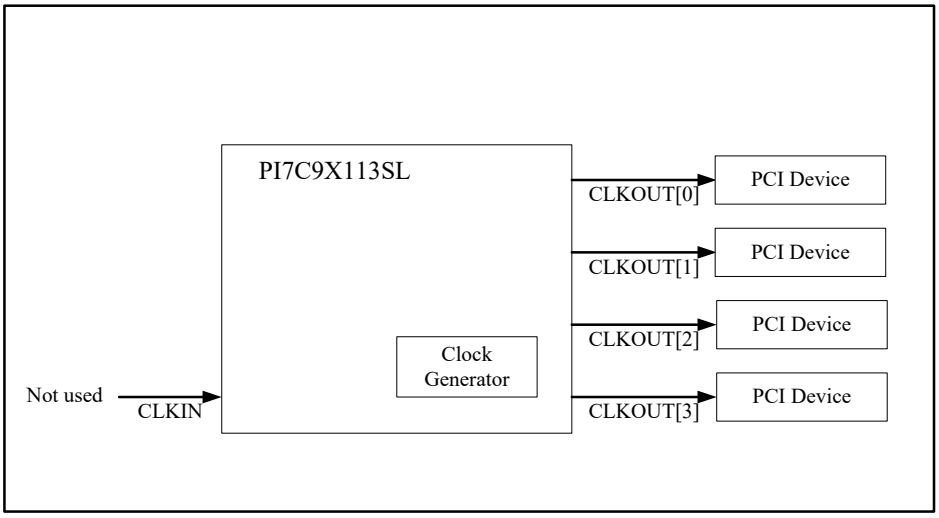


Figure 8-2 Topology of Internal Clock Generator and Internal Clock Buffering – External Feedback Mode

Note: Drawing removed. Please refer to item #5 of PI7C9X113SL Errata.

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Figure 8-3 Topology of External Clock Generator and Internal Clock Buffering – Internal Feedback Mode

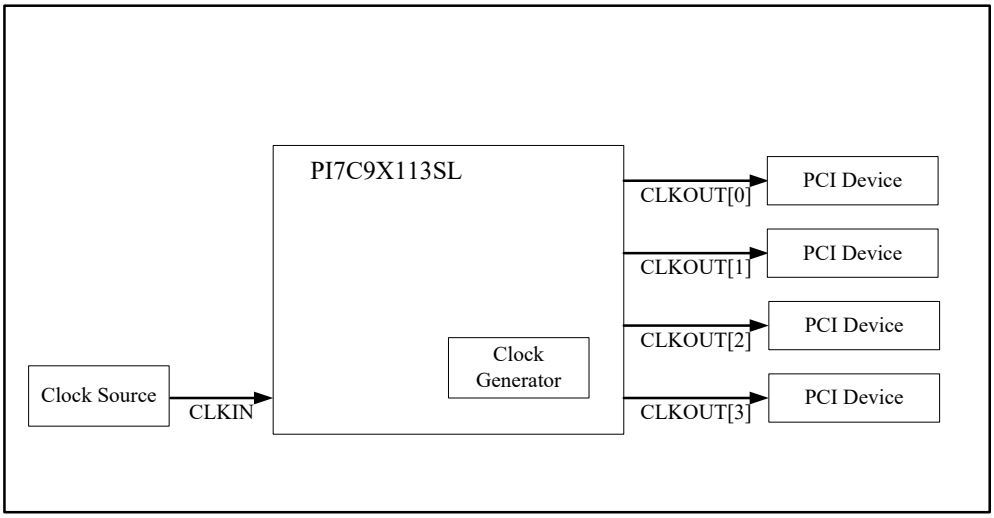


Figure 8-4 Topology of External Clock Generator and Internal Clock Buffering – External Feedback Mode

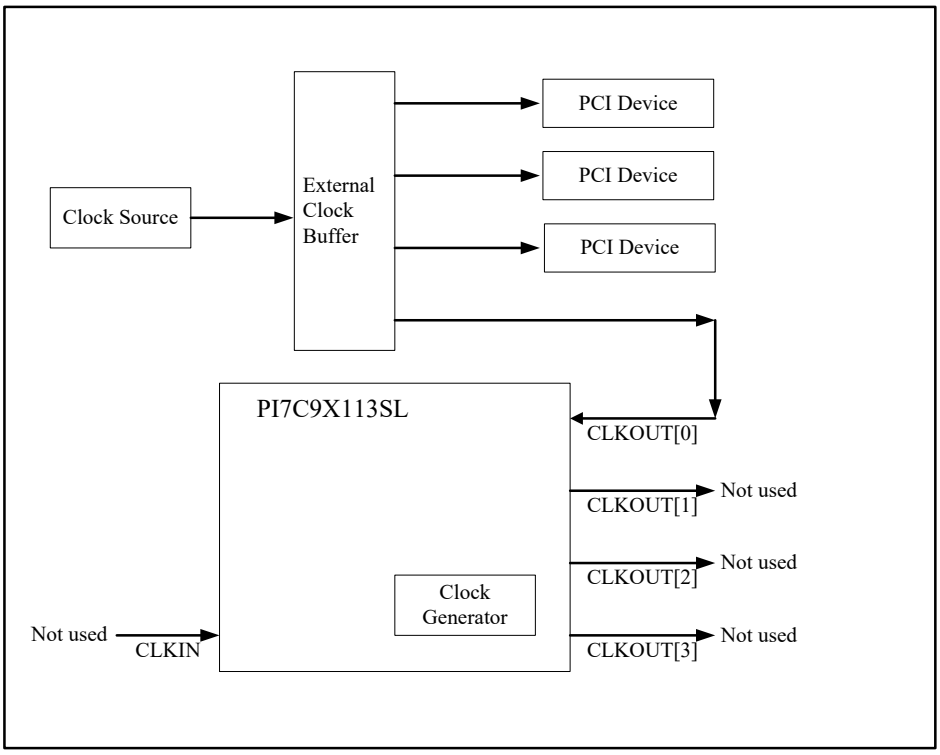
Note: Drawing removed. Please refer to item #5 of PI7C9X113SL Errata.

In this configuration, user simply connects the external clock source to CLKIN pin. And user needs to make sure the clock is preset (toggling) before the fundamental reset de-asserted (e.g. PERST_L). In this mode, the frequency is the same as the input clock source.

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Figure 8-5 Topology of External Clock Generator and External Clock Buffering



In this configuration, user simply connects the external clock from the clock buffers to CLKOUT0. And user needs to make sure the clock is preset (toggling) before the fundamental reset de-asserted (e.g. PERST_L deassertion).

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9 INTERRUPTS

PI7C9X113SL supports interrupt message packets on PCIe side. PI7C9X113SL supports PCI interrupt (INTA, B, C, D) pins or MSI (Message Signaled Interrupts) on PCI side. PCI interrupts and MSI are mutually exclusive. In order words, if MSI is enabled, PCI interrupts will be disabled. PI7C9X113SL support 64-bit addressing MSI.

PI7C9X113SL maps the PCI interrupts pins or MSI if enable on PCI side to interrupt message packets on PCIe side.

There are eight interrupt message packets. They are Assert_INTA, Assert_INTB, Assert_INTC, Assert_INTD, Deassert_INTA, Deassert_INTB, Deassert_INTC, and Deassert_INTD. PI7C9X113SL tracks the PCI interrupt (INTA, INTB, INTC, and INTD) pins and maps them to the eight interrupt messages. See Table 9-1 for interrupt mapping information.

Table 9-1 PCI Interrupt to PCIe Interrupt Message Mapping in Forward Bridge Mode

PCI Interrupts (from sources of interrupts)	PCIe Interrupt message packets (to host controller)
INTA	INTA message
INTB	INTB message
INTC	INTC message
INTD	INTD message

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10 EEPROM (I2C) INTERFACE AND SYSTEM MANAGEMENT BUS

10.1 EEPROM (I2C) INTERFACE

PI7C9X113SL supports EEPROM interface through I2C bus. In EEPROM interface, pin 4 is the EEPROM clock (SCL) and pin 6 is the EEPROM data (SDL). TM1 and TM0 are strapped accordingly to select EEPROM interface or System Management Bus. EEPROM (I2C) interface is enabled with TM1=0 and TM0=0. When EEPROM interface is selected, SCL is an output. SCL is the I2C bus clock to the I2C device. In addition, SDL is a bi-directional signal for sending and receiving data.

10.2 SYSTEM MANAGEMENT BUS

PI7C9X113SL supports SM bus protocol if TM1=0 and TM0=1. In addition, SMBCLK (pin 4) and SMBDAT (pin 6) are utilized as the clock and data pins respectively for the SM bus.

When SM bus interface is selected, SMBCLK pin is an input for the clock of SM bus and SMBDAT pin is an open drain buffer that requires external pull-up resistor for proper operation.

10.3 EEPROM AUTOLOAD CONFIGURATION

EEPROM Byte Addresses	Cfg Offset	Description
00-01h		EEPROM signature: Autoload will only proceed if it reads a value of 1516h on the first word loaded.
02h		Region Enable: Enables or disables certain regions of PCI configuration space from being loaded from the EEPROM. bit 0: reserved bit 4-1: 0000=stop autoload at offset 0Bh: Group 1 0001=stop autoload at offset 67h: Group 2 0011=stop autoload at offset AFh: Group 3 0111=stop autoload at offset D7h: Group 4 other combinations are undefined bit 7-5: reserved
03h		Enable Miscellaneous functions: (for transparent mode only) bit 0: ISA Enable control bit write protect: when this bit is set, 9x111 will change the bit 2 of 3Eh into RO, and ISA enable feature will not be available.
04-05h	00-01h	Vendor ID
06-07h	02-03h	Device ID
08h	08h	Revision ID
09h	09h	Class Code: low bytes of Class Code register
0A-0Bh	0A-0Bh	Class Code higher bytes: upper bytes of Class Code register
0Ch	34h	Capability Pointer
0D-0Eh	40-41h	PCI data prefetching control
0F-10h	42-43h	Chip control 0
11-14h	48-4Bh	Arbiter Mode/Enable/Priority
15-18h	68-6Bh	PCIE Transmitter/Receiver control
19-1Ah	81-82h	PCIX Capability
1Bh	108h	Uncorrectable Error Mask register
1C-1Eh	91-93h	Power Management Capability
1F-21h	A1-A3h	SI Capability
22-25h	A4-A7h	Secondary Clock and Clkrun Control
26-29h	A8-ABh	SSID/SSVID Capability
2A-2Dh	AC-AFh	SSID/SSVID
2E-30h	B1-B3h	PCI Express Capabilities
31-34h	B4-B7h	Device Capabilities
35-38h	BC-BFh	Link Capabilities
39-3Ch	C4-C7h	Slot Capabilities

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EEPROM Byte Addresses	Cfg Offset	Description
3D-40h	CC-CFh	XPIP Configuration Register 0
41-44h	D0-D3h	XPIP Configuration Register 1
45-48h	D4-D7h	XPIP Configuration Register 2
49-4Ah	D9-DAh	VPD Capability
4B-4Ch	F1-F2h	MSI Capability
4Dh	100h	Advance Error Reporting Capability
4E-4Fh	109-10Ah	Uncorrectable Error Mask register
50-51h	E0-E1h	Extended Cfg Access Address
52-55h	E4-E7h	Extended Cfg Access Data
56-57h	E0-E1h	Extended Cfg Access Address
58-5Bh	E4-E7h	Extended Cfg Access Data
5C-5Dh	E0 E1h	Extended Cfg Access Address
5E-61h	E4-E7h	Extended Cfg Access Data
62-63h	E0 E1h	Extended Cfg Access Address
64-67h	E4-E7h	Extended Cfg Access Data
68-77h		Reserved
79-7Bh	79-7Bh	GPIO Data and Control
7C-7Dh		Reserved
7Eh	86h	PCIX Bridge status
7F-82h	88-8Bh	Upstream Split Transaction
83-86h	8C-8Fh	Downstream Split Transaction
87-8Ah	94-97h	PM Control and Status
8B-8Eh	B4-B7h	Device Capabilities
8F-91h	B8-BAh	Device Control/Status
92h		Reserved
93h	C0h	Link Control/Status
94h		Reserved
95-96h	C2-C3h	Link Control/Status
97-98h	C8-C9h	Slot Control/Status
99-9Ah	3C-3Dh	Interrupt Control
9B-9Eh	DC-DFh	VPD data
9F-A2h	F4-F7h	Message Address
A3-A6h	F8-FBh	Message Upper Address
A7-A8h	FC-FDh	Message Data
A9h		Reserved
AA-ABh	7C-7Dh	Sec Interrupt Control
AC-ADh	310-311h	Replay Timer
AE-AFh	312-313h	Ack Latency Timer
B0-B3h	04-07h	Command/Status
B4-B6h	0C-0Eh	Cacheline/Primary Latency Timer/Header Type
B7h		Reserved
B8-BBh	18-1Bh	Bus Number/Secondary Latency Timer
BC-BFh	1C-1Fh	I/O Base/Limit / Secondary Status
C0-C3h	20-23h	Memory Base/Limit
C4-C7h	24-27h	Prefetch Memory Base/Limit
C8-CBh	28-2Bh	Prefetch Upper 32 Base
CC-CFh	2C-2Fh	Prefetch Upper 32 Limit
D0-D3h	30-33h	I/O Upper 16 Base/Limit
D4-D5h		Reserved
D6-D7h	3E-3Fh	Bridge Control
D8-FFh		Reserved

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11 RESET SCHEME

PI7C9X113SL requires the fundamental reset (PERST_L) input for internal logic. Also, PI7C9X113SL has a power-on-reset (POR) circuit to detect VDDCAUX power supply for auxiliary logic control.

- Cold Reset:

A cold reset is a fundamental or power-on reset that occurs right after the power is applied to PI7C9X113SL (during initial power up). See section 7.1.1 of PCI Express to PCI Bridge Specification, Revision 1.0 for details.

- Warm Reset:

A warm reset is a reset that triggered by the hardware without removing and re-applying the power sources to PI7C9X113SL.

- Hot Reset:

A hot reset is a reset that used an in-band mechanism for propagating reset across a PCIe link to PI7C9X113SL. PI7C9X113SL will enter to training control reset when it receives two consecutive TS1 or TS2 order-sets with reset bit set.

- DL_DOWN Reset:

If the PCIe link goes down, the Transaction and Data Link Layer will enter DL_DOWN status. PI7C9X113SL discards all transactions and returns all logic and registers to initial state except the sticky registers.

Upon receiving reset (cold, warm, hot, or DL_DOWN) on PCIe interface, PI7C9X113SL will generate PCI reset (RESET_L) to the downstream devices on the PCI bus in forward bridge mode. The PCI reset de-assertion follows the de-assertion of the reset received from PCIe interface. The reset bit of Bridge Control Register may be set depending on the application. PI7C9X113SL will tolerant to receive and process SKIP order-sets at an average interval between 1180 to 1538 Symbol Times. PI7C9X113SL does not keep PCI reset active when VD33 power is off even though VAUX (3.3v) is supported. It is recommended to add a weak pull-down resistor on its application board to ensure PCI reset is low when VD33 power is off (see section 7.3.2 of PCI Bus Power management Specification Revision 1.1).

PI7C9X113SL transmits one Electrical Idle order-set and enters to Electrical Idle.

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12 IEEE 1149.1 COMPATIBLE JTAG CONTROLLER

An IEEE 1149.1 compatible Test Access Port (TAP) controller and associated TAP pins are provided to support boundary scan in PI7C9X113SL for board-level continuity test and diagnostics. The supported TAP pins are TCK, TDI, TDO and TMS. All digital input, output, input/output pins are tested except TAP pins.

The IEEE 1149.1 Test Logic consists of a TAP controller, an instruction register, and a group of test data registers including Bypass and Boundary Scan registers. The TAP controller is a synchronous 16-state machine driven by the Test Clock (TCK) and the Test Mode Select (TMS) pins. An independent power on reset circuit is provided to ensure the machine is in TEST_LOGIC_RESET state at power-up. The JTAG signal lines are not active when the PCI resource is operating PCI bus cycles.

12.1 INSTRUCTION REGISTER

PI7C9X113SL implements a 5-bit Instruction register to control the operation of the JTAG logic. The defined instruction codes are shown in Table 14-1. Those bit combinations that are not listed are equivalent to the BYPASS (11111) instruction:

Table 12-1 Instruction Register Codes

Instruction	Operation Code (binary)	Register Selected	Operation
EXTEST	00000	Boundary Scan	Drives / receives off-chip test data
SAMPLE	00001	Boundary Scan	Samples inputs / pre-loads outputs
HIGHZ	00101	Bypass	Tri-states output and I/O pins except TDO pin
CLAMP	00100	Bypass	Drives pins from boundary-scan register and selects Bypass register for shifts
IDCODE	01100	Device ID	Accesses the Device ID register, to read manufacturer ID, part number, and version number
BYPASS	11111	Bypass	Selected Bypass Register
INT_SCAN	00010	Internal Scan	Scan test
MEM_BIST	01010	Memory BIST	Memory BIST test

12.2 BYPASS REGISTER

The required bypass register (one-bit shift register) provides the shortest path between TDI and TDO when a bypass instruction is in effect. This allows rapid movement of test data to and from other components on the board. This path can be selected when no test operation is being performed on the PI7C9X113SL.

12.3 DEVICE ID REGISTER

This register identifies Pericom as the manufacturer of the device and details the part number and revision number for the device.

Table 12-2 JTAG Device ID Register

Bit	Type	Value	Description
31:28	RO	01h	Version number
27:12	RO	E110h	Last 4 digits (hex) of the die part number
11:1	RO	23Fh	Pericom identifier assigned by JEDEC
0	RO	1b	Fixed bit equal to 1'b1

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12.4 BOUNDARY SCAN REGISTER

The boundary scan register has a set of serial shift-register cells. A chain of boundary scan cells is formed by connected the internal signal of the PI7C9X113SL package pins. The VDD, VSS, and JTAG pins are not in the boundary scan chain. The input to the shift register is TDI and the output from the shift register is TDO. There are 4 different types of boundary scan cells, based on the function of each signal pin.

The boundary scan register cells are dedicated logic and do not have any system function. Data may be loaded into the boundary scan register master cells from the device input pins and output pin-drivers in parallel by the mandatory SAMPLE and EXTEST instructions. Parallel loading takes place on the rising edge of TCK.

12.5 JTAG BOUNDARY SCAN REGISTER ORDER

TBD

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13 POWER MANAGEMENT

PI7C9X113SL supports D0, D3-hot, D3-cold Power States. D1 and D2 states are not supported. The PCI Express Physical Link Layer of the PI7C9X113SL device supports the PCI Express Link Power Management with L0, L0s, L1, L2/L3 ready and L3 Power States. For the PCI Port of PI7C9X113SL, it supports the standard PCI Power Management States with B0, B1, B2 and B3.

During D3-hot state, the main power supplies of VDDP, VDDC, and VD33 can be turned off to save power while keeping the VDDAUX, VDDCAUX, and VAUX with the auxiliary power supplies to maintain all necessary information to be restored to the full power D0 state. PI7C9X113SL has been designed to have sticky registers that are powered by auxiliary power supplies. PME_L pin allows PCI devices to request power management state changes. Along with the operating system and application software, PCI devices can achieve optimum power saving by using PME_L. PI7C9X113SL converts PME_L signal information to power management messages to the upstream switches or root complex.

PI7C9X113SL also supports ASPM (Active State Power Management) to facilitate the link power saving.

PI7C9X113SL supports WAKE_L signal but does not support beacon generation during power management.

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14 POWER SEQUENCING

The PI7C9X113SL requires two voltages: 3.3V I/O voltage and 1.1V core voltage. The 1.1V VDDCAUX is consider the same as core voltage, and can be combined as one. When designing the power supplies for PI7C9X113SL, the user can either apply all voltages at the same time, or turn on the higher voltage (3.3V) first, followed by the lower voltages (1.1V) within suggested limits. If all power rails are not applied at the same time, the PI7C9X113SL will not be damaged as long as 3.3V is applied either before or at the same time as 1.1V.

During power cycle, if there is a delay in applying 1.1V core voltage after the 3.3V is applied, the internal logic might be placed in an unknown state if the power off period is not long enough to cause PI7C9X113SL totally discharged. This condition in turn may produce undetermined I/O states on some pins. If the core logic is totally discharged before applying 3.3V, then all bi-directional I/O pins will stay at their default states.

The typical time for PI7C9X113SL to discharge completely is less than 3 seconds, but in extreme cases this period can be as long as 50 seconds. Certain precautions should be made if the delay between 3.3V and 1.1V is larger than 50us. Figure 14-1 below shows the I/O timing sequence with undetermined I/O state, and Figure 14-2 shows the recommended power sequence timing.

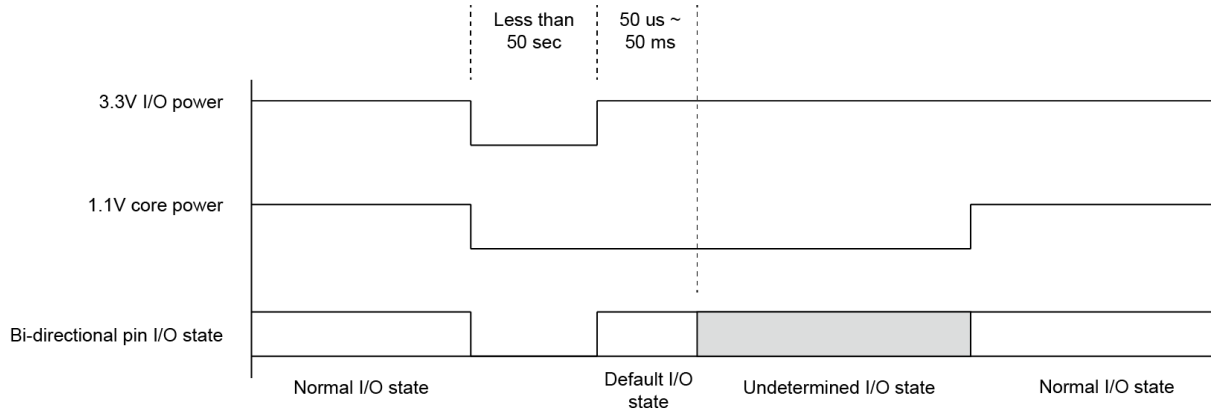


Figure 14-1 Timing Sequence with Undetermined I/O State

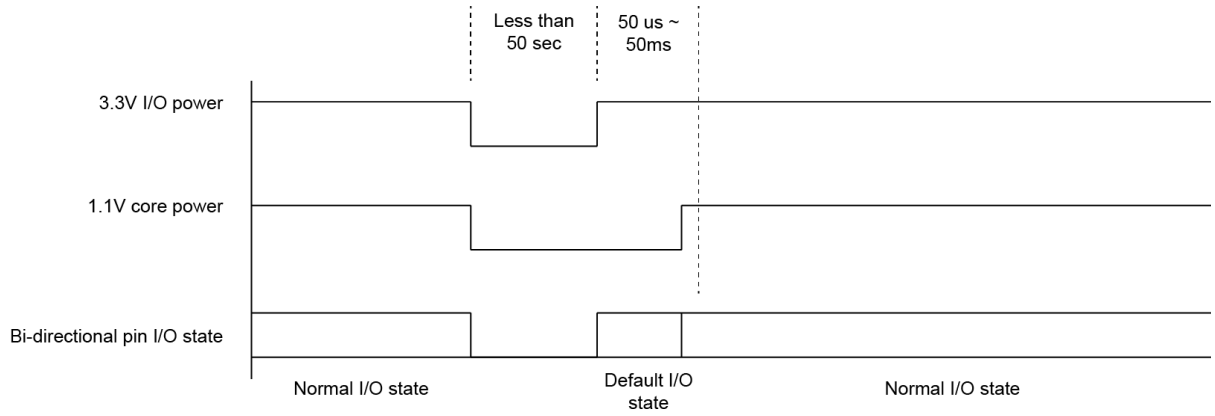


Figure 14-2 Recommended Power Sequence

If the gap between 3.3V IO power and 1.1V core power is too big, there might be glitch at pin RESET_L. The maximum gap is recommended to be 50us~50ms, customer needs to measure the waveform of RESET_L to make sure there is no glitch during the gap

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14.1 INITIAL POWER-UP (G3 TO L0)

As long as PERST# is active, all PCI Express functions are held in reset. The main supplies ramp up to their specified levels (3.3 V and 12 V). Sometime during this stabilization time, the REFCLK starts and stabilizes. After there has been time (T_{PVPERL}) for the power and clock to become stable, PERST# is deasserted high and the PCI Express functions can start up.

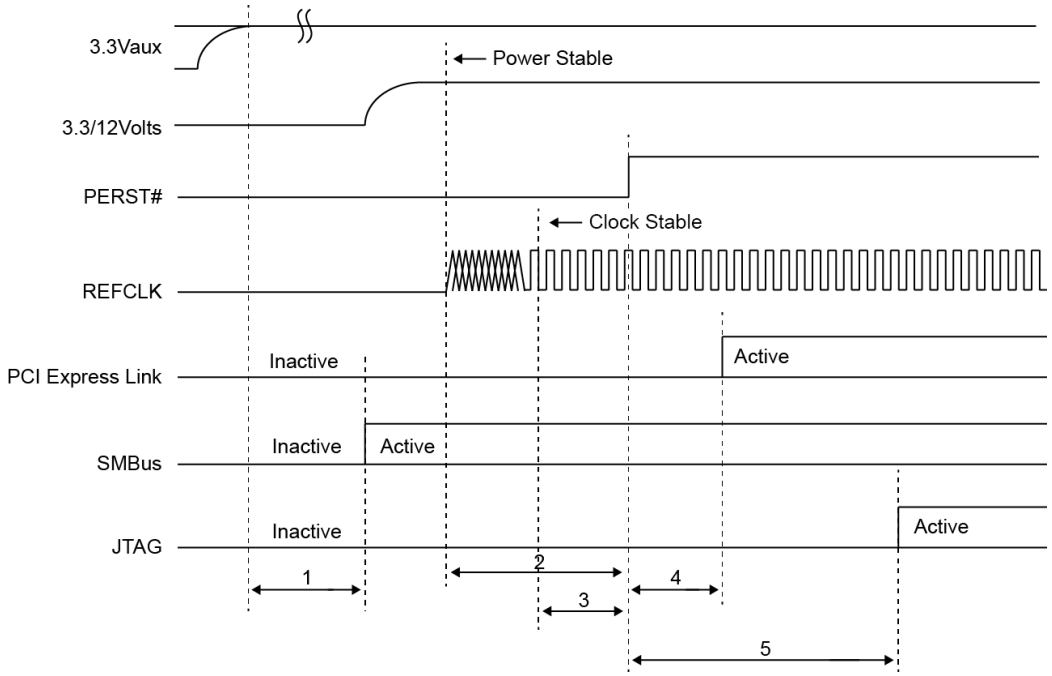


Figure 14-3 Initial Power-up

1. 3.3Vaux stable to SMBus driven (optional). If no 3.3Vaux on platform, the delay is from +3.3V stable
2. Minimum time from power rails within specified tolerance to PERST# inactive (T_{PVPERL})
3. Minimum clock valid to PERST# inactive ($T_{PERST-CLK}$)
4. Minimum PERST# inactive to PCI Express link out of electrical idle
5. Minimum PERST# inactive to JTAG driven (optional)

Table 14-1 Power Sequencing and Reset Signal Timings

Symbol	Parameter	Min	Max	Units
T_{PVPERL}[1]	Power stable to PERST# inactive	100		ms
$T_{PERST-CLK}$[2]	REF CLK stable before PERST# inactive	100		µs
T_{PERST}	PERST# active time	100		µs
T_{FAIL}[3]	Power level invalid to PERST# active		500	ns
T_{WKRF}[4]	WAKE# rise – fall time		100	ns

Note:
1. Any supplied power is stable when it meets the requirements specified for that power supply.
2. A supplied reference clock is stable when it meets the requirements specified for the reference clock. The PEREST# signal is asserted and de-asserted asynchronously with respect to the supplied reference clock.
3. The PEREST# signal must be asserted within T_{FAIL} of any supplied power going out specification.
4. Measured from WAKE# assertion/de-assertion to valid input level at the system PM controller. Since WAKE# is an open-drain signal, the rise time is dependent on the total capacitance on the platform and the system board pull-up resistor. It is the responsibility of the system designer to meet the rise time specification.

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14.2 POWER-OFF SEQUENCE

The power off sequence is the reverse of the power on sequence, that is, asserts the PERST# first, then after T_{PERST_CLK} disable the REFCLK, and power off core power and I/O power, but I/O power off should be the same time or later than the core power off.

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15 ELECTRICAL AND TIMING SPECIFICATIONS

15.1 ABSOLUTE MAXIMUM RATINGS

Table 15-1 Absolute Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Item	Rating
Storage Temperature	-65ºC to 150ºC
Junction Temperature, Tj	125ºC
PCI Express supply voltage to ground potential (VDDA, VDDC, and VDDCAUX)	-0.3V to 1.3V
PCI supply voltage to ground potential (VD33, VDDA33 and VAUX)	-0.3V to 3.8V
DC input voltage for PCI Express signals	-0.3V to 1.3V
DC input voltage for PCI signals	-0.3V to 5.75V

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

15.2 DC SPECIFICATIONS

Table 15-2 DC Electrical Characteristics

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
VDDA	Analog Power Supply for PCI Express Interface		1.1	1.15	1.2	V
VDDA33	High Power Supply for PCI Express Interface		3.0	3.3	3.6	V
VDDC	Digital Power Supply for the Core		1.1	1.15	1.2	V
VDDCAUX	Digital Auxiliary Power Supply for the Core		1.1	1.15	1.2	V
VD33	Digital Power Supply for PCI Interface		3.0	3.3	3.6	V
VAUX	Digital Auxiliary Power Supply for PCI Interface		3.0	3.3	3.6	V
V_{IH}	PCI Input High Voltage		1.55		5.5	V
V_{IL}	PCI Input Low Voltage		-0.3		1.08	V
I_{IL}	PCI Input Leakage Current	$0<V_{IN}<VD33$			±10	µA
V_{OH}	PCI Output High Voltage	I_{out} = -500µA	2.7			V
V_{OL}	PCI Output Low Voltage	I_{out} = 1500µA			0.36	V
C_{IN}	PCI Input Pin Capacitance				10	pF
C_{CLK}	PCI CLK Pin Capacitance		5		12	pF
C_{IDSEL}	PCI IDSEL Pin Capacitance				8	pF

In order to support auxiliary power management fully, it is recommended to have VD33/VDDC and VAUX/VDDCAUX separated. However, if auxiliary power management is not required, VD33 and VDDC can be connected to VAUX and VDDCAUX respectively.

The typical power consumption of PI7C9X113SL is less than 350 mW.

PI7C9X113SL is capable of sustaining 1500V human body model for the ESD protection without any damages.

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15.3 AC SPECIFICATIONS

Table 15-3 PCI Bus Timing Parameters

Symbol	Parameter	66 MHz		33 MHz		Units
		MIN	MAX	MIN	MAX	
Tsu	Input setup time to CLK – bused signals [1,2,3]	3		7		ns
Tsu (ptp)	Input setup time to CLK – point-to-point [1,2,3]	5		10, 12[4]		
Th	Input signal hold time from CLK [1,2]	0		0		
Tval	CLK to signal valid delay – bused signals [1,2,3]	2	6	2	11	
Tval (ptp)	CLK to signal valid delay – point-to-point [1,2,3]	2	6	2	12	
Ton	Float to active delay [1,2]	2		2		
Toff	Active to float delay [1,2]		14		28	

1. See Figure 15 –1 PCI Signal Timing Measurement Conditions.
2. All PCI interface signals are synchronized to CLKOUT0.
3. Point-to-point signals are REQ_L [7:0], GNT_L [7:0], LOO, and ENUM_L. Bused signals are AD, CBE, PAR, PERR_L, SERR_L, FRAME_L, IRDY_L, TRDY_L, LOCK_L, STOP_L and IDSEL.
4. REQ_L signals have a setup of 10ns and GNT_L signals have a setup of 12ns.

Figure 15-1 PCI Signal Timing Conditions

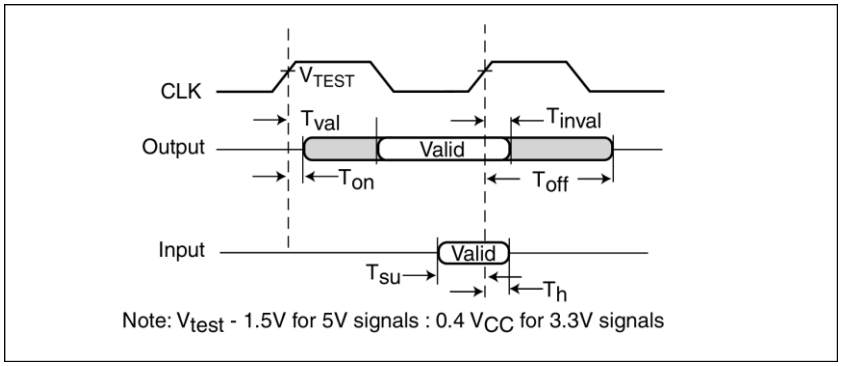


Table 15-4 PCI Express Interface - Differential Transmitter (TX) Output Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Unit Interval	UI	399.88	400.0	400.12	ps
Differential p-p TX voltage swing	$V_{TX-DIFF-P-P}$	800			mV ppd
Lower power differential p-p TX voltage swing	$V_{TX-DIFF-P-P-LOW}$	400			mV ppd
TX de-emphasis level ratio	$V_{TX-DE-RATIO}$	-3.0		-4.0	dB
Minimum TX eye width	T_{TX-EYE}	0.75			UI
Maximum time between the jitter median and max deviation from the median	$T_{TX-EYE-MEDIAN-to-MAX-JITTER}$			0.125	UI
Transmitter rise and fall time	$T_{TX-RISE-FALL}$	0.125			UI
Maximum TX PLL Bandwidth	BW_{TX-PLL}			22	MHz
Maximum TX PLL BW for 3dB peaking	$BW_{TX-PLL-LO-3DB}$	1.5			MHz
Absolute Delta of DC Common Mode Voltage During L0 and Electrical Idle	$V_{TX-CM-DC-ACTIVE-IDLE-DELTA}$	0		100	mV
Absolute Delta of DC Common Mode Voltage between D+ and D–	$V_{TX-CM-DC-LINE-DELTA}$	0		25	mV
Electrical Idle Differential Peak Output Voltage	$V_{TX-IDLE-DIFF-AC-p}$	0		20	mV
The Amount of Voltage Change Allowed During Receiver Detection	$V_{TX-RCV-DETECT}$			600	mV

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Parameter	Symbol	Min	Typ	Max	Unit
Transmitter DC Common Mode Voltage	$V_{TX-DC-CM}$	0		3.6	V
Transmitter Short-Circuit Current Limit	$I_{TX-SHORT}$			90	mA
DC Differential TX Impedance	$Z_{TX-DIFF-DC}$	80	100	120	Ω
Lane-to-Lane Output Skew	$L_{TX-SKEW}$			500 ps + 2 UI	ps

Table 15-5 PCI Express Interface - Differential Receiver (RX) Input Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Unit Interval	UI	399.88	400.0	400.12	ps
Differential RX Peak-to-Peak Voltage	$V_{RX-DIFF-PP-CC}$	175		1200	mV
Receiver eye time opening	T_{RX-EYE}	0.4			UI
Maximum time delta between median and deviation from median	$T_{RX-EYE-MEDIAN-to-MAX-JITTER}$			0.3	UI
Receiver DC common mode impedance	Z_{RX-DC}	40		60	Ω
DC differential impedance	$Z_{RX-DIFF-DC}$	80		120	Ω
RX AC Common Mode Voltage	$V_{RX-CM-AC-P}$			150	mV
DC input CM input impedance during reset or power down	$Z_{RX-HIGH-IMP-DC}$	200			kΩ
Electrical Idle Detect Threshold	$V_{RX-IDLE-DET-DIFFp-p}$	65		175	mV
Lane to Lane skew	$L_{RX-SKEW}$			20	ns

15.4 OPERATING AMBIENT TEMPERATURE

Table 15-6 Operating Ambient Temperature

(Above witch the useful life may be impaired.)

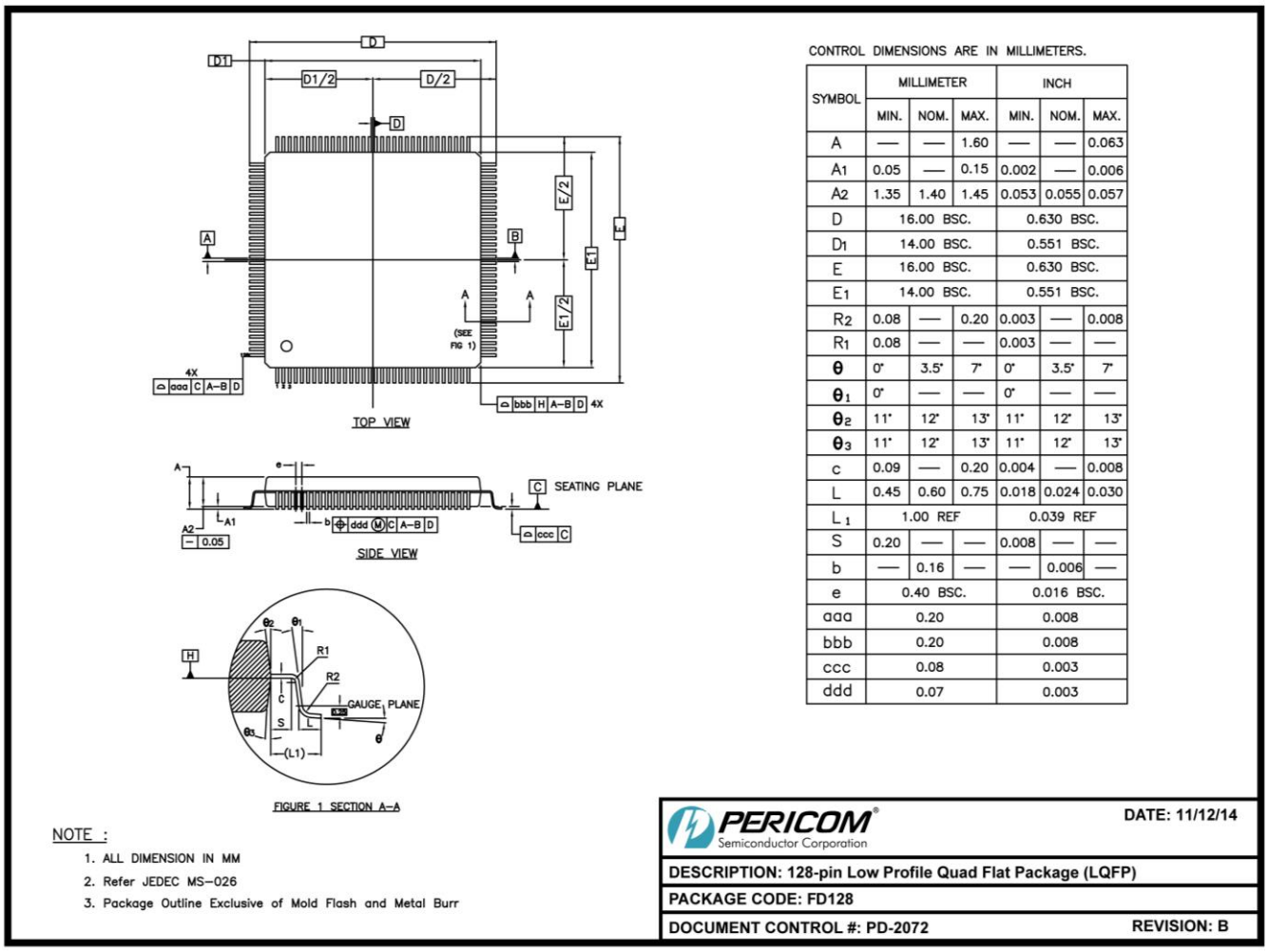
Item	Low	High	Unit
Ambient Temperature with power applied	-40	85	ºC

Note: Exposure to high temperature conditions for extended periods of time may affect reliability.

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16 PACKAGE INFORMATION

The package of PI7C9X113SL comes in 14mm x 14mm LQFP (128 Pin) package. The pin pitch is 0.4mm. This package also includes an exposed ground on the bottom surface of the package. Pericom highly recommends implementing this exposed ground pad on any customer boards. The following are the package information and mechanical dimension:



CONTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D	16.00 BSC.			0.630 BSC.		
D1	14.00 BSC.			0.551 BSC.		
E	16.00 BSC.			0.630 BSC.		
E1	14.00 BSC.			0.551 BSC.		
R2	0.08	—	0.20	0.003	—	0.008
R1	0.08	—	—	0.003	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	—	—	0°	—	—
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°
c	0.09	—	0.20	0.004	—	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
S	0.20	—	—	0.008	—	—
b	—	0.16	—	—	0.006	—
e	0.40 BSC.			0.016 BSC.		
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.07			0.003		

15-0005

Figure 16-1 Package Outline Drawing



X: Die Rev
YY: Year
WW: Workweek
1st X: Assembly Code
2nd X: Fab Code

Figure 16-2 Part Marking

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17 ORDERING INFORMATION

Orderable Part Number	Package Description	Pb-Free & Green	Temperature Range
PI7C9X113SLFDEX	128 – LQFP (Exposed ground pad)	YES	-40°C to 85°C

Notes:

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. E = Pb-free and Green
5. X suffix = Tape/Reel

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