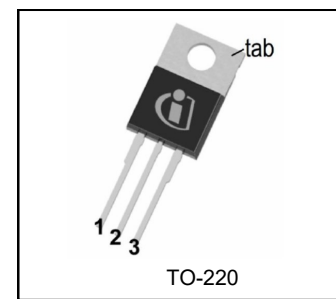
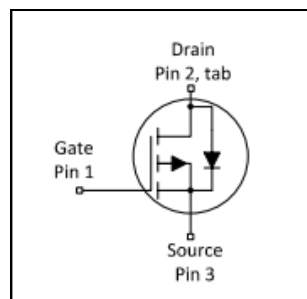


$V_{(BR)DSS}$	<b>-55V</b>
$R_{DS(on)}$ max.	<b>0.02<math>\Omega</math></b>
$I_D$	<b>-74A</b>



## Features

- Advanced Process Technology
- Ultra Low On-Resistance
- Dynamic dv/dt Rating
- 175°C Operating Temperature
- Fast Switching
- P-Channel
- Fully Avalanche Rated
- Lead-Free

## Description

Fifth Generation HEXFET Power MOSFETs utilizes advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit combined with the fast switching speed and ruggedized device design that HEXFET power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of other applications.

The TO-220 package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 watts. The low thermal resistance and low package cost of TO-220 contributes to the wide acceptance throughout the industry.

Base part number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRF4905PbF	TO-220	Tube	50	IRF4905PbF

Symbol	Parameter	Max.	Units
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ -10\text{V}$	-74	A
$I_D @ T_C = 100^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ -10\text{V}$	-52	
$I_{DM}$	Pulsed Drain Current ①	-260	
$P_D @ T_C = 25^\circ\text{C}$	Maximum Power Dissipation	200	W
	Linear Derating Factor	1.3	W/°C
$V_{GS}$	Gate-to-Source Voltage	$\pm 20$	V
$E_{AS}$	Single Pulse Avalanche Energy ②	930	mJ
$I_{AR}$	Avalanche Current ①	-38	A
$E_{AR}$	Repetitive Avalanche Energy ①	20	mJ
dv/dt	Peak Diode Recovery dv/dt③	-5.0	V/ns
$T_J$	Operating Junction and Storage Temperature Range	-55 to + 175	°C
$T_{STG}$			
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	
	Mounting torque, 6-32 or M3 screw	10 lbf•in (1.1N•m)	

## Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	0.75	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient	—	62	

### Static @ T<sub>J</sub> = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
V <sub>(BR)DSS</sub>	Drain-to-Source Breakdown Voltage	-55	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = -250μA
ΔV <sub>(BR)DSS</sub> /ΔT <sub>J</sub>	Breakdown Voltage Temp. Coefficient	—	-0.05	—	V/°C	Reference to 25°C, I <sub>D</sub> = -1mA
R <sub>DS(on)</sub>	Static Drain-to-Source On-Resistance	—	—	0.02	Ω	V <sub>GS</sub> = -10V, I <sub>D</sub> = -38A ④
V <sub>GS(th)</sub>	Gate Threshold Voltage	-2.0	—	-4.0	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -250μA
g <sub>fs</sub>	Forward Trans conductance	21	—	—	S	V <sub>DS</sub> = -25V, I <sub>D</sub> = -38A④
I <sub>DSS</sub>	Drain-to-Source Leakage Current	—	—	-25	μA	V <sub>DS</sub> = -55V, V <sub>GS</sub> = 0V
		—	—	-250		V <sub>DS</sub> = -44V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 150°C
I <sub>GSS</sub>	Gate-to-Source Forward Leakage	—	—	-100	nA	V <sub>GS</sub> = -20V
	Gate-to-Source Reverse Leakage	—	—	100		V <sub>GS</sub> = 20V

### Dynamic Electrical Characteristics @ T<sub>J</sub> = 25°C (unless otherwise specified)

Q <sub>g</sub>	Total Gate Charge	—	—	180	nC	I <sub>D</sub> = -38A V <sub>DS</sub> = -44V V <sub>GS</sub> = -10V, See Fig.6 and 13 ④
Q <sub>gs</sub>	Gate-to-Source Charge	—	—	32		
Q <sub>gd</sub>	Gate-to-Drain Charge	—	—	86		
t <sub>d(on)</sub>	Turn-On Delay Time	—	18	—	ns	V <sub>DD</sub> = -28V I <sub>D</sub> = -38A R <sub>G</sub> = 2.5Ω R <sub>D</sub> = 0.72Ω, See Fig.10④
t <sub>r</sub>	Rise Time	—	99	—		
t <sub>d(off)</sub>	Turn-Off Delay Time	—	61	—		
t <sub>f</sub>	Fall Time	—	96	—		
L <sub>D</sub>	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
L <sub>S</sub>	Internal Source Inductance	—	7.5	—		
C <sub>iss</sub>	Input Capacitance	—	3400	—	pF	V <sub>GS</sub> = 0V V <sub>DS</sub> = -25V f = 1.0MHz, See Fig.5
C <sub>oss</sub>	Output Capacitance	—	1400	—		
C <sub>rss</sub>	Reverse Transfer Capacitance	—	640	—		

### Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode)	—	—	-74	A	MOSFET symbol showing the integral reverse p-n junction diode.
I <sub>SM</sub>	Pulsed Source Current (Body Diode) ①	—	—	-260		
V <sub>SD</sub>	Diode Forward Voltage	—	—	-1.6	V	T <sub>J</sub> = 25°C, I <sub>S</sub> = -38A, V <sub>GS</sub> = 0V ④
t <sub>rr</sub>	Reverse Recovery Time	—	89	130	ns	T <sub>J</sub> = 25°C, I <sub>F</sub> = -38A
Q <sub>rr</sub>	Reverse Recovery Charge	—	230	350	nC	di/dt = 100A/μs ④

#### Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11).
- ② Starting T<sub>J</sub> = 25°C, L = 1.3mH, R<sub>G</sub> = 25Ω, I<sub>AS</sub> = -38A. (See fig. 12).
- ③ I<sub>SD</sub> ≤ -38A, di/dt ≤ -270A/μs, V<sub>DD</sub> ≤ V<sub>(BR)DSS</sub>, T<sub>J</sub> ≤ 175°C.
- ④ Pulse width ≤ 300μs; duty cycle ≤ 2%.

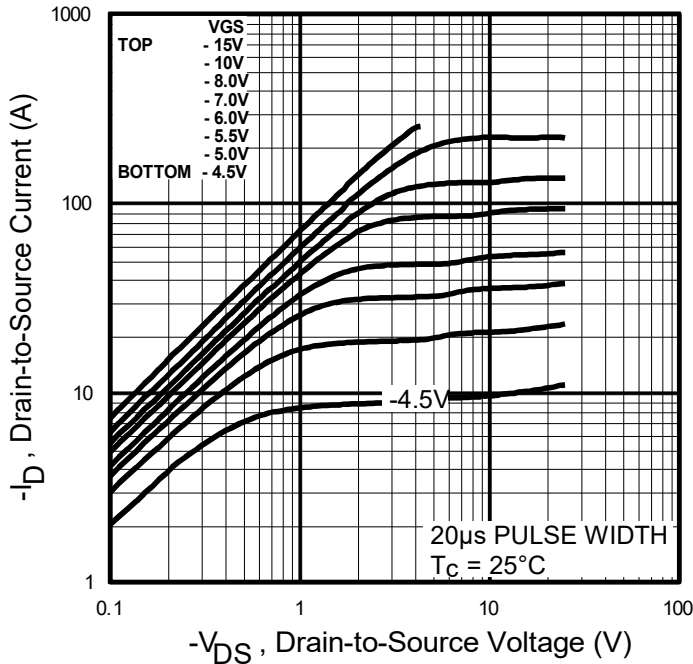


Fig. 1 Typical Output Characteristics

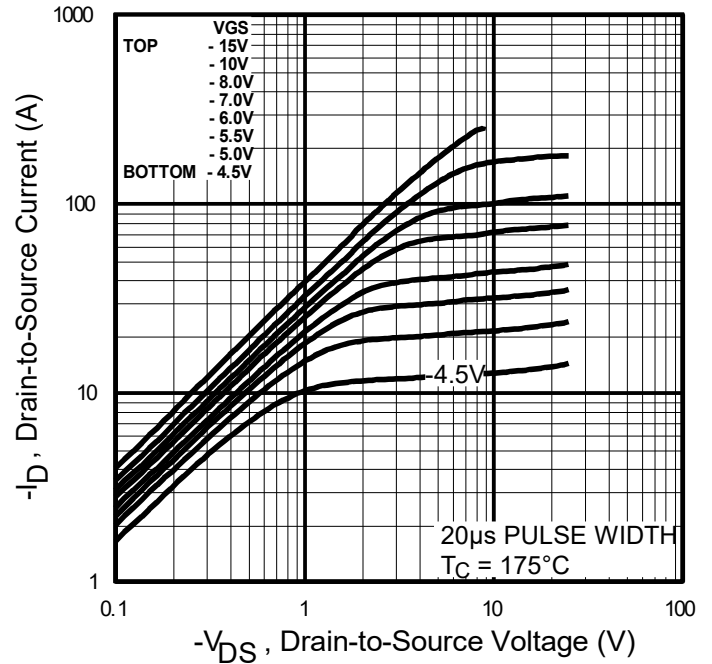


Fig. 2 Typical Output Characteristics

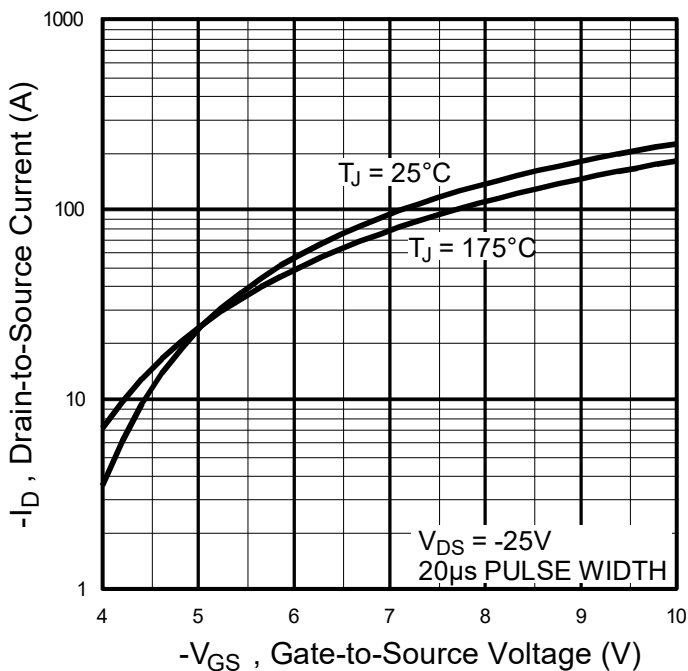


Fig. 3 Typical Transfer Characteristics

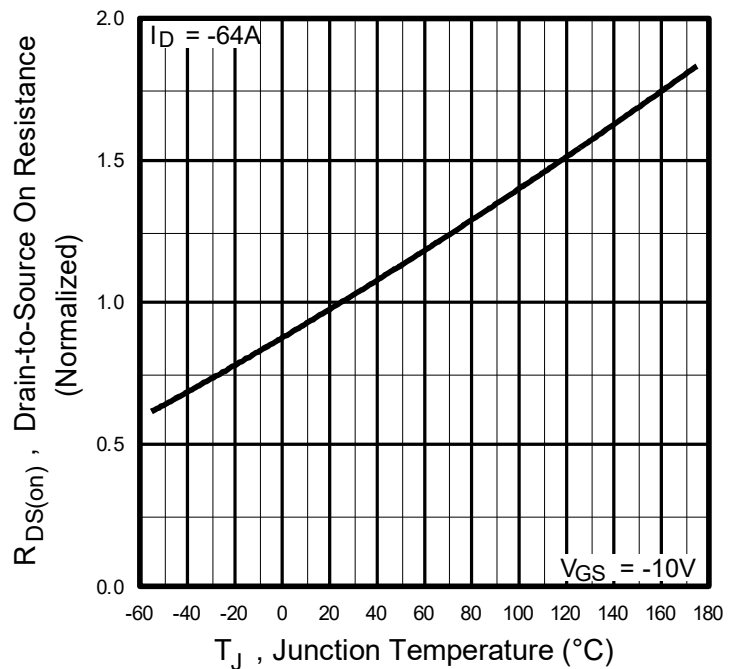
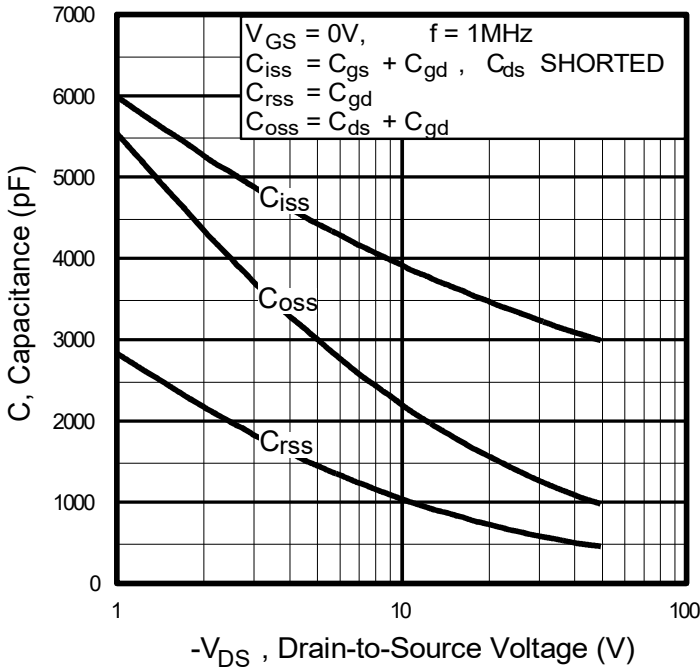
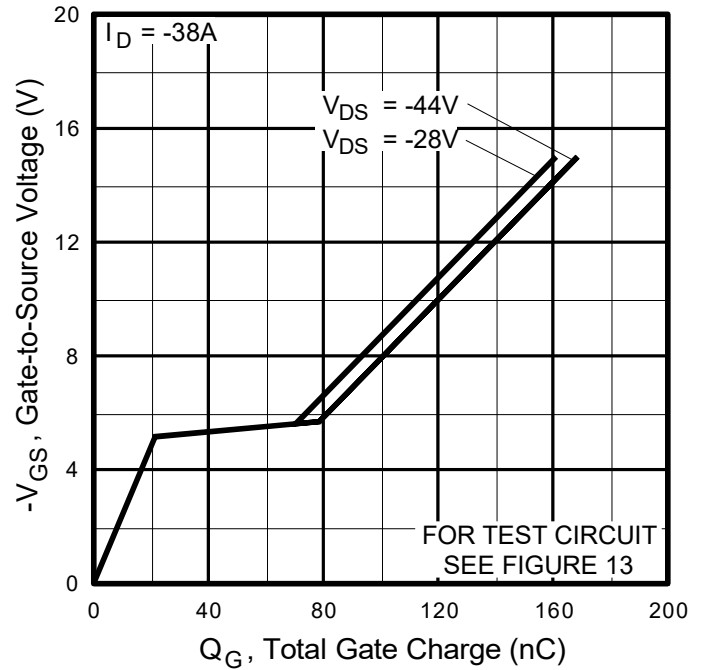


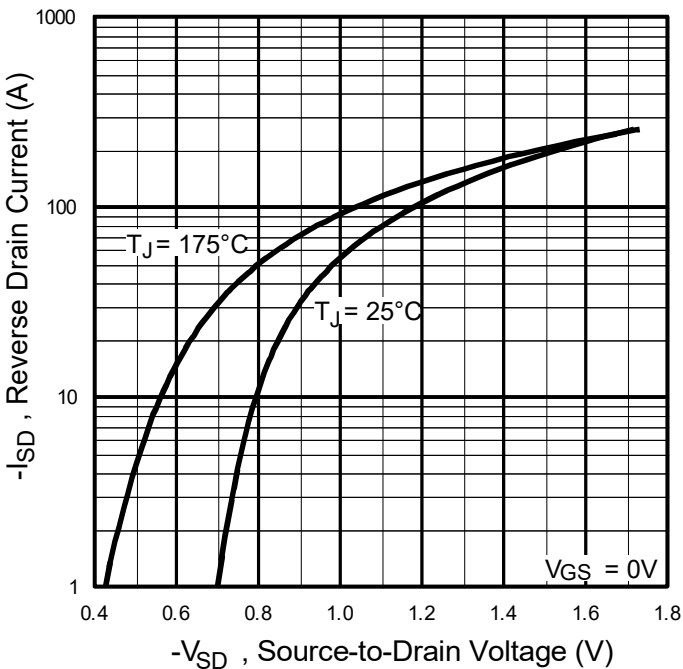
Fig. 4 Normalized On-Resistance vs. Temperature



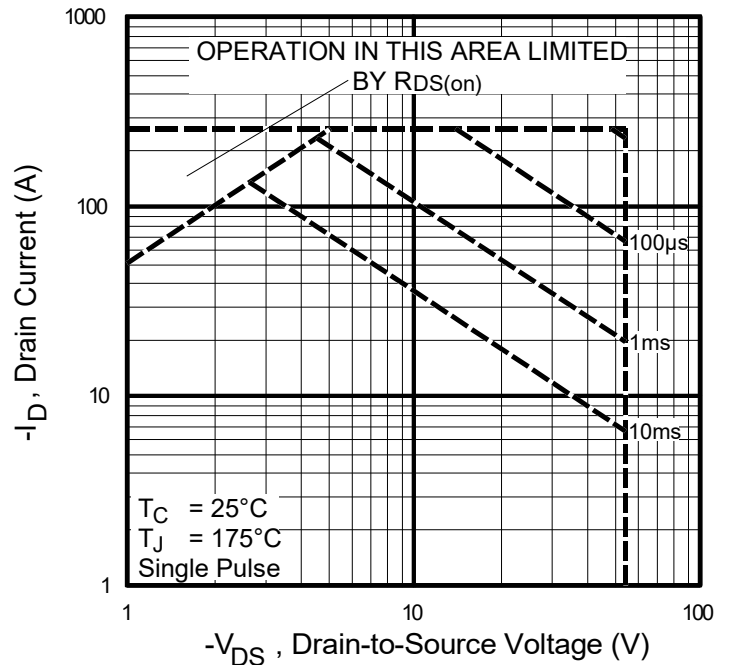
**Fig 5.** Typical Capacitance vs. Drain-to-Source Voltage



**Fig 6.** Typical Gate Charge vs. Gate-to-Source Voltage



**Fig. 7** Typical Source-to-Drain Diode Forward Voltage



**Fig 8.** Maximum Safe Operating Area

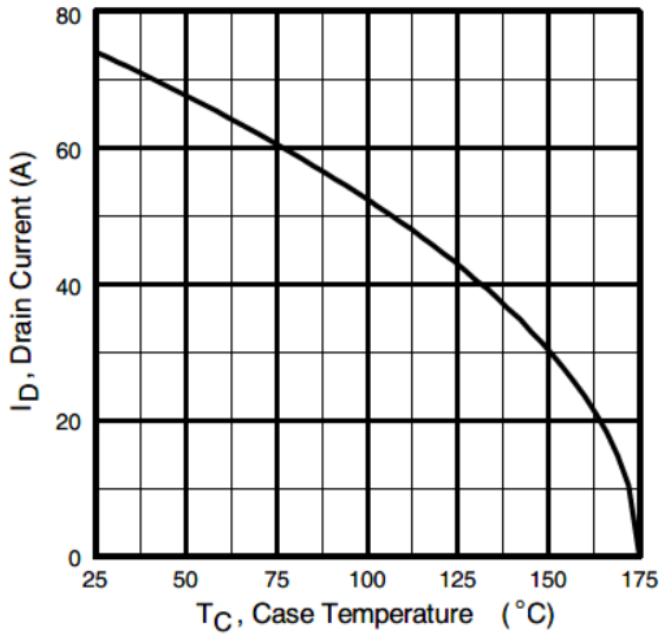


Fig 9. Maximum Drain Current vs. Case Temperature

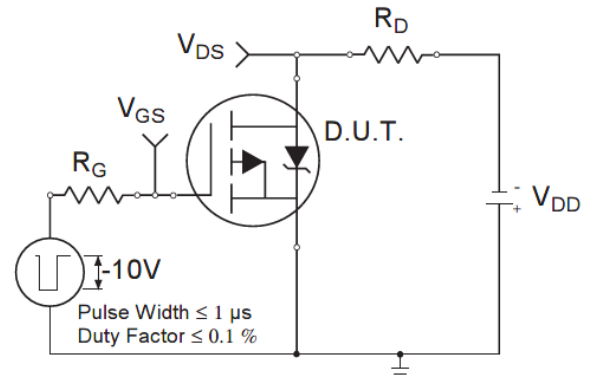


Fig 10a. Switching Time Test Circuit

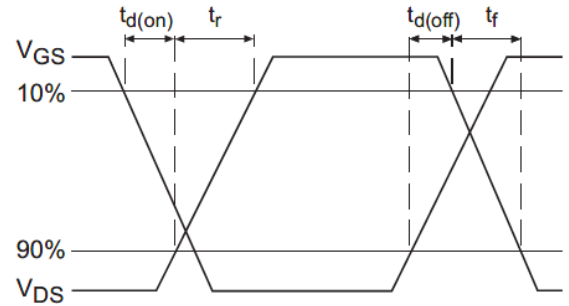


Fig 10a. Switching Time Waveforms

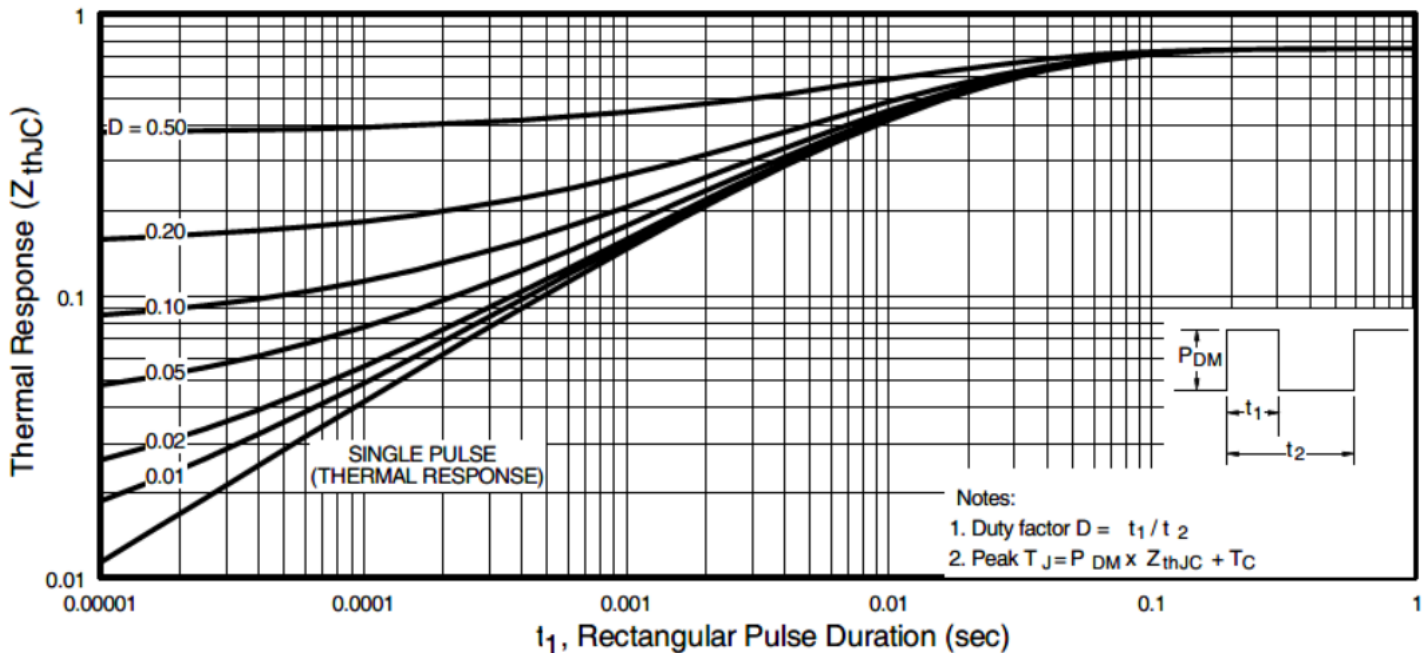


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

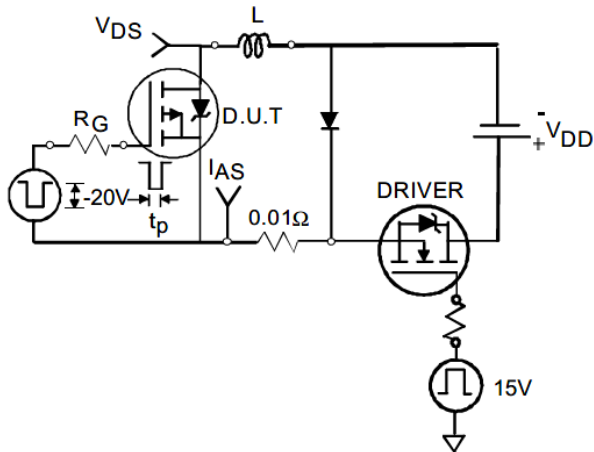


Fig. 12a. Unclamped Inductive Test Circuit

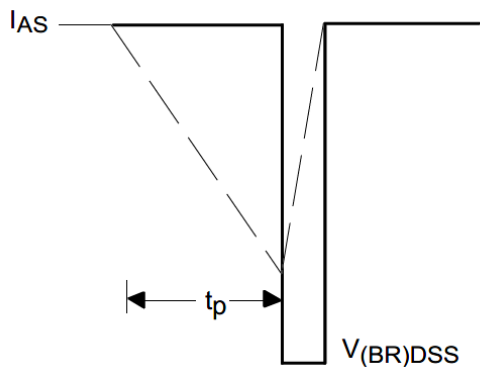


Fig. 12b. Unclamped Inductive Waveforms

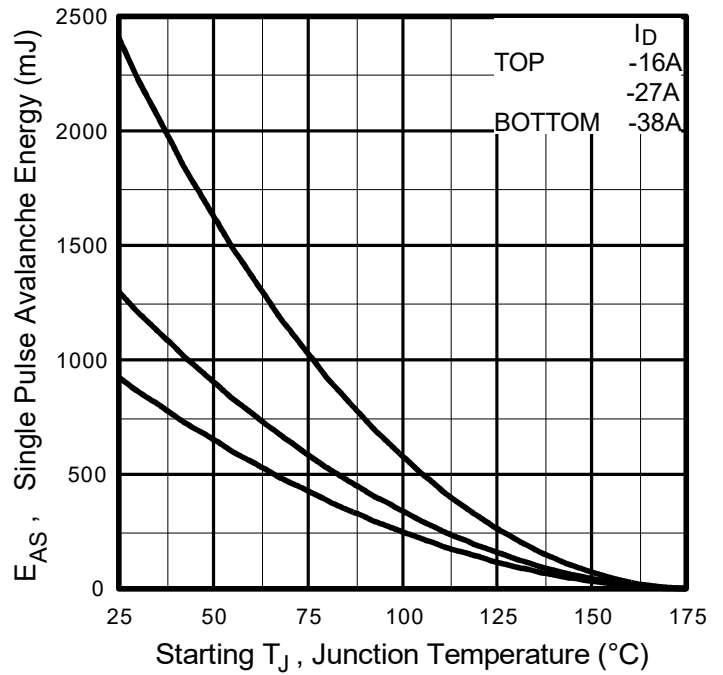


Fig 12c. Maximum Avalanche Energy vs. Drain Current

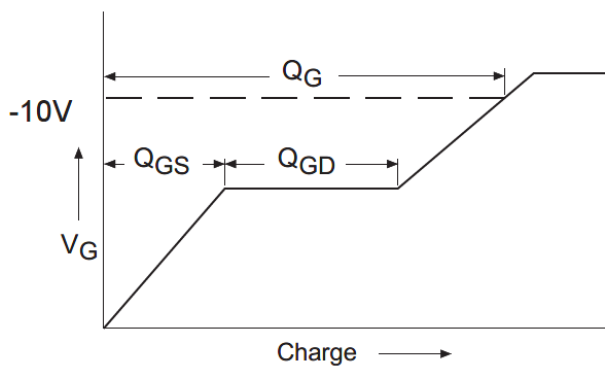


Fig 13a. Basic Gate Charge Waveform

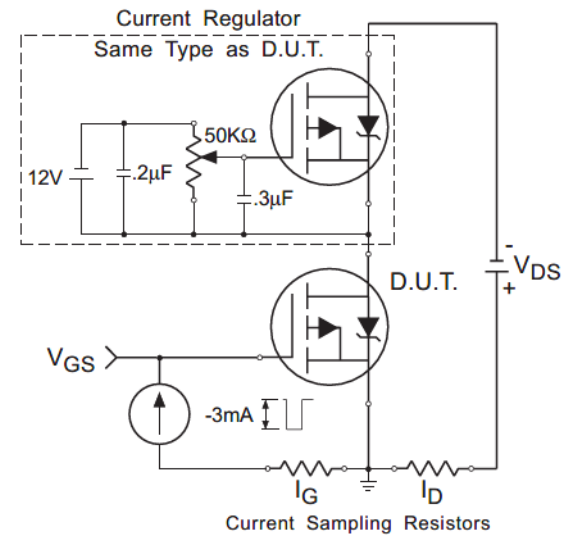
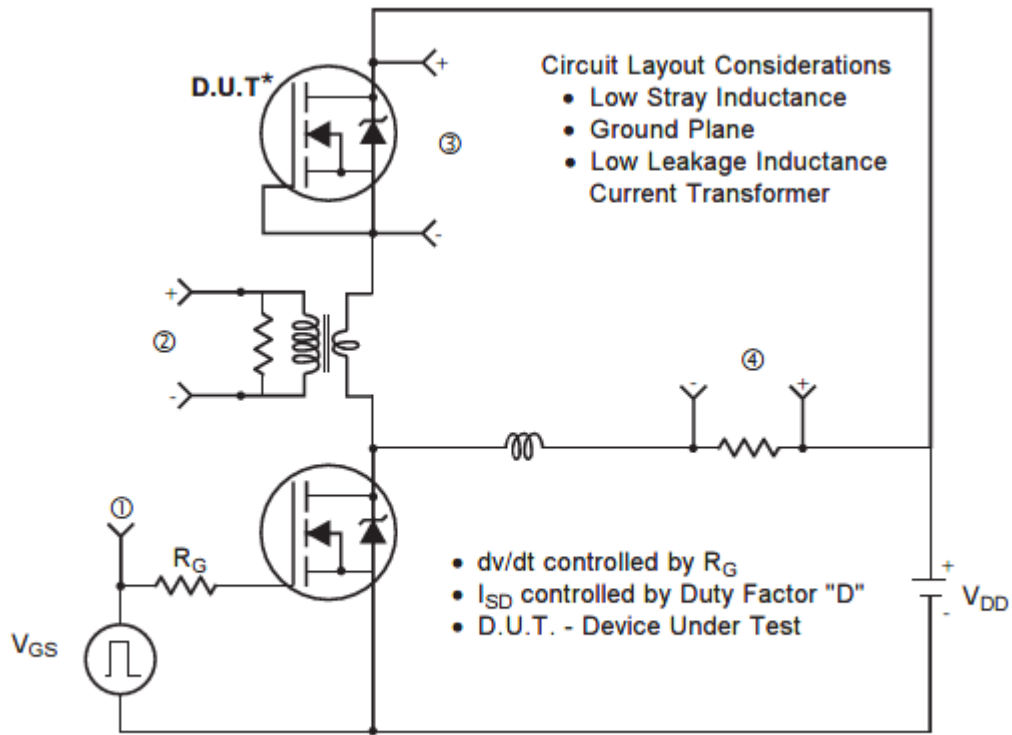


Fig 13b. Gate Charge Test Circuit



\* Reverse Polarity of D.U.T for P-Channel

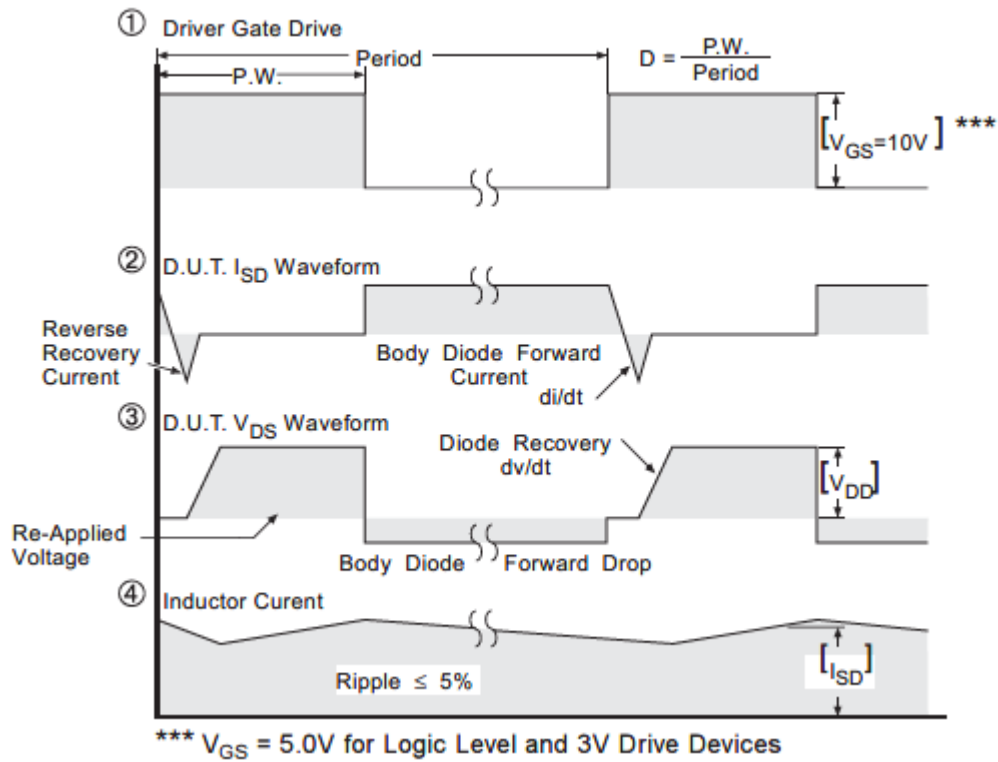
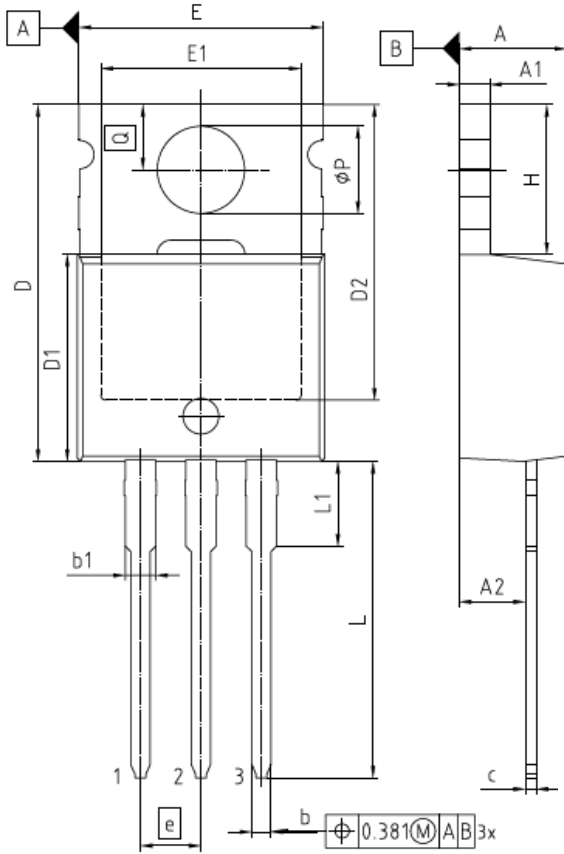


Fig 14. Peak Diode Recovery  $dv/dt$  Test Circuit for P-Channel HEXFET® Power MOSFETs

## TO-220 Package Outline (Dimensions are shown in millimeters (inches))



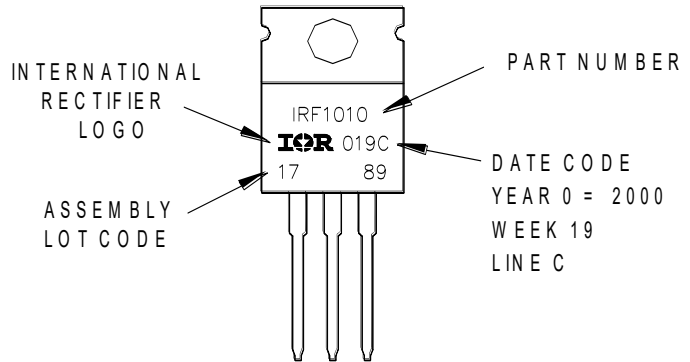
NOTES:  
 DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS  
 GATE BURRS ARE LESS THAN 0.5 mm

PACKAGE - GROUP NUMBER: <b>PG-TO220-3-U05</b>		
DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
<b>A</b>	3.56	4.83
<b>A1</b>	1.14	1.40
<b>A2</b>	2.03	2.92
<b>b</b>	0.38	1.01
<b>b1</b>	1.14	1.78
<b>c</b>	0.36	0.61
<b>D</b>	14.22	16.51
<b>D1</b>	8.38	9.20
<b>D2</b>	11.68	12.88
<b>E</b>	9.65	10.67
<b>E1</b>	6.86	8.89
<b>e</b>	2.54	
<b>N</b>	3	
<b>H</b>	5.84	6.86
<b>L</b>	12.70	14.73
<b>L1</b>	3.56	4.06
<b>phi P</b>	3.54	4.08
<b>Q</b>	2.54	3.42

## TO-220 Part Marking Information

EXAMPLE: THIS IS AN IRF1010  
 LOT CODE 1789  
 ASSEMBLED ON WW 19, 2000  
 IN THE ASSEMBLY LINE "C"

Note: "P" in assembly line position indicates "Lead - Free"



TO-220 packages are not recommended for Surface Mount Application.

## Revision History

Date	Rev.	Comments
2026-04-08	2.1	<ul style="list-style-type: none"> <li>Update datasheet to Infineon format</li> <li>Updated Part marking –page 8</li> <li>Added disclaimer on last page.</li> </ul>

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