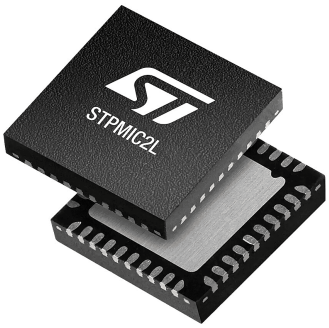
STPMIC2L

Datasheet

Power management IC for MPU with 3 buck converters and 7 LDOs



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STPMIC2L

Device summary	
Order code	STPMIC2LAPQR
	STPMIC2LBPQR
Packing	VFQFPN40L (5.0 x 5.0 x 1.0 mm)

Features

- Input voltage range from 2.8 V to 5.5 V
- 3 buck SMPS converters with adaptive constant-on-time (COT) topology
- 5 adjustable general-purpose LDOs
- 1 LDO for DDR3L/DDR4 termination (sink-source) or as a general-purpose LDO
- 1 LDO for USB PHY supply
- 2 MHz switching frequency buck converters with forced PWM
- User-programmable non-volatile memory (NVM), enabling scalability to support a wide range of applications
- Immediate output alternate settings toggle by dedicated power control pins
- Programmable output voltages turn ON/OFF sequences
- I²C and digital I/O control interfaces
- 5 GPO output controls for external command
- VFQFPN40L ((5.0 x 5.0x 1.0 mm)

Applications

- Power management for embedded microprocessor units
- Wearables and IoT
- Portable devices
- Human-machine interfaces
- Smart home
- Power management unit companion chip for STM32MP21/23/25 MPUs

Description

The STPMIC2L is a fully integrated power management IC designed for the STM32M2x MPU series applications requiring low power and high efficiency.

The device integrates advanced low-power features controlled by a host processor via I²C and I/O interfaces.

The STPMIC2L regulators are designed to supply power to the application processor as well as to the external system peripherals such as DDR, flash memories, and other system devices.

Three buck SMPS are optimized to provide excellent transient response and output voltage precision for a wide range of operating conditions. The converters use an advanced PWM phase shift synchronization technique with integrated PLL and a programmable spread-spectrum frequency modulation to reduce EMI.

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1 Device configuration table

The STPMIC2L has a non-volatile memory (NVM) that enables scalability to support a wide range of applications:

- Default output voltage, POWER_UP/POWER_DOWN sequence, protection behavior, auto turn-on functionality, and an I²C slave address.
- The STPMIC2LA and STPMIC2LB are preprogrammed devices to support the STM32MP2x series application processor versions.
- Straightforward NVM reprogramming via I²C to facilitate mass production directly in target applications.
- Possibility to lock NVM content to prevent further reprogramming by writing LOCK_NVM bit.

Table 1. .Default configuration table

	Default configuration table					
	STPMIC2LA			STPMIC2LB		
	Default output voltage	Default outputcurrent	Rank	Default outputvoltage	Default outputcurrent	Rank
LDO1	1.80 V	20 mA OCP level1	1	1.80 V	20 mA OCP level1	1
LDO2	3.3 V	0.4 A OCP level1	1	1.80 V	0.4 A OCP level1	1
LDO3	-	-	0	-	-	0
LDO4	3.3 V	40 mA OCP level0	5	3.3 V	40 mA OCP level0	5
LDO5	3.3 V	0.4 A OCP level0	5	2.9 V	0.4 A OCP level0	5
LDO6	1.80 V	0.4 A OCP level1	3	1.80 V	0.4 A OCP level1	3
LDO7	-	-	0	-	-	0
BUCK1	0.82 V	1.5 A OCP level1	2	0.82 V	1.5 A OCP level1	2
BUCK2	-	-	0	-	-	0
BUCK3	0.80 V	2.0 A OCP level1	4	0.80 V	2.0 A OCP level1	4
GPO1	-	-	0	-	-	0
GPO2	-	-	0	-	-	0
GPO3	-	-	0	-	-	0
GPO4	-	-	5	-	-	5
GPO5	-	-	5	-	-	5
VINOK_Rise	4.0 V		-	3.3 V		-
VINOK_Fall	3.5 V		-	2.8 V		-

All output voltages with Rank = 0 are, by default, programmed with 0 Dec (refer to Table 17 and Table 18).The startup sequence is split into six steps (Rank0 to Rank5).

Each BUCK converter or LDO regulator can be programmed to be automatically turned ON in one of these phases. Each rank phase is separated by a delay (1.5 ms, 3 ms, 4.5 ms, or 6 ms) programmed in the NVM:

- Rank = 0: rail not turned ON automatically, no output voltage appears after POWER-UP
- Rank = 1: rail automatically turned ON after 7 ms following a turn_ON condition
- Rank = 2: rail automatically turned ON after a further 1.5 ms (by default)
- Rank = 3: rail automatically turned ON after a further 1.5 ms (by default)
- Rank = 4: rail automatically turned ON after a further 1.5 ms (by default)
- Rank = 5: rail automatically turned ON after a further 1.5 ms (by default)
- Whatever the STPMIC2L version, the AUTO_TURN_ON option is set.

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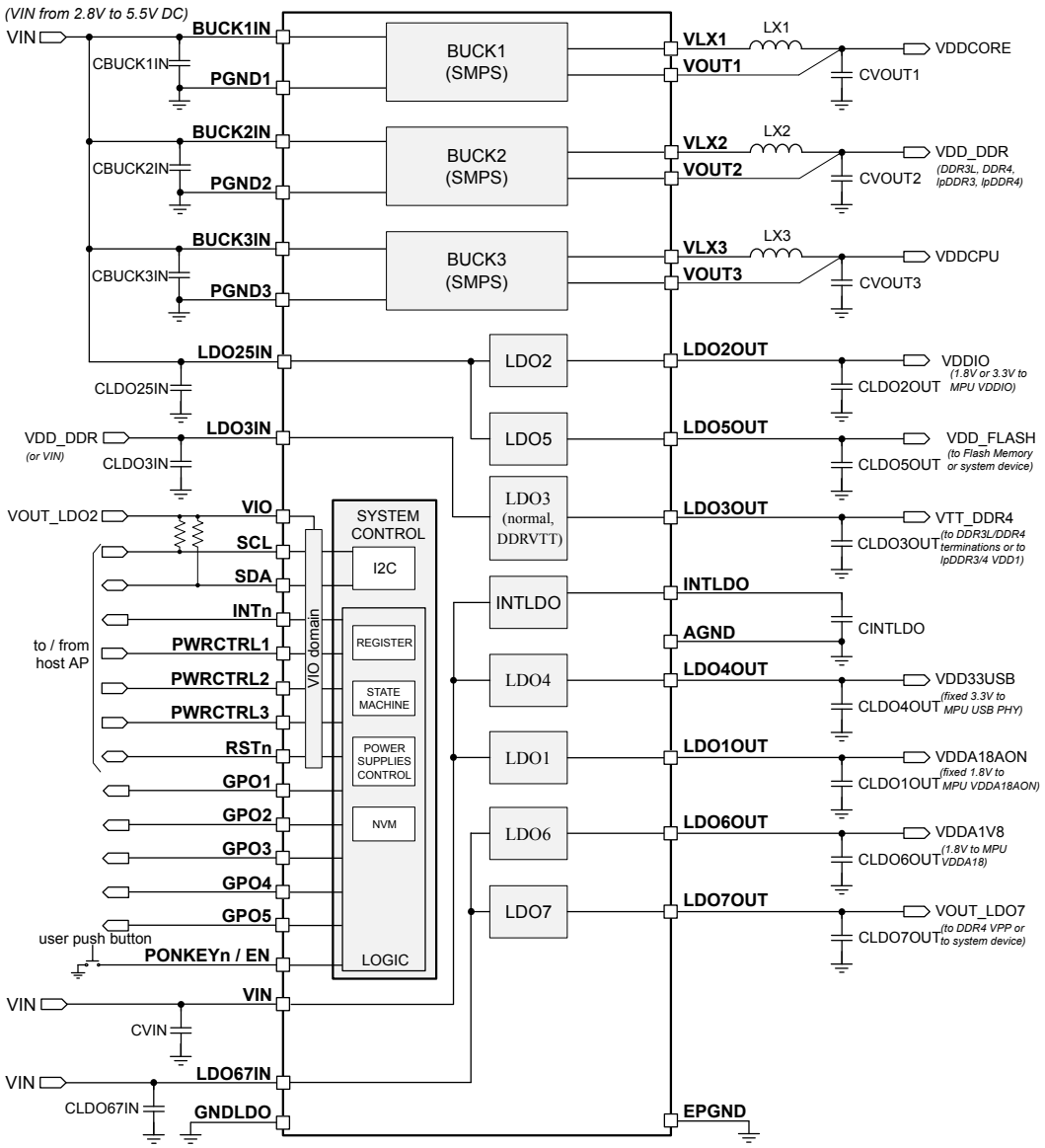
2 Typical application schematic

Figure 1. **Typical application schematic**



Note: All the input voltage pins must be connected at the same voltage supply value except the LDO3 sink/source.

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2.1 Recommended external components

Table 2. Passive components

Component	Manufacturer	Part number	Value	Size
CVIN, CLDO1OUT, CLDO2OUT, CLDO5OUT CLDO6OUT, CLDO7OUT, CLDO4OUT, CINTLDO	MURATA	GRM155R60J475ME47D	4.7 µF 6.3 V	0402
CBUCK1IN, CBUCK2IN, CBUCK3IN		GRM188R61A106ME69D	10 µF 10 V	0603
CVOUT1		GRM188R60J226MEA0D	4x 22 µF 6.3 V	0603
CVOUT2		GRM188R60J226MEA0D	3 x 22 µF 6.3 V	0603
CVOUT3		GRM188R60J226MEA0D	4x 22 µF 6.3 V	0603
CLDO25IN, CLDO67IN,		GRM155R61E105KA12D	1 µF 25 V	0402
CLDO3IN, CLDO3OUT (1)		GRM155R60J106ME05D	10 µF 6.3 V	0402
LX1		DFE252012F-R68M	0.68 µH	1008
LX2		DFE201610E-R68M	0.68 µH	0806
LX3		DFE252012F-R68M	0.68 µH	1008

1. *4.7 µF normal mode -10 µF sink/source mode*

Note: All the components above refer to a typical application. The operation of the device is not limited to the choice of these external components. For more details refer to the application note AN6116.

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2.2 Pin out and pin description

Figure 2. **Pin configuration VFQFPN40L top view**

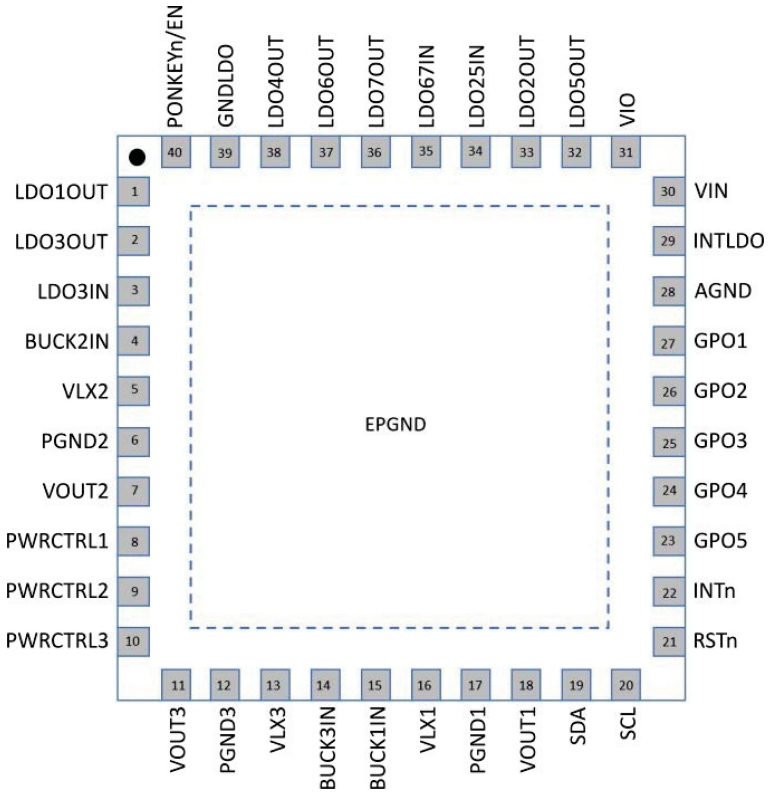

Table 3. **Pin description**

Pin name	A/D [1]	I/O [1]	Location	Description (default configuration)	Unused pin connection
LDO1OUT	A	O	1	Output voltage LDO1	Floating
LDO3OUT	A	O	2	Output voltage LDO3	Floating
LDO3IN	A	I	3	Power input LDO3	VIN
BUCK2IN	A	I	4	Power input Buck2	VIN
VLX2	A	O	5	LX node Buck2	Floating
PGND2	A	-	6	Power ground Buck2	GND
VOUT2	A	I	7	Input feedback signal Buck2	Floating
PWRCTRL1	D	I	8	Power control 1 mode (pull-up and pull-down, pull-up active by default)	VIO or Floating
PWRCTRL2	D	I	9	Power control 2 mode (pull-up and pull-down, pull-up active by default)	VIO or Floating
PWRCTRL3	D	I	10	Power control 3 mode (pull-up and pull-down, pull-up active by default)	VIO or Floating
VOUT3	A	I	11	Input feedback signal Buck3	Floating
PGND3	A	-	12	Power ground Buck2	GND
VLX3	A	O	13	LX node Buck3	Floating
BUCK3IN	A	I	14	Power input Buck3	VIN

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Pin name	A/D (1)	I/O (1)	Location	Description (default configuration)	Unused pin connection
BUCK1IN	A	I	15	Power input Buck3	VIN
VLX1	A	O	16	LX node Buck1	Floating
PGND	A	-	17	Power ground Buck1	GND
VOUT1	A	O	18	Input feedback signal Buck1	Floating
SDA	D	I/O	19	I^2C serial data	VIO
SCL	D	I	20	I^2C serial clock	VIO
RSTn	D	I/O	21	Bi-directional reset (active low with internal pull-up)	Floating
INTn	D	O	22	Interrupt (active low with internal pull-up)	Floating
GPO5	D	O	23	External Control pin 5	Floating
GPO4	D	O	24	External Control pin 4	Floating
GPO3	D	O	25	External Control pin 3	Floating
GPO2	D	O	26	External Control pin 2	Floating
GPO1	D	O	27	External Control pin 1	Floating
AGND	A	-	28	Main analog ground	GND
INTLDO	A	O	29	Internal LDO	4.7 µF capacitor
VIN	A	I	30	Main power input	VIN
VIO	A	I	31	I/O voltage (for all digital signals except PONKEYn/EN and GPOs)	VIO
LDO5OUT	A	O	32	Output voltage LDO5	Floating
LDO2OUT	A	O	33	Output voltage LDO2	Floating
LDO25IN	A	O	34	Power input LDO2 and LDO5	VIN
LDO67IN	A	I	35	Power input LDO6 and LDO7	VIN
LDO7OUT	A	O	36	Output voltage LDO7	Floating
LDO6OUT	A	O	37	Output voltage LDO6	Floating
LDO4OUT	A	O	38	Output voltage LDO4	Floating
GNDLDO	A	-	39	LDO GND	GND
PONKEYn/EN	D	I	40	User power ON key (active low with internal pull-up)	Floating
ePGND	A	-	ePad	Exposed pad to be connected to ground	GND

1. *A: analog; D: digital; I/O: input/Output*

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3 Electrical and timing characteristics

3.1 Absolute maximum ratings

Table 4. Absolute maximum ratings

Parameter	Min.	Unit
VIN, BUCKxIN, VLXx, LDO3IN, LDOxIN, PONKEYn/En, GPOx	-0.5 to +6.5	V
VIO, SDA, SCL, RSTn, PWRCTRLx, INTn	-0.5 to +4.2	
INTLDO	-0.5 to +2	
VOUT1, LDOxOUT	-0.5 to +5	
VOUT2, VOUT3	-0.5 to +3	
ESD HBM	±1000	
ESD CDM	±500	

Note: Stressing the device above the absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

3.2 Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Value	Unit
T_j	Absolute maximum junction temperature	-40 to +150	°C
T_A	Operating ambient temperature	-40 to +105	
T_{JAMR}	Absolute maximum junction temperature	-40 to +160	
Θ_{JC}	Junction-case package thermal resistance on 2s2p std JEDEC board (JESD51-7)	6	°C/W
Θ_{JA}	Junction-ambient package thermal resistance on 2s2p std JEDEC board (JESD51-7)	30	

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3.3 Consumption in typical application scenarios

STPMIC2L V_{IN} input current consumption (all supply pins connected to V_{IN} except V_{LDO3IN} = V_{OUT2}, V_{IN} = 5 V, V_{IO} = 3.3 V (from LDO2OUT),T_j = + 25 °C, unless otherwise specified.

Table 6. Consumption in typical application scenarios

Application mode	Application description	Conditions	Typ.	Unit
OFF	AP and peripherals are powered OFF, waiting for turn-on event to start	PMIC in OFF state Monitoring turn-on event from PONKEYn/EN, I²C and PWRCTRLx unused All regulators OFF (except INTLDO) GPOx are inactive	38 (1)	µA
STANDBY	AP is in STANDBY mode (suspend to flash). All peripherals are powered OFF.	PMIC in POWER_ON standby state IRQ from any source or turn-off event from EN. LDO1 ON, $V_{LDO1OUT}$ = 1.8 V (VDDA18AON) LDO2 ON, $V_{LDO2OUT}$ = 3.3 V (VDDIO) All other regulators OFF. All outputs without load. No activity on I²C.	218	
STOP	AP is in LPLV-STOP2 (Core-on-lv /CPU Off) DDR4 in self-refresh All peripherals are powered OFF	PMIC in POWER_ON RUN state Monitoring IRQ from any source or turn-off event from EN. Monitoring PWRCTRLx BUCK1 ON, V_{OUT1} = 0.82 V (VDDCORE) BUCK2 ON, V_{OUT2} = 1.2 V (VDD_DDR) LDO1 ON, V_{LDOOUT} = 1.8 V (VDDA18AON) LDO2 ON, V_{LDOOUT} = 3.3 V (VDDIO), LDO7 ON V_{LDOOUT} = 2.5 V (VPP_DDR) All other regulators OFF (GPOx assumed inactive), all outputs without load No activity on I²C	470	
RUN	AP is in RUN1 overdrive (core on / CPU ON-overdrive) DDR4 is running	PMIC in POWER_ON RUN state Monitoring IRQ from any source or turn-off event from EN Monitoring PWRCTRLx BUCK1 ON, V_{OUT1} = 0.82 V (VDDCORE) BUCK2 ON, V_{OUT2} = 1.2 V (VDD_DDR) BUCK3 ON, V_{OUT3} = 0.91 V (VDD_CPU) LDO1 ON, V_{LDOOUT} = 1.8 V (VDDA18AON) LDO3 ON, V_{LDOOUT} = sink/source mode (VTT_DDR) LDO2 ON, V_{LDOOUT} = 3.3 V (VDDIO) LDO7 ON, V_{LDOOUT} = 2.5 V (VPP_DDR) All other regulators OFF (GPOx assumed inactive), all outputs without load No activity on I²C	900	µA

1. *Current consumption, 100 µA max at T = -40 °C to +105 °C*

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3.4 Electrical and timing parameter specifications

All parameters are specified at V_{IN} = $V_{BUCKxIN}$ = V_{LDOxIN} = 5 V except V_{LDO3IN} = V_{OUT2}, V_{OUT1} = 0.82 V, V_{OUT2} = 1.2 V, V_{OUT3} = 0.91 V, $V_{LDO1OUT}$ = $V_{LDO6OUT}$ = 1.8 V, $V_{LDO2OUT}$ = $V_{LDO4OUT}$ = $V_{LDO5OUT}$ = 3.3 V, $V_{LDO3OUT}$ = snk/src, $V_{LDO7OUT}$ = 2.5 V, V_{IO} = $V_{LDO2OUT}$, T_j = -40 °C to + 125 °C, with recommended BOM, unless otherwise specified.

3.4.1 General section

Table 7. Electrical and timing parameter specifications (general section)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
General section						
V_{IN}	Input voltage range		2.8	3.6 or 5	5.5	V
V_{INPOR_Rise}	V_{INPOR} rising threshold		2.2	2.3	2.4	V
V_{INPOR_Fall}	V_{INPOR} falling threshold			2.1	2.2	V
V_{INOK_Rise}	V_{INOK} rising threshold	Programmable value defined in the NVM register	3	3.1	3.2	V
			3.2	3.3	3.4	
			3.35	3.5	3.6	
			3.8	4.0	4.1	
V_{INOK_HYST}	V_{INOK} hysteresis	Programmable value defined in the NVM register		200 300 400 500		mV
V_{INOK_Fall}	V_{INOK} falling threshold	Defined indirectly by $V_{INOK_Rise}$and V_{INOK_HYST} settings		V_{INOK_Rise} - V_{INOK_HYST}		mV
t_{VINOK_Fall}	V_{INOK} falling delay	When V_{IN} is crossing V_{INOK_Fall}, PMIC power-down, then cannot restart before t_{VINOK_Fall} delay, even if V_{IN} > V_{INOK_Rise}		100		ms
V_{INLOW_Rise}	V_{INLOW} rising threshold	Programmable value defined in V_{INLOW_CR} register	+20 +300	V_{INOK_Fall} + 50 to V_{INOK_Fall}+ 400	+80 +500	mV
V_{INLOW_HYST}	V_{INLOW} hysteresis	Programmable value defined in V_{INLOW_CR} register	90	100	110	mV
			180	200	220	
			270	300	330	
			360	400	440	
V_{INLOW_Fall}	V_{INLOW} falling threshold	Defined indirectly by V_{INLOW_Rise} and V_{INLOW_HYST} settings		V_{INLOW_Rise} + V_{INLOW_HYST}		mV
T_{WRN_Rise}	Warning temperature rising		115	125	135	°C
T_{WRN_Fall}	Warning temperature falling		95	105	120	°C
T_{SHDN_Rise}	Shutdown temperature rising		140	150	160	°C
T_{SHDN_Fall}	Shutdown temperature falling		105	115	130	°C

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Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t_{TSHDN_DLY}	Shutdown temperature falling delay			3		s
t_{OCPDB_LDO}	LDO OCP turn-off delay			5		ms
t_{OCPDB_BUCK}	BUCK OCP turn-off delay			5		ms
t_{HICCUP_DLY}	Hiccup mode OFF delay	Programmable value defined in NVM_BUCKS_IOUT_SHR2 NVM register		0 100 500 1000		ms
t_{WD}	Watchdog timer	Programmable value defined in the register		1 to 256		s
		Timer programming step		1		
NVM_{END}	NVM write cycles endurance	Recommended maximum writing cycles (1)			10	Cycle
V_{NVM_PROG}	NVM min voltage for write operation		3.8			V

1. *NVM writing procedures must be performed under controlled electrical/environmental values.*

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3.4.2 Digital interface

Table 8. Electrical and timing parameter specifications (digital interface)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Digital interface						
V_{IO}	V_{IO} input voltage for IO signal		1.7	1.8 or 3.3	3.6	V
V_{IL}	PONKEYn/EN input low voltage		0		0.3 x V_{INTLDO} (2)	V
	RSTn, PWRCTRLx input low voltage		0		0.3 x VIO	
	SDA, SCL input low voltage	I²C NXP UM10204 revision 5 compliant (October 2012)	0		0.3 x VIO	
V_{IH}	PONKEYn/EN input high voltage		0.7 x VINTLDO (2)		VIN	V
	RSTn, PWRCTRLx input high voltage		0.7 x VIO		VIO	
	SDA, SCL input high voltage	I²C NXP UM10204 revision 5 compliant (October 2012)	0.7 xVIO		VIO	
V_{HYST}	PONKEYn/EN input hysteresis			0.1 x VINTLDO (2)		V
	RSTn, PWRCTRLx, input hysteresis			0.1 x VIO		
	SDA, SCL input hysteresis	I²C NXP UM1020044 revision 5 compliant (October 2012)		0.1 x VIO		
V_{OL}	RSTn, INTn, GPOx output low voltage	IO = 4 mA			0.4	V
	SDA, SCL output low voltage	I_{IO} = 4 mA, I²C NXP UM1020044 revision 5 compliant (October 2012)			0.4	
V_{OH}	GPOx output high voltage	I_{IO} = 4 mA			V_{IN} – 0.4	V
R_{PD}	PWRCTRLx pins pull-down resistor	Internally connected to GND	60	90	140	KΩ
	PONKEYn/EN pin pull-downn resistor	Internally connected to GND	60	100	140	KΩ
R_{PU}	RSTn, INTn, PWRCTRLLxxx pins pull-up resistor	Internally connected to VIO	50	80	120	KΩ
	PONKEYn/EN pin pull- p resistor	Internally connected to VIN	80	120	140	
$t_{PONKEYnDB}$	PONKEYn/EN pin debounce filter duration	No debounce filter for EN		30		ms
t_{RSTnAS}	RSTn assertion time (1)		30			µs

1. *Pulse smaller than t_{RSTnAS} duration. PMIC R_{STn} has no debounce filter. PMIC must detect a pulse equal to or longer than t_{RSTn} as duration.*
2. *V_{INTLDO} = 1.8 V*

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3.4.3 LDO1

Table 9. Electrical and timing parameters specification (LDO1)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
LDO1						
V_{LDOIN}	Main input voltage range		2.8		5.5	V
V_{LDOOUT}	Output voltage			1.8		V
$V_{LDOOUT-ACC}$	Output voltage accuracy	2.8 V < V_{LDOIN} < 5.5 V 10 µA< I_{LDOOUT} < 20 mA	-4		4	%
I_{LDOLIM}	Output current limitation	2.8 V < V_{LDOIN} < 5.5 V	20	30		mA
I_{LDOQ}	Total quiescent current	I_{LDOOUT} = 0 mA, (relative to cumulative value on V_{IN})		4 (1)	7	µA
I_{LDOIN_LKG}	Input leakage current	LDO OFF, T_j = +25°C (relative to cumulative value on V_{IN})			2	µA
$V_{LDODROP}$	Dropout voltage			N/A (2)		mV
$V_{LDOOUT-LO}$	Load transient regulation	I_{LDOOUT} = 10 µA to 10 mA and reciprocally, ΔV_{LDOIN} = 0, t_R = t_F ~1 µs		10	15	mV
$V_{LDOOUT-LI}$	Line transient regulation	V_{LDOIN} = 4.5 V to 5 V and reciprocally, $\Delta I_{LDO1OUT}$ = 0, t_R = t_F ~10 µs		5	10	mV
P_{SRRLDO}	Power supply rejection ratio	ΔV_{LDOIN} = 300 mVPP, f = [0.1:20] kHz, T_j = 25°C, I_{LDOOUT} = 10 mA ΔV_{LDOIN} = 300 mVPP, f = [20:100] kHz, Tj = 25°C, I_{LDOOUT} = 10 mA	45 (3) 40 (3)	50 45		dB
N	Output noise	I_{LDOOUT} = 10 µA to 10 mA, f = 10 Hz to 5 MHz,		2.5	500	µVrms
		T_j = 25°C, all bucks enabled.		2.5	5	mVpp
t_{SSLDO}	Soft-start duration	2.8 V < V_{LDOIN} < 5.5 V, 0 < I_{LDOOUT} < 1 mA, C_{OUT} = 4.7 µF		160 (3)		µs
$V_{LDOOUT-SO}$	Startup overshoot	2.8 V < V_{LDOIN} < 5.5 V, I_{LDOOUT} <10 µA		1	4	%
t_{SDLDO}	Shutdown duration	Pull-down enabled, V_{LDOOUT} = 1.8 V to V_{LDOOUT} = 0.2 V, I_{LDOOUT} = no load			1.5	ms

1. *V_{IN} = V_{LDOIN} = 5 V, T_j = 25°C.*
2. *With V_{IN} min (2.8V), LDO1 is always able to maintain output voltage at 1.8V.*
3. *Value can be impacted by current limitation and C_{OUT} value.*

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3.4.4 LDO2, LDO5, LDO6 and LDO7

Table 10. Electrical and timing parameters specification (LDO2 / 5 / 6 / 7)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
LDO2, LDO5,LDO6, LDO7						
V_{LDOIN}	Main input voltage range		2.8		5.5	V
V_{LDOOUT}	Output voltage	$V_{LDOIN} > V_{LDOOUT} + V_{LDODROP}$ Programmable value.		0.9 to 4.0		V
		Voltage programming step		100		mV
$V_{LDOOUT-ACC}$	Output voltage accuracy	2.8 V < V_{LDOIN} < 5.5 V 1.7 V < V_{LDOOUT} < 3.3 V with $V_{LDOIN} > V_{LDOOUT} + V_{LDODROP}$ 100 µA < I_{LDOOUT} < 350 mA	-2		2	%
I_{LDOLIM}	Output current limitation	2.8 V < V_{LDOIN} < 5.5 V Programmable value in NVM_LDOS_IOUT_SHR.	50 100 200 400		75 150 300 600	mA
I_{LDOQ}	Total quiescent current	I_{LDOOUT} = 0 mA, (relative to cumulative value on V_{IN})		9 (1)	20	µA
I_{LDOIN_LKG}	Input leakage current	LDO OFF (relative to cumulative value on V_{IN})		0.5	2	µA
$V_{LDODROP}$	Dropout voltage (2)	V_{LDOOUT} = 2.9 V, I_{LDOOUT} = 350 mA		180	300	mV
$V_{LDOOUT-LO}$	Load transient regulation	I_{LDOOUT} = 1 mA to 180 mA and reciprocally, ΔV_{LDOIN} = 0, t_R = t_f ~1 µs		35		mV
$V_{LDOOUT-LI}$	Line transient regulation	V_{LDOIN} = 4.5 V to 5 V and reciprocally, $\Delta I_{LDO1OUT}$ = 0, t_R = t_F ~10 µs		10		mV
P_{SRRLDO}	Power supply rejection ratio	ΔV_{LDOIN} = 300 mVPP, f = [0.1:20] kHz, Tj = 25°C, I_{LDOOUT} = 200 mA ΔV_{LDOIN} = 300 mVPP, f = [20:100] kHz, Tj = 25°C, I_{LDOOUT} = 200 mA		43 37		dB
t_{SSLDO}	Soft-start duration	2.8 V < V_{LDOIN} < 5.5 V, 0 < I_{LDOOUT} < 1 mA C_{OUT} = 4.7 µF, V_{LDOOUT} = 3.3 V		160 (3)		µs
$V_{LDOOUT-SO}$	Startup overshoot	2.8 V < V_{LDOIN} < 5.5 V, 1.7 V < V_{LDOOUT} < 3.3 $V_{ILDOOUT}$ < 10 µA		1	2	%
t_{SDLDO}	Shutdown duration	Pull-down enabled, V_{LDOOUT} = 3.3 V to V_{LDOOUT} = 0.2 V, I_{LDOOUT} = no load			1.5	ms

1. *V_{IN} = V_{LDOIN} = 5 V, T_j = 25°C*
2. *Dropout is the smallest difference between a regulator's input and its output voltage, which is required to maintain regulation and enable the regulator to provide rated voltage and current.*
3. *Value can be impacted by current limitation and V_{OUT} and C_{OUT} values.*

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3.4.5 LDO3

Table 11. Electrical and timing parameter specifications (LDO3)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
LDO3 normal mode						
V_{LDOIN}	Main input voltage range		2.8		5.5	V
V_{LDOOUT}	Output voltage	$V_{LDOIN} > V_{LDOOUT} + V_{LDODROP}$ programmable value.		0.9 to 4.0		V
		Voltage programming step		100		mV
$V_{LDOOUT-ACC}$	Output voltage accuracy	2.8 V < V_{LDOIN} < 5.5 V, 1.7 V < V_{LDOOUT} < 3.3 V 100 µA < I_{LDOOUT} < 120 mA	-2		+2	%
I_{LDOLIM}	Output current limitation	2.8 V < V_{LDOIN} < 5.5 V	120	150	180	mA
I_{LDOQ}	Total quiescent current	I_{LDOOUT} = 0 mA		7 (1)	13	µA
I_{LDOIN_LKG}	Input leakage current	LDO output disabled, Tj = 25 °C		1	3	
$V_{LDODROP}$	Dropout voltage	V_{LDOOUT} = 3.3 V, I_{LDOOUT} = 100 mA		120	200	mV
$V_{LDOOUT-LO}$	Load transient regulation	I_{LDOOUT} = 100 µA to 50 mA, t_R = t_F =1 µs		20		
$V_{LDOOUT-LI}$	Line transient regulation	V_{LDOIN} = 4.5 V to 5 V, t_R = t_F = 10 µs. ΔI_{LDOOUT} = 0 mA		5		
P_{SRRLDO}	Power supply rejection ratio	ΔV_{LDOIN} = 3000 m_{VPP}, f = [0.1:22] kHz, Tj = 25 °C, I_{LDOOUT} = 0 mA		45		dB
		ΔV_{LDOIN} = 300 m_{VPP}, f = [20:100] kHz, T_j =25 °C, I_{LDOOUT} = 50 mA		40		
t_{SSLDO}	Soft-start duration	2.8 V < V_{LDDOIN} < 5.5 V, 0 < I_{LDOOUT} < 1 mA C_{OUT} = 4.7 µF, V_{OUT} =1.8 V		160 (2)		µs
$V_{LDOOUT-SO}$	Startup overshoot	2.8 V < V_{LDOIN} < 5.5 V, 1.7 V < V_{LDOOUT} < 3.3 V I_{LDOOUT} < 10 µA		1	2	%
t_{SDLDO}	Shutdown duration	Pull-down enabled, V_{LDOOUT} = 3.3 V to V_{LDOOUT} = 0.2 V, I_{LDOOUT} = no load			1.5	ms
LDO3 sink-source mode (DDR VTT supply)						
V_{LDOIN} = V_{OUT2} = 1.2 V, V_{IN} = 5.0 V, $V_{BUCK2IN}$ = 5.0 V, V_{LDOOUT} = V_{OUT} 2/2,T_j = -40 °C to +125 °C, recommended BOM, unless otherwise specified						
$V_{LDOIN-SS}$	Input voltage range		1.1	1.2	1.6	V
$V_{LDOOUT-SS}$	Output voltage			VOUT2/2		
$V_{LDOOUT-ACC-SS}$	Output voltage accuracy	1.1 V < V_{LDOIN} < 1.6 V, -215 mA < I_{LDOOUT} < +215 mA	-1.5		+1.5	%
$I_{LDOOUT-SS}$	Continuous output current	1.1 V < V_{LDOIN} < 1.6 V			120	mA_{RMS}
$I_{LDOLIM-SS}$	Output current limitation	V_{LDOIN} = 1.1 V to 5.5 V	±230		±500	mA
$I_{LDOQ-SS}$	Total quiescent current	I_{LDOOUT} = 0 mA, measured from LDO3IN pin		4 (1)	20	µA
$V_{LDOOUT-LO-SS}$	Load transient regulation	I_{LDOOUT}= ± [0:50] mA, t_R = t_F = 250 ns		30		mV

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Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{LDOOUT-LI-SS}$	Line transient regulation	V_{LDOIN} = V_{OUT2} = 1.2 V ±30 mV, t_R = t_F = 10 µs		5		mV
$t_{SSLDO-SS}$	Soft-start duration	1.1 V < V_{LDOIN} < 1.6 V, $\|I_{LDOOUT}\|$ <1 mA, C_{OUT} = 10 µF		20	40	µs
t_{SU_LDO}	Startup delay (delay before voltage starts to rise)	controlled by a PWRCTRLx. PWRCTRL delay = 0		16	20	µs
$V_{LDOOUT-SO-SS}$	Startup overshoot	1.1 V < V_{LDOIN} < 1.6 V, V_{LDOOUT} = VOUT2/2, L_{DOOUT} = 10 µA			4	%
$t_{SDLDO-SS}$	Shutdown duration	Pull-down enabled, V_{LDOOUT} = Vout2/2 to V_{LDOOUT} = 0.2 V, I_{LDOOUT} = no load			1.5	ms

1. *V_{1N} = V_{LD01N} = 5 V, T = 25°C*
2. *Value can be impacted by V_{0UT} and C_{0UT} values.*

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3.4.6 LDO4

Table 12. Electrical and timing parameter specifications (LDO4)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
LDO4						
V_{LDOIN}	Main input voltage range	V_{LDOIN} from V_{IN}	2.8		5.5	V
$V_{LDOOUT-ACC}$	Output voltage accuracy	V_{LDOIN} = 3.6 V to 5.5 V 100 µA < I_{LDOOUT} < 30 mA	3.23	3.3	3.40	
I_{LDOLIM}	Output current limitation	V_{LDOIN} = 3.6 V to 5.5 V	50	75	200	mA
I_{LDOQ}	Quiescent current	I_{LDOOUT} = 0 m		20 (1)	25	µA
$V_{LDODROP}$	Dropout voltage from V_{IN} pin	I_{LDOOUT} = 75 mA		45	90	mV
$V_{LDOOUT-LO}$	Load transient regulation	I_{LDOOUT} = 1 to 3 mA, t_R = t_F = 1 µs		40		
$V_{LDOOUT-LI}$	Line transient regulation	V_{IN} = 4.5 V to 5 V, I_{LDOOUT} = 0 mA, ΔI_{LDOOUT} = 0 mA		10		
P_{SRRLDO}	Power supply rejection ratio	ΔV_{LDOIN} = 300 mVPP, f = [0.1:20] kHz, T_j = 25°C, I_{LDOOUT} = 25 mA		55		dB
		ΔV_{LDOIN} = 300 mVPP, f = [20:100] kHz, T_j = 25°C, I_{LDOOUT} = 25 mA		40		
t_{SSLDO}	Soft-start duration	3.6 V < V_{LDOIN} < 5.5 V, 0 < I_{LDOOUT} < 1 mA, C_{OUT} = 4.7 µF		100 (2)		µs
$V_{LDOOUT-SO}$	Startup overshoot	3.6 V < V_{LDOIN} < 5.5 V, I_{LDOOUT} < 10 µA		1	2	%
t_{SDLDO}	Shutdown duration	Pull-down enabled, V_{LDOOUT} = 3.3 V to V_{LDOOUT} = 0.2 V, I_{LDOOUT} = no load			1.5	ms

1. *V_{IN} = V_{LD0IN} = 5 V, T = 25°C.*
2. *Value can be impacted by V_{0UT} and C_{0UT} values.*

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3.4.7 BUCK1

Table 13. Electrical and timing parameter specifications (BUCK1)

Symbol	Parameter	VOUT range	Test conditions	Min.	Typ.	Max.	Unit
BUCK1 (LV and HV)							
V_{BUCKIN}	Main input voltage range			2.8		5.5	V
V_{OUT}	Output voltage	LV	Programmable value		0.5 to 1.5		V
			Voltage programming step		10		mV
		HV	VBUCKIN > VOUT + VBUCKDROP Programmable value		1.5 to 4.2		V
			Voltage programming step		100		mV
$V_{OUT-ACC}$	Output Voltage Error amplifier accuracy (4)	LV	1 mA < I_{OUT} < 2000 mA 3.0 V < V_{BUCKIN} < 5.5 V 0.7 V < V_{OUT} < 1.0 V	-1.5		1.5	%
		HV	1 mA < I_{OUT} < 2000 mA 2.8 V < V_{BUCKIN} < 5.5 V 1.5 V < V_{OUT} < 4.2 V	-1.5		1.5	
$V_{OUT-REG}$	Output load regulation (1)	HV/LV	CCM mode 1 mA < I_{OUT} < 1.5 A	-1		1	
$V_{OUT-RIPP}$	Output voltage ripple (2)	LV	5 mA < I_{OUT} < 2000 mA 3.0 V < VBUCKIN < 5.5 V 0.7 V < V_{OUT} < 1.5 V (V_{OUT} = 1.2 V)		10		mVpp
		H	5 mA < I_{OUT} < 2000 mA 2.8 V < V_{BUCKIN} < 5.5 V 1.5 V < V_{OUT} < 4.2 V		15		
I_{OUT}	Max output current (4)		2.8 V < V_{BUCKIN} < 5.5 V Programmable value in NVM_BUCKS_IOUT_SHR1	500 1000 1500 2000			mA
I_{BCKLIM}	Inductor peak current limit		Depends on NVM_BUCKS_IOUT_SHR1 Max output current steps (0.5 A, 1 A, 1.5 A, 2 A) can be defined based on the selected inductor peak current limit level		1.5 2.1 2.8 3.3		A
f_{REFCLK}	Reference switching frequency				2		MHz
I_{Q_BCK}	Total quiescent current		I_{OUT} = 0 mA		115	300	µA
I_{BUCKIN_LKG}	Input leakage current		BUCK OFF, Tj = + 25 °C		0.01	1	µA
EFF_{BCK}	Efficiency		V_{BUCKIN}= 5 V, V_{OUT} = 0.8 V, T_J = +50 °C				%
			I_{OUT} = 10 mA		81		

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Symbol	Parameter	VOUT range	Test conditions	Min.	Typ.	Max.	Unit
EFF_{BCK}	Efficiency		I_{OUT} = 100 mA		83		%
			I_{OUT} = 300 mA		84		
			I_{OUT}= 1000 mA		82		
			I_{OUT} = 2000 mA		76		
V_{OUT-LO}	Load transient regulation (4)	LV	3.0 V < V_{BUCKIN} < 5.5 V 0.7 V < V_{OUT} < 1.0 V (typ 820 mV) 5 mA < I_{OUT} < 1.5 A ΔI_{OUT} = 1000 mA, tR/tF = 500 ns eg1: I_{OUT} = 5 mA <=> 1000 mA eg2: 1300 mA <=> 300 mA			+/-34	mV
		HV	5 mA < I_{OUT} < 2 A ΔI_{OUT} = 500 mA, t_R = t_F = 1 µs 3.0 V < V_{BUCKIN} < 5.5 V ΔV(in-out) > 1.5 V 1.8 V < V_{OUT} < 3.3 V			50	
V_{OUT-LI}	Line transient regulation		ΔV_{BKIN}= 600 mV, t_R = t_F = 10 µs, I_{OUT} = 300 mA, ΔV(in-out) > 1.5 V		1.5	10	mV
$V_{OUT-OVR}$	Power-up overshoot		2.8 V < V_{BKIN} < 5.5 V, I_{OUT} = 1 mA T_A= + 25°C, 0.5 V < V_{OUT} < 4.2 V			35	mV
$t_{NORM-CCM-BCK}$	Recovery time from Normal to Forced CCM mode		V_{OUT}_Norm = V_{OUT_CCM}, controlled by a PWRCTRLx			40 (4)	µs
t_{SU_BCK}	Start-up delay (delay before voltage starts to rise)		2.8 V < V_{BUCKIN} < 5.5 V, controlled by a PWRCTRLx		25 (3)	40 (4)	µs
t_{SS_BCK}	Soft-start duration	LV	2.8 V < V_{BUCKIN} < 5.5 V, 1 mA < I_{OUT} < 100 mA, V_{OUT}= 1.5 V	200		1500	µs
		HV	2.8 V<V_{BUCKIN}<5.5 V, 1 mA<I_{OUT}<100 mA V_{OUT} = 4.2 V	200		1500	
SR_{BCK}	Output voltage slew rate	LV	Slew rate during start-up	1		4.7	mV/µs
		HV	Slew rate during start-up	2.8		13.1	
			DVS slew rate of a voltage programmed change low to high or high to low, from V_{OUT} = 0.5 V to 1.5 V (LV) or V_{OUT} = 1.5 V to 4.2 V (HV)	1	3.1		
t_{SD_BCK}	Shutdown duration	LV	From V_{OUT} = 1.5 V to V_{OUT} < 0.2 V 2.8 V < V_{BUCKIN} < 5.5 V, I_{OUT} < 1 mA				ms
			Slow PD			1.5	
			Fast PD			0.3	
		HV	From V_{OUT} = 4.2 V to V_{OUT} < 0.2 V 2.8 V < V_{BUCKIN} < 5.5 V, I_{OUT} < 1 mA				
			Slow PD			1.5	
			Fast PD			0.3	

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1. *Guaranteed by design - not tested in production. Load transient performances are strongly impacted by the external passive component characteristics. The load transient is also influenced by the parasitic elements of the PCB layout. For more info see the forthcoming AN.*
2. *The output ripple voltage is the result of the inductor ripple current flowing through the output capacitor and depends on the capacitance value, ESR, and ESL. The actual output ripple voltage is also influenced by the parasitic elements of the PCB layout.*
3. *See startup sequence.*
4. *Guaranteed by design - not tested in production.*

3.4.8 BUCK2

Table 14. Electrical and timing parameter specifications

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
BUCK2						
V_{BUCKIN}	Main input voltage range		2.8		5.5	V
$V_{OUT-ACC}$	Output Voltage Error amplifier accuracy	Programmable value		0.5 to 1.5		V
		Voltage programming step		10		mV
		1 mA < I_{OUT} < 1000 mA 2.8 V < V_{BUCKIN} < 5.5 V 0.5 V < V_{OUT} < 1.5 V	-1.5		1.5	%
		1 mA < I_{OUT} < 1000 mA 3.0 V < V_{BUCKIN} < 5.5 V 1.0 V < V_{OUT} < 1.35 V	-1		1	
$V_{OUT-REG}$	Output Load Regulation	CCM mode 1 mA < I_{OUT} < 1.5 A	-1		1	
$V_{OUT-RIPP}$	Output voltage ripple	3.0 V < V_{BUCKIN} < 5.5 V 50 mA < I_{OUT} < 1000 mA, 1.0 V < V_{OUT} < 1.35 V		10		mVpp
I_{OUT}	Max output current	3.0 V < V_{BUCKIN} < 5.5 V Programmable value in NVM_BUCKS_IOUT_SHR1	500 1000 1500 2000			mA
I_{BKLIM}	Inductor peak current limit	Depends on NVM_BUCKS_IOUT_SHR1 Max output current steps (0.5 A, 1 A, 1.5 A, 2 A) can be defined based on the selected Inductor peak current limit level		1.5 2.1 2.8 3.3		A
f_{REFCLK}	Reference switching frequency			2		MHz
I_{Q_BCK}	Total quiescent current	I_{OUT} = 0 mA		115	300	µA
I_{BUCKIN_LKG}	Input leakage current	$B_{UCK\ OFF}$, T_j = + 25 °C		0.01	1	µA
E_{FFBCK}	Efficiency	V_{BUCKIN} = 5 V, V_{OUT} = 1.2 V, T_j = + 50 °C				%
		I_{OUT} = 10 mA		79		
		I_{OUT} = 100 mA		81		

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Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
E_{FFBCK}	Efficiency	I_{OUT} = 300 mA		81		%
		I_{OUT} = 1000 mA		80		
		I_{OUT} = 1500 mA		77		
V_{OUT-LO}	Load transient regulation	3.0 V < V_{BUCKIN} < 5.5 V 1.0 V < V_{OUT} < 1.35 V (Typ: 1.2 V) 5 mA < I_{OUT} < 1.0 A ΔI_{OUT} = 450 mA, t_R = t_F = 500 ns eg1: I_{OUT} = 5 mA <=> 450 mA eg2: 1000 mA <=> 550 mA			+/-30	mV
V_{OUT-LI}	Line transient regulation	ΔV_{BKIN} = 600 mV, t_R = t_F =10 µs ΔI_{OUT} = 0		1.5	5	mV
$V_{OUT-OVR}$	Power-up overshoot	2.8 V < V_{BKIN} < 5.5 V, I_{OUT} =1 mA, T_A = +25°C 0.5 V < V_{OUT} < 1.5 V			30	mV
$t_{NORM-CCM-BCK}$	Recovery time from Normal to Forced CCM mode	V_{OUT_Norm} = V_{OUT_CCM} controlled by a PWRCTRLx			40	µs
t_{SU_BCK}	Start-up delay (delay before voltage starts to rise)	2.8 V < V_{BUCKIN} < 5.5 V controlled by a PWRCTRLx		25	40	
t_{SS_BCK}	Soft-start duration	2.8 V < V_{BUCKIN} < 5.5 V 1 mA < I_{OUT} < 100 mA V_{OUT} = 1.5 V	200		1500	
S_{RBCK}	Output voltage slew rate	Slew rate during start-up	1		4.54	mV/µs
		DVS slew rate of a voltage programmed change low to high or high to low, from V_{OUT} = 0.5 V to 1.5 V	1	3.1		
t_{SD_BCK}	Shutdown duration	From V_{OUT} = 1.5 V to V_{OUT} < 0.2 V 2.8 V < V_{BUCKIN} < 5.5 V, I_{OUT} < 1 mA				
		Slow PD			1.5	ms
		Fast PD			0.3	

1. *Guaranteed by design - not tested in production. Load transient performances are strongly impacted by the external passive component characteristics. The load transient is also influenced by the parasitic elements of the PCB layout. For more info see the forthcoming AN.*
2. *The output ripple voltage is the result of the inductor ripple current flowing through the output capacitor and depends on the capacitance value, ESR, and ESL. The actual output ripple voltage is also influenced by the parasitic elements of the PCB layout.*
3. *See startup sequence.*
4. *Guaranteed by design - not tested in production.*

3.4.9 BUCK3

Table 15. Electrical and timing parameters specification (BUCK3)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
BUCK3						
V_{BUCKIN}	Main input voltage		2.8		5.5	V

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Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{OUT}	Output voltage Error amplifier accuracy (1)	Programmable value		0.5 to 1.5		V
		Voltage programming step		10		mV
		1 mA < I_{OUT} < 2000 mA 3.0 V < V_{BUCKIN} < 5.5 V 0.7 V < V_{OUT} < 1.0 V	-1.5		1.5	%
$V_{OUT-REG}$	Output load regulation (4)	CCM mode 1 mA < I_{OUT} < 1.5 A	-1		1	
$V_{OUT-RIPP}$	Output voltage ripple (2)	3.0 V < V_{BUCKIN} < 5.5 V 5 mA < I_{OUT} < 1000 mA, 0.7 V < V_{OUT} < 1.0 V		25		mVpp
I_{OUT}	Max output current (4)	2.8 V < V_{BUCKIN} < 5.5 V Programmable value in NVM_BUCKS_IOUT_SHR1	500 1000 1500 2000			mA
I_{BCKLIM}	Inductor peak current limit	Depends on NVM_BUCKS_IOUT_SHR1 Max output current steps (0.5A, 1A, 1.5A, 2A) can be defined based on the selected Inductor peak current limit level		1.5 2.1 2.8 3.3		A
f_{REFCLK}	Reference switching frequency			2		MHz
I_{Q_BCK}	Total quiescent current	I_{OUT} = 0 mA		115	300	µA
I_{BUCKIN_LKG}	Input leakage current	BUCK OFF, Tj = +25 °C		0.01	1	µA
E_{FFBCK}	Efficiency	V_{BUCKIN} = 5 V, V_{OUT} = 0.91 V, HP mode, T_J = +50 °C				%
		I_{OUT} =10 mA		79		
		I_{OUT} = 100 mA (best efficiency load MP21)		81		
		I_{OUT} = 400 mA (best efficiency load MP23)		81		
		I_{OUT} = 1000 mA		80		
		I_{OUT} = 1500 mA		77		
		I_{OUT} = 2000 mA		75		
V_{OUT-LO}	Load transient regulation	3.0 V < V_{BUCKIN} < 5.5 V 0.7 V < V_{OUT} < 1.0 V (Typ: 0.91 V) 5 mA < I_{OUT} < 2000 mA Δ_{IOUT} = 1300 mA, t_R = t_F ~500 ns			+/-35 (3)	mV
V_{OUT-LI}	Line transient regulation	HP mode, ΔV_{BKIN} = 600 mV, t_R= t_F ~10 µs Δ_{IOUT} = 0		1.5	5	mV
$V_{OUT-OVR}$	Power-up overshoot	2.8 V < V_{BKIN}< 5.5 V, I_{OUT} ~ 1 mA, T_A = +25°C 0.5 V < V_{OUT} < 1.5 V			35	mV
$t_{NORM-CCM-BK}$	Recovery time from normal to forced CCM mode	V_{OUT_LP} = V_{OUT_HP} controlled by a PWRCTRLx			40 (4)	µs

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Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t_{SU_BCK}	Start-up delay (delay before voltage starts to rise)	2.8 V < V_{BUCKIN} < 5.5 V controlled by a PWRCTRLx		25	40 (4)	µs
t_{SS_BCK}	Soft-start duration	2.8 V < V_{BUCKIN} < 5.5 V 1 mA < I_{OUT} < 100 mA V_{OUT} = 0.8 V	200		1500	
S_{RBCK}	Output voltage slew rate	Slew rate during start-up	1		4.7	mV/µs
		DVS slew rate of a voltage programmed change low to high or high to low, from V_{OUT} = 0.5 V to 1.5 V	1	3.1		
t_{SD_BCK}	Shutdown duration	From V_{OUT} = 1.5 V to V_{OUT} < 0.2 V 2.8 V < V_{BUCKIN} < 5.5 V, I_{OUT} < 1 mA				ms
		Slow PD			1.5	
		FastPD			0.3	

1. *Guaranteed by design - not tested in production. Load transient performances are strongly impacted by the external passive component characteristics. The load transient is also influenced by the parasitic elements of the PCB layout. For more info see the forthcoming AN.*
2. *The output ripple voltage is the result of the inductor ripple current flowing through the output capacitor and depends on the capacitance value, ESR, and ESL. The actual output ripple voltage is also influenced by the parasitic elements of the PCB layout.*
3. *See startup sequence.*
4. *Guaranteed by design - not tested in production.*

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4 Power regulator descriptions

4.1 Overview

The STPMIC2L has a large input voltage range from 2.8 V to 5.5 V to supply applications typically from a 5 V DC wall-adaptor or from a 1-cell 3.6 V Li-Ion/Li-PO battery.

The STPMIC2L provides all the regulators needed to power supply a core chipset composed of the MPU, a DDR DRAM and a flash memory. GPOs enable control of discrete regulators to power supply application peripherals:

- 7 LDOs
- 3 step-down (buck) converters

Table 16. General description

Regulator	Output voltage (V)	Programming step (mV)	Rated output current (mA)	Application use (example)
LDO1	1.8	-	20	MPU' VDDA 18AON
LDO2 LDO5 LDO6 LDO7	0.9 V to 4.0 V	100	400/200/100/50	LDO2: VDDIO @ 3.3 V or @1.8 V LDO5: VDD_FLASH_MEM LDO6: VDDA18 LDO7: VPP_DDR
LDO3 normal mode	0.9 V to 4.0 V	100	120	General purpose / lpDDR VDD1
LDO3 sink-source mode	$V_{OUT}2/2$	-	+/-120 (rms) +/-230 (peak)	DDR3L/DDR4 terminations (VTT)
LDO4	3.3	-	50	MPU' VDD33USB
BUCK1	LV Mode 0.5 V to 1.5 V HV Mode 1.5 V to 4.2 V	10 100	2000, 1500, 1000, 500	MPU VDDCORE
BUCK2 / BUCK3	0.5 V to 1.5 V	10	2000, 1500, 1000, 500	Bk2: MPU VDDQDDR (DDR3L, DDR4, lpDDR3, lpDDR4) Bk3: MPU VDDCPU
GPO1, GPO5	-	-	-	External Control 1, 5

Note: V_{IN} is the main STPMIC2L supply. All buck converters and linear regulators have dedicated or shared power supply pins. The dedicated V_{IO} supply is for all digital interface pins except GPOs.

No other supply voltages must be applied before V_{IN} or set higher than V_{IN}.

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4.2 LDO regulators

4.2.1 LDO common features

Enable/disable - each LDO can be enabled or disabled independently:

- Automatically during the POWER_UP or POWER_DOWN sequence, depending on the NVM settings.
- By software (I²C access): Setting the EN bit in the related LDO control register.
- By PWRCTRLx pin state change: The PWRCTRLx pins need to be programmed by I²C to enable this feature.

$V_{LDO\ OUT}$ voltage setting - LDO output voltage can be set:

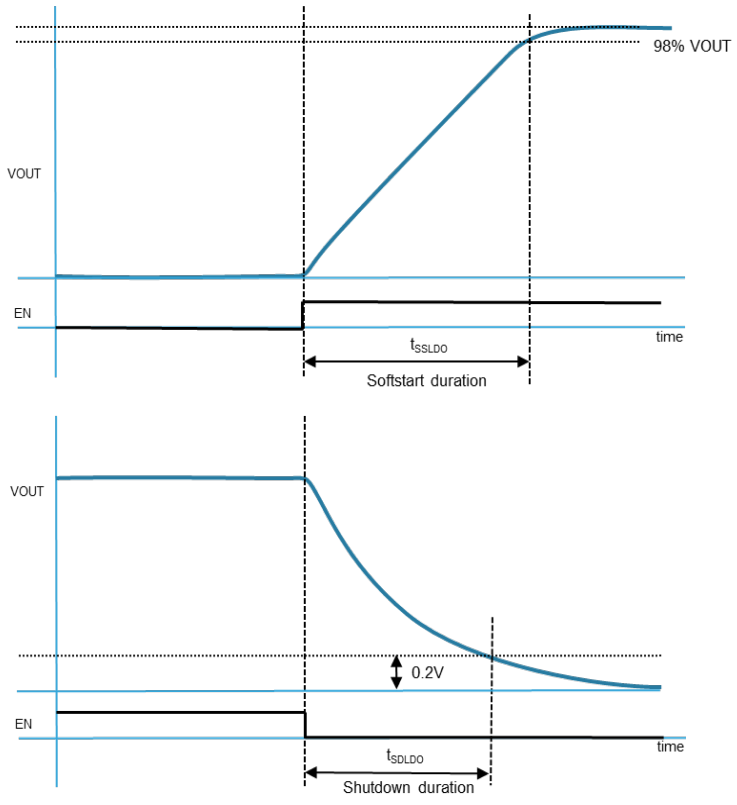
- Automatically during the POWER_UP or POWER_DOWN sequence depending on the NVM settings.
- By software (I²C access): Setting the V_{OUT} bitfield in the related LDO control register.
- By PWRCTRLx pin state change: the PWRCTRLx pins need to be programmed by I²C to select the output voltages needed to meet the MPU application requirements.

The LDO can be enabled or disabled as in normal operation. See the "**Enable/disable**" description above.

Soft start: This feature aims to limit input inrush current during the LDO startup phase. LDO soft-start duration is defined by the t_{SSLDO} parameter.

See figure below.

Figure 3. LDO startup/shutdown timings



Output discharge: When the LDO is disabled, a pull-down discharge is automatically enabled. It allows the LDO output voltage to discharge within a t_{SDLDO} time delay. The LDO output is low before disabling the next regulators in the next ranking slot. It is active by default. It can be disabled by software to put the LDO output in high impedance when the LDO is disabled (LDOS_PD_CR register).

OCP and hiccup management: Each LDO supports OCP and can operate in hiccup mode. When the output load of the LDO exceeds the I_{LDOLIM} overcurrent limit threshold, the LDO starts decreasing the output voltage, limiting the output current to I_{LDOLIM}. If the overcurrent lasts longer than t_{OCPDB_LDO}:

- An interrupt is generated (if the interrupt has been unmasked by software).

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- Hiccup mode (default behavior): The LDO is turned OFF for the t_{HICCUP_DLY} duration and then turned ON again.
- Fail-safe mode (alternative behavior): The PMIC is turned OFF for the t_{HICCUP_DLY} duration and then turned ON again (or goes into FAIL_SAFE_LOCK state).

See Section 5.4.17 for details on OCP & hiccup management.

LDO2, LDO5, LDO6 and LDO7 have programmable I_{LDOLIM} overcurrent limit thresholds. I_{LDOLIM} thresholds are programmed in the NVM_LDOS_IOUT_SHR NVM register.

4.2.2 LDO3 special features

The LDO3 is a multipurpose LDO with two operating modes:

- **Normal mode** – The LDO3 works as general-purpose LDO as well as LDO2, 5, 6 and 7.
- **Sink-source mode** – The LDO3 can regulate the output voltage working in sink-source mode. This mode is dedicated to supplying the termination of DDR3/DDR3L or DDR4 IC memories with fixed output voltage. If the LDO3 is used in this mode, LDO3IN must be powered from the output of BUCK2 (see Figure 4). The output voltage is fixed and follows VOUT2/2, even during the BUCK2 ramp-up and ramp-down phases. The overcurrent limitation works both during sink and source output current modes.

4.2.3 LDO4 special features

The LDO4 is dedicated to supply the MPU USB HS PHY.

The LDO4 output voltage is fixed at 3.3 V.

4.2.4 LDO output voltage settings

Table 17. LDO output voltage settings

	VOUT [4:0] (decimal)	VOUT [V] LDO2/LDO3 (normal mode)/LDO5/LDO6/LDO7
Step 100 mV	0	0.9
	1	1.0
	2	1.1
	3	1.2
	4	1.3
	5	1.4
	6	1.5
	7	1.6
	8	1.7
	9	1.8
	10	1.9
	11	2.0
	12	2.1
	13	2.2
	14	2.3
	15	2.4
	16	2.5
	17	2.6
	18	2.7
	19	2.8
	20	2.9

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	VOUT [4:0] (decimal)	VOUT [V] LDO2/LDO3 (normal mode)/LDO5/LDO6/LDO7
Step 100 mV	21	3.0
	22	3.1
	23	3.2
	24	3.3
	25	3.4
	26	3.5
	27	3.6
	28	3.7
	29	3.8
	30	3.9
	31	4.0

4.2.5 Examples of DDR memory power supply topology using LDOs

Figure 4. LDO3 uses in LDO mode with lpDDR4

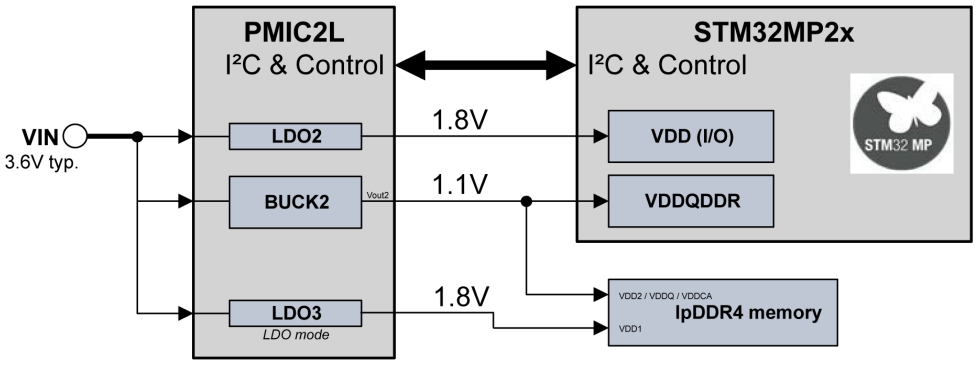
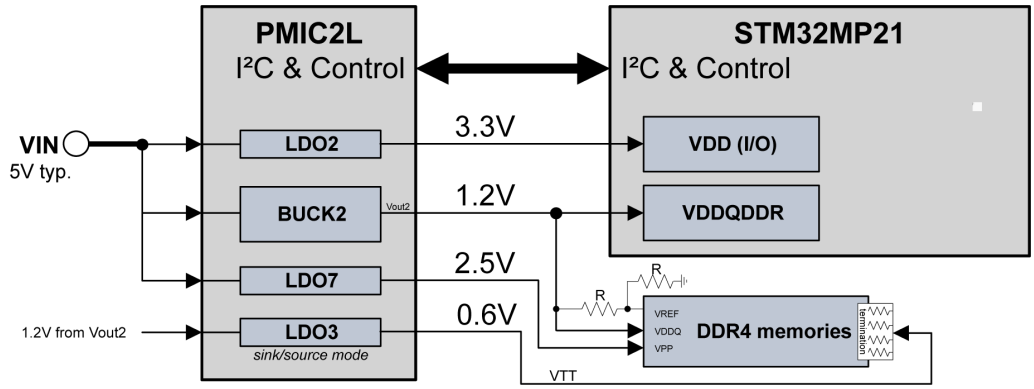


Figure 5. LDO3 uses in SINK/SOURCE mode with DDR4



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4.3 Buck converters

General description

The STPMIC2L includes 3 buck converters that are optimized to supply circuits with high current consumption and meet fast transient response requirements.

All converters are based on an adaptive constant-on-time controller (COT) that guarantees excellent transient response and high efficiency across a wide range of operating conditions.

The switching frequency of the converter is typically 2 MHz in a steady-state CCM condition. In a typical MPU application:

- BUCK1 is primarily dedicated to supply power to the VDDCORE domain.
- BUCK2 is primarily dedicated to supply power to the VDDQDDR domain.
- BUCK3 is primarily dedicated to supply power to the VDDCPU domain.

All BUCK converters have excellent load transient responses across operating conditions.

4.3.1 Buck converters common features

Enable/Disable: each buck can be enabled or disabled independently (same behavior as LDO: see Section 4.2.1).

V_{OUT} voltage setting: Output voltage can be set:

- Automatically during a POWER_UP or POWER_DOWN sequence depending on the NVM settings.
- By software (I²C access): Setting the V_{OUT} bitfield in the related buck control register.
- By PWRCTRLx pin state change: The BUCKx converter behaves according to BUCKx_MAIN_CR and BUCKx_ALT_CR content setting. BUCKx_MAIN_CR or BUCKx_ALT_CR is selected by the PWRCTRL pin allocated to BUCKx (see Section 5.4.11.

Forced PWM mode (CCM mode): Each buck can be forced to work in PWM mode to keep a constant frequency and low ripple.

Normal and forced PWM modes are activated by two PREG_MODE [1:0] register bits as follows:

00: Normal (or auto mode)

01: reserved

10: Forced PWM (CCM)

11: reserved

Clock synchronization and clock phase shifting: In normal mode, when all buck converters work in a steady state in CCM mode or in forced PWM, they are synchronized with a clock shifted by the following:

- 0°: BUCK1
- 135°: BUCK2
- 225° : BUCK3

Note: It is possible to force synchronization of all buck converters by phase shifting by setting all buck converters in forced CCM mode. This improves EMI and avoids peak current on the main power supply input source.

Dynamic voltage scaling (DVS): When the buck output voltage is increased/decreased dynamically by the software, the buck output voltage (V_{OUT}) is stepped up/down following the S_{RBK} slew rate.

When a lower V_{OUT} is set, part of the buck converter output energy is discharged from the output capacitor following the S_{RBK} slew rate, providing current back to the input supply capacitor. This operation improves the total power efficiency.

Frequency spreading: Switching frequency spreading is supported to help manage EMC.

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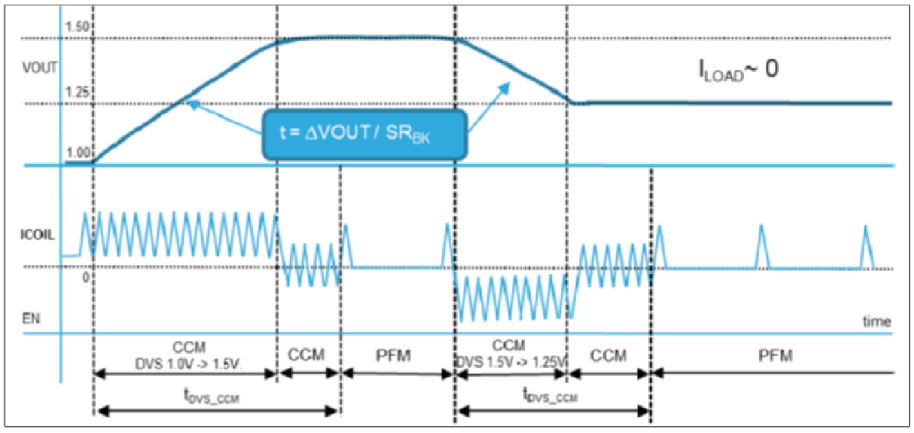
Figure 6. **Buck dynamic voltage scaling (DVS)**



OCP and hiccup management: Each buck converter supports OCP and can operate in hiccup mode. When the output load of the buck exceeds the I_{OUT} max output current (related to inductor peak current limit threshold I_{BKLIM}), the PWM pulse is immediately stopped, and the buck starts to decrease output voltage, limiting the output current. If the overcurrent lasts longer than t_{OCPDB_BUCK}:

- An interrupt is generated (if the interrupt has been unmasked by software).
- Default behavior: the buck is turned OFF for t_{HICCUP_DLY} duration and then turned ON again.
- Alternative behavior: the PMIC is turned OFF for t_{HICCUP_DLY} duration and then turned ON again (or goes to FAIL_SAFE_LOCK state).

See Section 5.4.17 for details on OCP & hiccup management.

All buck converters have a programmable I_{OUT} max current threshold. I_{OUT} thresholds are programmed in the NVM_BUCKS_IOUT_SHR NVM register.

Output discharge: When the buck is disabled, a configurable pull-down (PD) discharge is automatically enabled. The buck output voltage discharges in t_{SD_BKtime} duration (with typical recommended BOM) so that the buck converter output voltage is low before disabling the next regulators in the next ranking slot. Four values are configurable by software at runtime: no pull-down, slow-PD, fast-PD and forced slow-PD by setting BUCKS_PD_CR. Fast discharge output can be modified by software in fast-PD when the buck is disabled, or it can be disabled by software to place the buck converter output in high impedance when it is disabled. See Figure 7 which shows fast-PD and slow-PD behavior.

Startup sequence: When a buck is enabled, a startup delay (t_{SU_BCK}) occurs before the output voltage starts to rise, and is followed by a soft-start voltage ramp (t_{SS_BCK}). See Figure 7.

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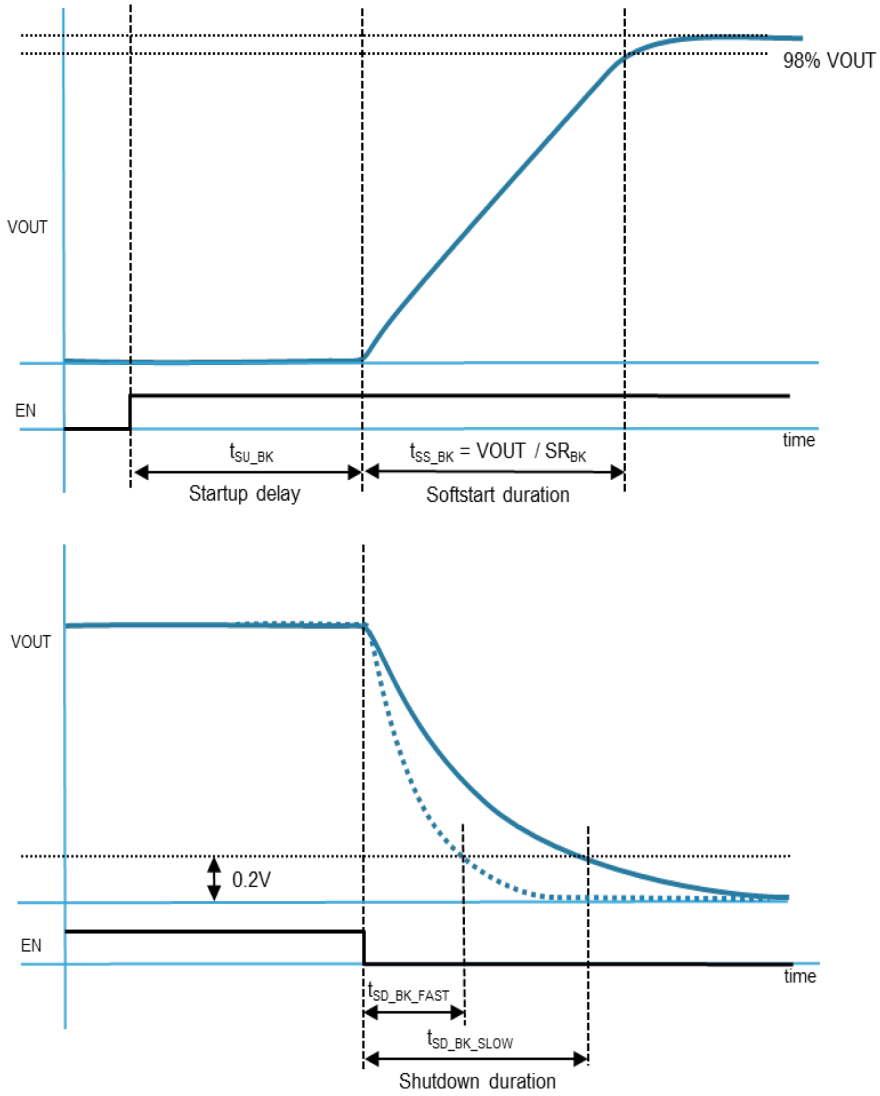
Figure 7. **Buck startup/shutdown timings**



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4.3.2 Buck output voltage settings

Table 18. **Buck output voltage settings**

	V_{OUT} [6:0] (decimal)	V_{OUT} [V] BUCK1_LV	V_{OUT} [V] BUCK1_HV	V_{OUT} [V] BUCK2/3
Step 10 mV LV	0	0.50	1.5	0.50
	1	0.51	1.5	0.51
	2	0.52	1.5	0.52
	3	0.53	1.5	0.53
	4	0.54	1.5	0.54
	5	0.55	1.5	0.55
	6	0.56	1.5	0.56
	7	0.57	1.5	0.57
	8	0.58	1.5	0.58
	9	0.59	1.5	0.59
	10	0.60	1.5	0.60
	11	0.61	1.5	0.61
	12 to 94	…	1.5	...
	95	1.45	1.5	1.45
	96	1.46	1.5	1.46
	97	1.47	1.5	1.47
	98	1.48	1.5	1.48
	99	1.49	1.5	1.49
	100	1.50	1.5	1.50
Step 100 mV HV	101	1.50	1.6	1.50
	102	1.50	1.7	1.50
	103	1.50	1.8	1.50
	104	1.50	1.9	1.50
	105	1.50	2.0	1.50
	106	1.50	2.1	1.50
	107	1.50	2.2	1.50
	108	1.50	2.3	1.50
	109	1.50	2.4	1.50
	110	1.50	2.5	1.50
	111	1.50	2.6	1.50
	112	1.50	2.7	1.50
	113 to 122	1.50	…	1.50
	123	1.50	3.8	1.50
	124	1.50	3.9	1.50
	125	1.50	4.0	1.50
	126	1.50	4.1	1.50
	127	1.50	4.2	1.50

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5 Feature descriptions

5.1 Functional state machine

Overview

STPMIC2L integrates advanced low-power features controlled by the application processor through I²C, four digital control pins (PONKEYn/EN, PWRCTRL1/2/3, and RSTn) and one interrupt output line (INTn).

The main parameter settings can be programmed in a non-volatile memory (NVM) as default values at the startup time. See Section 5.2

All regulators can be independently controlled from the PWRCTRLx pins. This allows flexible configuration and fast transition between different power strategies at the application level.

Other features are provided to fulfill high-end application processors and advanced operating system needs:

- Multiple turn-on/turn-off conditions
- Mask_reset and restart_request options
- Overcurrent and overvoltage protection
- Thermal protection
- Watchdog
- Interrupt controller
- Safety management

PMIC state machine - STPMIC2L state machine is described in Figure 8

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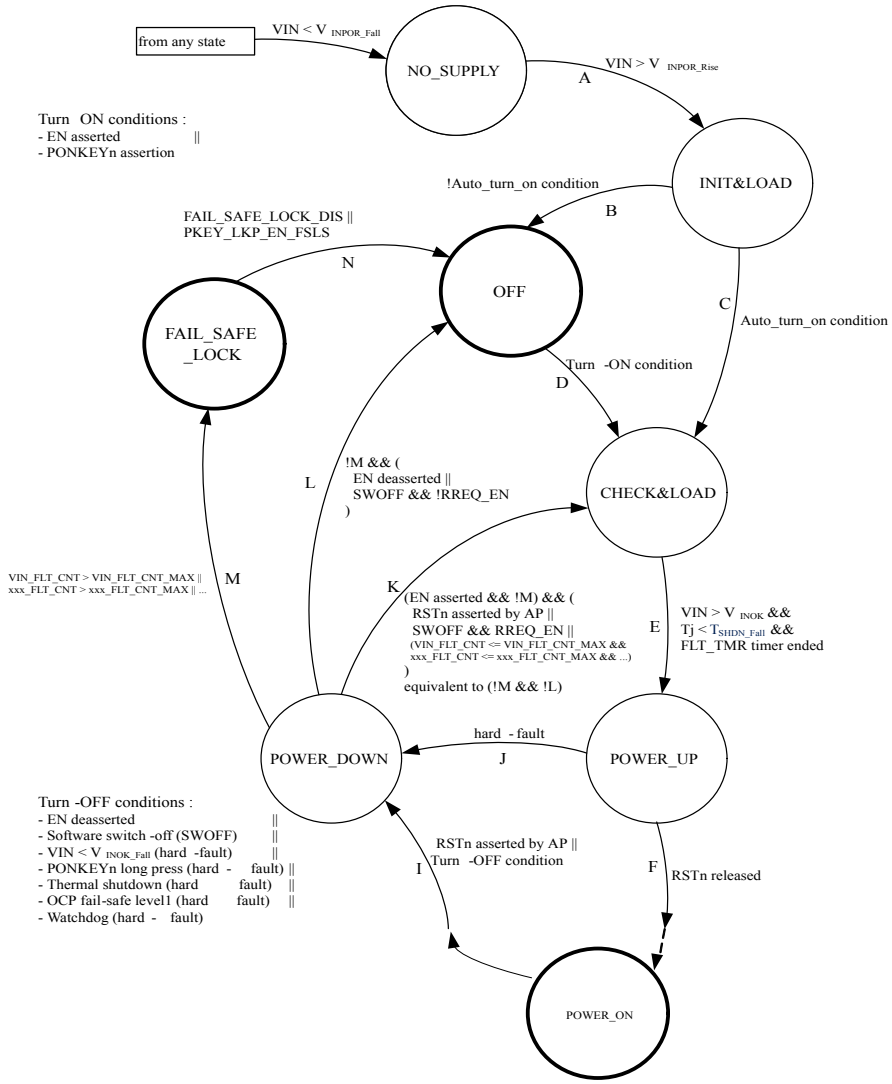
Figure 8. **PMIC state machine**



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5.1.1 Transition conditions

Table 19. PMIC state machine transition conditions

Transition symbol	State transition	Transition condition
A	NO_SUPPLY to INIT&LOAD	V_{IN} > V_{INPOR_Rise}
B	INIT&LOAD to OFF	**Not auto_turn_on condition:** Init_OK && load NVM_OK && !(AUTO_TURN_ON || PONKEYn_low || EN deasserted)
C	INIT&LOAD to CHECK&LOAD	**Auto_turn_on condition:** Init_OK && load NVM_OK && (AUTO_TURN_ON || PONKEYn_low || EN_asserted)
D	OFF to CHECK&LOAD	**Turn-on condition:** PONKEYn falling edge || EN asserted
E	CHECK&LOAD to POWER_UP	**CHECK&LOAD is a transitory state going to POWER_UP:** V_{IN} > V_{INOK} && T_j < T_{SHDN_Fall} && FLT_TMR timer ended
F	POWER_UP to POWER_ON	When power-up sequence ends without hard-fault, the PMIC released RSTn, Transition F occurs when RSTn signal goes higher than V_{IH}.
I	POWER_ON to POWER_DOWN	**EN deasserted ||** **RSTn signal asserted by AP ||** **Turn-off condition:** Software switch-off (SWOFF) || V_{IN} < V_{INOK_Fall} (hard-fault) || PONKEYn long press (hard-fault) || Thermal shutdown (hard-fault) || OCP fail-safe level1 (hard-fault) || Watchdog (hard-fault)
J	POWER_UP to POWER_DOWN	**Turn-off condition (hard-fault):** V_{IN} < V_{INOK_Fall} (hard-fault) || PONKEYn long press (hard-fault) || Thermal shutdown (hard-fault) || OCP fail-safe level1 (hard-fault) || Watchdog (hard-fault)
K	POWER_DOWN to CHECK&LOAD	(EN asserted && !M) || RSTn asserted by AP || (SWOFF && RREQ_EN) || (VIN_FLT_CNT <= VIN_FLT_CNT_MAX && PKEY_FLT_CNT <= PKEY_FLT_CNT_MAX && TSHDN_FLT_CNT <= TSHDN_FLT_CNT_MAX && OCP_FLT_CNT <= OCP_FLT_CNT_MAX && WDG_FLT_CNT <= WDG_FLT_CNT_MAX)
L	POWER_DOWN to OFF	!M && (EN deasserted || (SWOFF && !RREQ_EN))
M	POWER_DOWN to FAIL_SAFE_LOCK	VIN_FLT_CNT > VIN_FLT_CNT_MAX || PKEY_FLT_CNT > PKEY_FLT_CNT_MAX || TSHDN_FLT_CNT > TSHDN_FLT_CNT_MAX ||

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Transition symbol	State transition	Transition condition
		OCP_FLT_CNT > OCP_FLT_CNT_MAX || WDG_FLT_CNT > WDG_FLT_CNT_MAX
N	FAIL_SAFE_LOCK to OFF	**Transition to force leaving the fail-safe locked state:** FAIL_SAFE_LOCK_DIS (NVM bit) || PKEY_LKP_EN_FSLS (PONKEY Long Key Press Fail-Safe-Lock-Skip bit / EN deasserted Fail-Safe-Lock-Skip)

5.1.2 State explanations

5.1.2.1 *NO_SUPPLY*

V_{IN} is below V_{INPOR_Fall} (see). No output state can be guaranteed in this state.

5.1.2.2 *INIT&LOAD*

The INIT&LOAD state is immediately reached when V_{IN} exceeds V_{INPOR_Rise}.

STPMIC2L releases internal POR circuitry, it initializes, all registers are reset, the NVM load is performed (see Section 5.2.2), and RSTn is asserted.

If the Auto_turn_on condition is true, PMIC makes a transition to the CHECK&LOAD state. Prior to leaving the INIT&LOAD state, the TURN_ON_SR is reset, and then the TURN_ON_SR[AUTO] bit is set.

If the Auto_turn_on condition is false, STPMIC2L evaluates the PONKEYn/En status. If the turn-on condition is not recognized, STPMIC2L makes the transition to the OFF state, otherwise it sets the proper bit in TURN_ON_SR and makes the transition to the CHECK&LOAD state (see Table 1).

5.1.2.3 *OFF*

The OFF state is entered from the INIT&LOAD state, the POWER_DOWN state, or the FAIL_SAFE_LOCK state.

In the OFF state, the PMIC is in the lowest power consumption state, and all regulators are turned OFF. The voltage references are OFF and RSTn is asserted by PMIC.

All fail-safe counters are reset (xxx_FLT_CNT). Fail-safe timers (FLT_TMR), reset-fault-counter-timers (RST_FLT_CNT_TMR), and watchdog timers are stopped.

The transition to the CHECK&LOAD state (see Table 1) is triggered by a turn-on condition (see Section 5.4.5: Turn-on conditions).

Prior to leaving the OFF state, the TURN_ON_SR is reset, then the related turn-on condition bit is set in the TURN_ON_SR register.

5.1.2.4 *CHECK&LOAD*

CHECK&LOAD is a transitional state from a user point of view. It prepares the PMIC to power-up. The PMIC enables internal reference voltages, thermal monitoring, and V_{IN} monitoring.

The NVM is reloaded into shadow registers. Some registers are initialized with default values from the NVM content.

RSTn is asserted by the PMIC.

After the CHECK&LOAD state, the PMIC always transitions to the POWER-UP state if power-up conditions are fulfilled (see Transition conditions) and the fault timer (FLT_TMR) ends. The fault timer waits before restarting the PMIC after a hard-fault (see Section 5.2.2).

5.1.2.5 *POWER_UP*

The PMIC starts sequential regulators following a sequence that is predefined in the NVM and a default voltage that is predefined in the NVM (see Section 5.2).

During the power-up sequence, RSTn is asserted by the PMIC. When the power-up sequence ends without a hard-fault, the PMIC releases an RSTn signal.

5.1.2.6 *POWER_ON*

When the PMIC transitions from Power_up to Power_on, it always goes into the Run state first.

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In the **POWER_ON** state, the PMIC can be set to deliver power at full performance and features. Each regulator can switch power states (MAIN_CR or ALT_CR) depending on the PWRCTRLx pin settings (see Section 5.4.11).

Note: When a turn-off condition or RSTn assertion from MPU occurs, the STPMIC2L moves to the P0WER_D0WN state. In case of a hard-fault turn-off condition, before the STPMIC2L leaves the P0WER_0N state:

- *The corresponding hard-fault counter is incremented (see Table 22:xxx_FLT_CNT ++).*
- *The FLT_TMR is loaded with the corresponding hard-fault duration and started (see Table 22).*

5.1.2.7 *POWER_DOWN*

The PMIC asserts RSTn, then sequentially turns off the regulators starting with the regulators not enabled in the power-up sequence (= rank0: enabled by software at runtime), then in reverse sequence order in the POWER_UP state (see Section 5.5.2: Non-volatile memory (NVM)).

When the POWER_DOWN sequence ends, before transition to the next state, the watchdog is disabled (WDG_EN = 0) and status registers are updated according to the turn-off condition source:

- TURN_ON_SR and TURN_OFF_SR and RESTART_SR and OCP_SR1 and OCP_SR2 are reset (cleared)
- If RSTn is asserted by AP (PMIC transition to K in Table 1):
  - RESTART_SR[R_RST] bit is set
- Else If SWOFF && RREQ_EN && PONKEYn set in NVM_MAIN_CTRL_SHR3 (PMIC transition to K inTable 1):
  - RESTART_SR[R_SWOFF] bit is set
- Else If SWOFF && EN asserted && EN set in NVM_MAIN_CTRL_SHR3 (PMIC transition to K in Table 1):
  - RESTART_SR[R_SWOFF] bit is set
- Else If EN asserted following a pulse deassertion on EN generating a turn-OFF condition (PMIC transition to K in Table 1):
  - RESTART_SR[R_EN] bit is set
- Else If SWOFF && !RREQ_EN (PMIC transition to L inTable 1):
  - TURN_OFF_SR[SWOFF] is set
- Else If EN deasserted (PMIC transition to L in Table 1):
  - TURN_OFF_SR[EN] is set
- Else (it is a hard-fault turn-off condition, then depending on the hard-fault source):
  - If hard-fault is OCP:
    - OCP_SR1 or OCP_SR2 is updated with the OCP fault source
  - If PMIC transitions to M:
    - TURN_OFF_SR is updated with fault source
  - If PMIC transitions to K:
    - RESTART_SR is updated with fault source

Note: If another turn-off condition is triggered during the POWER DOWN sequence, it is ignored. So, only the original power-down trigger source is registered.

When a hard fault occurs first and EN feature is active, the choice between K and L transitions depends on EN status at the end of the POWER_DOWN sequence; in this scenario, TURN_OFF_SR/RESTART_SR are updated with both hard-fault source and EN bit, to keep trace of the original POWER_DOWN root cause.

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5.1.2.8 *FAIL_SAFE_LOCK*

The FAIL_SAFE_LOCK state is entered from the POWER_DOWN state with M transition (a hard-fault counter xxx_FLT_CNT that exceeds the max number of PMIC restart occurrences xxx_FLT_CNT_MAX).

In the FAIL_SAFE_LOCK state, the PMIC is in the lowest power consumption state: all regulators are turned OFF, voltage references are OFF, and RSTn is asserted by the PMIC.

The PMIC is locked in that state until it POR: a turn-on condition does not power-up the PMIC.

Nevertheless, the PMIC is allowed to skip the FAIL_SAFE_LOCK state in specific conditions of N transition (see Table 1).

5.2 POWER_UP / POWER_DOWN sequence

The PMIC starts and stops regulators following sequential rank procedures called POWER_UP and POWER_DOWN, respectively.

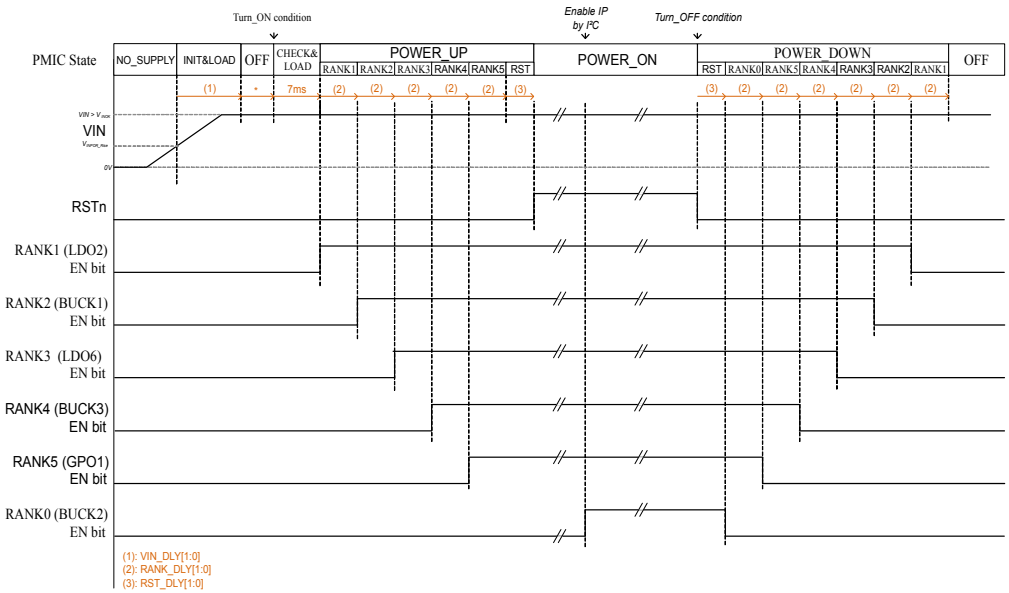
During POWER_UP each regulator is started at one of the 6-rank phases programmed in the NVM. Each rank phase is separated by a delay (1.5 ms, 3 ms, 4.5 ms, and 6 ms) programmed in the NVM.

An additional delay can be programmed in the NVM to release the RSTn signal later than last rank phase. This delay is also applied after the Turn_OFF condition, in between RSTn signal assertion and when the first regulator is powered off (RANK0).

The default rank sequence for each regulator, default output voltage of each regulator, default rank duration, and additional RSTn default delays are predefined in the NVM. Those values can be adapted by reprogramming the PMIC NVM with expected values.

An additional VIN_DLY [1:0] delay (0, 10 ms, 50 ms, 100ms) can be programmed in NVM to prevent the PMIC from power-up; to wait for VIN to stabilize.

Figure 9. PMIC POWER_UP and POWER_DOWN sequence example



(*) device will remain in OFF state until a turn on condition is triggered.

Note: RANK0 means that the regulator is not turned ON.

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5.2.1 NO_SUPPLY and INIT&LOAD:

The PMIC is initially in NO_SUPPLY state with $V_{IN} < V_{INPOR\_Fall}$. A power source is inserted making V_{IN} rise. Once $V_{IN} > V_{INPOR\_Rise}$, the PMIC goes in INIT&LOAD state. The PMIC reads NVM and performs internal initialization. Then, the PMIC launches the VIN_DLY[1:0] delay. Once the VIN_DLY elapsed, the PMIC can transition to OFF state (or directly to CHECK&LOAD state if AUTO_TURN_ON bit is set in NVM).

The VIN_DLY is convenient when the PMIC starts immediately after V_{IN} rise; especially when AUTO_TURN_ON bit is set in NVM.

5.2.2 OFF and CHECK&LOAD

The PMIC is initially in the OFF state. The RSTn pin is asserted by the PMIC. Once a Turn_ON condition occurs, the PMIC goes into the CHECK&LOAD state. As the turn-ON condition is valid (for example: $V_{IN} > V_{INOK}$), the PMIC goes into the POWER_UP state.

5.2.3 POWER_UP

The PMIC starts sequential regulators following a sequence that is predefined in the NVM and a default voltage that is predefined in the NVM (see Figure 9).

During the power-up sequence, RSTn is asserted by the PMIC. When the power-up sequence ends without a hard-fault, the PMIC releases an RSTn signal.

5.2.4 POWER_ON

In the POWER_ON state, all regulators are managed by the application processors software (I²C control) or by the PWRCTRL pin (see Section 5.4.11). In the example of Figure 9, LDO3 is enabled by the AP's software at runtime.

5.2.5 POWER_DOWN

The PMIC asserts RSTn, then sequentially turns off the regulators starting with the regulators not enabled in the power-up sequence (= rank0: enabled by software at runtime), then in reverse sequence order in the POWER_UP state (see).

When the POWER_DOWN sequence ends, before transition to the next state, the watchdog is disabled (WDG_EN = 0) and status registers are updated according to the turn-off condition source:

- TURN_ON_SR and TURN_OFF_SR and RESTART_SR and OCP_SR1 and OCP_SR2 are reset (cleared)
- If RSTn is asserted by AP (PMIC transition to K in Table 19):
  - RESTART_SR[R_RST] bit is set
- Else If SWOFF && RREQ_EN && PONKEYn set in NVM_MAIN_CTRL_SHR3 (PMIC transition to K in Table 19):
  - RESTART_SR[R_SWOFF] bit is set
- Else If SWOFF && EN asserted && EN set in NVM_MAIN_CTRL_SHR3 (PMIC transition to K in Table 19):
  - RESTART_SR[R_SWOFF] bit is set
- Else If EN asserted following a pulse deassertion on EN generating a turn-OFF condition (PMIC transition to K in Table 19):
  - RESTART_SR[R_EN] bit is set
- Else If SWOFF && !RREQ_EN (PMIC transition to L in Table 19):
  - TURN_OFF_SR[SWOFF] is set
- Else If EN deasserted (PMIC transition to L in Table 19):
  - TURN_OFF_SR[EN] is set
- Else (it is a hard-fault turn-off condition, then depending on the hard-fault source):
  - If hard-fault is OCP:
    - OCP_SR1 or OCP_SR2 is updated with the OCP fault source
  - If PMIC transitions to M:
    - TURN_OFF_SR is updated with fault source
  - If PMIC transitions to K:
    - RESTART_SR is updated with fault source

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Note: If another turn-off condition is triggered during the POWER DOWN sequence, it is ignored. So, only the original power-down trigger source is registered.

When a hard fault occurs first and EN feature is active, the choice between K and L transitions depends on EN status at the end of the POWER_DOWN sequence; in this scenario, TURN_OFF_SR/RESTART_SR are updated with both hard fault source and EN bit, to keep trace of the original POWER_DOWN root cause.

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5.3 Digital pin description

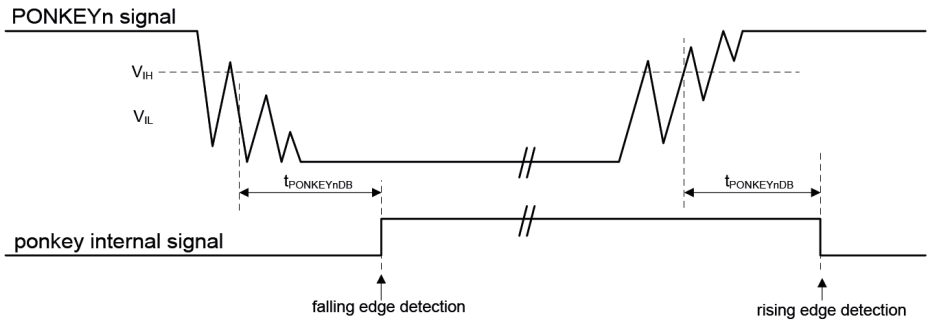
5.3.1 PONKEYn/EN

The PONKEYn/EN pin is a multifunction pin that can be configured (see PKEY_EN_CFG NVM pin) with two different functions: as PONKEYn, it is intended to be connected to a push-button at the application level. If the push-button is pressed by a user, the PONKEYn signal is grounded. If the push-button is released by the user, the PONKEYn signal is floating, but the internal PMIC R_{PU} ties PONKEYn to V_{IN}. When configured as Enable, it turns the PMIC on or off based on the programmed polarity.

Main characteristics as PONKEYn:

- Digital input
- Active low
- Programmable pull-up (RPU) internally connected to V_{IN}.
- Debounce filter on rising and falling edges (see Figure 10)
- Turn-ON condition on falling edge (after debounce) when PMIC is in the OFF state
- Turn-ON condition on low level from a PMIC POR (see Section 5.4.2)
- Interrupt on falling and rising edges (after debounce)
- Turn-OFF condition on PONKEYn long press (duration programmable)

Figure 10. PONKEYn debounce filter behavior



PONKEYn falling edge: the debounce filter timer is enabled once the PONKEYn voltage is lower than V_{IL}. If a bounce voltage higher than V_{IH} occurs, the debounce filter timer is canceled and so on.

PONKEYn rising edge: the debounce filter timer is enabled once the PONKEYn voltage is higher than V_{IH}. If a bounce voltage lower than V_{IL} occurs, the debounce filter timer is canceled and so on.

Main characteristics as EN:

- Digital input, level sensitive with V_{IL}/V_{IH} thresholds 1.8 V compatible
- Active high or low (programmable polarity)
- NVM or user-level programmable pull-up (RPU) internally connected to V_{IN} or pull-down (RPD)
- 30 µs rising and falling deglitch
- Turn-ON and Turn-OFF conditions when (respectively) asserted or deasserted based on programmed polarity
- When configured, the following functionalities are disabled: PONKEYn turn-ON event (implicit) and long press Turn-OFF event and fail-safe skip, AUTO_TURN_ON, RREQ_EN.

RPU and RPD settings are independent of PONKEYn/EN configuration.

5.3.2 RSTn

The RSTn is a bidirectional reset pin both for the PMIC and the application processor:

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- Digital input: active low input reset (when not asserted by the PMIC): the application processor can assert RSTn low to force the PMIC to power cycle.
- Open drain output: the PMIC can assert RSTn low to reset the application processor, typically during a power-ON or a power-OFF sequence and a power cycling reset sequence. Pull-up (R_{PU}) is internally connected to V_{IO}.

5.3.3 INTn

The PMIC asserts INTn low when a PMIC interrupt is pending (and not masked):

- Digital output (open drain)
- Active low
- Pull-up (RPU) internally connected to V_{IO}.

5.3.4 PWRCTRL1, PWRCTRL2, PWRCTRL3

Power control signals aim to control the regulator's behavior. Typically, power control signals are driven to ‘1’ or ‘0’ by the application processor to manage different power modes at application level.

PWRCTRLx pin characteristics:

- Digital input
- Level-sensitive
- Programmable polarity
- Rising and falling delay cells
- Inactive by default
- Programmable pull-up (RPU) internally connected to V_{IO} or pull-down (RPD), and RPU is active by default.
- No debounce

See section Section 5.4.11 for behavior description.

5.3.5 GPO1 to GPO5

General Purpose Output driven by PMIC via GPOx_MAIN_CR, GPOx_ALT_CR like other regulators and PWRTCTRL. A GPO can also be driven at power-up/power-down programmable in NVM like any regulator.

GPOx are mainly targeted to control external discrete regulators or an additional PMIC (driven by EN pin). GPO can also be used to control any external peripherals on an application.

GPOx pin characteristics:

- Digital output (push-pull on V_{IN})
- Programmable polarity (an external discrete regulator usually has active high Enable pin input but sometimes Enable pin is active low)
- The GPO are in high impedance when $0 < V_{IN} < V_{IN\_POR}$.
- The GPO are 0 (GND) when the STPMIC2L is in off state.

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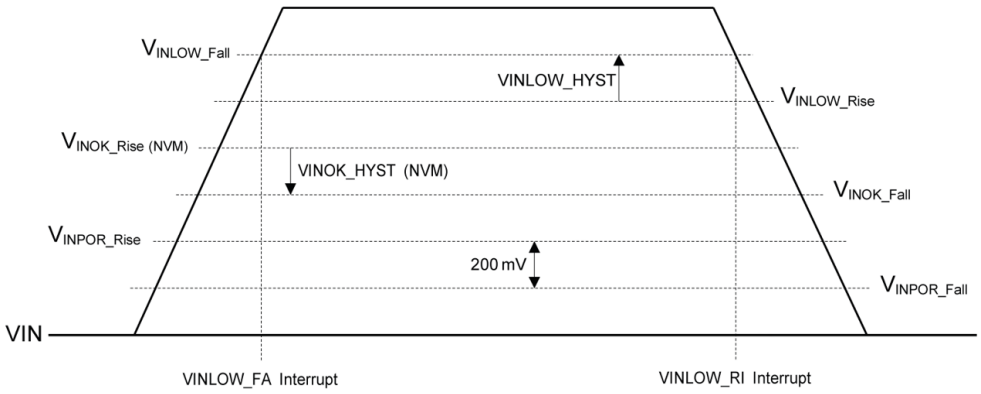
5.4 Feature descriptions

5.4.1 V_{IN} monitoring

The main input supply pin V_{IN} is monitored permanently by the PMIC state machine. There are different threshold triggers on V_{IN}. The lowest to the highest thresholds are: V_{INPOR}, V_{INOK}, and V_{INLOW} as presented in Figure 11

Figure 11. V_{IN} monitoring thresholds



5.4.2 V_{INPOR}

V_{INPOR} is the minimum voltage required to supply the PMIC internal circuitry. It is specified by two hardcoded thresholds with 200 mV hysteresis:

Below V_{INPOR_Fall}, the PMIC is considered as not supplied.

Above V_{INPOR_Rise}, the PMIC internal circuitry is functional.

Note: Once V_{IN} rises above V_{INPOR_Rise}, PMIC internal circuitry remains functional until V_{IN} falls below V_{INPOR_Fall}. Refer to Section 3.4.1 for threshold values.

5.4.3 V_{INOK}

V_{INOK} is the minimal voltage required to allow the PMIC to work in the POWER_ON state.

It is specified by V_{INOK_Rise} threshold and V_{INOK_HYST} hysteresis values that can be adjusted in the NVM, respectively by the V_{INOK_RISE} [1:0] and V_{INOK_HYST} [1:0] bits field.

If V_{IN} falls below V_{INOK_Fall} (V_{INOK_Fall}=V_{INOK_Rise}–V_{INOK_HYST}), then it is considered as a hard-fault turn-OFF condition and the PMIC immediately starts the POWER_DOWN sequence (see Section 5.2.5). Following this condition, the PMIC waits for the t_{VINOK_Fall} delay before it can restart, even if V_{IN} returns higher than V_{INOK_Rise} before the t_{VINOK_Fall} delay ends.

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5.4.4 V_{INLOW}

V_{INLOW} operates as a flag: V_{INLOW_Fall} and V_{INLOW_Rise} are configurable software thresholds that notify the AP (via an interrupt line) when the V_{IN} voltage crosses one of those two thresholds.

V_{INLOW} can be enabled and configured by programming the register V_{INLOW_CR}.

V_{INLOW_Rise} and V_{INLOW_Fall} thresholds generate, respectively, V_{INLOW_RI} and V_{INLOW_FA} interrupts, allowing the application processor to take relevant actions. They can be unmasked independently.

The V_{INLOW_RI} interrupt is asserted once V_{IN} goes below the V_{INLOW_Rise} threshold.

The V_{INLOW_FA} interrupt is asserted once V_{IN} goes higher than the V_{INLOW_Fall} threshold.

5.4.5 Turn-on conditions

A turn-on condition is required to power-up the PMIC and to reach the POWER_ON state. A turn-on condition is only valid from the OFF state, or alternatively from the NO_SUPPLY state (the PMIC has no V_{IN} initially).

The PMIC manages several turn-on conditions:

- PONKEYn pin assertion or EN pin assertion
- AUTO turn-on (AUTO_TURN_ON bit set in the NVM, only if pin EN is not configured)
- Fail-safe restart condition

Note: A fail-safe restart condition is not a real turn-on condition, but rather an allowed restart condition following a failure event triggering a turn-off event. See Section 5.4.7.

5.4.5.1 PONKEYn/En turn-on detection conditions

A turn-on condition can be triggered by external signal source from PONKEYn/EN pin:

1. If PONKEYn is set in the PKEY_EN_CFG bit (NVM):
   a. PONKEYn is tied low initially. The PMIC is in a NO_SUPPLY state. When the V_{IN} voltage rises and crosses the V_{INPOR_Rise} threshold, the PMIC goes into the INIT&LOAD state (transition A), and then it goes into the CHECK&LOAD state (transition C).
   b. PONKEYn is initially released. The PMIC is in the OFF state. When the PONKEYn is asserted, a turn-on condition occurs.

2. If EN is set in the PKEY_EN_CFG bit (NVM): 2. If EN is set in the PKEY_EN_CFG bit (NVM):

EN asserted: always a turn-on condition (except if PMIC is in FAIL_SAFE_LOCK state).

Table 20. Turn-on conditions from external trigger source summary

Source	Turn-on condition	Debounce
PONKEYn	PONKEYn signal low from the PMIC in a NO_SUPPLY state when V_{IN} rises and crosses V_{INPOR_Rise}	30 µs
PONKEYn	PONKEYn signal falling edge when the PMIC is in the OFF state	$t_{PONKEYnDB}$
EN	EN asserted (signal high or low depending of EN polarity set in NVM)	30 µs

5.4.6 AUTO turn-ON

AUTO turn-ON allows the PMIC to be turned ON automatically when V_{IN} rises from $V_{IN} < V_{INPOR\_Fall}$. An AUTO turn-ON event is triggered only from a NO_SUPPLY state transition:

1. V_{IN} rises from V_{INPOR_Fall} to V_{INPOR_Rise}
2. PMIC goes into INIT&LOAD state, then the AUTO_TURN_ON bit is enabled in the NVM
3. PMIC goes into the CHECK&LOAD state, waiting for $V_{IN}>V_{INOK}$
4. PMIC POWER_UP

The AUTO turn-ON is enabled in the NVM by default.

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5.4.7 Turn-off conditions

Turn-off conditions are triggered by events or stimulus leading the PMIC to perform a POWER_DOWN sequence.

Following the POWER_DOWN sequence, the PMIC can switch to the OFF state or to the FAIL_SAFE_LOCK state or restart automatically (power cycle), depending on the source that has triggered the turn-off condition.

There are six sources triggering a turn-off condition detailed in Table 21

Table 21. Turn-off condition trigger sources

Source	Type	Turn-off condition	Power cycle condition
EN (2)	Switch-off	EN deasserted (signal low or high depending of EN polarity set in NVM)	EN = asserted (2) (short deassertion pulse)
Software switch-off	switch-off	Writing 1 to SWOFF bit	RREQ_EN = 1 (1) EN = asserted (2)
V_{INOK_Fall}	hard-fault	V_{IN} falls below V_{INOK_Fall} threshold (with V_{IN} staying higher than $V_{IN\_POR\_Fall}$). See VIN monitoring	VIN_FLT_CNT <= VIN_FLT_CNT_MAX && EN = asserted (2)
PONKEYn long key press	hard-fault	PKEY_LKP_OFF bit set or NVM_PKEY_LKP_OFF bit set (NVM). Long key press duration can be set in PKEY_LKP_TMR [3:0] bit field or in NVM_PKEY_LKP_TMR[1:0] bit field (NVM) PONKEYn signal is asserted low for a duration > PKEY_LKP_TMR [3:0]	PKEY_FLT_CNT <= PKEY_FLT_CNT_MAX
Thermal shutdown	hard-fault	PMIC junction temperature exceeds T_{SHDN_Rise} threshold. See AUTO turn-ON	TSHDN_FLT_CNT <= TSHDN_FLT_CNT_MAX && EN = asserted (2)
Overcurrent protection	hard-fault	Overcurrent detected on a regulator (related regulator NVM_FS_OCP_xxx (1) bit set in NVM or FS_OCP_xxx (1) bit set by software).	OCP_FLT_CNT <= OCP_FLT_CNT_MAX && EN = asserted (2)
Watchdog	hard-fault	Watchdog feature active and timer expired. See Section 5.4.7.1	WDG_FLT_CNT <= WDG_FLT_CNT_MAX && EN = asserted (2)

1. *xxx: instance name of the regulator, eg: LDO2, BUCK1*
2. *EN set in PKEY_EN_CFG bit in NVM*

5.4.7.1 *Turn OFF condition triggered by software switch-off*

When the software sets the SWOFF bit, the PMIC starts a POWER_DOWN sequence immediately, then the PMIC goes into the OFF state. The TURN_OFF_SR is set accordingly.

PONKEYn set in PKEY_EN_CFG bit in NVM : If the software has set both the RREQ_EN and SWOFF bits, the PMIC restarts automatically after the POWER_DOWN sequence (transition K) and goes into the POWER_ON state. The RESTART_SR register is set accordingly.

EN set in PKEY_EN_CFG bit in NVM: If software set SWOFF bit while EN is asserted, the PMIC will restart automatically after the POWER_DOWN sequence (transition K) and goes in POWER_ON state.

The RESTART_SR register is set accordingly.

5.4.7.2 *Turn-OFF condition triggered by a hard fault*

Each hard-fault source has a hard-fault counter: see Table 22.

Each time a hard-fault event occurs, a turn-off condition is triggered, and it is managed by fail-safe management. See Section 5.4.8.

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5.4.8 Fail-safe management

Each hard-fault source has an independent fail-safe counter that is incremented each time a hard-fault turn-off condition occurs (see Table 22). If the counter value is below (or equal to) the max limit, then the PMIC restarts (= power cycling on fault condition). Alternatively, if the counter is higher than the max limit, then the PMIC goes into the FAIL_SAFE_LOCK state to avoid cyclic hard failures.

Sequence details:

When a turn-off condition is triggered by a hard-fault source (see Table 21):

- The corresponding hard-fault counter is incremented (see Table 22: xxx_FLT_CNT ++)
- The FLT_TMR is loaded with the corresponding hard-fault duration and starts (see Table 22)
- The PMIC switches to the POWER_DOWN sequence
- Once the POWER_DOWN sequence ends:
  - If all counters xxx_FLT_CNT <= xxx_FLT_CNT_MAX, then the PMIC goes into the CHECK&LOAD state, then PMIC waits for a FLT_TMR timer expiration before restarting (see Table 22), then it goes into POWER_UP, and then it goes in POWER_ON state. The corresponding bit in the RESTART_SR status register is set.
  - Else if one of the counters xxx_FLT_CNT > xxx_FLT_CNT_MAX, then PMIC goes into the FAIL_SAFE_LOCK state. The corresponding bit in the TURN_OFF_SR status register is set. Even when the FAIL_SAFE_LOCK is skipped, the PMIC waits for FLT_TMR expiration before restarting.

Note: If EN set in PKEY_EN_CFG bit in NVM, it is assumed that EN is kept asserted during the above sequence.

Table 22. Hard-fault fail-safe counters and waits before restarting timer

Source	Fail-safe counters	Max fault iteration (NVM shadow register)	Wait before restart timer duration FLT_TMR[x]
V_{INOK_Fall}	VIN_FLT_CNT [3:0]	VIN_FLT_CNT_MAX [3:0]	t_{VINOK_Fall}
PONKEYn long press	PKEY_FLT_CNT [3:0]	PKEY_FLT_CNT_MAX [3:0]	0
Thermal shutdown	TSHDN_FLT_CNT [3:0]	TSHDN_FLT_CNT_MAX [3:0]	t_{TSHDN_DLY}
Overcurrent protection (OCP)	OCP_FLT_CNT [3:0]	OCP_FLT_CNT_MAX [3:0]	t_{HICCUP_DLY}
Watchdog	WDG_FLT_CNT [3:0]	WDG_FLT_CNT_MAX [3:0]	0

Notes:

- 1- When a counter (xxx_FLT_CNT [3:0]) reaches 0xF, all following counter increments keep the counter value at 0xF (and do not restart at 0). This allows for infinite PMIC restart iterations to be set when xxx_FLT_CNT_MAX [3:0] is set to 0xF.
- 2- Setting 0 in xxx_FLT_CNT_MAX makes the PMIC go into the FAIL_SAFE_LOCK state after the first corresponding turn-off hard-fault condition (PMIC restarts 0 time).
- 3- Setting 0xF in xxx_FLT_CNT_MAX makes the PMIC always restart after any corresponding turn-off fault condition as highlighted above (PMIC restarts indefinitely).
- 4- Programming the NVM with t_{HICCUP_DLY} ='0' means no wait before restart.

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5.4.9 Hard-fault counters reset and auto-reset

To avoid reaching the FAIL_SAFE_LOCK state due to isolated turn-off hard-fault conditions, all counters can be reset automatically when no turn-off hard-fault condition occurs in RST_FTL_CNT_TMR timer duration.

(See Table 23 for timer duration NVM settings):

From the NO_SUPPLY state and until a first turn-off condition occurs, the RST_FTL_CNT_TMR timer is disabled.

Once and each time a turn-off hard-fault condition occurs, the RST_FTL_CNT_TMR timer is reset to the RST_FLT_CNT_TMR [1:0] value and restarted.

When the RST_FTL_CNT_TMR timer elapses:

- All counters (*_FLT_CNT) are reset
- The RST_FTL_CNT_TMR timer is stopped until a new turn-off hard-fault condition occurs

If PMIC reaches the FAIL_SAFE_LOCK state before the RST_FTL_CNT_TMR timer elapses, then RST_FTL_CNT_TMR timer is reset and stopped.

A RSTn condition has no effect on the RST_FTL_CNT_TMR timer.

In the OFF state, the RST_FTL_CNT_TMR timer is reset and stopped, and all counters (*_FLT_CNT) are reset.

Table 23. Reset fault counter timer settings

RST_FLT_CNT_TMR [1:0] (NVM shadow register)	Timer duration
00	disabled
01	1 min
10	6 min
11	60 min

5.4.10 FAIL_SAFE_LOCK state skipping

When the PMIC enters the FAIL_SAFE_LOCK state, it remains in this state until PMIC POR (V_{IN} < V_{INPOR_Fall}).

Alternatively, there are three programmable options to force the PMIC to switch from the FAIL_SAFE_LOCK state to the OFF state:

- Set the bit FAIL_SAFE_LOCK_DIS in the NVM. It disables the FAIL_SAFE_LOCK feature (when the PMIC enters into the FAIL_SAFE_LOCK state, it immediately transitions to the OFF state).
- A PKEY_EN_FAIL_SAFE_LOCK_SKIP condition.
  - A PKEY_EN_FAIL_SAFE_LOCK_SKIP condition can be reached only if the PKEY_LKP_EN_FSLS (1) bit is set prior to entering the FAIL_SAFE_LOCK state (or if the NVM_PKEY_LKP_EN_FSLS bit is set in NVM, which automatically sets the PKEY_LKP_EN_FSLS bit) and:
- A PONKEYn long key press event (if PONKEYn is set in the PKEY_EN_CFG bit (NVM))
- An EN pin deassertion (if EN is set in the PKEY_EN_CFG bit (NVM)).

PKEY_LKP_EN_FSLS: PONKEY Long Key Press Fail-Safe-Lock-Skip bit / EN deasserted Fail-Safe-Lock-Skip bit).

Note: When the PMIC performs the transition from the FAIL_SAFE_LOCK state to the OFF state, a turn-ON condition should occur to power-up the PMIC (the AUTO_TURN_ON bit has no effect on the FAIL_SAFE_LOCK state to the OFF state transition).

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5.4.11 Power control management (PWRCTRLx)

PWRCTRL1, PWRCTRL2 and PWRCTRL3 are digital inputs controlled by an application processor (see Section 5.3.4). They are dedicated to managing different application power modes or special regulator reset features.

PWRCTRL1, PWRCTRL2 and PWRCTRL3 can be independently muxed onto each regulator instance (BUCKx, LDOx or GPOx).

For example, BUCK1 may be controlled by PWRCTRL2, and BUCK2, BUCK3, and LDO5 can be controlled by PWRCTRL1, and so on.

A regulator instance and external command (GPO) can be controlled by a single PWRCTRL signal. For each regulator instance, a PWRCTRL input can be used either to:

- Switch between the xxx_MAIN_CR register or the xxx_ALT_CR register of a regulator (where xxx is the regulator instance)

– The regulator behaves according to the selected xxx_MAIN_CR or xxx_ALT_CR register

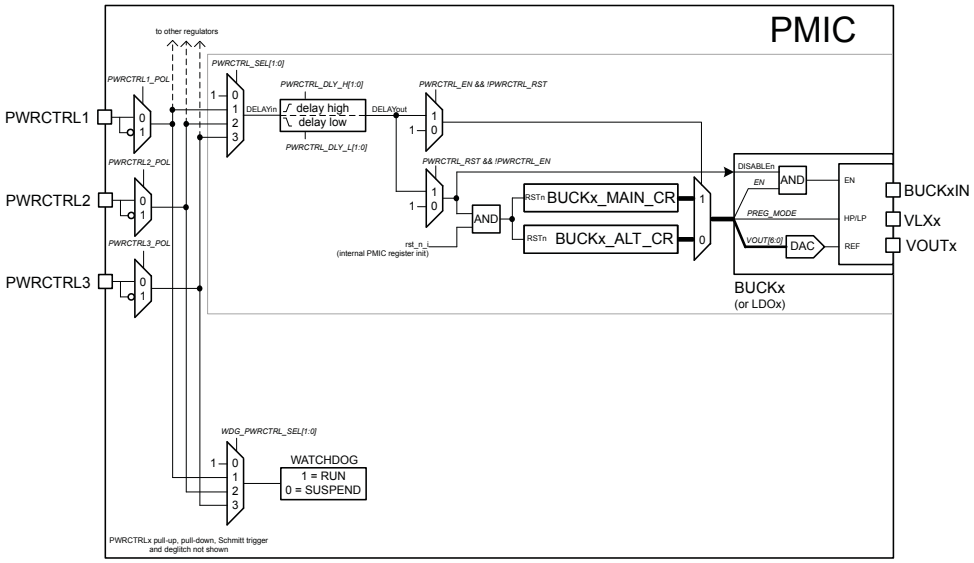
- Reset a regulator instance to its default value (from the NVM)

PWRCTRL1, PWRCTRL2 or PWRCTRL3 can be used to suspend the watchdog, typically when the AP is in low-power mode.

Figure 12 provides the logic circuitry principle showing:

- How a buck converter is controlled by a PWRCTRLx

Figure 12. PWRCTRLx logic circuitry principle



PWRCTRL1_POL, PWRCTRL2_POL and PWRCTRL3_POL bits set the polarity of PWRCTRL1, PWRCTRL2 and PWRCTRL3, respectively. Those settings are applicable for all regulators and external command (GPO) (not linked to a single regulator).

PWRCTRLx_POL: polarity of PWRCTRLx signal (with x = 1, 2, 3): 0: active low; 1: active high. See Table 24.

Table 24. PWRCTRLx polarity truth table

PWRCTRLx input level	PWRCTRLx_POL	PWRCTRLx logic level
0	0	Active
1	0	Inactive
0	1	Inactive
1	1	Active

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Note: x is the instance number of the PWRCTRL pin.

WDG_PWRCTRL_SEL [1:0]: Watchdog control source selection. When PWRCTRLx is active, the watchdog timer is suspended. When PWRCTRLx is inactive, the watchdog timer is running (if watchdog is enabled) (see Section 5.4.7.2).

Note: There is one instance of the following registers per regulator instance:

PWRCTRL_SEL [1:0]: BUCKx control/reset source selection.

PWRCTRL_DLY_H [1:0]: BUCKx control/reset source shift delay from low to high level (typically to perform the power-ON sequence between different regulators; driven by a PWRCTRL signal). 0 = no delay; 1 = 1.5 ms delay; 2 = 3 ms delay; and 3 = 6 ms delay.

PWRCTRL_DLY_L [1:0]: BUCKx control/reset source shift delay from high to low level (typically to emulate the power-OFF sequence between different regulators; driven by a PWRCTRL signal). 0 = no delay; 1 = 1.5 ms delay; 2 = 3 ms delay; and 3 = 6 ms delay.

PWRCTRL_EN: BUCKx control source enable. 0: disable, 1: enable. When enabled, BUCKx is controlled by a PWRCTRL signal:

- If PWRCTRL is inactive, the BUCKx_MAIN_CR register is used to control BUCKx
- If PWRCTRL is active, the BUCKx_ALT_CR register is used to control BUCKx

PWRCTRL_RST: BUCKx independent reset source enable. 0: disable, 1: enable. When enabled, BUCKx is reset by a PWRCTRL signal. See Section 5.4.13 for details:

1. If PWRCTRL is active
2. BUCKx is disabled (forced by the DISABLEn signal in Figure 15)
3. The BUCKx_MAIN_CR and BUCKx_ALT_CR registers are reset to default value (the NVM default value is reloaded in both registers).
4. If PWRCTRL is inactive, the BUCKx_MAIN_CR register is used to control BUCKx.

Notes:

- If both PWRCTRL_EN and PWRCTRL_RST are set by mistake, both the control source and independent reset features are disabled (no effect).
- The above bitfield descriptions are also applicable for LDOs and GPOs replacing BUCKx with LDOx and GPOx repectively.

Table 25. Regulator control truth table

PWRCTRLx logic level	PWRCTRL_RST	PWRCTRL_EN	Regulator control register
active or inactive	0	0	xxx_MAIN_CR
active	0	1	xxx_ALT_CR
inactive	0	1	xxx_MAIN_CR
active	1	0	xxx regulator disabled (OFF) xxx_MAIN_CR & xxx_ALT_CR registers are reset to default value
inactive	1	0	xxx_MAIN_CR
active or inactive	1	1	xxx_MAIN_CR

Note: x is the instance number of the PWRCTRL pin; xxx is the instance name of a regulator.

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5.4.12 PWRCTRL delays high and delay low behaviors

PWRCTRL delay blocks are independent for each regulator. A delay block allows a PWRCTRLx signal to shift by preprogrammed delays. Each delay block is composed of two parts (a delay high and a delay low). The first operates at a high input level, and the second operates at a low input level.

Delay blocks are typically used to emulate power sequences between regulators when entering or leaving a low-power mode.

High level delay behavior:

When the input signal goes from low to high level, the “high-level delay timer” (PWRCTRL_DLY_H [1:0]) is started. Once the timer expires, the output goes high.

If the input signal changes from high to low before the “high-level delay timer” expires, the “high-level delay timer” is stopped and reset, and the output keeps the previous value.

Low level delay behavior:

Same behavior as for the high-level delay but on low-level input.

When the input signal goes from high to low level, the “low-level delay timer” (PWRCTRL_DLY_L [1:0]) is started. Once the timer expires, the output goes low.

If the input signal changes from low to high before the “low-level delay timer” expires, the “low-level delay timer” is stopped and reset, and the output keeps the previous value.

Note: The "high-level delay timer" and "low-level delay timer" are both driven from a level (and not from an edge) to ensure that the output is always copying the input after any delay expires.

Figure 13 illustrates this example, using the PWRCTRL2 to control the BUCK1 and the BUCK2:

Settings for the Figure 13 example:

// BUCK1 settings

BUCK1_PWRCTRL_CR[PWRCTRL_SEL[1:0]] = 2; // PWRCTRL2 as BUCK1 control source

BUCK1_PWRCTRL_CR[PWRCTRL_DLY_H[1:0]] = 0; // no delay on PWRCTRL2 going from low to high for BUCK1

BUCK1_PWRCTRL_CR[PWRCTRL_DLY_L[1:0]] = 2; // 3 ms delay on PWRCTRL2 going from high to low for BUCK1

BUCK1_PWRCTRL_CR[PWRCTRL_EN] = 1; // enable the PWRCTRL input feature for BUCK1

// BUCK2 settings

BUCK2_PWRCTRL_CR[PWRCTRL_SEL[1:0]] = 2; // PWRCTRL2 as BUCK2 control source

BUCK2_PWRCTRL_CR[PWRCTRL_DLY_H[1:0]] = 2; // 3 ms delay on PWRCTRL2 going from low to high for BUCK2

BUCK2_PWRCTRL_CR[PWRCTRL_DLY_L[1:0]] = 0; // no delay on PWRCTRL2 going from high to low for BUCK2

BUCK2_PWRCTRL_CR[PWRCTRL_EN] = 1; // enable the PWRCTRL input feature for BUCK2.

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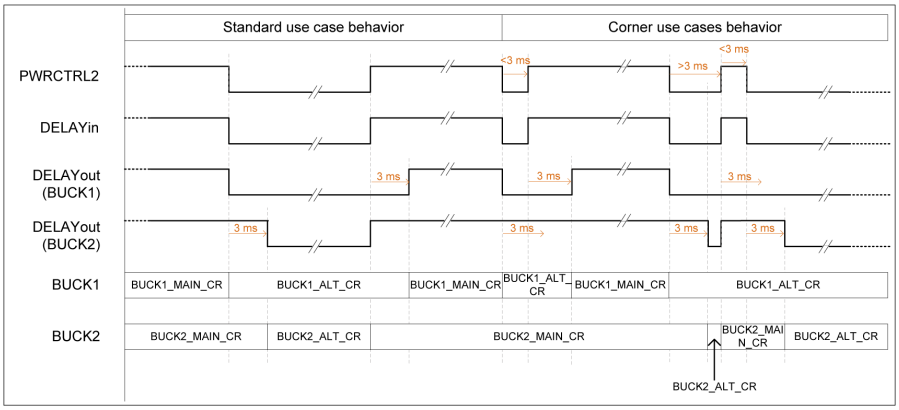
Figure 13. **Delay rising and delay falling behaviors example**



5.4.13 Regulator independent reset detailed behaviors (PWRCTRL_RST)

The independent reset feature is controlled by a PWRCTRLx input pin (PWRCTRL_SRC[1:0]) and it is enabled by setting the PWRCTRL_RST bit. This feature allows a regulator to reset to its default NVM value from an AP hardware signal “on the fly” (which cannot be done by I²C access).

When the PWRCTRLx input pin is active, regulator xxx is forced into OFF mode. xxx_MAIN_CR and xxx_ALT_CR registers are both reset to default value (NVM default value is reloaded in both registers from the related NVM shadow register).

When the PWRCTRLx input pin is inactive, regulator xxx is controlled by xxx_MAIN_CR register content.

Figure 14 provides an example to illustrate (see Section 5.4.13 for using the PWRCTRL2 to control the LDO2 independent reset).

Assumptions and settings for the Figure 14 example:

LDO2 reset value (from the NVM):

- LDO2_MAIN_CR[VOUT] = 2.9 V
- LDO2_MAIN_CR[EN] = 1

Software settings:

PWRCTRL2_POL = 0; // PWRCTRL2 active low

// LDO2 settings

LDO2_PWRCTRL_CR[PWRCTRL_SEL [1:0]] = 3; // PWRCTRL2 as LDO2 control source

LDO2_PWRCTRL_CR[PWRCTRL_DLY_H [1:0]] = 0; // no delay on PWRCTRL2 going high for LDO2

LDO2_PWRCTRL_CR[PWRCTRL_DLY_L [1:0]] = 0; // no delay on PWRCTRL2 going low for LDO2

LDO2_PWRCTRL_CR[PWRCTRL_RST] = 1; // enable the PWRCTRL2 input to control LDO2 independent reset

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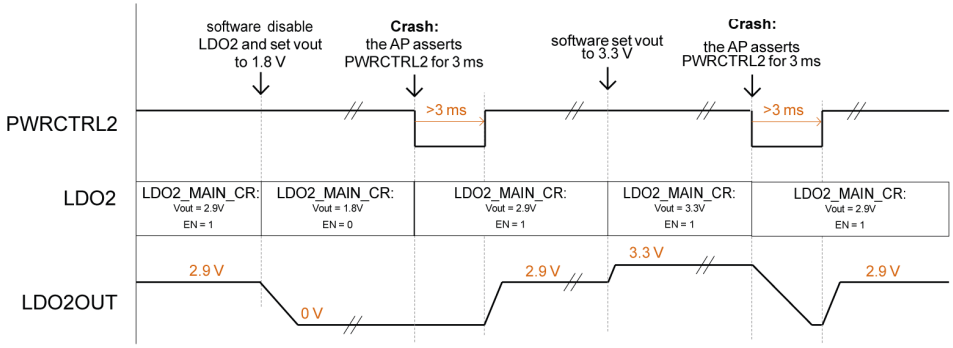
Figure 14. **Regulator independent reset behaviors example**



5.4.14 Reset management (RSTn) and mask_reset software option

RSTn is a bidirectional reset pin both for the PMIC and the application processor. It has a digital input/open drain output topology with an internal pull-up resistor (RPU).

- When the PMIC asserts RSTn, it drives the RSTn signal low (open drain internal transistor). The application processor is forced into a reset state.
- When the PMIC does not assert RSTn, the RSTn pin is in high impedance and the RSTn signal goes high (due to the pull-up resistor) if the RSTn signal is not asserted low externally (for example by a reset push-button or from an application processor asserting the reset signal low). In that case, the PMIC RSTn pin becomes a digital input and it monitors the RSTn signal.

In the POWER_ON state, the RSTn pin can be driven by the application processor or a reset push-button.

When the application processor asserts RSTn low for longer than the t_{RSTnAS} duration, it immediately triggers a reset sequence of the PMIC by performing a non-interruptible power cycle:

1. The PMIC asserts RSTn low (forcing the AP to keep it in reset, and in the case that the AP releases the reset before the end of the sequence)
2. POWER_DOWN sequence
3. CHECK&LOAD
4. POWER_UP sequence
5. PMIC deasserts RSTn and monitors RSTn
6. PMIC waits for the RSTn signal to go high before entering POWER_ON (to prevent an infinite loop of reset sequence)

The PMIC can detect a negative pulse on RSTn shorter than the t_{RSTnAS} duration. The PMIC must detect a negative pulse longer or equal to the t_{RSTnAS} duration.

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5.4.15 The mask_reset software option

From step 2 to step 4 (in the above sequence), LDOs, GPOs and buck regulators follow a POWER_DOWN sequence followed by a POWER_UP sequence as defined in Section 5.2; except for regulators having the **mask_reset** option bit set.

The **mask_reset** option can be defined for each regulator by setting the corresponding MRST bit in corresponding BUCKS_MRST_CR or LDOS_MRST_CR or GPOS_MRST_CR registers.

When the **mask_reset** option is set to a regulator, the MAIN and ALTERNATE related registers are not reset and content is maintained during and after the reset power cycle. Nevertheless, the PWRCTRLx settings are reset for all regulators, including those having the **mask_reset** option set:

- POWER_DOWN is not performed.
- MAIN and ALTERNATE register values are not reset, and their contents are maintained with the current value.
- PWRCTRLx register settings are reset (xxx_PWRCTRL_CR).

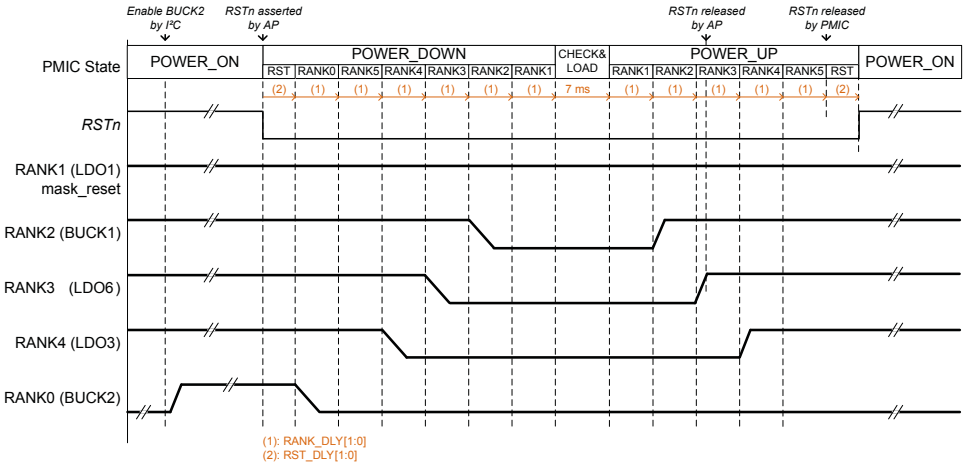
The PMIC always ends the power cycle in the POWER_ON state, regardless of the PWRCTRLx value, as all PWRCTRLx settings have been reset during the power cycle.

If RSTn is asserted in MAIN mode, regulators with the **mask_reset** option set are not impacted at all by the reset sequence, keeping V_{OUT}, EN, and PREG_MODE unchanged.

In case RSTn is asserted in the ALTERNATE mode, V_{OUT}, EN, and PREG_MODE switch to the content of the [regulator]_MAIN_CR register values when the POWER_DOWN sequence ends before the POWER_UP sequence starts.

Figure 15 illustrates a reset power-cycle of the PMIC.

Figure 15. Reset power-cycle sequence example.



For RANK_DLY and RST_DLY see Table 84.

Settings related to the example in Figure 15:

LDO1 with mask_reset option set (LDOS_MRST_CR[LDO2_MRST] = 1) is not impacted by the reset power-cycle.

BUCK1 and BUCK3 are powered down and up at their respective ranks defined in the NVM. BUCK2 is enabled by I²C. So, it is powered down first and not restarted (as not defined in the NVM to start). The mask_reset is valid once. It is cleared in the CHECK&LOAD state. So, it is cleared following a turn-OFF condition, a VINPOR, and a RSTn assertion.

When RSTn is released by the application processor, the PMIC keeps RSTn asserted (the RSTn signal stays low), meaning that the application processor is kept in reset until the PMIC releases the RSTn signal.

5.4.16 Thermal protection

The PMIC implements a thermal protection to prevent overheating damage. PMIC junction temperature is permanently monitored by an embedded thermal sensor.

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The first level of thermal protection consists of an alarm sent by an interrupt to the application processor:

- When Tj rises above the TWRN_Risethreshold, the PMIC generates an THW_RI interrupt.
- When Tj falls below the TWRN_Fallthreshold, the PMIC generates an THW_FA interrupt.

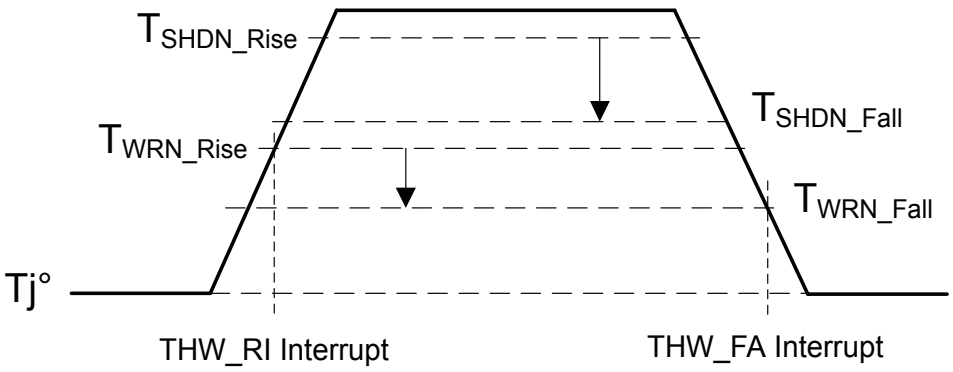
The application processor is able to decrease the application activity load to decrease the application power consumption. Alternatively, a second level of thermal protection may occur.

The second level of thermal protection consists of triggering a turn-OFF hard-fault condition:

- When Tj rises above the TSHDN_Risethreshold, the PMIC generates a turn-OFF hard-fault condition, and the thermal fail-safe counter is incremented (TSHDN_FLT_CNT ++):
  - If the thermal fail-safe counter reaches the maximum number of power cycles defined in the NVM (TSHDN_FLT_CNT > TSHDN_FLT_CNT_MAX), then the PMIC goes into the FAIL_SAFE_LOCK state.
  - Alternatively, whenTj falls below the TSHDN_Fall threshold and a tTSHDN_DLY delay ends, the PMIC restarts.

See Section 5.4.8 for details about fail-safe counter management.

Figure 16. Thermal protection thresholds



5.4.17 Overcurrent (OCP) and Hiccup mode

All regulators implement protection against overcurrent (OC) on their output.

Note: Short-circuits (SC) are managed by the overcurrent protection.

For each regulator, the PMIC embeds 2 levels of protection against overcurrent and short-circuits:

- Level 0 (default): independent regulator OCP Hiccup mode management
- Level 1: PMIC OCP fail-safe management (see Section 5.4.8: Fail-safe management)

The default level of protection is defined in the NVM (NVM_FS_OCP_SHR1/2) for each regulator, and can be changed at runtime by software (FS_OCP_CR1/2),

5.4.17.1 Level 0: independent regulator OCP Hiccup mode management

Each PMIC regulator operates independently in Hiccup mode:

- When a short-circuit or an overcurrent occurs, the output current is limited to ILDOLIM (for LDO) and IBKLIM (for buck).
- If the SC or OC lasts more than t_{OCPDB_LDO} or t_{OCPDB_BUCK} (respectively for LDO or buck):
  - The regulator turns OFF for the t_{HICCUP_DLY} duration
  - An interrupt is generated (if the interrupt is unmasked by software)
- Once the t_{HICCUP_DLY} timer elapses, the regulator turns ON
  - If the SC or OC is removed, the LDO operates normally
  - If the SC or OC stays present, the regulator goes into step 1, repeating the cycle until the overload disappears (hiccup)

Notes:

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- 1) When the t_{HICCUP_DLY} timer duration is set to 0, the regulator is turned-OFF (interrupt-generated) and it does not restart (step 3 is skipped).
- 2) The t_{HICCUP_DLY} timer duration can be adjusted in the NVM by setting the HICCUP_DLY[1:0] bit field in the NVM_BUCKS_IOUT_SHR2 shadow register then programming the NVM.
- 3) The t_{HICCUP_DLY} timer is reset if a POWER_DOWN occurs at the same time. In this way, the IP can restart with its assigned RANK at the next POWER_UP. This happens even if the mask reset is set and/or t_{HICCUP_DLY} is set to '0'.

5.4.17.2 *Level 1: PMIC OCP fail-safe management*

Each PMIC regulator can be set independently to trigger a hard-fault condition when an overcurrent or a short circuit occurs:

- When a short-circuit or an overcurrent occurs, the output current is limited to I_{LDOLIM} (for LDO) and I_{BKLIM} (for buck).
- If the SC or OC lasts longer than t_{OCPDB_LDO} or t_{OCPDB_BUCK} (for LDO or buck respectively), the PMIC generates a turn-OFF hard-fault condition. OCP_SR1 or OCP_SR2 is updated with the OCP fault source, and the OCP fail-safe counter (1) is incremented (OCP_FLT_CNT ++):
  - If the OCP fail-safe counter reaches the maximum number of power cycles defined in the NVM (OCP_FLT_CNT > OCP_FLT_CNT_MAX), the PMIC goes in FAIL_SAFE_LOCK state.
  - Alternatively, when the t_{HICCUP_DLY} delay ends, the PMIC restarts.

There is a single OCP fail-safe counter (OCP_FLT_CNT) for all regulators. It is incremented each time a regulator triggers a hard-fault regardless of the regulator instance.

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5.4.18 Watchdog management

The PMIC has an internal watchdog timer. A watchdog timer expiration generates a turn-off hard-fault condition (see Section 5.4.7) followed either by a PMIC restart (power cycling) or by the PMIC going into the FAIL_SAFE_LOCK state.

The watchdog can be enabled/disabled by software or at power-up (NVM settings) respectively:

- Software: set/reset WDG_EN bit at runtime
- NVM: set/reset NVM_WDG_EN bit, then program the NVM

The watchdog timer duration can be set in a range from 1 s to 256 s (1 s steps) by setting the WDG_TMR_SET[7:0] bitfield. The default watchdog timer duration can be set in the NVM by setting NVM_WDG_TMR_SET[1:0], then programming the NVM.

Note: Each time the NVM is reloaded (typically in the CHECK&LOAD state), the NVM_WDG_EN bit is copied into the WDG_EN bit and the NVM_WDG_TMR_SET [1:0] bitfield-related duration is set in the WDG_TMR_SET [7:0] bitfield. In the POWER_ON state, the software can override the default watchdog values (NVM) by setting the WDG_EN bit and/or the WDG_TMR_SET [7:0] bitfield.

As soon as the watchdog is enabled, the software should periodically set the WDG_RST bit (self-cleared) to reload the timer down counter WDG_TMR_CNT [7:0] with the value defined in the WDG_TMR_SET [7:0] bitfield.

The software can read the watchdog timer down counter (WDG_TMR_CNT [7:0]) to check the remaining duration before expiration.

A turn-OFF hard-fault condition occurs if the watchdog timer expires. The turn-off condition is followed by a POWER_DOWN sequence either by a PMIC restart (POWER_UP then POWER_ON) or by the PMIC going into the FAIL_SAFE_LOCK state. (See Section 5.4.8 for details about the behavior following a turn-off hard-fault event).

Enabling the watchdog (from WDG_EN = 0 to 1) to reload the timer down counter (WDG_TMR_CNT [7:0]) with the value defined in the WDG_TMR_SET [7:0] bitfield.

When enabled, the watchdog timer remains active in the POWER_ON state.

The watchdog timer can be disabled at runtime by setting WDG_EN = 0. Alternatively, the watchdog timer is automatically disabled when PMIC goes into the OFF state or the FAIL_SAFE_LOCK state (regardless of turn-OFF condition source).

When enabled (WDG_EN = 1), the watchdog timer can be suspended automatically from one PWRCTRLx signal. The WDG_PWRCTRL_SEL [1:0] bitfield allows for selection of the PWRCTRLx source to suspend the watchdog. It is suitable to automatically suspend/freeze the watchdog when the application is in low-power mode:

- When PWRCTRLx is inactive (the application is running), the watchdog timer down counter is running. The software should set the WDG_RST bit periodically to reload the timer down counter.
- When PWRCTRLx is active (the application is in low-power mode), the watchdog timer down counter is suspended (frozen). When PWRCTRLx becomes inactive (the application leaves the low-power mode), the watchdog down counter restarts from the current WDG_TMR_CNT [7:0] value (counter WDG_TMR_CNT [7:0] is not reloaded from WDG_TMR_SET [7:0] value).

5.5 Programming

5.5.1 I²C interface

The I²C interface works in slave mode. It supports both standard and fast modes with a data rate up to 400 Kb/s. It also supports fast mode plus (FM+) with a data rate up to 1 Mb/s.

Fm and Fm+ standards are supported with total spike pulse time (t_{SP}) up to 25 ns max while the V_{OL} = 0.4 V is guaranteed with I_{OL} up to 4 mA.

The STPMIC2L I²C interface is intended to be addressed exclusively via a dedicated microprocessor I²C BUS.

5.5.1.1 Device ID

There is a device ID system to address the STPMIC2L.

The address is stored in the NVM_I²C_ADDR_SHR[6:0] shadow register bitfield. The hard-coded I²C default address defined in the NVM is 0x33.

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Table 26. **Device ID format**

b7	b6	b5	b4	b3	b2	b1	b0
AddID6	AddID5	AddID4	AddID3	AddID2	AddID1	AddID0	R/W

5.5.1.2 *Read/write operation.*

Each transaction is composed of a start condition followed by a packet number (8-bit long) representing either a device ID plus R/W command, register address, or register data coming to/from the slave.

An acknowledgment is needed after each packet (see Table 30). This acknowledgment is given by the receiver of the packet. Transaction examples are given in Table 31 and Table 32. Multi-read and multi-write operations are supported.

Table 27. **Register address format**

b7	b6	b5	b4	b3	b2	b1	b0
RegAdd7	RegAdd6	RegAdd5	RegAdd4	RegAdd3	RegAdd2	RegAdd1	RegAdd0

Table 28. **Register data format**

b7	b6	b5	b4	b3	b2	b1	b0
DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

Figure 17. **I²C read operation**

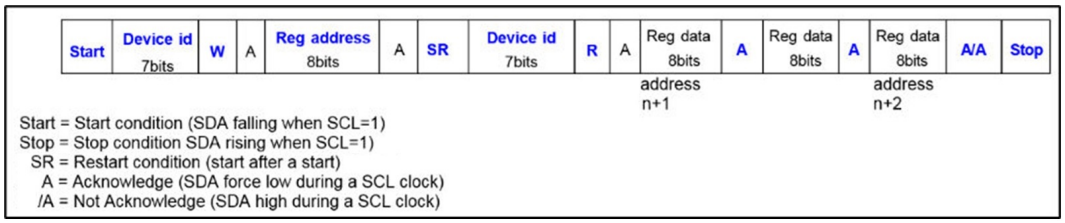
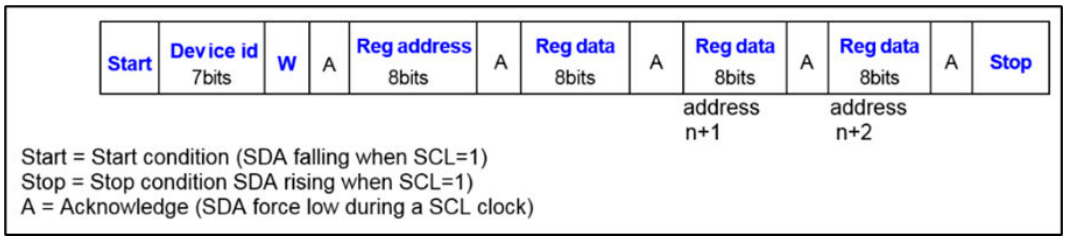


Figure 18. **I²C write operation**



5.5.2 Non-volatile memory (NVM)

The PMIC's built-in non-volatile memory provides high flexibility to support a wide range of applications.

Its write management through I²C allows for the customization of the PMIC directly in the final applications during product development and mass production.

The NVM read operation is performed automatically in the INIT&LOAD state and in the CHECK&LOAD state to set control registers with default values and configure the POWER_UP and POWER_DOWN sequences.

The NVM write operation can be performed several times (NVMEND cycles max) during application development debugging procedures. Once the final settings have been defined, these can be written in the NVM content of each part mounted on the customer application, which is written in the production line in a controlled environment.

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In addition, the PMIC supports the NVM CRC check (or checksum) to guarantee its content integrity. The CRC is computed by the PMIC during an NVM write operation. After the NVM write operation, the user reads back the NVM content to check that the content is OK (and implicitly that the computed CRC is valid). Then, each time the PMIC reads the NVM (in the INIT&LOAD and in the CHECK&LOAD states) if the CRC is not OK, the PMIC does not start up.

5.5.2.1 *NVM read operation*

The NVM read operation is fully managed by the PMIC.

For each read operation, the PMIC automatically loads the NVM content into NVM shadow registers. It means that the shadow register content is a copy of the NVM content.

When the PMIC power supply is connected (VIN > VINPOR_Rise), the PMIC state machine goes into the INIT&LOAD state (see Section 5.1). In this state, an NVM read operation is performed to check if the PMIC can start up automatically, depending on the AUTO_TURN_ON NVM bit value.

If the AUTO_TURN_ON bit is not set, the PMIC goes into the OFF state, or the PMIC goes into the CHECK&LOAD state and continues to POWER_UP automatically.

Before each POWER_UP sequence, the NVM read operation is performed in the CHECK&LOAD state. The NVM content is loaded into shadow registers and NVM content integrity is checked with CRC. Additionally, the PMIC initializes BUCK and LDO control registers with values predefined in the NVM and it configures the POWER_UP and POWER_DOWN sequence of regulators.

5.5.2.2 *NVM write operation (PMIC customization)*

The NVM write operation can be performed through the I²C interface for customization purposes (see max cycles in NVMEND).

The writing procedure can be performed in two ways:

- Customizing a pre-programmed device directly from the application host processor via the I²C interface:

NVM write operation generic sequence:

1. Apply V_{IN} to the application: The PMIC goes into the POWER_ON state (*)
2. Write NVM shadow registers with expected customization values
3. Initiate a “NVM program operation” command - write NVM_CMD [1:0] = ‘01’
4. Wait for the NVM write operation to be completed: wait for NVM_BUSY to become 0
5. Check for the NVM write operation to succeed: NVM_WRITE_FAIL = 0 in NVM_SR
6. Check new NVM content by initiating an NVM read operation: write NVM_CMD [1:0] = ‘10’ and wait for NVM_BUSY to become 0
7. A power OFF/ON cycle is needed to load the new NVM content.

The following conditions should be fulfilled to allow an NVM write operation:

- V_{IN} must be minimum VNVM_PROG

The NVM write operation works at least in the POWER_ON state to allow the application to reprogram the NVM at runtime (via I²C). Writing into NVM shadow registers does not affect NVM content until the NVM write operation is executed.

WARNING: If V_{IN} goes below VNVM_PROG during the write operation, the NVM content integrity may be corrupted and the PMIC may not start up anymore.

*. The PMIC has the AUTO_TURN_ON bit set by default to power up automatically. This allows the NVM write operation without generating turn-on conditions.

5.5.2.3 *I²C address:*

Special care must be taken when a new I²C address needs to be programmed.

When a different I²C address is written in NVM_I²C_ADDR_SHR, this new address becomes effective after an NVM write operation and only after reloading the NVM (INIT&LOAD or CHECK&LOAD state).

If an NVM write operation is not performed following the I²C address change in the shadow register, the previously programmed I²C address is loaded from the NVM during the next POWER_UP sequence.

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5.5.2.4 *LOCK_NVM write operation*

When the PMIC is customized with the LOCK_NVM bit set in the NVM_I²C_ADD_SHR, followed by a programming command (NVM_CMD [1:0] = 0b01), then the NVM write operation becomes disabled immediately. Any new programming command execution is ignored and the NVM_WRITE_FAIL bit is set in NVM_SR.

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6 Register descriptions

6.1 Register map

All NVM_xxx bits of shadow registers have related xxx mirror bits in the control registers section, allowing the software to override the NVM's predefined values at runtime. Each time the NVM is reloaded, the related xxx mirror bits are also reloaded with the NVM's predefined values.

All bits reserved in registers with R/W must not be modified.

So, before writing on a register with a reserved bit, the user should read the content of the register and should only modify bits that are not reserved, then write to the register.

hex	Register Name	R/W	BITS[7:0]							
			7	6	5	4	3	2	1	0
Status registers										
0x00	Product_ID	R	PMIC_REF_ID[3:0]				PMIC_NVM_ID[3:0]			
0x01	Version_SR	R	MAJOR_VERSION[3:0]				MINOR_VERSION[3:0]			
0x02	TURN_ON_SR	R	-	-	-	-	AUTO	-	-	PKEY_EN
0x03	TURN_OFF_SR	R	EN	-	WDG_FLT	THSDN_FLT	OCP_FLT	VIN_FLT	PKEY_FLT	SWOFF
0x04	RESTART_SR	R	R_EN	R_RST	R_WDG_FLT	R_THSDN_FLT	R_OCP_FLT	R_VIN_FLT	R_PKEY_FLT	R_SWOFF
0x05	OCP_SR1	R	-	-	-	-	-	OCP_BUCK3	OCP_BUCK2	OCP_BUCK1
0x06	OCP_SR2	R	-	OCP_LDO7	OCP_LDO6	OCP_LDO5	OCP_LDO4	OCP_LDO3	OCP_LDO2	OCP_LDO1
0x07	EN_SR1	R	-	-	-	-	-	EN_BUCK3	EN_BUCK2	EN_BUCK1
0x08	EN_SR2	R	-	OCP_LDO7	OCP_LDO6	EN_LDO5	EN_LDO4	EN_LDO3	EN_LDO2	EN_LDO1
0x09	FS_CNT_SR1	R	VIN_FLT_CNT[3:0]				PKEY_FLT_CNT[3:0]			
0x0A	FS_CNT_SR2	R	THSDN_FLT_CNT[3:0]				OCP_FLT_CNT[3:0]			
0x0B	FS_CNT_SR3	R	-	-	-	-	WDG_FLT_CNT[3:0]			
0x0C	MODE_SR	R	OP_MODE[3:0]				-	PWRCTRL3	PWRCTRL 2	PWRCTRL 1
0x0D	GPO_SR	R	-	-	-	EN_GPO5	EN_GPO4	EN_GPO3	EN_GPO2	EN_GPO1
Control registers										
0x10	MAIN_CR	R/W	-	-	-	PWRCTRL_POL3	PWRCTRL_POL2	PWRCTRL_POL1	RREQ_EN	SWOFF
0x11	VINLOW_CR	R/W	-	-	VINLOW_HYST[1:0]		VINLOW_RISE[2:0]			VINLOW_EN
0x12	PKEY_LKP_CR	R/W	PKEY_LKP_OFF	PKEY_LKP_EN_FS LS	-	-	PKEY_LKP_TMR[3:0]			
0x13	WDG_CR	R/W	-	-	-	-	WDG_PWRCTRL[1:0]		WDG_RST	WDG_EN

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hex	Register Name	R/W	BITS[7:0]							
			7	6	5	4	3	2	1	0
Status registers										
0x14	WDG_TMR_CR	R/W	WDG_TMR_SET[7:0]							
0x15	WDG_TMR_SR	R	WDG_TMR_CNT[7:0]							
0x16	FS_OCP_CR1	R/W	-	-	-	-	-	FS_OCP_BUCK3	FS_OCP_BUCK2	FS_OCP_BUCK1
0x17	FS_OCP_CR2	R/W	-	FS_OCP_LDO7	FS_OCP_LDO6	FS_OCP_LDO5	FS_OCP_LDO4	FS_OCP_LDO3	FS_OCP_LDO2	FS_OCP_LDO1
0x18	PADS_PULL_CR	R/W	PWRCTRL3_PULL[1:0]		PWRCTRL2_PULL[1:0]		PWRCTRL1_PULL[1:0]		PKEY_EN_PULL[1:0]	
0x19	BUCKS_PD_CR	R/W	-	-	BUCK3_PD[1:0]		BUCK2_PD[1:0]		BUCK1_PD[1:0]	
0x1B	LDOS_PD_CR	R/W	-	LDO7_PD	LDO6_PD	LDO5_PD	LDO4_PD	LDO3_PD	LDO2_PD	LDO1_PD
0x1C	GPO_MRST_CR	R/W	-	-	GPO5_MRST	GPO4_MRST	GPO3_MRST	GPO2_MRST	GPO1_MRST	-
0x1D	BUCKS_MRST_CR	R/W	-	-	-	-	-	BUCK3_MRST	BUCK2_MRST	BUCK1_MRST
0x1E	LDOS_MRST_CR	R/W	-	LDO7_MRST	LDO6_MRST	LDO5_MRST	LDO4_MRST	LDO3_MRST	LDO2_MRST	LDO1_MRST
0x1F	SSMOD_CR	R/W	SSMOD_EN	SSMOD_CFG	SSMOD_DEEP[1:0]		SSMOD_STEP[3:0]			
Buck control registers										
0x20	BUCK1_MAIN_CR1	R/W	-	VOUT[6:0]						
0x21	BUCK1_MAIN_CR2	R/W	-	-	-	-	-	PREG_MODE[1:0]		EN
0x22	BUCK1_ALT_CR1	R/W	-	VOUT[6:0]						
0x23	BUCK1_ALT_CR2	R/W	-	-	-	-	-	PREG_MODE[1:0]		EN
0x24	BUCK1_PWRCTRL_CR	R/W	PWRCTRL_DLY_H[1:0]		PWRCTRL_DLY_L[1:0]		PWRCTRL_SEL[1:0]		PWRCTRL_RST	PWRCTRL_EN
0x25	BUCK2_MAIN_CR1	R/W	-	VOUT[6:0]						
0x26	BUCK2_MAIN_CR2	R/W	-	-	-	-	-	PREG_MODE[1:0]		EN
0x27	BUCK2_ALT_CR1	R/W	-	VOUT[6:0]						
0x28	BUCK2_ALT_CR2	R/W	-	-	-	-	-	PREG_MODE[1:0]		EN
0x29	BUCK2_PWRCTRL_CR	R/W	PWRCTRL_DLY_H[1:0]		PWRCTRL_DLY_L[1:0]		PWRCTRL_SEL[1:0]		PWRCTRL_RST	PWRCTRL_EN
0x2A	BUCK3_MAIN_CR1	R/W	-	VOUT[6:0]						

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hex	Register Name	R/W	BITS[7:0]							
			7	6	5	4	3	2	1	0
Status registers										
0x2B	BUCK3_MAIN_CR2	R/W	-	-	-	-	-	PREG_MODE[1:0]		EN
0x2C	BUCK3_ALT_CR1	R/W	-	VOUT[6:0]						
0x2D	BUCK3_ALT_CR2	R/W	-	-	-	-	-	PREG_MODE[1:0]		EN
0x2E	BUCK3_PWRCTRL_CR	R/W	PWRCTRL_DLY_H[1:0]		PWRCTRL_DLY_L[1:0]		PWRCTRL_SEL[1:0]		PWRCTRL_RST	PWRCTRL_EN
0x43	GPO1_MAIN_CR	R/W	-	-	-	-	-	-	-	EN
0x44	GPO1_ALT_CR	R/W	-	-	-	-	-	-	-	EN
0x45	GPO1_PWRCTRL_CR	R/W	PWRCTRL_DLY_H[1:0]		PWRCTRL_DLY_L[1:0]		PWRCTRL_SEL[1:0]		PWRCTRL_RST	PWRCTRL_EN
0x46	GPO2_MAIN_CR	R/W	-	-	-	-	-	-	-	EN
0x47	GPO2_ALT_CR	R/W	-	-	-	-	-	-	-	EN
0x48	GPO2_PWRCTRL_CR	R/W	PWRCTRL_DLY_H[1:0]		PWRCTRL_DLY_L[1:0]		PWRCTRL_SEL[1:0]		PWRCTRL_RST	PWRCTRL_EN
LDO control registers										
0x4C	LDO1_MAIN_CR	R/W	-	-	-	-	-	-	-	EN
0x4D	LDO1_ALT_CR	R/W	-	-	-	-	-	-	-	EN
0x4E	LDO1_PWRCTRL_CR	R/W	PWRCTRL_DLY_H[1:0]		PWRCTRL_DLY_L[1:0]		PWRCTRL_SEL_L[1:0]		PWRCTRL_RST	PWRCTRL_EN
0x4F	LDO2_MAIN_CR	R/W	-	-	VOUT[4:0]					EN
0x50	LDO2_ALT_CR	R/W	-	-	VOUT[4:0]					EN
0x51	LDO2_PWRCTRL_CR	R/W	PWRCTRL_DLY_H[1:0]		PWRCTRL_DLY_L[1:0]		PWRCTRL_SEL[1:0]		PWRCTRL_RST	PWRCTRL_EN
0x52	LDO3_MAIN_CR	R/W	SNK_SRC	-	VOUT[4:0]					EN
0x53	LDO3_ALT_CR	R/W	SNK_SRC	-	VOUT[4:0]					EN
0x54	LDO3_PWRCTRL_CR	R/W	PWRCTRL_DLY_H[1:0]		PWRCTRL_DLY_L[1:0]		PWRCTRL_SEL[1:0]		PWRCTRL_RST	PWRCTRL_EN
0x55	LDO4_MAIN_CR	R/W	-	-	-	-	-	-	-	EN
0x56	LDO4_ALT_CR	R/W	-	-	-	-	-	-	-	EN

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hex	Register Name	R/W	BITS[7:0]							
			7	6	5	4	3	2	1	0
Status registers										
0x57	LDO4_PWRCTRL_CR	R/W	PWRCTRL_DLY_H[1:0]		PWRCTRL_DLY_L[1:0]		PWRCTRL_SEL[1:0]		PWRCTRL_RST	PWRCTRL_EN
0x58	LDO5_MAIN_CR	R/W	-	-	VOUT[4:0]					EN
0x59	LDO5_ALT_CR	R/W	-	-	VOUT[4:0]					EN
0x5A	LDO5_PWRCTRL_CR	R/W	PWRCTRL_DLY_H[1:0]		PWRCTRL_DLY_L[1:0]		PWRCTRL_SEL[1:0]		PWRCTRL_RST	PWRCTRL_EN
0x5B	LDO6_MAIN_CR	R/W	-	-	VOUT[4:0]					EN
0x5C	LDO6_ALT_CR	R/W	-	-	VOUT[4:0]					EN
0x5D	LDO6_PWRCTRL_CR	R/W	PWRCTRL_DLY_H[1:0]		PWRCTRL_DLY_L[1:0]		PWRCTRL_SEL[1:0]		PWRCTRL_RST	PWRCTRL_EN
0x5E	LDO7_MAIN_CR	R/W	-	-	VOUT[4:0]					EN
0x5F	LDO7_ALT_CR	R/W	-	-	VOUT[4:0]					EN
0x60	LDO7_PWRCTRL_CR	R/W	PWRCTRL_DLY_H[1:0]		PWRCTRL_DLY_L[1:0]		PWRCTRL_SEL_L[1:0]		PWRCTRL_RST	PWRCTRL_EN
GPO control registers										
0x67	GPO3_MAIN_CR	R/W	-	-	-	-	-	-	-	EN
0x68	GPO3_ALT_CR	R/W	-	-	-	-	-	-	-	EN
0x69	GPO3_PWRCTRL_CR	R/W	PWRCTRL_DLY_H[1:0]		PWRCTRL_DLY_L[1:0]		PWRCTRL_SEL[1:0]		PWRCTRL_RST	PWRCTRL_EN
0x6A	GPO4_MAIN_CR	R/W	-	-	-					EN
0x6B	GPO4_ALT_CR	R/W	-	-	-					EN
0x6C	GPO4_PWRCTRL_CR	R/W	PWRCTRL_DLY_H[1:0]		PWRCTRL_DLY_L[1:0]		PWRCTRL_SEL_L[1:0]		PWRCTRL_RST	PWRCTRL_EN
0x6D	GPO5_MAIN_CR	R/W	-		-		-		-	EN
0x6E	GPO5_ALT_CR	R/W	-	-	-	-	-	-	-	EN
0x6F	GPO5_PWRCTRL_C	R/W	PWRCTRL_DLY_H[1:0]		PWRCTRL_DLY_L[1:0]		PWRCTRL_SEL[1:0]		PWRCTRL_RST	PWRCTRL_EN
Interrupt control registers										
0x70	INT_PENDING_R1	R	-	-	VINLOW_RI	VINLOW_FA	-	-	PKEY_RI	PKEY_FA
0x71	INT_PENDING_R2	R	-	-	-	-	-	-	THW_RI	THW_FA

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hex	Register Name	R/W	BITS[7:0]							
			7	6	5	4	3	2	1	0
Status registers										
0x72	INT_PENDING_R3	R	-	-	-	-	-	BUCK3_OCP	BUCK2_OCP	BUCK1_OCP
0x73	INT_PENDING_R4	R	-	LDO7_OCP	LDO6_OCP	LDO5_OCP	LDO4_OCP	LDO3_OCP	LDO2_OCP	LDO1_OCP
0x74	INT_CLEAR_R1	W/R0/SC	-	-	VINLOW_RI_CLR	VINLOW_FA_CLR	-	-	PKEY_RI_CLR	PKEY_FA_CLR
0x75	INT_CLEAR_R2	W/R0/SC	-	-	-	-	-	-	THW_RI_CLR	THW_FA_CLR
0x76	INT_CLEAR_R3	W/R0/SC	-	-	-	-	-	BUCK3_OCP_CLR	BUCK2_OCP_CLR	BUCK1_OCP_CLR
0x77	INT_CLEAR_R4	W/R0	-	LDO7_OCP_CLR	LDO6_OCP_CLR	LDO5_OCP_CLR	LDO4_OCP_CLR	LDO3_OCP_CLR	LDO2_OCP_CLR	LDO1_OCP_CLR
0x78	INT_MASK_R1	R/W	-	-	VINLOW_RI_MASK	VINLOW_FA_MASK	-	-	PKEY_RI_MASK	PKEY_FA_MASK
0x79	INT_MASK_R2	R/W	-	-	-	-	-	-	THW_RI_MASK	THW_FA_MASK
0x7A	INT_MASK_R3	R/W	-	-	-	-	-	BUCK3_OCP_MASK	BUCK2_OCP_MASK	BUCK1_OCP_MASK
0x7B	INT_MASK_R4	R/W	-	LDO7_OCP_MASK	LDO6_OCP_MASK	LDO5_OCP_MASK	LDO4_OCP_MASK	LDO3_OCP_MASK	LDO2_OCP_MASK	LDO1_OCP_MASK
0x7C	INT_SRC_R1	R	-	-	VINLOW	!VINLOW	-	-	PKEY	!PKEY
0x7D	INT_SRC_R2	R	-	-	-	-	-	-	THW	!THW
0x7E	INT_SRC_R3	R	-	-	-	-	-	BUCK3_OCP_STATUS	BUCK2_OCP_STATUS	BUCK1_OCP_STATUS
0x7F	INT_SRC_R4	R	-	LDO7_OCP_STATUS	LDO6_OCP_STATUS	LDO5_OCP_STATUS	LDO4_OCP_STATUS	LDO3_OCP_STATUS	LDO2_OCP_STATUS	LDO1_OCP_STATUS
0x80	INT_DBG_LATCH_R1	W/R0/SC	-	-	VINLOW_RI_FRC	VINLOW_FA_FRC	-	-	PKEY_RI_FRC	PKEY_FA_FRC
0x81	INT_DBG_LATCH_R2	W/R0/SC	-	-	-	-	-	-	THW_RI_FRC	THW_FA_FRC
0x82	INT_DBG_LATCH_R3	W/R0/SC	-	-	-	-	-	BUCK3_OCP_FRC	BUCK2_OCP_FRC	BUCK1_OCP_FRC
0x83	INT_DBG_LATCH_R4	W/R0/SC	-	LDO7_OCP_FRC	LDO6_OCP_FRC	LDO5_OCP_FRC	LDO4_OCP_FRC	LDO3_OCP_FRC	LDO2_OCP_FRC	LDO1_OCP_FRC
NVM user control registers										
0x8E	NVM_SR	R	-	-	-	-	-	-	WRITE_FAIL	BUSY
0x8F	NVM_CR	R/W	-	-	-	-	-	-	CMD[1:0]	
NVM user shadow registers										

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hex	Register Name	R/W	BITS[7:0]							
			7	6	5	4	3	2	1	0
Status registers										
0x90	MAIN_CTRL_SHR1	R/W	VINOK_HYST[1:0]		VINOK_RISE[1:0]		NVM_WDG_TMR_SET[1:0]		NVM_WDG_EN	AUTO_TURNON
0x91	MAIN_CTRL_SHR2	R/W	RANK_DLY[1:0]		RST_DLY[1:0]		NVM_PKEY_LKP_OFF	NVM_PKEY_LKP_FSLS	NVM_PKEY_LKP_TMR[1:0]	
0x92	NVM_RANK_SHR1	R/W	-	-	BUCK2_RANK[2:0]			BUCK1_RANK[2:0]		
0x93	NVM_RANK_SHR2	R/W						BUCK3_RANK[2:0]		
0x94	NVM_FREE_SHR1	R/W	NVM_FREE1[7:0]							
0x95	NVM_FREE_SHR2	R/W	NVM_FREE2[7:0]							
0x96	NVM_RANK_SHR5	R/W	-	-	LDO2_RANK[2:0]			LDO1_RANK[2:0]		
0x97	NVM_RANK_SHR6	R/W	-	-	LDO4_RANK[2:0]			LDO3_RANK[2:0]		
0x98	RANK_SHR7	R/W	-	-	LDO6_RANK[2:0]			LDO5_RANK[2:0]		
0x99	RANK_SHR8	R/W	-	-	-			LDO7_RANK[2:0]		
0x9A	NVM_BUCK_MODE_SHR1	R/W	-	-	-	BUCK3_PREG_MODE [1:0]	BUCK2_PREG_MODE [1:0]		BUCK1_PREG_MODE[1:0]	
0x9B	NVM_FREE_SHR3	R/W	NVM_FREE3 [7:0]							
0x9C	NVM_BUCK1_VOUT_SHR	R/W	BUCK1_VRANGE_CFG	NVM_VOUT[6:0]						
0x9D	NVM_BUCK2_VOUT_SHR	R/W	-	NVM_VOUT[6:0]						
Ox9E	NVM_BUCK3_SHR	R/W	-	NVM_VOUT[6:0]						
0x9F	NVM_GPO_CONFIG_SHR	R/W	-	-	-	GPO5_POL	GPO4_POL	GPO3_POL	GPO2_POL	GPO1_POL
0xA0	NVM_GPO_RANK_SHR1	R/W	-	-	GPO2_RANK[2:0]			GPO1_RANK[2:0]		
0xA1	NVM_GPO_RANK_SHR2	R/W	-	-	GPO4_RANK[2:0]			GPO3_RANK[2:0]		
0xA2	NVM_GPO_RANK_SHR3	R/W	-	-	-	-	-	GPO5_RANK[2:0]		
0xA3	NVM_LDO2_SHR	R/W	-	-	NVM_VOUT[4:0]					-
0xA4	NVM_LDO3_SHR	R/W	SNK_RSC	-	NVM_VOUT[4:0]					-

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hex	Register Name	R/W	BITS[7:0]							
			7	6	5	4	3	2	1	0
Status registers										
0xA5	NVM_LDO5_SHR	R/W	-	-	NVM_VOUT[4:0]					-
0xA6	NVM_LDO6_SHR	R/W	-	-	NVM_VOUT[4:0]					-
0xA7	NVM_LDO7_SHR	R/W	-	-	NVM_VOUT[4:0]					-
0xA8	NVM_FREE_SHR4	R/W	-	-	NVM_FREE4[7:0]					
0xA9	NVM_PD_SHR1	R/W	-	-	NVM_BUCK3_PD[1:0]		NVM_BUCK2_PD[1:0]		NVM_BUCK1_PD[1:0]	
0xAA	NVM_FREE_SHR5	R/W	NVM_FREE5[7:0]							
0xAB	NVM_PD_SHR3	R/W	-	NVM_LDO 7_PD	NVM_LDO 6_PD	NVM_LDO 5_PD	NVM_LDO 4_PD	NVM_LDO 3_PD	NVM_LDO 2_PD	NVM_LDO1_PD
0xAC	NVM_BUCKS_IOUT_SHR1	R/W	-	-	-	BUCK3_ILIM[1:0]	BUCK2_ILIM[1:0]		BUCK1_ILIM[1:0]	
0xAD	NVM_BUCKS_IOUT_SHR2	R/W	HICCUP_DLY[1:0]		-	-	-	-	-	-
0xAE	NVM_LDOS_IOUT_SHR	R/W	LDO7_ILIM[1:0]		LDO6_ILIM[1:0]		LDO5_ILIM[1:0]		LDO2_ILIM[1:0]	
0xAF	NVM_FS_OCP_SHR1	R/W	-	-	-	-	-	NVM_FS_OCP_BUCK3	NVM_FS_OCP_BUCK2	NVM_FS_OCP_BUCK1
0xB0	NVM_FS_OCP_SHR2	R/W	-	NVM_FS_OCP_LDO7	NVM_FS_OCP_LDO6	NVM_FS_OCP_LDO5	NVM_FS_OCP_LDO4	NVM_FS_OCP_LDO3	NVM_FS_OCP_LDO2	NVM_FS_OCP_LDO1
0xB1	NVM_FS_SHR1	R/W	VIN_FLT_CNT_MAX[3:0]				PKEY_FLT_CNT_MAX[3:0]			
0xB2	NVM_FS_SHR2	R/W	TSHDN_FLT_CNT_MAX[3:0]				OCP_FLT_CNT_MAX[3:0]			
0xB3	NVM_FS_SHR3	R/W	-	FS_LOCK_DIS	RST_FLT_CNT_TMR[1:0]		WDG_FLT_CNT_MAX[3:0]			
0xB5	NVM_I²C_ADDR_SHR	R/W	LOCK_NVM	I²C_ADDR[6:0]						
0xB6	NVM_USER_SHR1	R/W	NVM_USER1[7:0]							
0xB7	NVM_USER_SHR2	R/W	NVM_USER2[7:0]							
0xB9	NVM_MAIN_CTRL_SHR3	R/W	VIN_DLY[1:0]		-		NVM_PKEY_EN_PULL[1:0]		EN_POL_CFG	PKEY_EN_CFG

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6.2 Status registers

6.2.1 Product ID status register (PRODUCT_ID_SR)

Table 29. PRODUCT_ID_SR

7	6	5	4	3	2	1	0
PMIC_REF_ID [3:0]				PMIC_NVM_ID [3:0]			
R	R	R	R	R	R	R	R

- Address: 0x00
- Default: 0x3X (X depends on PMIC variant)
- Description: PMIC product ID status register.

[7:4]	**PMIC_REF_ID [3:0]**: PMIC family of devices 0001: STPMIC2L product family (fixed value)
[3:0]	Version A and B only 0000: customized 0001: A 0002: B 0011: reserved

6.2.2 Version status register (VERSION_SR)

Table 30. VERSION_SR

7	6	5	4	3	2	1	0
MAJOR_VERSION [3:0]				MINOR_VERSION [3:0]			
R	R	R	R	R	R	R	R

- Address: 0x01
- Default: 0x12
- Description: PMIC version status register.

[7:4]	MAJOR_VERSION [3:0]
[3:0]	MINOR_VERSION [3:0]

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6.2.3 Turn-on status register (TURN_ON_SR)

Table 31. **TURN_ON_SR**

7	6	5	4	3	2	1	0
-	-	-	-	AUTO	-	-	PKEY_EN
R	R	R	R	R	R	R	R

- Address: 0x02
- Default: 0b0000x00x where x depends on the turn-on condition
- Description: Stores last condition, which has turned on the PMIC.

From the NO_SUPPLY state, if the AUTO_TURN_ON bit is set in the NVM, the TURN_ON_SR [AUTO] is set.

In the OFF state, the TURN_ON_SR is cleared. When a turn-on condition occurs, the related turn-on bit is set in TURN_ON_SR before leaving the OFF state.

The TURN_ON_SR is cleared in the POWER_DOWN state.

[7:4]	reserved
[3]	**AUTO**: The PMIC turn-on condition is triggered by the AUTO_TURN_ON bit in the NVM. See Section 5.4.5. AUTO turn-ON. 0: False 1: True
[2]	reserved
[1]	reserved
[0]	**PKEY_EN**: The PMIC turn-on condition is triggered by the PONKEYn or EN signals. See Section 5.4.5. 0: False 1: True

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6.2.4 Turn-off status register (TURN_OFF_SR)

Table 32. **TURN_OFF_SR**

7	6	5	4	3	2	1	0
EN	-	WDG_FLT	TSHDN_FLT	OCP_FLT	VIN_FLT	PKEY_FLT	SWOFF
R	R	R	R	R	R	R	R

- Address: 0x03
- Default: 0bx0xxxxx where x depends on the turn-off condition
- Description: Stores last condition, which has turned off the PMIC.

The TURN_OFF_SR register is reset in the POWER_DOWN state. Then TURN_OFF_SR is set either when going into the OFF state or when going into the FAIL_SAFE_LOCK state (see Section 5.4.7 and Section 5.1.2).

[7]	**EN**: Last turn-off is due to EN de-activation. (PKEY_EN_CFG bit is set, and PONKEYn/EN pad deasserted depending on EN_POL_CFG) 0: False 1: True
[6]	reserved
[5]	**WDG_FLT**: Last turn-off is due to watchdog hard-fault source while WDG_FLT_CNT > WDG_FLT_CNT_MAX. 0: False 1: True
[4]	**THSDN_FLT**: Last turn-off is due to thermal shutdown hard-fault source while TSHDN_FLT_CNT > TSHDN_FLT_CNT_MAX. 0: False 1: True
[3]	**OCP_FLT**: Last turn-off is due to regulator overcurrent hard-fault source while OCP_FLT_CNT > OCP_FLT_CNT_MAX. 0: False 1: True
[2]	**VIN_FLT**: Last turn-off is due to V_{IN} falling below V_{INOK_Fall} hard-fault source while VIN_FLT_CNT > VIN_FLT_CNT_MAX. (This is valid only if V_{IN} is kept higher than V_{INPOR_Fall}; or the PMIC fully resets) 0: False 1: True
[1]	**PKEY_FLT**: Last turn-off is due to PONKEYn long key press hard-fault source while PKEY_FLT_CNT > PKEY_FLT_CNT_MAX. 0: False 1: True
[0]	**SWOFF**: Last turn-off is due to software switch OFF (SWOFF bit set and RREQ_EN bit clear in the MAIN_CR register). 0: False 1: True

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6.2.5 Restart status register (RESTART_SR)

Table 33. **RESTART_SR**

7	6	5	4	3	2	1	0
R_EN	R_RST	R_WDG_FLT	R_TSHDN_FLT	R_OCP_FLT	R_VIN_FLT	R_PKEY_FLT	R_SWOFF
R	R	R	R	R	R	R	R

- Address: 0x04
- Default: 0bxxxxxxxx where x depends on a power-OFF condition which restarts the PMIC
- Description: Stores last condition, which has restarted the PMIC (power cycle).

The RESTART_SR register is reset in the POWER_DOWN state. Then RESTART_SR is set when going into the CHECK&LOAD state (see Section 5.4.7 and Section 5.1.2).

[7]	**R_EN**: Last restart is due to EN pin activation (PKEY_EN_CFG bit is set, and PONKEYn/EN pad asserted depending on EN_POL_CFG) 0: False 1: True
[6]	**R_RST**: Last restart is due to RSTn pin asserted low by the application processor (or by a user reset button) 0: False 1: True
[5]	**R_WDG_FLT**: Last restart is due to watchdog hard-fault source while WDG_FLT_CNT <= WDG_FLT_CNT_MAX. 0: False 1: True
[4]	**R_TSHDN_FLT**: Last restart is due to thermal shutdown hard-fault source while TSHDN_FLT_CNT <= TSHDN_FLT_CNT_MAX. 0: False 1: True
[3]	**R_OCP_FLT**: Last restart is due to regulator overcurrent hard-fault source while OCP_FLT_CNT <= OCP_FLT_CNT_MAX. (overcurrent source is saved in OCP_SR1 or in OCP_SR2) 0: False 1: True
[2]	**R_VIN_FLT**: Last restart is due to V_{IN} falling below V_{INOK_Fall} hard-fault source while VIN_FLT_CNT <= VIN_FLT_CNT_MAX. (This is valid only if VIN is kept higher than V_{INPOR_Fall}; or PMIC fully resets) 0: False 1: True
[1]	**R_PKEY_FLT**: Last restart is due to PONKEYn long key press hard-fault source while PKEY_FLT_CNT <= PKEY_FLT_CNT_MAX. 0: False 1: True
[0]	**R_SWOFF**: Last restart is due to a restart request from AP: • setting both SWOFF and RREQ_EN bits in MAIN_CR register if PONKEYn is set in PKEY_EN_CFG NVM register. • setting SWOFF bit and EN is asserted if EN is set in PKEY_EN_CFG NVM register. 0: False

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	1: True

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6.2.6 Overcurrent protection status register 1 (OCP_SR1)

Table 34. Overcurrent protection status register 1 (OCP_SR1)

7	6	5	4	3	2	1	0
-	-	-	-	-	OCP_BUCK3	OCP_BUCK2	OCP_BUCK1
R	R	R	R	R	R	R	R

- Address: 0x05
- Default: 0b000000xx where x depends on regulator that has triggered the OCP.
- Description: If the PMIC turned OFF or restarted due to an OCP from regulator, OCP_SR1 or OCP_SR2 store the regulator instance that triggered the OCP.

The OCP_SR1 register is reset in the POWER_DOWN state. If an OCP hard-fault condition occurred, then the OCP_SR1 register is set before leaving the POWER_DOWN state (see Section 5.4.7.1 and Section 5.4.5 and Section 5.1.2).

[7:2]	reserved
[2]	**OCPBUCK3**: Last turn-off or restart is due to overcurrent protection on BUCK3. 0: False 1: True
[1]	**OCP_BUCK2**: Last turn-off or restart is due to overcurrent protection on BUCK2. 0: False 1: True
[0]	**OCP_BUCK1**: Last turn-off or restart is due to overcurrent protection on BUCK1. 0: False 1: True

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6.2.7 Overcurrent protection status register 2 (OCP_SR2)

Table 35. Overcurrent protection status register 2 (OCP_SR2)

7	6	5	4	3	2	1	0
-	OCP_LDO7	OCP_LDO6	OCP_LDO5	OCP_LDO4	OCP_LDO3	OCP_LDO2	OCP_LDO1
R	R	R	R	R	R	R	R

- Address: 0x06
- Default: 0b0xxxxxx where x depends on the regulator that has triggered the OCP.
- Description: If the PMIC is turned OFF or is restarted due to an OCP from a regulator, OCP_SR1 or OCP_SR2 store the regulator instance that triggered the OCP.

The OCP_SR2 register is reset in the POWER_DOWN state. If an OCP hard-fault condition occurred, then the OCP_SR2 register is set before leaving the POWER_DOWN state (see Section 5.4.7.1, Section 5.4.5 and Section 5.1.2).

[7]	reserved
[6]	OCP_LDO7: Last turn-off or restart is due to overcurrent protection on LDO7 . 0: False 1: True
[5]	OCP LDO6: Last turn-off or restart is due to overcurrent protection on LDO6. 0: False 1: True
[4]	**OCP_LDO5**: Last turn-off or restart is due to overcurrent protection on LDO5. 0: False 1: True
[3]	**OCP_LDO4**: Last turn-off or restart is due to overcurrent protection on LDO4. 0: False 1: True
[2]	**OCP_LDO3**: Last turn-off or restart is due to overcurrent protection on LDO3. 0: False 1: True
[1]	**OCP_LDO2**: Last turn-off or restart is due to overcurrent protection on LDO2. 0: False 1: True
[0]	**OCPLDO1**:Last turn-off or restart is due to overcurrent protection on LDO1. 0: False 1: True

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6.2.8 Enable status register 1 (EN_SR1)

Table 36. **EN_SR1**

7	6	5	4	3	2	1	0
-	-	-	-	-	EN_BUCK3	EN_BUCK2	EN_BUCK1
R	R	R	R	R	R	R	R

- Address: 0x07
- Default: 0b00000xxx where x depends on regulator status (0 = disabled, 1 = enabled)
- Description: This register reflects the IP current enable status despite the setting in MAIN or ALT configurations.

[7:3]	reserved
[2]	EN BUCK3: Current internal enable status of BUCK3. 0: Disabled 1: Enabled
[1]	**EN_BUCK2**: Current internal enable status of BUCK2. 0: Disabled 1: Enabled
[0]	**EN_BUCK1**: Current internal enable status of BUCK1. 0: Disabled 1: Enabled

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6.2.9 Enable status register 2 (EN_SR2)

Table 37. **EN_SR2**

7	6	5	4	3	2	1	0
-	EN_LDO7	EN_LDO6	EN_LDO5	EN_LDO4	EN_LDO3	EN_LDO2	EN_LDO1
R	R	R	R	R	R	R	R

- Address: 0x08
- Default: 0x0xxxxxxx where x depends on regulator status (0 = disabled, 1 = enabled)
- Description: This register reflects the IP current enable status despite the setting in MAIN or ALT configurations.

[7]	reserved
6	EN LDO7: Current internal enable status of LDO7. 0: Disabled 1: Enabled
5	EN LDO6: Current internal enable status of LDO6. 0: Disabled 1: Enabled
[4]	**EN_LDO5**: Current internal enable status of LDO5. 0: Disabled 1: Enabled
[3]	**EN_LDO4**: Current internal enable status of LDO4. 0: Disabled 1: Enabled
[2]	**EN_LDO3**: Current internal enable status of LDO3. 0: Disabled 1: Enabled
[1]	**EN_LDO2**: Current internal enable status of LDO2. 0: Disabled 1: Enabled
[0]	**ENLDO1**:Current internal enable status of LDO1. 0: Disabled 1: Enabled

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6.2.10 Fail-safe counter status register 1 (FS_CNT_SR1)

Table 38. FS_CNT_SR1

7	6	5	4	3	2	1	0
VIN_FLT_CNT [3:0]				PKEY_FLT_CNT [3:0]			
R	R	R	R	R	R	R	R

- Address: 0x09
- Default: 0x00
- Description: Fail-safe counters store the number of hard-fault occurrences. There is one fail-safe counter by hard fault source (see Section 5.4.5). FS_CNT_SR1 is reset in the OFF state.

[7:4]	**VIN_FLT_CNT [3:0]**: number of occurrences triggered by a V_{IN} falling below V_{INOK_Fall} hard-fault source. (This is valid only if V_{IN} is kept higher than V_{INPOR_Fall}; or PMIC fully resets)
[3:0]	**PKEY_FLT_CNT [3:0]**: number of occurrences triggered by a PONKEYn long key press hard-fault source.

Note: When a counter (xxx_FLT_CNT [3:0]) reaches 0xF, all next counter increments keep the counter value at 0xF (and do not restart to 0).

6.2.11 Fail-safe counter status register 2 (FS_CNT_SR2)

Table 39. FS_CNT_SR2

7	6	5	4	3	2	1	0
TSHDN_FLT_CNT [3:0]				OCP_FLT_CNT [3:0]			
R	R	R	R	R	R	R	R

- Address: 0x0A
- Default: 0x00
- Description: Fail-safe counters store the number of hard-fault occurrences. There is one fail-safe counter by hard fault source (see Section 5.4.5). FS_CNT_SR2 is reset in the OFF state.

[7:4]	**TSHDN_FLT_CNT [3:0]**: Number of occurrences triggered by a thermal shutdown hard-fault source.
[3:0]	**OCP_FLT_CNT [3:0]**: Number of occurrences triggered by regulator overcurrent hard-fault source.

Note: When a counter (xxx_FLT_CNT [3:0]) reaches 0xF, all next counter increments keep the counter value at 0xF (and do not restart to 0).

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6.2.12 Fail-safe counter status register 3 (FS_CNT_SR3)

Table 40. FS_CNT_SR3

7	6	5	4	3	2	1	0
-	-	-	-	WDG_FLT_CNT [3:0]			
R	R	R	R	R	R	R	R

- Address: 0x0B
- Default: 0x00
- Description: Fail-safe counters store the number of hard-fault occurrences. There is one fail-safe counter by hard fault source (see Section 5.4.5). FS_CNT_SR3 is reset in OFF state.

[7:4]	reserved
[3:0]	**WDG_FLT_CNT [3:0]**: number of occurrences triggered by watchdog hard-fault source.

Note: When a counter (xxx_FLT_CNT [3:0]) reaches 0xF, all next counter increments keep the counter value at 0xF (and do not restart to 0).

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6.2.13 Mode status register (MODE_SR)

Table 41. **MODE_SR**

7	6	5	4	3	2	1	0
OP_MODE [3:0]				-	PWRCTRL3	PWRCTRL2	PWRCTRL1
R	R	R	R	R	R	R	R

- Address: 0x0C
- Default: 0bxxxx0xxx where x depends on source state
- Description: Contains the current state of the related source.

[7:4]	**OP_MODE**: PMIC operating state 0000: PMIC is in POWER_ON state 0001: RESERVED 0010: PMIC is in INIT&LOAD state 0100: PMIC is in OFF state 0110: PMIC is in CHECK&LOAD state 1000: PMIC is in POWER_UP state 1110: PMIC is in WAIT_RSTREL state 1010: PMIC is in POWER_DOWN state 1100: PMIC is in FAIL_SAFE_LOCK state
[3	reserved
[2]	**PWRCTRL3**: logic state of the PWRCTRL3 input (see Table 25) 0: PWRCTRL3 is active 1: PWRCTRL3 is inactive
[1]	**PWRCTRL2**: logic state of the PWRCTRL2 input (see Table 25) 0: PWRCTRL2 is active 1: PWRCTRL2 is inactive
[0]	**PWRCTRL1**: logic state of the PWRCTRL1 input (see Table 25) 0: PWRCTRL1 is active 1: PWRCTRL1 is inactive

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6.2.14 GPO status register (GPO_SR)

Table 42. **GPO_SR**

7	6	5	4	3	2	1	0
-			GPO5_EN	GPO4_EN	GPO3_EN	GPO2_EN	GPO1_EN
R	R	R	R	R	R	R	R

- Address: 0x0D
- Default: 0b000xxxxx where x depends on source state
- Description: Contains current state of the related GPO.

[7:5]	reserved
[4]	**GPO5_EN**: logic state of the GPO5 input: 0: GPO5 is inactive 1: GPO5 is active
[3]	**GPO4_EN**: logic state of the GPO4 input: 0: GPO4 is inactive 1: GPO4 is active
[2]	**GPO3_EN**: logic state of the GPO3 input: 0: GPO3 is inactive 1: GPO3 is active
[1]	**GPO2_EN**: logic state of the GPO2 input: 0: GPO2 is inactive 1: GPO2 is active
[0]	**GPO1_EN**: logic state of the GPO1 input: 0: GPO1 is inactive 1: GPO1 is active

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6.3 Control registers

6.3.1 Main control register (MAIN_CR)

Table 43. **MAIN_CR**

7	6	5	4	3	2	1	0
-	-	-	PWRCTRL_POL[2]	PWRCTRL_POL [1:0]		RREQ_EN	SWOFF
R	R/W	R/W	R	R/W	R/W	R/W	R/W

- Address: 0x10
- Default: 0b00000000
- Description: main control register (see Table 28). This register is initialized to the default value in the CHECK&LOAD state.

[7:5]	reserved
[4]	**PWRCTRL_POL**: Specifies PWRCTRL1 pin polarity. 0: PWRCTRL1 active low 1: PWRCTRL1 active high
[3:2]	**PWRCTRL_POL**: Specifies PWRCTRL1 pin polarity. 0: PWRCTRL1 active low 1: PWRCTRL1 active high (see Table 28)
[1]	**RREQ_EN**: Allows the PMIC power cycle when the software switch OFF bit is (SWOFF) set. 0: PMIC goes in OFF state when SWOFF bit is set 1: PMIC performs a power cycle when the SWOFF bit is set *Note: if EN is set in PKEY_EN_CFG NVM register, this bit has no effect and is automatically cleared.*
[0]	**SWOFF**: Software switch OFF bit. 0: no effect 1: switch-OFF requested (turn-off condition). The PMIC goes into the POWER_DOWN state immediately.

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6.3.2 VINLOW monitoring control register (VINLOW_CR)

Table 44. **VINLOW_CR**

7	6	5	4	3	2	1	0
-	-	VINLOW_HYST [1:0]		VINLOW_RISE [2:0]			VINLOW_EN
R	R	R/W	R/W	R/W	R/W	R/W	R/W

- Address: 0x11
- Default: 0x00
- Description: V_{INLOW} monitoring control register (see VIN monitoring). This register is initialized to the default value in the CHECK&LOAD state.

[7:6]	reserved
[5:4]	**VINLOW_HYST [1:0]**: V_{INLOW} threshold hysteresis 00: 100 mV 01: 200 mV 10: 300 mV 11: 400 mV
[3:1]	**VINLOW_RISE [2:0]**: V_{INLOW_Rise} threshold 000: V_{INOK_Fall} + 50 mV 001: V_{INOK_Fall} + 100 mV 010: V_{INOK_Fall} + 150 mV 011: V_{INOK_Fall} + 200 mV 100: V_{INOK_Fall} + 250 mV 101: V_{INOK_Fall} + 300 mV 110: V_{INOK_Fall} + 350 mV 111: V_{INOK_Fall} + 400 mV
[0]	**VINLOW_EN**: V_{INLOW} monitoring enable bit 0: V_{INLOW} monitoring is disabled 1: V_{INLOW} monitoring is enabled

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6.3.3 PONKEYn long key press control register (PKEY_LKP_CR)

Table 45. **PKEY_LKP_CR**

7	6	5	4	3	2	1	0
PKEY_LKP_OFF	PKEY_LKP_EN_FSLS	-	-	PKEY_LKP_TMR[3:0]			
R/W	R/W	R	R	R/W	R/W	R/W	R/W

- Address: 0x12
- Default: 0bXX00XXXX where X depends on the value programmed in the NVM
- Description: PONKEYn long key press control register. This register is initialized to the default value in the CHECK&LOAD state.

[7]]	**PKEY_LKP_OFF**: (see Section 5.4.4) 0: no effect 1: A PONKEYn long key press triggers a turn-off condition Default value is defined by NVM_PKEY_LKP_OFF NVM bit
[6]	**PKEY_LKP_EN_FSLS**: PONKEYn long key press / EN (Enable) as FS_LOCK state skipping 0: no effect 1: A PONKEYn long key press / EN allows the PMIC to go from the FAIL_SAFE_LOCK state to the OFF state Default value is defined by the NVM_PKEY_LKP_EN_FSLS NVM bit
[5:4]	reserved
[3:0]	**PKEY_LKP_TMR [3:0]**: PONKEYn long key press timer duration 0000: 1 s 0001: 2 s 0010: 3 s 0011: 4 s 0100: 5 s 0101: 6 s 0110: 7 s 0111: 8 s 1000: 9 s 1001: 10 s 1010: 11 s 1011: 12 s 1100: 13 s 1101: 14 s 1110: 15 s 1111: 16 s Default value is defined by the NVM_PKEY_LKP_TMR[1:0] NVM bitfield

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6.3.4 Watchdog control register (WDG_CR)

Table 46. **WDG_CR**

7	6	5	4	3	2	1	0
-	-	-	-	WDG_PWRCTRL_SEL[1:0]		WDG_RST	WDG_EN
R	R	R	R	R/W	R/W	W/R0/SC	R/W

- Address: 0x13
- Default: 0b0000000X where X depends on the value programmed in the NVM
- Description: Watchdog control register (see Section 5.4.7.2). This register is initialized to the default value in the CHECK&LOAD state.

[7:4]	Reserved
[3:2]	**WDG_PWRCTRL_SEL [1:0]**: Watchdog suspends source selection. 00: No source (if WDG_EN = 1, watchdog timer always runs) 01: PWRCTRL1 WDG suspends control source 10: PWRCTRL2 WDG suspends control source 11: PWRCTRL3 WDG suspends control source When the watchdog is enabled (WDG_EN = 1): if the PWRCTRLx control source is inactive, the watchdog timer runs; if the PWRCTRLx control source is active, the watchdog timer is suspended
[1]	**WDG_RST**: watchdog timer reset 0: NA 1: Watchdog down counter WDG_TMR_CNT [7:0] is reloaded with the value in WDG_TMR_SET [7:0] (self-cleared bit)
[0]	**WDG_EN**: watchdog enable bit 0: watchdog is disabled 1: watchdog is enabled Default value is defined by the NVM_WDG_EN NVM bit

6.3.5 Watchdog timer control register (WDG_TMR_CR)

Table 47. **WDG_TMR_CR**

7	6	5	4	3	2	1	0
WDG_TMR_SET [7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	W/R0	R/W

- Address: 0x14
- Default: 0xXX where X depends on the value programmed in NVM
- Description: Watchdog timer control register. This register is initialized to the default value in the CHECK&LOAD state.

[7:0]	WDG_TMR_SET [7:0]: Watchdog timer duration settings: 0x00 = 1 s 0x00 = 2 s … 0xFF= 256 s Default value is defined by the NVM_WDG_TMR_SET [1:0] NVM bit

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6.3.6 Watchdog timer status register (WDG_TMR_SR)

Table 48. **WDG_TMR_SR**

7	6	5	4	3	2	1	0
WDG_TMR_SET [7:0]							
R	R	R	R	R	R	R	R

- Address: 0x15
- Default: 0x00
- Description: Watchdog timer status register. Watchdog down counter providing remaining duration (in seconds) before watchdog expiration.

This register is initialized to the default value in the CHECK&LOAD state.

[7:0]	**WDG_TMR_CNT [7:0]:** Watchdog timer down counter 0xFF = 256 s … 0x01 = 2 s 0x00 = 1 s

6.3.7 Fail-safe overcurrent protection control register 1 (FS_OCP_CR1)

Table 49. **FS_OCP_CR1**

7	6	5	4	3	2	1	0
-	-	-	-	-	FS_OCP_BUCK3	FS_OCP_BUCK2	FS_OCP_BUCK1
R	R	R	R	R	R/W	R/W	R/W

- Address: 0x16
- Default: 0b000000XX where X depends on the value programmed in the NVM
- Description: Fail-safe overcurrent protection control registers 1 (see Section 5.4.7.1). This register is initialized to the default value in the CHECK&LOAD state.

[7:3]	reserved
[2]	**FS_OCP_BUCK3**: BUCK3 OCP management mode selection. 0: OCP hiccup mode (Level 0) 1: OCP fail-safe PMIC turn-off (Level 1)
[1]	**FS_OCP_BUCK2**: BUCK2 OCP management mode selection. 0: OCP hiccup mode (Level 0) 1: OCP fail-safe PMIC turn-off (Level 1)
[0]	**FS_OCP_BUCK1**: BUCK1 OCP management mode selection. 0: OCP hiccup mode (Level 0) 1: OCP fail-safe PMIC turn-off (Level 1)

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6.3.8 Fail-safe overcurrent protection control register 2 (FS_OCP_CR2)

Table 50. **FS_OCP_CR2**

7	6	5	4	3	2	1	0
-	FS_OCP_LDO7	FS_OCP_LDO6	FS_OCP_LDO5	FS_OCP_LDO4	FS_OCP_LDO3	FS_OCP_LDO2	FS_OCP_LDO1
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

- Address: 0x17
- Default: 0b0xxxxxxx where X depends on the value programmed in NVM
- Description: Fail-safe overcurrent protection control registers 2 (see Section 5.4.7.1). This register is initialized to the default value in the CHECK&LOAD state.

[7]	reserved
[6]	**FS_OCP_LDO7**: LDO7 OCP management mode selection. 0: OCP hiccup mode (Level 0) 1: OCP fail-safe PMIC turn-off (Level 1)
[5]	**FS_OCP_LDO6**: LDO6 OCP management mode selection. 0: OCP hiccup mode (Level 0) 1: OCP fail-safe PMIC turn-off (Level 1)
[4]	**FS_OCP_LDO5**: LDO5 OCP management mode selection. 0: OCP hiccup mode (Level 0) 1: OCP fail-safe PMIC turn-off (Level 1)
[3]	**FS_OCP_LDO4**: LDO4 OCP management mode selection. 0: OCP hiccup mode (Level 0) 1: OCP fail-safe PMIC turn-off (Level 1)
[2]	**FS_OCP_LDO3**: LDO3 OCP management mode selection. 0: OCP hiccup mode (Level 0) 1: OCP fail-safe PMIC turn-off (Level 1)
[1]	**FS_OCP_LDO2**: LDO2 OCP management mode selection. 0: OCP hiccup mode (Level 0) 1: OCP fail-safe PMIC turn-off (Level 1)
[0]	**FS_OCP_LDO1**: LDO1 OCP management mode selection. 0: OCP hiccup mode (Level 0) 1: OCP fail-safe PMIC turn-off (Level 1)

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6.3.9 Pads pull control register (PADS_PULL_CR)

Table 51. **PADS_PULL_CR**

7	6	5	4	3	2	1	0
PWRCTRL3_PULL [1:0]		PWRCTRL2_PULL [1:0]		PWRCTRL1_PULL [1:0]		PKEY_EN_PULL [1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

- Address: 0x18
- Default: 0b010101xx where xx depends on the value programmed in NVM
- Description: Pads pull control register. This register is initialized to the default value in the CHECK&LOAD state.

[7:6]	**PWRCTRL3_PULL[1:0]**: PWRCTRL3 pad pull resistor selection. 00: no pull 01:pull-up active (RPU) 10:pull-down active (RPD) 11: no pull
[5:4]	**PWRCTRL2_PULL[1:0]**: PWRCTRL2 pad pull resistor selection. 00: no pull 01:pull-up active (RPU) 10:pull-down active (RPD) 11: no pull
[3:2]	**PWRCTRL1_PULL[1:0]**: PWRCTRL1 pad pull resistor selection. 00: no pull 01:pull-up active (RPU) 10:pull-down active (RPD) 11: no pull
[1:0]	**PKEY_EN_PULL[1:0]**: PONKEYn/En pad pull resistor selection. 00: no pull 01: pull-up active (RPU) 10: pull-down active (RPD) 11: no pull Default value is defined by NVM_PKEY_EN_PULL[1:0] NVM bitfield

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6.3.10 Buck pull-down control register 1 (BUCKS_PD_CR)

Table 52. **BUCKS_PD_CR**

7	6	5	4	3	2	1	0
-	-	BUCK3_PD [1:0]		BUCK2_PD [1:0]		BUCK1_PD [1:0]	
R	R	R/W	R/W	R/W	R/W	R/W	R/W

- Address: 0x19
- Default: 0b00xxxxxx where X depends on the value programmed in the NVM
- Description: Bucks pull-down control register 1. This register is initialized to the default value in the INIT&LOAD and in the CHECK&LOAD states.

[7:6]	reserved
[5:4]	**BUCK3_PD [1:0]**: BUCK3 pull-down selection. 00: no pull-down 01: slow pull-down active when BUCK3 is disabled (EN = 0) 10: fast pull-down active when BUCK3 is disabled (EN = 0) 11: slow pull-down forced active
[3:2]	**BUCK2_PD [1:0]**: BUCK2 pull-down selection. 00: no pull-down 01: slow pull-down active when BUCK2 is disabled (EN = 0) 10: fast pull-down active when BUCK2 is disabled (EN = 0) 11: slow pull-down forced active
[1:0]	**BUCK1_PD [1:0]**: BUCK1 pull-down selection. 00: no pull-down 01: slow pull-down active when BUCK1 is disabled (EN = 0) 1 0: fast pull-down active when BUCK1 is disabled (EN = 0) 11: slow pull-down forced active

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6.3.11 LDO pull-down control register (LDOS_PD_CR)

Table 53. **LDOS_PD_CR**

7	6	5	4	3	2	1	0
-	LDO7_PD	LDO6_PD	LDO5_PD	LDO4_PD	LDO3_PD	LDO2_PD	LDO1_PD
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

- Address: 0x1B
- Default: 0b0xxxxxxx where X depends on the value programmed in NVM
- Description: LDO pull-down control register. This register is initialized to the default value in the INIT&LOAD and in the CHECK&LOAD states.

[7]	**reserved**
[6]	**LDO7_PD**: 0: no pull-down 1: pull-down active when LDO7 is disabled (EN = 0)
[5]	**LDO6_PD**: 0: no pull-down 1: pull-down active when LDO6 is disabled (EN = 0)
[4]	**LDO5_PD**: 0: no pull-down 1: pull-down active when LDO5 is disabled (EN = 0)
[3]	**LDO4_PD**: 0: no pull-down 1: pull-down active when LDO4 is disabled (EN = 0)
[2]	**LDO3_PD**: 0: no pull-down 1: pull-down active when LDO3 is disabled (EN = 0)
[1]	**LDO2_PD**: 0: no pull-down 1: pull-down active when LDO2 is disabled (EN = 0)
[0]	**LDO1_PD**: 0: no pull-down 1: pull-down active when LDO1 is disabled (EN = 0)

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6.3.12 Mask reset buck control register (BUCKS_MRST_CR)

Table 54. **BUCKx_MRST_CR**

7	6	5	4	3	2	1	0
-	-	-	-	-	BUCK3_MRST	BUCK2_MRST	BUCK1_MRST
R	R	R	R	R	R/W	R/W	R/W

- Address: 0x1D
- Default: 0x00
- Description: Mask reset buck control register.

See Section 5.4.15. This register is initialized to the default value in the CHECK&LOAD state; writable in POWER_ON states only.

[7:3]	**reserved**
[2]	**BUCK3_MRST**: mask reset setting 0: inactive 1: active
[1]	**BUCK2_MRST**: mask reset setting 0: inactive 1: active
[0]	**BUCK1_MRST**: mask reset setting 0: inactive 1: active

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6.3.13 Mask reset LDO control register (LDOS_MRST_CR)

Table 55. **LDOS_MRST_CR**

7	6	5	4	3	2	1	0
-	LDO7_MRST	LDO6_MRST	LDO5_MRST	LDO4_MRST	LDO3_MRST	LDO2_MRST	LDO1_MRST
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

- Address: 0x1E
- Default: 0x00
- Description: Mask reset LDO control register.

See Section 5.4.15. This register is initialized to the default value in the CHECK&LOAD state; writable in POWER_ON states only.

[7]	**reserved**
[6]	**LDO7_MRST**: mask reset setting 0: inactive 1: active
[5]	**LDO6_MRST**: mask reset setting 0: inactive 1: active
[4]	**LDO5_MRST**: mask reset setting 0: inactive 1: active
[3]	**LDO4_MRST**: mask reset setting 0: inactive 1: active
[2]	**LDO3_MRST**: mask reset setting 0: inactive 1: active
[1]	**LDO2_MRST**: mask reset setting 0: inactive 1: active
[0]	**LDO1_MRST**: mask reset setting 0: inactive 1: active

6.3.14 Mask reset GPO control register (GPOx_MRST)

Table 56. **GPOx_MRST_CR**

7	6	5	4	3	2	1	0
-	-	GPO5_MRST	GPO4_MRST	GP3_MRST	GP2_MRST	GP1_MRST	-
R	R	R/W	R/W	R/W	R/W	R/W	R/W

- Address: 0x1C
- Default: 0b00000000 where X depends on the value programmed in NVM
- Description: Mask reset GPO control register.

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This register is initialized to the default value in the INIT&LOAD and in the CHECK&LOAD states.

[7:6]	-	Reserved; read as 0
[5:1]	GPO_MRST	GPO(i+1)th mask reset setting For every bit: 0: mask reset inactive for GPO (i+1)th 1: mask reset inactive for GPO (i+1)th
[0]	-	Reserved; reead as 0

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6.3.15 Spread-spectrum control register (SSMOD_CR)

Table 57. **SSMOD CR**

7	6	5	4	3	2	1	0
SSMOD_EN	SSMOD_CFG	SSMOD_DEEP[1:0]		SSMOD_STEP[1:0]			
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

- Address: 0x1F
- Default: 0x00
- Description: Spread-spectrum modulation control register.

This register is initialized to the default value in the CHECK&LOAD state; writable in POWER_ON states only.

[7]	**SSMOD_EN**: Spread-spectrum modulation enable 0: inactive 1: active
[6]	**SSMOD_CFG**: Spread-spectrum modulation waveform shape 0: triangular 1: sawtooth
[5:4]	**SSMOD_DEEP**: Spread-spectrum modulation analog parameters configuration setting
[3;0]	**SSMOD_STEP**: Spread-spectrum modulation period setting Triangular modulation: (SSMOD_STEP+1)*30 µs Sawtooth modulation: (SSMOD_STEP+1)*16 µs

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6.4 Power supply control registers

6.4.1 BUCKx MAIN mode control register 1 (BUCKx_MAIN_CR1) (x = 1 to 3)

Table 58. BUCKx_MAIN_CR1

7	6	5	4	3	2	1	0
-	VOUT [6:0]						
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

- Address: 0x20/0x25/0x2A
- Default: 0b0XXXXXXX where X depends on the value programmed in the NVM
- Description: BUCK1 to BUCK3 MAIN mode control register 1.

This register is initialized to the default value in the CHECK&LOAD state. The user can write to this register to set the voltage of BUCKx, which is applied to the MAIN mode (see Section 5).

[7]	reserved
[6:0]	VOUT [6:0]: Buck output voltage settings. See Table 18. BUCK output voltage settings. The default value is defined in the VOUT [6:0] bitfield of NVM_BUCKx_VOUT_SHR NVM shadow registers.

6.4.2 BUCKx MAIN mode control register 2 (BUCKx_MAIN_CR2) (x = 1 to 3)

Table 59. BUCKx_MAIN_CR2

7	6	5	4	3	2	1	0
-	-	-	-	-	PREG_MODE [1:0]		EN
R	R	R	R	R	R/W	R/W	R/W

- Address: 0x21/0x26/0x2B
- Default: 0b00000XXX where X depends on the value programmed in NVM
- Description: BUCK1 to BUCK3 MAIN mode control register 2.

This register is initialized to the default value in the CHECK&LOAD state. The user can write to this register to control the enable and regulation modes of BUCKx, which are applied to the MAIN mode (see Section 5).

[7:3]	reserved
[2:1]	**PREG_MODE**: select regulation mode 00: BUCKx operates in normal mode (HP) 01: reserved 10: BUCKx operates in forced PWM mode (CCM) 11: reserved The default value is defined in the BUCKx_PREG_MODE[1:0] bitfield of NVM_BUCK_MODE_SHR1 NVM shadow register.
[0]	**EN**: 0: BUCKx is disabled 1: BUCKx is enabled The default value is defined in the BUCKx_RANK [2:0] bitfield of NVM_RANK_SHR1/2, NVM shadow registers. If BUCKx_RANK [2:0] = 0, BUCKx is disabled at power-up; if BUCKx_RANK [2:0] = y (with 6 > y > 0) BUCKx is enabled at power-up at rank y (see Section 5.2).

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6.4.3 BUCKx ALTERNATE mode control register 1 (BUCKx_ALT_CR1) (x = 1 to 3)

Table 60. BUCKx_ALT_CR1

7	6	5	4	3	2	1	0
-	VOUT [6:0]						
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

- Address: 0x22/0x27/0x2C
- Default: 0b0XXXXXXX where X depends on the value programmed in NVM
- Description: BUCK1 to BUCK3 ALT mode control register 1.

This register is initialized to the default value in the CHECK&LOAD state. The user can write to this register to set the voltage of BUCKx, which is applied to the ALTERNATE mode (see Section 5).

[7]	**reserved**
[6:0]	**VOUT [6:0]**: Buck output voltage settings. See Table 18. The default value is the same as BUCKx_MAIN_CR1.

6.4.4 BUCKx ALTERNATE mode control register 2 (BUCKx_ALT_CR2) (x = 1 to 3)

Table 61. BUCKx_ALT_CR2

7	6	5	4	3	2	1	0
-	-	-	-	-	PREG_MODE [1:0]		EN
R	R	R	R	R	R/W	R/W	R/W

- Address: 0x23/0x28/0x2D
- Default: 0b00000XXX where X depends on the value programmed in NVM
- Description: BUCK1 to BUCK3 ALTERNATE mode control register 2.

This register is initialized to the default value in the CHECK&LOAD state. The user can write to this register to control the enable and regulation modes of BUCKx, which are applied to the ALTERNATE mode (see Section 5).

[7:3]	**reserved**
[2:1]	**PREG_MODE [1:0]**: select regulation mode 00: BUCKx operates in normal mode (HP) 01: reserved 10: BUCKx operates in forced PWM mode (CCM) 11: Reserved The default value is the same as BUCKx_MAIN_CR2.
[0]	**EN**: 0: BUCKx is disabled 1: BUCKx is enabled The default value is the same as BUCKx_MAIN_CR2.

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6.4.5 BUCKx PWRCTRL control register (BUCKx_PWRCTRL_CR) (x = 1 to 3)

Table 62. **BUCKx_PWRCTRL_CR**

7	6	5	4	3	2	1	0
PWRCTRL_DLY_H [1:0]		PWRCTRL_DLY_L [1:0]		PWRCTRL_SEL [1:0]		PWRCTRL_RST	PWRCTRL_EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

- Address: 0x24/0x29/0x2E
- Default: 0x00
- Description: BUCK1 to BUCK3 PWRCTRL control register.

This register is initialized to the default value in the CHECK&LOAD state. The user can write to this register to allocate a PWRCTRL signal for controlling the BUCKx (see Section 5).

[7:6]	**PWRCTRL_DLY_H [1:0]**: BUCKx control/reset source shift delay from low to High level 00: no delay 01: 1.5 ms delay 10: 3 ms delay 11: 6 ms delay
[5:4]	**PWRCTRL_DLY_L [1:0]**: BUCKx control/reset source shift delay from high to Low level 00: no delay 01: 1.5 ms delay 10: 3 ms delay 11: 6 ms delay
[3:2]	**PWRCTRL_SEL[1:0]**: BUCKx control/reset PWRCTRL source selection 00: No control source 01: PWRCTRL1 control source 10: PWRCTRL2 control source 11: PWRCTRL3 control source
[1]	**PWRCTRL_RST**: BUCKx independent reset source enable 0: no effect 1: reset enable (when the selected PWRCTRL source is active, BUCKx is disabled and the BUCKx control registers are reset to the default value. When the selected PWRCTRL source is inactive, BUCKx operates according to BUCKx_MAIN_CR1 / 2. See Table 18).
[0]	**PWRCTRL_EN**: BUCKx control source enable 0: disable (BUCKx operates according to BUCKx_MAIN_CR1 / 2) 1: enable (BUCKx operates according to BUCKx_MAIN_CR1 / 2 or BUCKx_ALT_CR1 / 2 depending on the PWRCTRL selected source. See Table 18).

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6.4.6 GPOx MAIN mode control register (GPOx_MAIN_CR) (x = 1 to 5)

Table 63. **GPOx_MAIN_CR**

7	6	5	4	3	2	1	0
-		-	-	-	-	-	EN
R	R	R	R	R	R	R	R/W

- Address: 0x43/0x46/0x67/0x6A/0x6D
- Default: 0b0000000X where X depends on the value programmed in the NVM
- Description: GPOx MAIN mode control register.

This register is initialized to the default value in the CHECK&LOAD state. The user can write to this register to control enable of GPOx, which is applied to the MAIN mode (see Section 5).

[7:1]	**reserved**
[0]	**EN**: 0: GPOx is disabled 1: GPOx is enabled The default value is defined in the GPOx_RANK [2:0] bitfield of the NVM_GPO_RANK_SHR1/2/3 NVM shadow registers. If GPOx_RANK [2:0] = 0, GPOx is disabled at power-up. If GPOx_RANK [2:0] = y (with 6 > y > 0), GPOx is enabled at power-up at rank y (see Section 5.2).

6.4.7 GPOx ALTERNATE mode control register (GPOx_ALT_CR) (x = 1 to 5)

Table 64. **GPOx_ALT_CR**

7	6	5	4	3	2	1	0
-		-	-	-	-	-	EN
R	R	R	R	R	R	R	R/W

- Address: 0x44/0x47/0x68/0x6B/0x6E
- Default: 0b0000000X where X depends on the value programmed in the NVM
- Description: GPOx ALTERNATE mode control register.

This register is initialized to the default value in the CHECK&LOAD state. The user can write to this register to control enable of GPOx, which is applied to the ALTERNATE mode (see Section 5.4.11).

[7:1]	**reserved**
[0]	**EN**: 0: GPOx is disabled 1: GPOx is enabled The default value is the same as GPOx_MAIN_CR

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6.4.8 GPOx PWRCTRL control register (GPOx_PWRCTRL_CR) (x = 1 to 5)

Table 65. GPOx_PWRCTRL_CR

7	6	5	4	3	2	1	0
PWRCTRL_DLY_H [1:0]		PWRCTRL_DLY_L [1:0]		PWRCTRL_SEL [1:0]		PWRCTRL_RST	PWRCTRL_EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

- Address: 0x45/0x48/0x69/0x6C/0x6F
- Default: 0x00
- Description: GPOx PWRCTRL control register.

This register is initialized to the default value in the CHECK&LOAD state. The user can write to this register to allocate a PWRCTRL signal for controlling the GPOx.

[7:6]	**PWRCTRL_DLY_H [1:0]**: GPOx control/reset source shift delay from low to **H**igh level 00: no delay 01: 1.5 ms delay 10: 3 ms delay 11: 6 ms delay
[5:4]	**PWRCTRL_DLY_L [1:0]**: GPOx control/reset source shift delay from high to **L**ow level 00: no delay 01: 1.5 ms delay 10: 3 ms delay 11: 6 ms delay
[3:2]	**PWRCTRL_SEL [1:0]**: GPOx control/reset PWRCTRL source selection 00: No control source 01: PWRCTRL1 control source 10: PWRCTRL2 control source 11: PWRCTRL3 control source
[1]	**PWRCTRL_RST**: GPOx independent reset source enable 0: no effect 1: reset enable (when the selected PWRCTRL source is active, GPOx is disabled and the GPOx control registers are reset to the default value. When the selected PWRCTRL source is inactive, GPOx operates according to GPOx_MAIN_CR).
[0]	**PWRCTRL_EN**: GPOx control source enable 0: disable (GPOx operates according to GPOx_MAIN_CR1/2) 1: enable (GPOx operates according to GPOx_MAIN_CR or GPOx_ALT_CR depending on the PWRCTRL selected source).

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6.4.9 LDOx MAIN mode control register (LDOx_MAIN_CR) (x = 2/5/6/7)

Table 66. LDOx_MAIN_CR

7	6	5	4	3	2	1	0
-	-	VOUT [4:0]					EN
R	R	R/W	R/W	R/W	R/W	R/W	R/W

- Address: 0x4F/0x58/0x5B/0x5E
- Default: 0b00XXXXXX where X depends on the value programmed in NVM
- Description: LDO2, LDO5, LDO6 and LDO7 MAIN mode control register.

This register is initialized to the default value in the CHECK&LOAD state. The user can write to this register to control enable and set the voltage of the related LDO instance which is applied to the MAIN mode (see Section 5.4)

[7:6]	reserved
[5:1]	**VOUT [4:0]**: LDOx output voltage settings. See Table 17. The default value is defined in the VOUT [4:0] bitfield of NVM_LDOx_SHR NVM shadow registers.
[0]	**EN**: 0: LDOx is disabled 1: LDOx is enabled The default value is defined in the LDOx_RANK [2:0] bitfield of the NVM_RANK_SHR5/7/8 NVM shadow registers. If LDOx_RANK [2:0] = 0, LDOx is disabled at power up; if LDOx_RANK [2:0] = y (with 6 > y > 0) LDOx is enabled at power up at rank y.

6.4.10 LDOx ALTERNATE mode control register (LDOx_ALT_CR) (x = 2/5/6/7)

Table 67. LDOx_ALT_CR

7	6	5	4	3	2	1	0
-	-	VOUT [4:0]					EN
R	R	R/W	R/W	R/W	R/W	R/W	R/W

- Address: 0x50/0x59/0x5C/0x5F
- Default: 0b00XXXXXX where X depends on the value programmed in the NVM
- Description:LDO2/LDO5/LDO6/LDO7 ALTERNATE mode control register.

This register is initialized to the default value in the CHECK&LOAD state. The user can write to this register to control enable and set the voltage of the related LDO instance, which is applied to the ALTERNATE mode (see Section 5).

[7:6]	reserved
[5:1]	**VOUT [4:0]**: LDOx output voltage settings. (See Table 17) The default value is the same as LDOx_MAIN_CR
[0]	**EN**: 0: LDOx is disabled 1: LDOx is enabled The default value is the same as LDOx_MAIN_CR

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6.4.11 LDOx PWRCTRL control register (LDOx_PWRCTRL_CR) (x = 1 to 7)

Table 68. **LDOx_PWRCTRL_CR**

7	6	5	4	3	2	1	0
PWRCTRL_DLY_H [1:0]		PWRCTRL_DLY_L [1:0]		PWRCTRL_SEL [1:0]		PWRCTRL_RST	PWRCTRL_EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

- Address: 0x4E/0x51/0x54/0x57/0x5A/0x5D/0x60
- Default: 0x00
- Description: LDO1 to LDO7 PWRCTRL control register.

This register is initialized to the default value in the CHECK&LOAD state. The user can write to this register to allocate a PWRCTRL signal for controlling the LDOx (see Section 5).

[7:6]	**PWRCTRL_DLY_H [1:0]**: LDOx control/reset source shift delay from low to **H**igh level 00: no delay 01: 1.5 ms delay 10: 3 ms delay 11: 6 ms delay
[5:4]	**PWRCTRL_DLY_L [1:0]**: LDOx control/reset source shift delay from high to **L**ow level 00: no delay 01: 1.5 ms delay 10: 3 ms delay 11: 6 ms delay
[3:2]	**PWRCTRL_SEL[1:0]**: LDOx control/reset PWRCTRL source selection. 00: No control source 01: PWRCTRL1 control source 10: PWRCTRL2 control source 11: PWRCTRL3 control source
[1]	**PWRCTRL_RST**: LDOx independent reset source enable 0: no effect 1: reset enable (when the selected PWRCTRL source is active, LDOx is disabled and LDOx control registers are reset to the default value. When the selected PWRCTRL source is inactive, LDOx operates according to LDOx_MAIN_CR. See Section 5.4.11).
[0]	**PWRCTRL_EN**: LDOx control source enable 0: disable (LDOx operates according to LDOx_MAIN_CR) 1: enable (LDOx operates according to LDOx_MAIN_CR or LDOx_ALT_CR depending on the PWRCTRL selected source. See Section 5.4.11).

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6.4.12 LDO3 MAIN mode control register (LDO3_MAIN_CR)

Table 69. LDO3_MAIN_CR

7	6	5	4	3	2	1	0
SNK_SRC	-	VOUT [4:0]					EN
R/W	R	R/W	R/W	R/W	R/W	R/W	R/W

- Address: 0x52
- Default: 0bX0XXXXXX where X depends on the value programmed in the NVM
- Description: LDO3 MAIN mode control register.

This register is initialized to the default value in the CHECK&LOAD state. The user can write to this register to control enable and SNK_SRC mode, and set the voltage of LDO3, which is applied to the MAIN mode (see Section 5).

[7]	**SNK_SRC**: select sink/source mode operation (see Section 4.2.2). 0: LDO3 operates in normal mode 1: LDO3 operates in sink/source mode The default value is defined by the SNK_SRC bit of the NVM_LDO3_SHR NVM shadow register
[6]	**reserved**
[5:1]	**VOUT [4:0]**: LDO3 output voltage settings. Table 17 The default value is defined in the VOUT [4:0] bit field of the NVM_LDO3_SHR NVM shadow registers
[0]	**EN**: 0: LDO3 is disabled 1: LDO3 is enabled The default value is defined in the LDO3_RANK [2:0] bitfield of the NVM_RANK_SHR6 NVM shadow registers. If LDO3_RANK [2:0] = 0, LDO3 is disabled at power-up; if LDO3_RANK = y, LDO3 is enabled at power-up at rank y.

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6.4.13 LDO3 ALTERNATE mode control register (LDO3_ALT_CR)

Table 70. LDO3_ALT_CR

7	6	5	4	3	2	1	0
SNK_SRC	-	VOUT [4:0]					EN
R/W	R	R/W	R/W	R/W	R/W	R/W	R/W

- Address: 0x53
- Default: 0bX0XXXXXX where X depends on the value programmed in the NVM
- Description: LDO3 ALTERNATE mode control register.

This register is initialized to the default value in the CHECK&LOAD state. The user can write to this register to control enable or SNK_SRC mode and set the voltage of LDO3, which is applied to the ALTERNATE mode (see Section 5).

[7]	**SNK_SRC**: select sink/source mode operation (see Section 4.2.2) 0: LDO3 operates in sink/source mode 1: LDO3 operates in sink/source mode The default value is the same as LDO3_MAIN_CR
[6]	**reserved**
[5:1]	**VOUT [4:0]**: LDO3 output voltage settings. See Table 17. The default value is the same as LDO3_MAIN_CR
[0]	**EN**: 0: LDO3 is disabled 1: LDO3 is enabled The default value is the same as LDO3_MAIN_CR

6.4.14 LDO1/4 MAIN mode control register (LDO1/4_MAIN_CR) (x = 1/4)

Table 71. LDO1/4_MAIN_CR

7	6	5	4	3	2	1	0
-		-	-	-	-	-	EN
R	R	R	R	R	R	R	R/W

- Address: 0x4C/0x55
- Default: 0b0000000X where X depends on the value programmed in the NVM
- Description: LDO1/4 MAIN mode control register.

This register is initialized to the default value in the CHECK&LOAD state. The user can write to this register to control enable or to force the power input source of LDO1/4 , which is applied to the MAIN mode (see Section 5).

[7:1]	**reserved**
[0]	**EN**: 0: LDO1/4 is disabled 1: LDO1/4 is enabled The default value is defined in the LDO1/4 _RANK[2:0] bitfield of the NVM_RANK_SHR5/6 NVM shadow registers. If LDO1/4 _RANK[2:0] = 0, LDO1/4 is disabled at power-up.

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6.4.15 LDO1/4 ALTERNATE mode control register (LDO1/4_ALT_CR)

Table 72. LDO4_ALT_CR

7	6	5	4	3	2	1	0
-		-	-	-	-	-	EN
R	R	R	R	R	R	R	R/W

- Address: 0x4D/0x56
- Default: 0b0000000X where X depends on the value programmed in the NVM
- Description: LDO1/4 ALTERNATE mode control register.

This register is initialized to the default value in the CHECK&LOAD state. The user can write to this register to control enable or to force the power input source of LDO1/4, which is applied to the ALTERNATE mode (see Section 5).

[7:1]	**reserved**
[0]	**EN**: 0: LDO1/4 is disabled 1: LDO1/4 is enabled The default value is the same as LDO1/4_MAIN_CR

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6.5 Interrupt registers

6.5.1 Interrupt management overview

Interrupts are probed in the POWER_ON state only. All interrupts are masked by default. All interrupt registers are reset to the default value if RSTn is asserted.

INT_PENDING_Rx

- Stores events of interrupt sources, regardless of interrupt masking.
- Corresponding bits are kept set until they are cleared (using INT_CLEAR_Rx registers).

INT_CLEAR_Rx

- Setting a bit in these registers clears the corresponding pending bit in the INT_PENDING_Rx registers. A bit in the INT_PENDING_Rx registers can be cleared only if the corresponding interrupt source disappears. Alternatively, the bit stays set after being cleared. In the case of the INT_PENDING_Rx bit generated by edge triggering, it can be directly deleted without checking the INT_SOURCE_RX.

INT_MASK_Rx

- Clearing a bit in these registers unmasks the corresponding interrupt.
- The INTn pin is forced low as long as the corresponding interrupt bit is set in INT_PENDING_Rx.

INT_SOURCE_Rx

- These registers provide the actual state of interrupt sources.
- If an interrupt source is present, the corresponding bit is set. If the interrupt source disappears, the corresponding bit is cleared.

INT_DBG_LATCH_Rx

Setting a bit in these registers emulates the corresponding interrupt event. These registers aim to test and to debug the application processor software interrupt handler.

6.5.2 Interrupt pending register 1 (INT_PENDING_R1)

Table 73. INT_PENDING_R1

7	6	5	4	3	2	1	0
-	-	VINLOW_RI	VINLOW_FA	-	-	PKEY_RI	PKEY_FA
R	R	R	R	R	R	R	R

- Address: 0x70
- Default: 0x00
- Description: Interrupt pending register 1 (see Interrupt registers). This register is reset to the default value if RSTn is asserted. For all bits:

0: interrupt not pending

1: interrupt pending

[7:6]	**reserved**
[5]	**VINLOW_RI**: Voltage on the VIN pin falls below the VINLOW_Rise threshold
[4]	**VINLOW_FA**: Voltage on the VIN pin rises above the VINLOW_Fall threshold
[3:2]	**reserved**
[1]	**PKEY_RI**: PONKEYn rising edge
[0]	**PKEY_FA**: PONKEYn falling edge

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6.5.3 Interrupt pending register 2 (INT_PENDING_R2)

Table 74. **INT_PENDING_R2**

7	6	5	4	3	2	1	0
-	-	-	-	-	-	THW_RI	THW_FA
R	R	R	R	R	R	R	R

- Address: 0x71
- Default: 0x00
- Description: Interrupt pending register 2 (see Interrupt registers). This register is reset to the default value as long as RSTn is asserted. For all bits:

0: interrupt not pending

1: interrupt pending

[7:2]	reserved
[1]	**THW_RI**: Temperature rises above the TWRN_Rise threshold
[0]	**THW_FA**: Temperature falls below the TWRN_Fall threshold

6.5.4 Interrupt pending register 3 (INT_PENDING_R3)

Table 75. **INT_PENDING_R3**

7	6	5	4	3	2	1	0
-	-	-	-	-	BUCK3_OCP	BUCK2_OCP	BUCK1_OCP
R	R	R	R	R	R	R	R

- Address: 0x72
- Default: 0x00
- Description: Interrupt pending register 3 (see Interrupt registers). This register is reset to the default value if RSTn is asserted. For all bits:

0: interrupt not pending

1: interrupt pending

[7:2]	**reserved**
[2]	**BUCK3_OCP**: Overcurrent detected on BUCK3
[1]	**BUCK2_OCP**: Overcurrent detected on BUCK2
[0]	**BUCK1_OCP**: Overcurrent detected on BUCK1

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6.5.5 Interrupt pending register 4 (INT_PENDING_R4)

Table 76. INT_PENDING_R4

7	6	5	4	3	2	1	0
-	LDO7_OCP	LDO6_OCP	LDO5_OCP	LDO4_OCP	LDO3_OCP	LDO2_OCP	LDO1_OCP
R	R	R	R	R	R	R	R

- Address: 0x73
- Default: 0x00
- Description: Interrupt mask register 1 to 4 (see Interrupt registers). This register is reset to the default value if RSTn is asserted. For all bits:

0: interrupt not pending

1: interrupt pending

[7]	**reserved**
[6]	**LDO7_OCP**: Overcurrent detected on LDO7
[5]	**LDO6_OCP**: Overcurrent detected on LDO6
[4]	**LDO5_OCP**: Overcurrent detected on LDO5
[3]	**LDO4_OCP**: Overcurrent detected on LDO4
[2]	**LDO3_OCP**: Overcurrent detected on LDO3
[1]	**LDO2_OCP**: Overcurrent detected on LDO2
[0]	**LDO1_OCP**: Overcurrent detected on LDO1

6.5.6 Interrupt clear registers (INT_CLEAR_Rx) (x = 1 to 4)

Table 77. INT_CLEAR_Rx

7	6	5	4	3	2	1	0
Same as INT_PENDING_Rx							
W/R0	W/R0	W/R0	W/R0	W/R0	W/R0	W/R0	W/R0

- Address: 0x74/0x75/0x76/0x77
- Default: 0x00
- Description: Interrupt clear registers 1 to 4 (see Interrupt registers).

Writing 1 clears the corresponding interrupt bit in INT_PENDING_Rx.

The bit is self-cleared, and always reads 0.

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6.5.7 Interrupt mask registers (INT_MASK_Rx) (x = 1 to 4)

Table 78. INT_MASK_Rx

7	6	5	4	3	2	1	0
Same as INT_PENDING_Rx							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

- Address: 0x78/0x79/0x7A/0x7B
- Default: 0xFF
- Description: Interrupt mask registers 1 to 4 (see Interrupt registers).

Writing 0 unmasks the corresponding interrupt bit in INT_PENDING_Rx. These registers are reset to the default value if RSTn is asserted.

For all bits:

0: interrupt is unmasked

1: interrupt is masked

6.5.8 Interrupt source registers (INT_SRC_Rx) (x = 1 to 4)

Table 79. INT_SRC_Rx

7	6	5	4	3	2	1	0
Same as INT_PENDING_Rx							
R	R	R	R	R	R	R	R

- Address: 0x7C/0x7D/0x7E/0x7F
- Default: 0xXX where X depends on the actual state of interrupt sources
- Description: Interrupt source registers 1 to 4 (see Interrupt registers).

For all bits:

0: interrupt source is not present

1: interrupt source is present

6.5.9 Interrupt debug latch registers (INT DBG LATCH Rx) (x = 1 to 4)

Table 80. INT_DBG_LATCH_Rx

7	6	5	4	3	2	1	0
Same as INT_PENDING_Rx							
W/R0	W/R0	W/R0	W/R0	W/R0	W/R0	W/R0	W/R0

- Address: 0x80/0x81/0x82/0x83
- Default: 0x00
- Description: Interrupt debug latch registers 1 to 4 (see Interrupt registers).

Setting a bit emulates the corresponding interrupt event. The bit is self-cleared, and always reads 0.

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6.6 NVM register

6.6.1 NVM status register (NVM_SR)

Table 81. **NVM_SR**

7	6	5	4	3	2	1	0
-	-	-	-	-	-	NVM_WRITE_FAIL	NVM_BUSY
R	R	R	R	R	R	R	R

- Address: 0x8E
- Default: 0x00
- Description: NVM status register.

[7:2]	**reserved**
[1]	**NVM_WRITE_FAIL**: Error in writing to the NVM. The LOCK_NVM bit is set. 0: Write is successful or no write operation done 1: Write to the NVM failed
[0]	**NVM_BUSY**: NVM controller status 0: NVM controller is in an idle state 0: NVM controller is in an idle state 1: NVM controller is in a busy state Self-cleared when the operation is completed

6.6.2 NVM control register (NVM_CR)

Table 82. **NVM_CR**

7	6	5	4	3	2	1	0
-	-	-	-	-	-	NVM_CMD[1:0]	
R	R	R	R	R	R	R/W	R/W

- Address: 0x8F
- Default: 0x00
- Description: NVM control register.

[7:2]	**reserved**
[1:0]	**NVM_CMD[1:0]**: NVM controller command bits to control the NVM operation on the NVM shadow register bits. 00: No operation 01: Program (write shadow register to the NVM) 10: Read (load NVM content into shadow register) 11: No operation Self-cleared when the operation is completed.

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6.7 NVM shadow registers

All NVM shadow registers are reloaded from the NVM content in the INIT&LOAD state and in the CHECK&LOAD state. Then mirror registers or mirror bit fields are set to the default value.

6.7.1 NVM main control shadow register 1 (NVM_MAIN_CTRL_SHR1)

Table 83. **NVM_MAIN_CTRL_SHR1**

7	6	5	4	3	2	1	0
VINOK_HYST[1:0]		VINOK_RISE[1:0]		NVM_WDG_TMR_SET[1:0]		NVM_WDG_EN	AUTO_TURN_ON
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

- Address: 0x90
- Default: Depends on the PMIC part number
- Description: NVM main control shadow register 1.

[7:6]	**VINOK_HYST[1:0]**: VINOK_HYST threshold voltage 00: 200 mV 01: 300 mV 10: 400 mV 11: 500 mV
[5:4]	**VINOK_RISE[1:0]**: VINOK_Rise threshold voltage 00: 3.1 V 01: 3.3 V 10: 3.5 V 11: 4.0 V
[3:2]	**NVM_WDG_TMR_SET [1:0]**: watchdog timer duration default value 00: 10 s 01: 20 s 10: 50 s 11: 100 s
[1]	**NVM_WDG_EN**: watchdog default value 0: Watchdog is disabled 1: Watchdog is enabled
[0]	**AUTO_TURN_ON**: 0: PMIC does not start automatically on VIN rising 1: PMIC starts automatically on VIN rising *Note: It is ignored if PKEY_EN_CFG is set to '1'.*

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6.7.2 NVM main control shadow register 2 (NVM_MAIN_CTRL_SHR2)

Table 84. NVM_MAIN_CTRL_SHR2

7	6	5	4	3	2	1	0
RANK_DLY[1:0]		RST_DLY[1:0]		NVM_PKEY_LKP_OFF	NVM_PKEY_LKP_EN_FSLS	NVM_PKEY_LKP_TMR[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: 0x91
Default: Depends on the PMIC part number
Description: NVM main control shadow register 2.

[7:6]	**RANK_DLY[1:0]**: Power-up/power-down step (RANK) duration: 00: 1.5 ms 01: 3 ms 10: 4.5 ms 11: 6 ms (see Section 5.4.15)
[5:4]	**RST_DLY[1:0]**: RST release delay after POWER_UP sequence: 00: no delay 01: 1.5 ms 10: 3 ms 11: 6 ms (see Section 5.4.15)
[3]	**NVM_PKEY_LKP_OFF**: PONKEYn long key press turn-off condition default value (see Section 5.4.7) 0: no effect 1: A PONKEYn long key press triggers a turn-off condition *Note: This bit is valid only if PONKEYn is selected (PKEY_EN_CFG = 0)*
[2]	**NVM_PKEY_LKP_EN_FSLS**[CJ1] : PONKEYn long key press / EN (Enable) fail-safe lock state skipping default value (see Section 5.4.10) 0: no effect 1: A PONKEYn long key press or Enable allows the PMIC to go from the FAIL_SAFE_LOCK state to the OFF state
[1:0]	**NVM_PKEY_LKP_TMR[1:0]**: PONKEYn long key press timer duration default value 00: 2 s 01: 5 s 10: 10 s 11: 15 s *Note: Those bits are valid only if PONKEYn is selected (PKEY_EN_CFG = 0)*

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6.7.3 NVM rank shadow register 1 (NVM_RANK_SHR1)

Table 85. **NVM_RANK_SHR1**

7	6	5	4	3	2	1	0
-	-	BUCK2_RANK[2:0]			BUCK1_RANK[2:0]		
R	R	R/W	R/W	R/W	R/W	R/W	R/W

- Address: 0x92
- Default: Depends on the PMIC part number
- Description: NVM rank shadow register 1 (see Table 1).

[7:6]	reserved
[5:3]	**BUCK2_RANK[2:0]**: 000: rank0 001: rank1 010: rank2 011: rank3 100: rank4 101: rank5 110: rank0 111: rank0
[2:0]	**BUCK1_RANK[2:0]**: 000: rank0 001: rank1 010: rank2 011: rank3 100: rank4 101: rank5 110: rank0 111: rank0

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6.7.3.1 NVM rank shadow register 2 (NVM_RANK_SHR2)

Table 86. **NVM_RANK_SHR2**

7	6	5	4	3	2	1	0
-	-	-	-	-	BUCK3_RANK[2:0]		
R	R	R	R	R	R/W	R/W	R/W

- Address: 0x93
- Default: Depends on the PMIC part number
- Description: NVM rank shadow register 2 (see Table 1).

[7:3]	reserved
[2:0]	**BUCK3_RANK[2:0]**: 000: rank0 001: rank1 010: rank2 011: rank3 100: rank4 101: rank5 110: rank0 111: rank0

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6.7.4 NVM rank shadow register 5 (NVM_RANK_SHR5)

Table 87. **NVM_RANK_SHR5**

7	6	5	4	3	2	1	0
-	-	LDO2_RANK[2:0]			LDO1_RANK[2:0]		
R	R	R/W	R/W	R/W	R	R	R

Address: 0x96
Default: Depends on the PMIC part number
Description: NVM rank shadow register 5 (see Table 1).

[7:6]	reserved
[5:3]	**LDO2_RANK[2:0]**: 000: rank0 001: rank1 010: rank2 011: rank3 100: rank4 101: rank5 110: rank0 111: rank0
[2:0]	**LDO1 RANK[2:0]**: 000: rank0 001: rank1 010: rank2 011: rank3 100: rank4 101: rank5 110: rank0 111: rank0

6.7.5 NVM rank shadow register 6 (NVM_RANK_SHR6)

Table 88. **NVM_RANK_SHR6**

7	6	5	4	3	2	1	0
-	-	LDO4_RANK[2:0]			LDO3_RANK[2:0]		
R	R	R/W	R/W	R/W	R/W	R/W	R/W

Address: 0x97
Default: Depends on the PMIC part number
Description: NVM rank shadow register 6 (see Table 1).
Same bit field as Table 87

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6.7.6 NVM rank shadow register 7 (NVM_RANK_SHR7)

Table 89. NVM_RANK_SHR7

7	6	5	4	3	2	1	0
-	-	LDO6_RANK[2:0]			LDO5_RANK[2:0]		
R	R	R/W	R/W	R/W	R/W	R/W	R/W

Address: 0x98
Default: Depends on the PMIC part number
Description: NVM rank shadow register 7.
Same bit field as Table 87.

6.7.7 NVM rank shadow register 8 (NVM_RANK_SHR8)

Table 90. NVM_RANK_SHR8

7	6	5	4	3	2	1	0
-	-	-	-	-	LDO7_RANK[2:0]		
R	R	R/W	R/W	R/W	R	R	R

Address: 0x99
Default: Depends on the PMIC part number
Description: NVM rank shadow register 8 (see Table 1).

[7:3]	reserved
[2:0]	**LD07_RANK[2:0]**: 000: rank0 001: rank1 010: rank2 011: rank3 100: rank4 101: rank5 110: rank0 111: rank0

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6.7.8 NVM BUCK mode shadow register 1 (NVM_BUCK_MODE_SHR1)

Table 91. NVM_BUCK_MODE_SHR1

7	6	5	4	3	2	1	0
-	-	BUCK3_PREG_MODE[1:0]		BUCK2_PREG_MODE[1:0]		BUCK1_PREG_MODE[1:0]	
R	R	R/W		R/W		R/W	

- Address: 0x9A
- Default: Depends on the PMIC part number
- Description: NVM BUCK mode shadow register 1 (see Table 1).

[7:6]	**reserved**
[5:4]	**BUCK3_PREG_MODE[1:0]:** 00: BUCK3 operates in high-power mode (HP) 01: reserved 10: BUCK3 operates in forced PWM mode (CCM) 11: reserved
[3:2]	**BUCK2_PREG_MODE[1:0]:** 00: BUCK2 operates in high-power mode (HP) 01: reserved 10: BUCK2 operates in forced PWM mode (CCM) 11: reserved
[1:0]	**BUCK1_PREG_MODE[1:0]:** 00: BUCK1 operates in high-power mode (HP) 01: reserved 10: BUCK1 operates in forced PWM mode (CCM) 11: reserved

6.7.9 NVM BUCK1 output voltage shadow register (NVM_BUCK1_VOUT_SHR)

Table 92. NVM_BUCK1_VOUT_SHR

7	6	5	4	3	2	1	0
BUCK1_VRANGE_CFG	VOUT[6:0]						
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

- Address: 0x9C
- Default: Depends on the PMIC part number
- Description: NVM BUCK1 output voltage shadow registers.

The contents of these registers are copied into BUCK1_MAIN_CR1 and BUCK1_ALT_CR1 in the CHECK&LOAD state (see Table 18).

[7]	**BUCK1_VRANGE_CFG:** BUCK1 range voltage setting 1: High Voltage Range 0: Low Voltage Range
[6:0]	**VOUT[6:0]:** BUCK1 default output voltage settings. See Table 1

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6.7.10 NVM BUCK2 output voltage shadow register (NVM_BUCK2_VOUT_SHR)

Table 93. NVM_BUCK2_VOUT_SHR

7	6	5	4	3	2	1	0
-	VOUT[6:0]						
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

- Address: 0x9D
- Default: Depends on the PMIC part number
- Description: NVM BUCK2 output voltage shadow registers.

The contents of these registers are copied into BUCK2_MAIN_CR1 and BUCK2_ALT_CR1 in the CHECK&LOAD state (see Table 18).

[7]	reserved
[6:0]	**VOUT[6:0]:** BUCK2 default output voltage settings. See Table 1. .Default configuration table.

6.7.11 NVM BUCK3 output voltage shadow register (NVM_BUCK3_VOUT_SHR)

Table 94. NVM_BUCK3_VOUT_SHR

7	6	5	4	3	2	1	0
-	VOUT[6:0]						
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

- Address: 0x9E
- Default: Depends on the PMIC part number
- Description: NVM BUCK3 output voltage shadow registers.

The contents of these registers are copied into BUCK3_MAIN_CR1 and BUCK3_ALT_CR1 in the CHECK&LOAD state (see Table 18).

[7]	reserved
[6:0]	**VOUT[6:0]:** BUCK3 default output voltage settings. See Table 1.

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6.7.12 NVM GPO Config shadow register (NVM_GPO_CONFIG_SHR)

Table 95. **NVM_GPO_CONFIG_SHR**

7	6	5	4	3	2	1	0
-	-	-	GPO5_PWRCTRL_POL	GPO4_PWRCTRL_POL	GPO3_PWRCTRL_POL	GPO2_PWRCTRL_POL	GPO1_PWRCTRL_POL
R	R	R	R/W	R/W	R/W	R/W	R/W

- Address: 0x9F
- Default: Depends on the PMIC part number
- Description: GPO config shadow register.

[7:5]	**reserved**
[4]	**GPO5_POL:**GPO5 polarity configuration 0: GPO5 is active high 1: GPO5 is active low
[3]	**GPO4_POL:** GPO4 polarity configuration 0: GPO4 is active high 1: GPO4 is active low
[2]	**GPO3_POL:** GPO3 polarity configuration 0: GPO3 is active high 1: GPO3 is active low
[1]	**GPO2_POL:** GPO2 polarity configuration 0: GPO2 is active high 1: GPO2 is active low
[0]	**GPO1_POL:** GPO1 polarity configuration 0: GPO1 is active high 1: GPO1 is active low

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6.7.13 NVM GPO Rank shadow register 1 (NVM_GPO_RANK_SHR1)

Table 96. NVM_GPO_RANK_SHR1

7	6	5	4	3	2	1	0
-	-	GPO2_RANK[2:0]			GPO1_RANK[2:0]		
R	R	R/W	R/W	R/W	R/W	R/W	R/W

- Address: 0xA0
- Default: Depends on the PMIC part number
- Description: GPO Rank shadow register 1 (see Table 1).

[7:6]	reserved
[5:3]	**GPO2_RANK[2:0]:** 000: rank0 001: rank1 010: rank2 011: rank3 100: rank4 101: rank5 110: rank0 111: rank0
[2:0]	**GPO1_RANK[2:0]:** 000: rank0 001: rank1 010: rank2 011: rank3 100: rank4 101: rank5 110: rank0 111: rank0

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6.7.14 NVM GPO Rank shadow register 2 (NVM_GPO_RANK_SHR2)

Table 97. **NVM_GPO_RANK_SHR2**

7	6	5	4	3	2	1	0
-	-	GPO4_RANK[2:0]			GPO3_RANK[2:0]		
R	R	R/W	R/W	R/W	R/W	R/W	R/W

- Address: 0xA1
- Default: Depends on the PMIC part number.
- Description: GPO Rank shadow register 2 (see Table 1).

[7:6]	reserved
[5:3]	**GPO4_RANK[2:0]:** 000: rank0 001: rank1 010: rank2 011: rank3 100: rank4 101: rank5 110: rank0 111: rank0
[2:0]	**GPO3_RANK3[2:0]:** 000: rank0 001: rank1 010: rank2 011: rank3 100: rank4 101: rank5 110: rank0 111: rank0

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6.7.15 NVM GPO Rank shadow register 3 (NVM_GPO_RANK_SHR3)

Table 98. NVM_GPO_RANK_SHR3

7	6	5	4	3	2	1	0
-	-	-	-	-	GPO5_RANK[2:0]		
R	R	R	R	R	R/W	R/W	R/W

- Address: 0xA2
- Default: Depends on the PMIC part number.
- Description: GPO Rank shadow register 3 (see Table 1).

[7:3]	reserved
[2:0]	**GPO5_RANK[2:0]:** 000: rank0 001: rank1 010: rank2 011: rank3 100: rank4 101: rank5 110: rank0 111: rank0

6.7.16 NVM LDOx shadow register (NVM_LDOx_SHR) (x = 2/5/6/7)

Table 99. NVM_LDOx_SHR

7	6	5	4	3	2	1	0
-	-	VOUT[4:0]					-
R	R	R/W	R/W	R/W	R/W	R/W	R

- Address:0xA3/A5 to 0xA7
- Default: Depends on the PMIC part number
- Description: NVM LDO2/LDO5/LDO6/LDO7 output voltage shadow registers.

The contents of these registers are copied into LDOx_MAIN_CR and LDOx_ALT_CR in the CHECK&LOAD state (see Section 5.1.2.4).

[7:6]	**reserved**
[5:1]	**VOUT[4:0]**: LDOx default output voltage settings. See Table 1.
[0]	**reserved**

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6.7.17 NVM LDO3 control shadow register (NVM_LDO3_SHR)

Table 100. NVM_LDO3_SHR

7	6	5	4	3	2	1	0
NVM_SNK_SRC	-	VOUT[4:0]					-
R/W	R	R/W	R/W	R/W	R/W	R/W	R

- Address: 0xA4
- Default: Depends on the PMIC part number
- Description: NVM LDO3 control shadow register.

The content of this register is copied into LDO3_MAIN_CR and LDO3_ALT_CR in the CHECK&LOAD state (see Section 5.1.2.4).

[7]	**NVM_SNK_SRC:** Select default sink/source mode operation. 0: LDO3 operates in normal mode by default 1: LDO3 operates in sink/source mode by default
[6]	**reserved**
[5:1]	**VOUT[4:0]**: LDOx default output voltage settings. See Table 1.
[0]	**reserved**

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6.7.18 NVM pull-down control shadow register 1 (NVM_PD_SHR1)

Table 101. NVM_PD_SHR1

7	6	5	4	3	2	1	0
-	-	NVM_BUCK3_PD[1:0]		NVM_BUCK2_PD[1:0]		NVM_BUCK1_PD[1:0]	
R	R	R	R/W	R/W	R/W	R/W	R/W

- Address: 0xA9
- Default: Depends on the PMIC part number
- Description: NVM pull-down control shadow register 1.

The content of this register is copied into BUCKS_PD_CR in the INIT&LOAD and the CHECK&LOAD states.

[7:6]	**reserved**
[5:4]	**NVM_BUCK3_PD[1:0]**: BUCK3 pull-down selection. 00: no pull-down 01: slow pull-down active when BUCK3 is disabled (EN = 0) 10: fast pull-down active when BUCK3 is disabled (EN = 0) 11: slow pull-down forced active
[3:2]	**NVM_BUCK2_PD[1:0]**: BUCK2 pull-down selection. 00: no pull-down 01: slow pull-down active when BUCK2 is disabled (EN = 0) 10: fast pull-down active when BUCK2 is disabled (EN = 0) 11: slow pull-down forced active
[1:0]	**NVM_BUCK1_PD[1:0]**: BUCK1 pull-down selection. 00: no pull-down 01: slow pull-down active when BUCK1 is disabled (EN = 0) 10: fast pull-down active when BUCK1 is disabled (EN = 0) 11: slow pull-down forced active

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6.7.19 NVM pull-down control shadow register 3 (NVM_PD_SHR3)

Table 102. **NVM_PD_SHR3**

7	6	5	4	3	2	1	0
-	NVM_LDO7_PD	NVM_LDO6_PD	NVM_LDO5_PD	NVM_LDO4_PD	NVM_LDO3_PD	NVM_LDO2_PD	NVM_LDO1_PD
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

- Address: 0xAB
- Default: Depends on the PMIC part number
- Description: NVM pull-down control shadow register 3.

The content of this register is copied into LDOS_PD_CR in the INIT&LOAD and the CHECK&LOAD states.

[7]	**reserved**
[6]	**NVM_LDO7_PD**: 0: no pull-down 1: pull-down active when LDO7 is disabled (EN = 0)
[5]	**NVM_LDO6_PD**: 0: no pull-down 1: pull-down active when LDO6 is disabled (EN = 0)
[4]	**NVM_LDO5_PD**: 0: no pull-down 1: pull-down active when LDO5 is disabled (EN = 0)
[3]	**NVM_LDO4_PD**: 0: no pull-down 1: pull-down active when LDO4 is disabled (EN = 0)
[2]	**NVM_LDO3_PD**: 0: no pull-down 1: pull-down active when LDO3 is disabled (EN = 0)
[1]	**NVM_LDO2_PD**: 0: no pull-down 1: pull-down active when LDO2 is disabled (EN = 0)
[0]	**NVM_LDO1_PD**: 0: no pull-down 1: pull-down active when LDO1 is disabled (EN =0)

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6.7.20 NVM BUCKs output current limitation shadow register 1 (NVM_BUCKS_IOUT_SHR1)

Table 103. NVM_BUCKS_IOUT_SHR1

7	6	5	4	3	2	1	0
-	-	BUCK3_ILIM[1:0]		BUCK2_ILIM[1:0]		BUCK1_ILIM[1:0]	
R	R	R/W	R/W	R/W	R/W	R/W	R/W

- Address: 0xAC
- Default: Depends on the PMIC part number
- Description: NVM BUCKs output current limitation shadow register 1.

[7:6]	**reserved**
[5:4]	**BUCK3_ILIM [1:0]**: output current limitation 00: 500 mA 01: 1000 mA 10: 1500 mA 11: 2000 mA
[3:2]	**BUCK2_ILIM[1:0]**: output current limitation 00: 500 mA 01: 1000 mA 10: 1500 mA 11: 2000 mA
[1:0]	**BUCK1_ILIM[1:0]**: output current limitation 00: 500 mA 01: 1000 mA 10: 1500 mA 11: 2000 mA

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6.7.21 NVM BUCKs output current limitation shadow register 2 (NVM_BUCKS_IOUT_SHR2)

Table 104. **NVM_BUCKS_IOUT_SHR2**

7	6	5	4	3	2	1	0
HICCUP_DLY[1:0]		-	-	-	-	-	-
R/W	R/W	R	R	R	R	R	R

- Address: 0xAD
- Default: Depends on the PMIC part number
- Description: NVM BUCKs output current limitation shadow register 2.

[7:6]	**HICCUP_DLY[1:0]**: output current limitation 00: 0 ms 01: 100 ms 10: 500 ms 11: 1000 ms
[5:0]	**reserved**

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6.7.22 NVM LDOs output current limitation shadow register (NVM_LDOS_IOUT_SHR)

Table 105. **NVM_LDOS_IOUT_SHR**

7	6	5	4	3	2	1	0
LDO7_ILIM[1:0]		LDO6_ILIM[1:0]		LDO5_ILIM[1:0]		LDO2_ILIM[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

- Address: 0xAE
- Default: Depends on the PMIC part number
- Description: NVM LDOs output current limitation shadow register.

[7:6]	**LDO7_ILIM**[1:0] :output current limitation 00: 50 mA 01: 100 mA 10: 200 mA 11: 400 mA
[5:4]	**LDO6_ILIM[1:0]**: output current limitation 00: 50 mA 01: 100 mA 10: 200 mA 11: 400 mA
[3:2]	**LDO5_ILIM[1:0]**: output current limitation 00: 50 mA 01: 100 mA 10: 200 mA 11: 400 mA
[1:0]	**LDO2_ILIM[1:0]**: output current limitation 00: 50 mA 01: 100 mA 10: 200 mA 11: 400 mA

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6.7.23 NVM fail-safe overcurrent protection shadow register 1 (NVM_FS_OCP_SHR1)

Table 106. NVM_FS_OCP_SHR1

7	6	5	4	3	2	1	0
-	-	-	-	-	NVM_FS_OCP_BUCK3	NVM_FS_OCP_BUCK2	NVM_FS_OCP_BUCK1
R	R	R	R	R	R/W	R/W	R/W

- Address: 0xAF
- Default: Depends on the PMIC part number
- Description: NVM fail-safe overcurrent protection shadow register 1 (see Section 5.4.7.1

[7:3]	**reserved**
[2]	**NVM_FS_OCP_BUCK3**: BUCK3 OCP management mode selection. 0: OCP Hiccup mode (Level 0) 1: OCP fail-safe PMIC turn-off (Level 1)
[1]	**NVM_FS_OCP_BUCK2**: BUCK2 OCP management mode selection. 0: OCP Hiccup mode (Level 0) 1: OCP fail-safe PMIC turn-off (Level 1)
[0]	**NVM_FS_OCP_BUCK1**: BUCK1 OCP management mode selection. 0: OCP Hiccup mode (Level 0) 1: OCP fail-safe PMIC turn-off (Level 1)

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6.7.24 NVM fail-safe overcurrent protection shadow register 2 (NVM_FS_OCP_SHR2)

Table 107. **NVM_FS_OCP_SHR2**

7	6	5	4	3	2	1	
-	NVM_FS_OCP_LDO7	NVM_FS_OCP_LDO6	NVM_FS_OCP_LDO5	NVM_FS_OCP_LDO4	NVM_FS_OCP_LDO3	NVM_FS_OCP_LDO2	NVM_
R/W	R/W	R/W	R/W	R/W	R/W	R/W	

- Address: 0xB0
- Default: Depends on the PMIC part number
- Description: NVM fail-safe overcurrent protection shadow register 2 (see Section 5.4.17).

[7]	**reserved**
[6]	**NVM_FS_OCP_LDO7**: LDO7 OCP management mode selection. 0: OCP Hiccup mode (Level 0) 1: OCP fail-safe PMIC turn-off (Level 1)
[5]	**NVM_FS_OCP_LDO6**: LDO6 OCP management mode selection. 0: OCP Hiccup mode (Level 0) 1: OCP fail-safe PMIC turn-off (Level 1)
[4]	**NVM_FS_OCP_LDO5**: LDO5 OCP management mode selection. 0: OCP Hiccup mode (Level 0) 1: OCP fail-safe PMIC turn-off (Level 1)
[3]	**NVM_FS_OCP_LDO4**: LDO4 OCP management mode selection. 0: OCP Hiccup mode (Level 0) 1: OCP fail-safe PMIC turn-off (Level 1)
[2]	**NVM_FS_OCP_LDO3**: LDO3 OCP management mode selection. 0: OCP Hiccup mode (Level 0) 1: OCP fail-safe PMIC turn-off (Level 1)
[1]	**NVM_FS_OCP_LDO2**: LDO2 OCP management mode selection. 0: OCP Hiccup mode (Level 0) 1: OCP fail-safe PMIC turn-off (Level 1)
[0]	**NVM_FS_OCP_LDO1**:LDO1 OCP management mode selection. 0: OCP Hiccup mode (Level 0) 1: OCP fail-safe PMIC turn-off (Level 1)

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6.7.25 NVM fail-safe shadow register 1 (NVM_FS_SHR1)

Table 108. **NVM_FS_SHR1**

7	6	5	4	3	2	1	0
VIN_FLT_CNT_MAX[3:0]				PKEY_FLT_CNT_MAX[3:0]			
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

- Address: 0xB1
- Default: Depends on the PMIC part number
- Description: NVM fail-safe shadow register 1 (see Section 5.4.8).

[7:4]	**VIN_FLT_CNT_MAX[3:0]**: setting of the maximum number of occurrences triggered by a VIN falling below VINOK_Fall hard-fault source. 0000: 0 hard-faults allowed (PMIC goes in FAIL_SAFE_LOCK_STATE when the 1st hard-fault condition occurs) 0001: 1 hard-fault allowed (the PMIC goes in FAIL_SAFE_LOCK_STATE when the 2nd hard-fault condition occurs) … 1110: 14 hard-faults allowed (the PMIC goes in FAIL_SAFE_LOCK_STATE when the 15th hard-fault condition occurs) 1111: ∞ hard-faults allowed (fail-safe disabled: the PMIC always restarts when the hard-fault condition occurs)
[3:0]	**PKEY_FLT_CNT_MAX[3:0]**: setting of the maximum number of occurrences triggered by a PONKEYn long key press hard-fault source. 0000: 0 hard-faults allowed (the PMIC goes in FAIL_SAFE_LOCK_STATE when the 1st hard-fault condition occurs) 0001: 1 hard-fault allowed (the PMIC goes in FAIL_SAFE_LOCK_STATE when the 2nd hard-fault condition occurs) … 1110: 1 hard-faults allowed (the PMIC goes in FAIL_SAFE_LOCK_STATE when the 15th hard-fault condition occurs) 1111: ∞ hard-faults allowed (fail-safe disabled: the PMIC always restarts when a hard-fault condition occurs)

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6.7.26 NVM fail-safe shadow register 2 (NVM_FS_SHR2)

Table 109. **NVM_FS_SHR2**

7	6	5	4	3	2	1	0
TSHDN_FLT_CNT_MAX[3:0]				OCP_FLT_CNT_MAX[3:0]			
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

- Address: 0xB2
- Default: Depends on the PMIC part number
- Description: NVM fail-safe shadow register 2 (see Section 5.4.8).

[7:4]	**TSHDN_FLT_CNT_MAX[3:0]**: setting of the maximum number of occurrences triggered by a thermal shutdown hard-fault source. 0000:0 hard-faults allowed (the PMIC goes in FAIL_SAFE_LOCK_STATE when the 1st hard-fault condition occurs) 0001: 1 hard-fault allowed (the PMIC goes in FAIL_SAFE_LOCK_STATE when the 2nd hard-fault condition occurs) 1110: 14 hard-faults allowed (the PMIC goes in FAIL_SAFE_LOCK_STATE when the 15th hard-fault condition occurs) 1111: ∞ hard-faults allowed (fail-safe disabled: the PMIC always restarts when a hard-fault condition occurs)
[3:0]	**OCP_FLT_CNT_MAX[3:0]**: setting of the maximum number of occurrences triggered by regulator overcurrent hard-fault source. 0000:0 hard-faults allowed (the PMIC goes in FAIL_SAFE_LOCK_STATE when the 1st hard-fault condition occurs) 0001: 1 hard-fault allowed (the PMIC goes in FAIL_SAFE_LOCK_STATE when the 2nd hard-fault condition occurs) 1110: 14 hard-faults allowed (the PMIC goes in FAIL_SAFE_LOCK_STATE when the 15th hard-fault condition occurs) 1111: ∞ hard-faults allowed (fail-safe disabled: the PMIC always restarts when a hard-fault condition occurs)

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6.7.27 NVM fail-safe shadow register 3 (NVM_FS_SHR3)

Table 110. NVM_FS_SHR3

7	6	5	4	3	2	1	0
-	FAIL_SAFE_LOCK_DIS	RST_FLT_CNT_TMR[1:0]		WDG_FLT_CNT_MAX[3:0]			
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

- Address: 0xB3
- Default: Depends on the PMIC part number
- Description: NVM fail-safe shadow register 3 see Section 5.4.8.

[7]	reserved
[6]	**FAIL_SAFE_LOCK_DIS**: disable fail-safe lock state (pass through) 0: FAIL_SAFE_LOCK feature enabled (the PMIC stays in the FAIL_SAFE_LOCK state) 1: FAIL_SAFE_LOCK feature disabled (the PMIC passes through the FAIL_SAFE_LOCK state to go into the OFF state)
[5:4]	**RST_FLT_CNT_TMR [1:0]**: reset fault counter timer settings. When the timer elapses, it automatically clears all fault counters (*_FLT_CNT) 00: disabled 01: 1 minute 10: 6 minutes 11: 60 minutes
[3:0]	**WDG_FLT_CNT_MAX [3:0]**: setting of the maximum number of occurrences triggered by a watchdog hard-fault source. 0000:0 hard-faults allowed (the PMIC goes into the FAIL_SAFE_LOCK_STATE when the 1st hard-fault condition occurs) 0001: 1 hard-fault allowed (PMIC goes into the FAIL_SAFE_LOCK_STATE when the 2nd hard-fault condition occurs) 1110: 14 hard-faults allowed (the PMIC goes into the FAIL_SAFE_LOCK_STATE when the 15th hard-fault condition occurs) 1111: ∞ hard-faults allowed (fail-safe disabled: the PMIC always restarts when a hard-fault condition occurs)

6.7.28 NVM I²C device address shadow register (NVM_I²C_ADDR_SHR)

Table 111. NVM_I²C_ADD_SHR

7	6	5	4	3	2	1	0
LOCK_NVM	I²C_ADDR[6:0]						
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

- Address: 0xB5
- Default: Depends on the PMIC part number
- Description: NVM I²C device address shadow register.

The contents of this register take effect after the NVM programming command, then the NVM reloads (INIT&LOAD state or CHECK&LOAD state or NVM read command).

The LOCK_NVM bit takes effect on both shadow registers write and NVM programming command. A successful program operation is enough to have the lock active (without any reload).

[7]	**LOCK_NVM**: NVM write access lock: 0: NVM write allowed 1: NVM write disabled
[6:0]	**I²C_ADDR [6:0]**: I²C device address.

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6.7.29 NVM user free shadow register (NVM_USER_SHRx) (x = 1 to 5, y = 1 to 2)

Table 112. NVM_USER_SHRx

7	6	5	4	3	2	1	0
NVM_USERx[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

- Address: 0x94/0x95/0x9B/0xA8/0xAA/0xB6/0xB7
- Default: According to NVM content
- Description: User free shadow register 1 and 2.

Free usage scratch registers save end-product application data in the NVM. It requires an NVM programing command to save content in the NVM.

[7:0]	**NVM_USERx [7:0]**: User-defined value

6.7.30 NVM main control shadow register 3 (NVM_MAIN_CTL_SHR4)

Table 113. NVM_MAIN_CTRL_SHR4

7	6	5	4	3	2	1	0
VIN_DLY[1:0]		-	-	NVM_PKEY_EN_PULL[1:0]		EN_POL_CFG	PKEY_EN_CFG
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

- Address: 0xB9
- Default: 0x00 According to NVM
- Description: NVM main control shadow register 4.

[7:6]	**VIN_DLY [1:0]:** V_{IN} additional delay 00: no delay (default) 01: 10ms delay 10: 50ms delay 11: 100ms delay
[5:4]	**reserved [1:0]**
[3:2]	**NVM_PKEY_EN_PULL [1:0]**: PONKEYn/EN pad pull resistor selection. 00: no pull 01: pull-up active (R_{PU}) 10: pull-down active (R_{PD}) 11: no pull
[1]	**EN_POL_CFG:** EN polarity config 0: active high (default) 1: active low
[0]	**PKEY_EN_CFG**: PONKEYn/EN feature enabled. 0: PONKEY functionality enabled (default) 1: EN functionality enable

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7 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

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7.1 VFQFPN 40L (5.0X5.0x1.0) package information

Figure 19. **VFQFPN 40L (5.0X5.0x1.0) package outline**

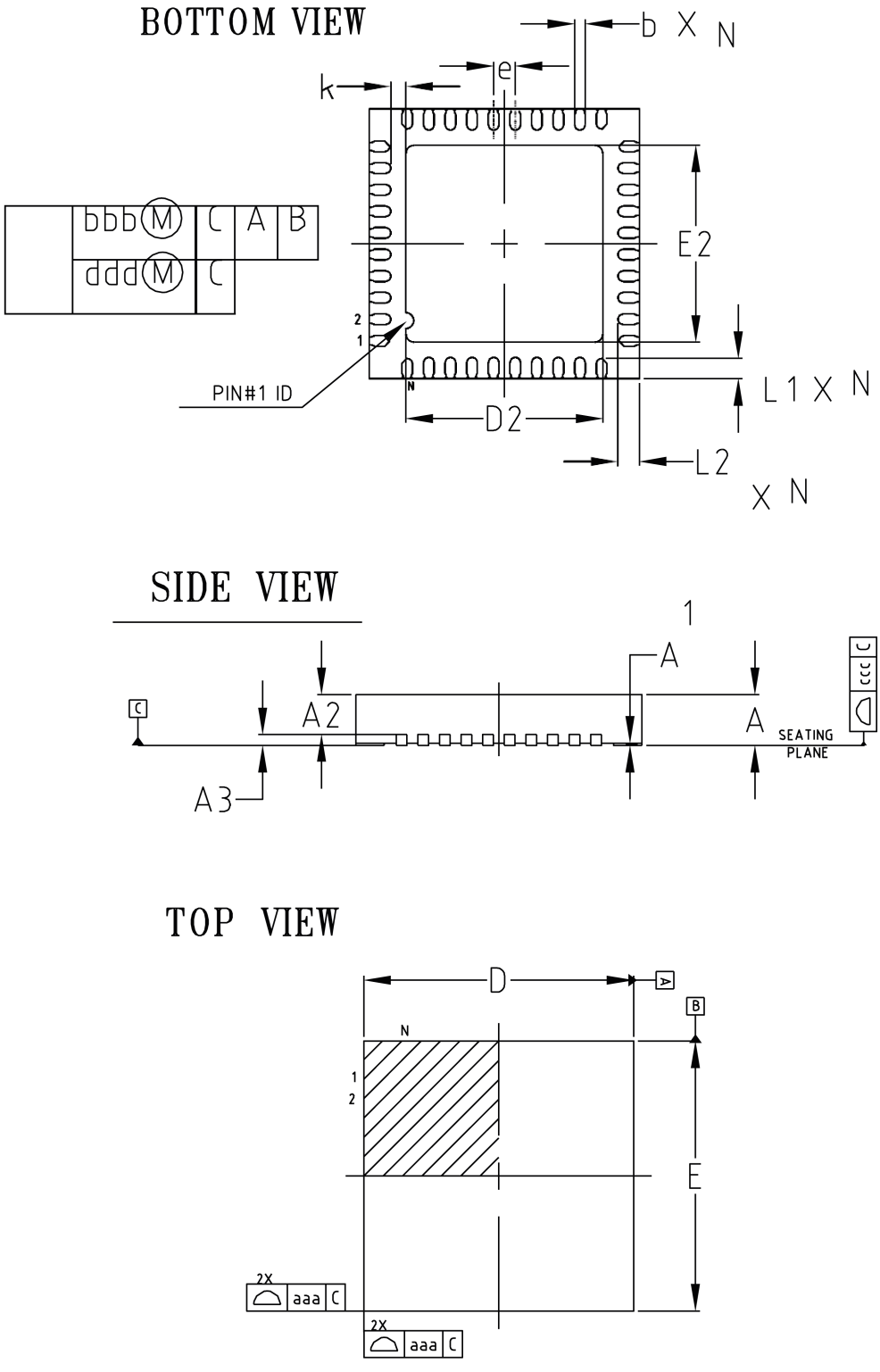

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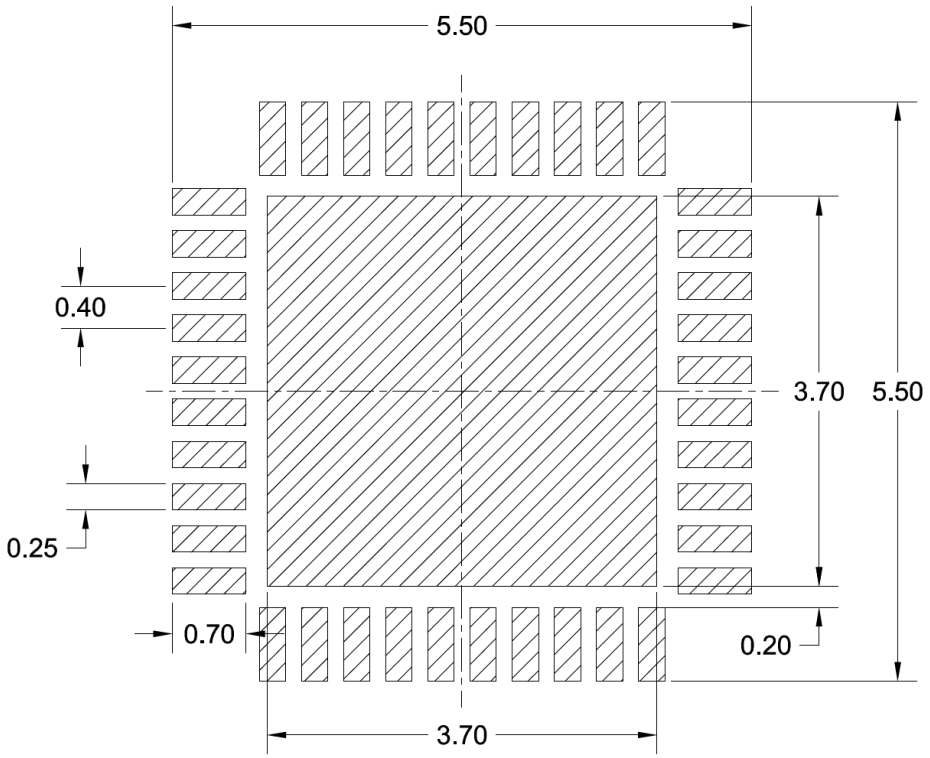
Table 114. **VFQFPN 40L (5.0X5.0x1.0) mechanical data**

DATABOOK				
SYMBOL	**MIN.**	**NOM.**	**MAX.**	**NOTE**
A	0.80	0.85	1.00	4
A1	0.00	-	0.05	12
A2	0.55	0.65	0.75	4
A3		0.20 REF.		4
b	0.15	0.20	0.25	4,9
D		5.00 BSC		4
D2	3.55	3.65	3.75	
e		0.40 BSC		4
E		5.00 BSC		4
E2	3.55	3.65	3.75	
L1	0.277	0.377	0.477	4
L2	0.30	0.40	0.50	
k	0.20			
N		40		15

Figure 20. **Suggested footprint**



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8 Ordering information

Table 115. **Ordering information**

Order code	Part number	Marking	VIO (LDO2) programming option	Packing
STPMIC2LAPQR	STPMIC2LA	PM2LA	3.3 V	VFQFPN40L (5.0x5.0x1.0)
STPMIC2LBPQR	STPMIC2LB	PM2LB	1.8 V	

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Revision history

Table 116. **Document revision history**

Date	Version	Changes
09-Oct-2025	1	First release.
24-Oct-2025	2	Minor text changes.
22-Jan.2026	3	Updated Section 5.5.1

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