

TOSHIBA Field Effect Transistor Silicon N Channel MOS Type

# SSM6N05FU

## High Speed Switching Applications

- Small package
- Low on resistance :  $R_{on} = 0.8 \Omega$  (max) (@ $V_{GS} = 4$  V)  
:  $R_{on} = 1.2 \Omega$  (max) (@ $V_{GS} = 2.5$  V)
- Low gate threshold voltage

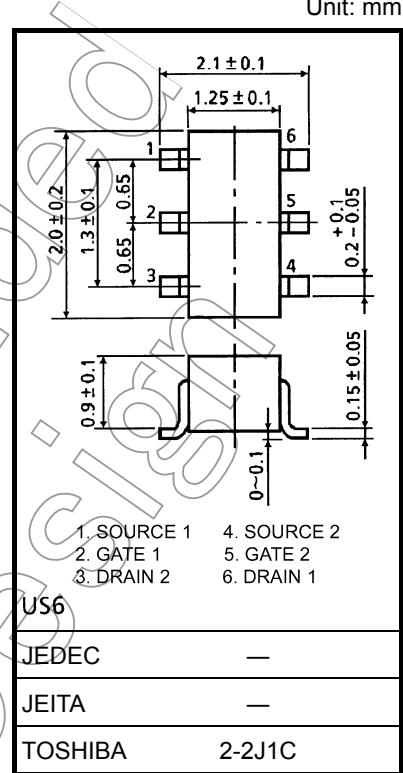
## Absolute Maximum Ratings ( $T_a = 25^\circ\text{C}$ ) (Q1, Q2 Common)

Characteristics	Symbol	Rating	Unit
Drain-Source voltage	$V_{DS}$	20	V
Gate-Source voltage	$V_{GSS}$	$\pm 12$	V
Drain current	DC	$I_D$	mA
	Pulse	$I_{DP}$	
Drain power dissipation ( $T_a = 25^\circ\text{C}$ )	$P_D$ (Note 1)	300	mW
Channel temperature	$T_{ch}$	150	$^\circ\text{C}$
Storage temperature range	$T_{stg}$	-55~150	$^\circ\text{C}$

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc.).

Note 1: Total rating, mounted on FR4 board  
(25.4 mm  $\times$  25.4 mm  $\times$  1.6 t, Cu Pad: 0.32 mm<sup>2</sup>  $\times$  6)



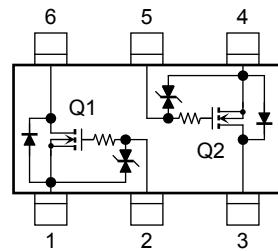
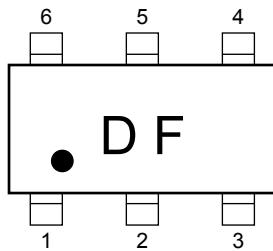
Weight: 6.8 mg (typ.)

## Handling Precaution

When handling individual devices (which are not yet mounting on a circuit board), be sure that the environment is protected against electrostatic electricity. Operators should wear anti-static clothing, and containers and other objects that come into direct contact with devices should be made of anti-static materials.

## Marking

## Equivalent Circuit (top view)

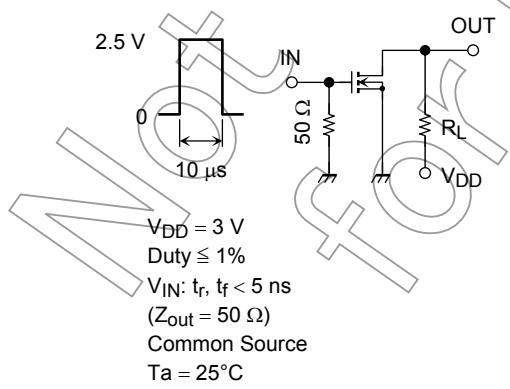
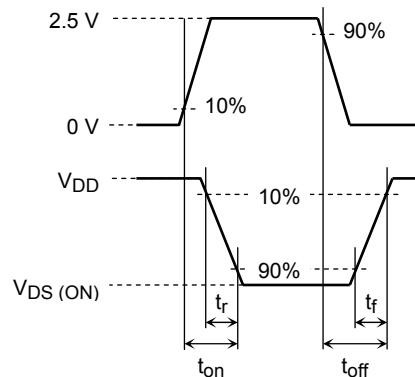
Electrical Characteristics ( $T_a = 25^\circ\text{C}$ ) (Q1, Q2 common)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current	$I_{GSS}$	$V_{GS} = \pm 12\text{ V}$ , $V_{DS} = 0$	—	—	$\pm 1$	$\mu\text{A}$
Drain-Source breakdown voltage	$V_{(\text{BR})\text{DSS}}$	$I_D = 1\text{ mA}$ , $V_{GS} = 0$	20	—	—	V
Drain cut-off current	$I_{DSS}$	$V_{DS} = 20\text{ V}$ , $V_{GS} = 0$	—	—	1	$\mu\text{A}$
Gate threshold voltage	$V_{th}$	$V_{DS} = 3\text{ V}$ , $I_D = 0.1\text{ mA}$	0.6	—	1.1	V
Forward transfer admittance	$ Y_{fs} $	$V_{DS} = 3\text{ V}$ , $I_D = 200\text{ mA}$ (Note2)	350	—	—	$\text{mS}$
Drain-Source ON resistance	$R_{DS(\text{ON})}$	$I_D = 200\text{ mA}$ , $V_{GS} = 4\text{ V}$ (Note2)	—	0.6	0.8	$\Omega$
		$I_D = 200\text{ mA}$ , $V_{GS} = 2.5\text{ V}$ (Note2)	—	0.85	1.2	
Input capacitance	$C_{iss}$	$V_{DS} = 3\text{ V}$ , $V_{GS} = 0$ , $f = 1\text{ MHz}$	—	22	—	$\text{pF}$
Reverse transfer capacitance	$C_{rss}$		—	9	—	$\text{pF}$
Output capacitance	$C_{oss}$		—	21	—	$\text{pF}$
Switching time	Turn-on time	$t_{on}$	$V_{DD} = 3\text{ V}$ , $I_D = 100\text{ mA}$ , $V_{GS} = 0\text{~}2.5\text{ V}$	60	—	ns
	Turn-off time	$t_{off}$		70	—	

Note2: Pulse test

## Switching Time Test Circuit

## (a) Test circuit

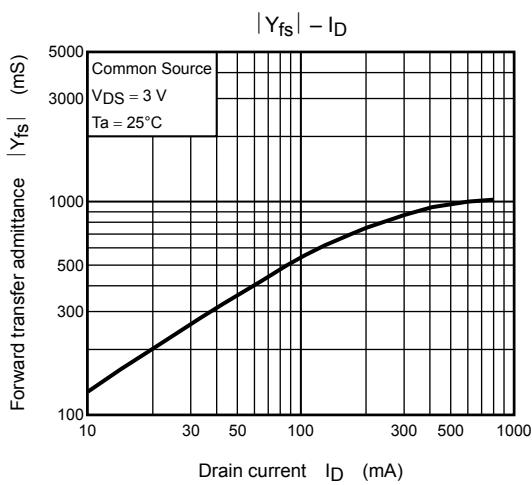
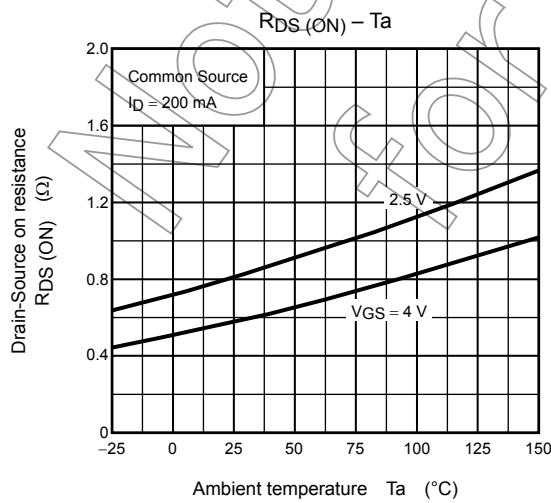
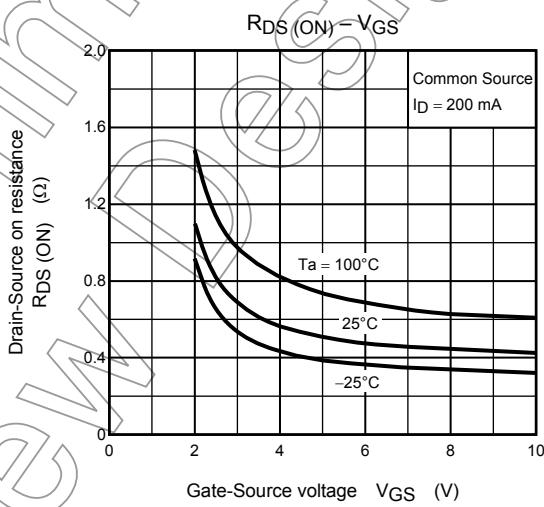
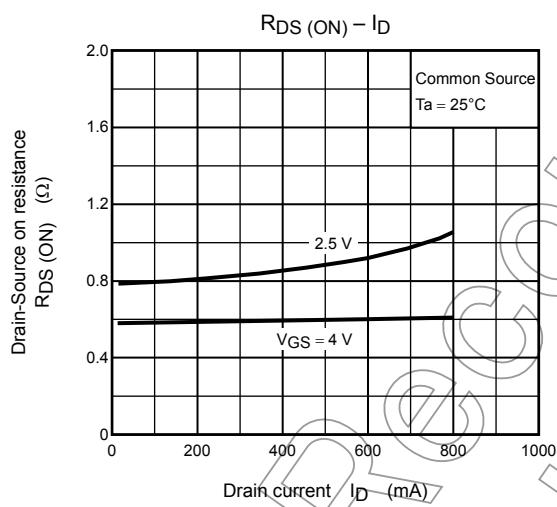
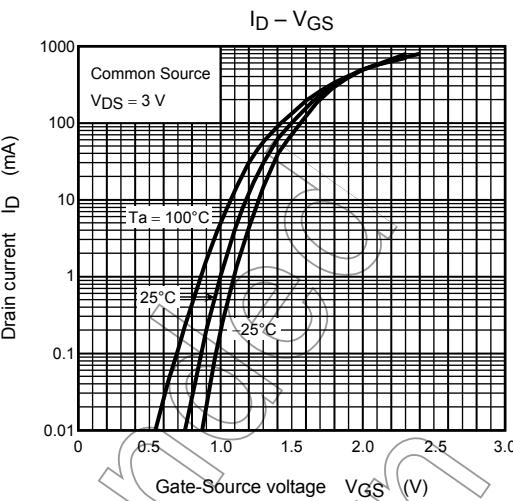
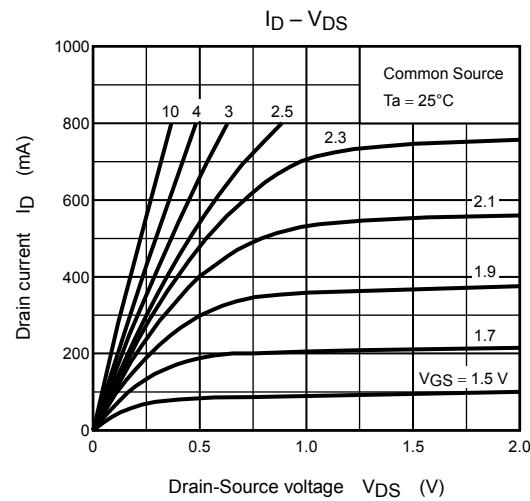
(b)  $V_{IN}$ (c)  $V_{OUT}$ 

## Precaution

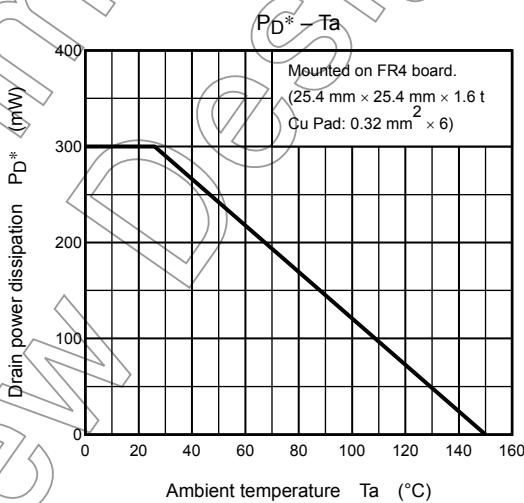
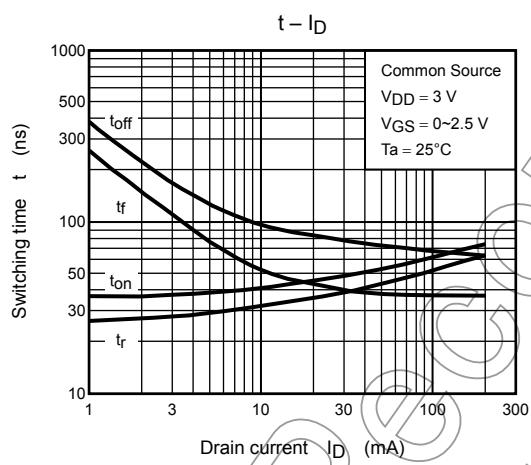
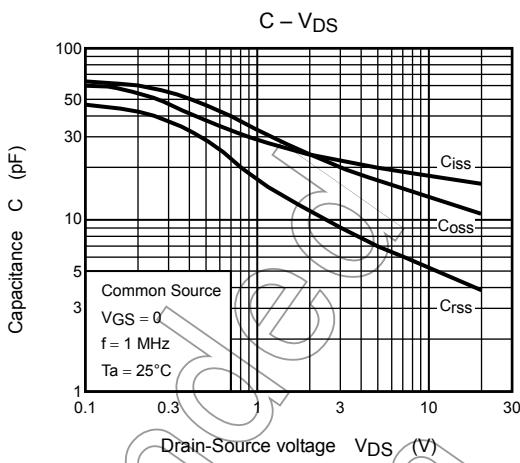
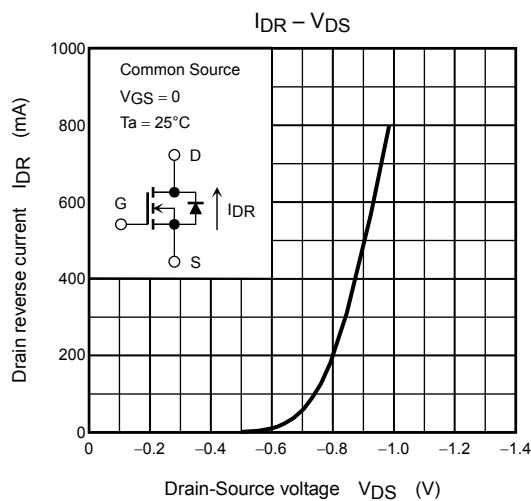
$V_{th}$  can be expressed as voltage between gate and source when low operating current value is  $I_D = 100\text{ }\mu\text{A}$  for this product. For normal switching operation,  $V_{GS(\text{on})}$  requires higher voltage than  $V_{th}$  and  $V_{GS(\text{off})}$  requires lower voltage than  $V_{th}$ . (Relationship can be established as follows:  $V_{GS(\text{off})} < V_{th} < V_{GS(\text{on})}$ )

Please take this into consideration for using the device.

(Q1, Q2 common)



(Q1, Q2 common)



\*: Total rating

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