

Evaluation Board for the **AD7124-8** 8-Channel, Low Noise, Low Power, 24-bit Σ - Δ ADC with In-Amp and Reference

FEATURES

Full featured evaluation board for the **AD7124-8**
PC control in conjunction with Analog Devices, Inc. System
Demonstration Platform (**EVAL-SDP-CB1Z**)
PC software for control and data analysis (time domain)
Standalone capability

EVALUATION KIT CONTENTS

EVAL-AD7124-8SDZ evaluation board
Evaluation software CD for the **AD7124-8**

ONLINE RESOURCES

Documents Needed

AD7124-8 data sheet
EVAL-AD7124-8SDZ user guide

Required Software

AD7124-8 EVAL+ Software

EQUIPMENT NEEDED

EVAL-AD7124-8SDZ evaluation board
EVAL-SDP-CB1Z System Demonstration Platform
DC signal source
USB cable
PC running Windows with USB 2.0 port

GENERAL DESCRIPTION

The **EVAL-AD7124-8SDZ** evaluation kit features the **AD7124-8** 24-bit, low power, low noise analog-to-digital converter (ADC).

A 7 V to 9 V external supply is regulated to 3.3 V to supply the **AD7124-8** and support all necessary components. The **EVAL-AD7124-8SDZ** board connects to the USB port of the PC by connecting to the **EVAL-SDP-CB1Z** motherboard.

The **AD7124-8 EVAL+ Software** fully configures the **AD7124-8** device register functionality and provides dc time domain analysis in the form of waveform graphs, histograms, and associated noise analysis for ADC performance evaluation.

The **EVAL-AD7124-8SDZ** is an evaluation board that allows the user to evaluate the features of the ADC. The user PC software executable controls the **AD7124-8** over the USB through the **EVAL-SDP-CB1Z** System Demonstration Platform (SDP) board.

Full specifications on the **AD7124-8** are available in the product data sheet, which should be consulted in conjunction with this user guide when working with the evaluation board.

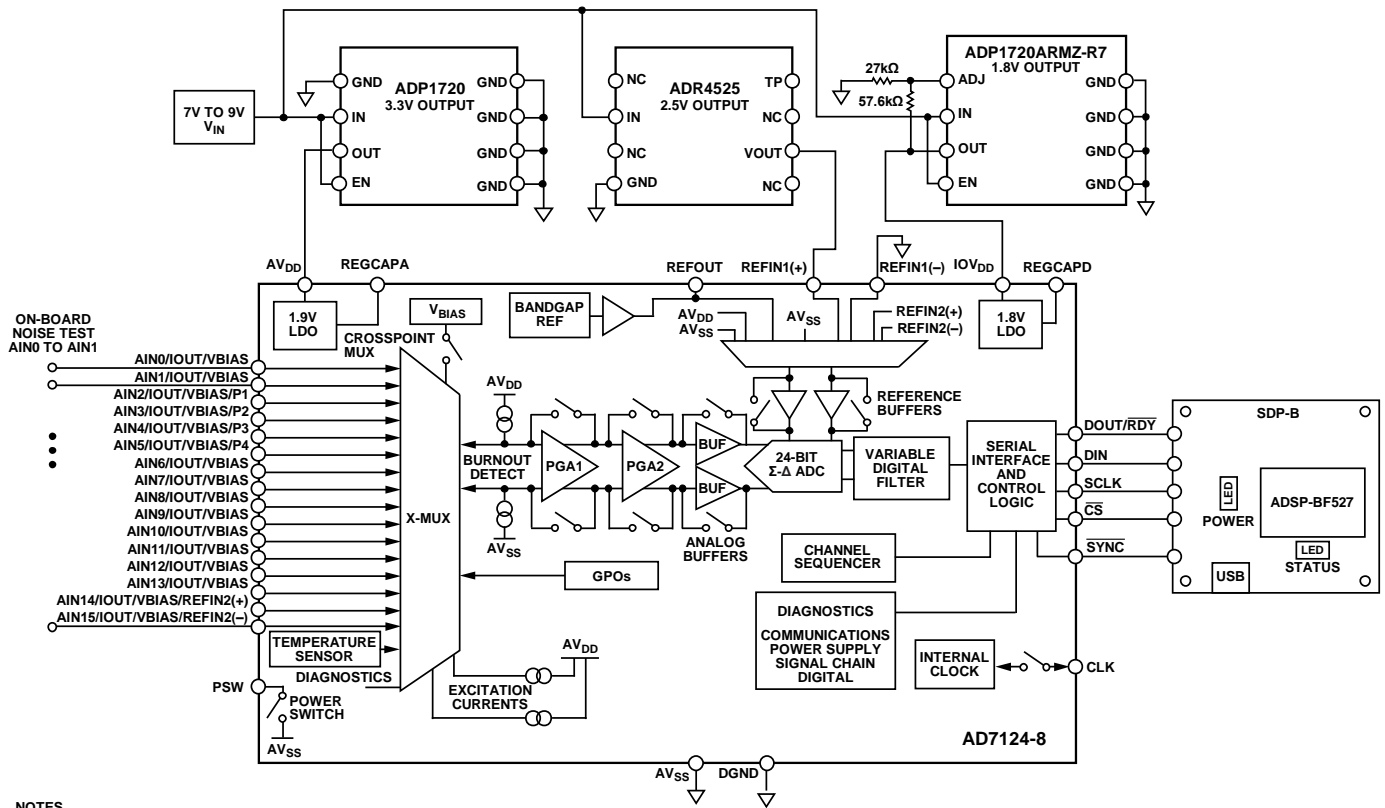
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REVISION HISTORY

7/15—Revision 0: Initial Version

EVAL-AD7124-8SDZ BLOCK DIAGRAM



NOTES
1. FOR SIMPLICITY, DECOUPLING NOT SHOWN.

Figure 1.

13305-001

EVAL-AD7124-8SDZ QUICK START GUIDE

To begin using the evaluation board, do the following:

1. With the [EVAL-SDP-CB1Z](#) board disconnected from the USB port of the PC, install the [AD7124-8 EVAL+ Software](#) (the software is included on the CD in the evaluation board kit and can be downloaded [online](#)). Restart the PC after the software installation is complete. (For complete software installation instructions, see the Software Installation Procedures section.)
2. Connect the [EVAL-SDP-CB1Z](#) board to the [EVAL-AD7124-8SDZ](#) board.
3. Screw the two boards together using the plastic screw and washer set included in the evaluation board kit to connect the boards firmly together.
4. Apply an external voltage in the range of 7 V to 9 V to the J3 or J5 connector of the [EVAL-AD7124-8SDZ](#) board. This provides the power supply for the board.
5. Connect the [EVAL-SDP-CB1Z](#) board to the PC using the supplied USB cable. If you are using Windows® XP, you may need to search for the [EVAL-SDP-CB1Z](#) drivers. Choose to automatically search for the drivers for the [EVAL-SDP-CB1Z](#) board if prompted by the operating system.
6. From the **Programs** menu, go to the **Analog Devices** subfolder, and click **AD7124 Eval+** to launch the [AD7124-8 EVAL+ Software](#) (see the Launching the Software section).

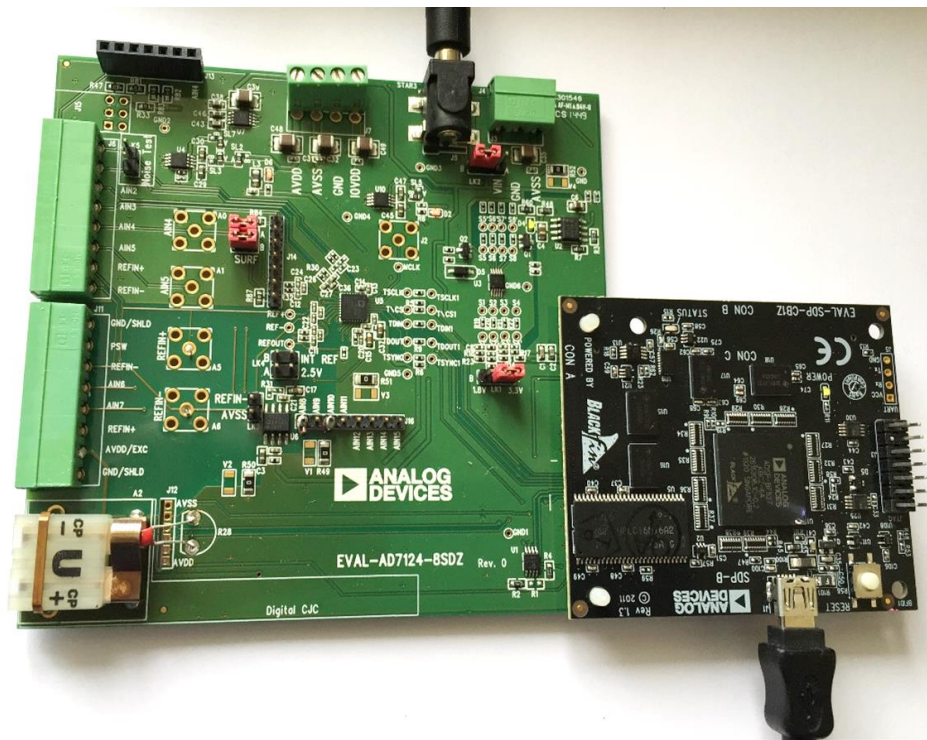


Figure 2. Hardware Configuration, Setting up the [EVAL-AD7124-8SDZ](#) Evaluation Board

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EVALUATION BOARD HARDWARE

DEVICE DESCRIPTION

The [AD7124-8](#) is a low power, low noise, complete analog front end for high precision measurement applications. It contains a low noise, 24-bit Σ - Δ ADC. It can be configured to have eight differential inputs or 15 single-ended or pseudo-differential inputs. The on-chip low noise instrumentation amplifier means that signals of small amplitude can interface directly to the ADC. Other on-chip features include a low drift 2.5 V reference, excitation currents, reference buffers, multiple filter options, and many diagnostic features.

Complete specifications for the [AD7124-8](#) are provided in the product data sheet and must be consulted in conjunction with this user guide when using the evaluation board. Full details about the [EVAL-SDP-CB1Z](#) are available at analog.com.

HARDWARE LINK OPTIONS

The default link options are listed in Table 1. By default, the board operates from a wall wart (dc plug) power supply via Connector J5. The supply required for the [AD7124-8](#) comes from the on-board [ADP1720](#) low dropout regulators (LDOs), which generate their voltage from Connector J5.

Table 1. Default Link and Solder Link Options

| Link No. | Default Option | Description |
|-------------------|----------------|--|
| LK1 | A | Connects the AV_{DD} voltage to the power supply sequencer, ADM1185 . When AV_{DD} equals 3.3 V, LK1 must be in Position A. When AV_{DD} equals 1.8 V, LK1 must be in Position B. |
| LK2 | B | Selects the connector for the external 7 V to 9 V power supply. In Position A, this link selects the external 7 V to 9 V power supply to come from Connector J3. In Position B, this link selects the external 7 V to 9 V power supply to come from Connector J5. |
| LK3 | Inserted | Inserting this link connects $REFIN(-)$ to AV_{SS} . |
| LK4 | 2.5 V | Selects the reference source for the ADC. In position 2.5 V, $REFIN1(+)$ is connected to the external 2.5 V reference (ADR4525). In position INT REF, $REFIN1(+)$ is connected to the $REFOUT$ pin of the AD7124-8 . This allows the internal reference of the AD7124-8 to connect as an external reference. |
| LK5 | Inserted | This link shorts $AIN0$ to $AIN1$. This is useful to perform noise tests on the AD7124-8 . It is possible to enable the internal bias on $AIN0$ or $AIN1$ so that $AIN0$ and $AIN1$ are at an appropriate voltage for the noise test. |
| LK6 | Inserted | LK6 can be used to connect the $AIN4$ and $AIN5$ channels to external components such as an external amplifier. Jumpers in position A and B at LK6 must be opened to include the external component on the front end. Jumper A and Jumper B of this link can be used to connect the $AIN4$ and $AIN5$ channels to external components such as an external amplifier. For this, the jumpers must be open. When Jumper A and Jumper B are in place, connect $AIN4$ and $AIN5$ to the on-board thermistor used for cold junction measurements. |
| SL2 | A | Sets the voltage applied to the AV_{DD} pin. In Position A, this link sets the voltage applied to the AV_{DD} pin to be a 3.3 V supply from the ADP1720-3.3 (U7) regulator or a 1.8 V supply from the ADP1720 (U4) regulator. In Position B, this link supplies the voltage to the AV_{DD} pin from an external voltage source via Connector J9. |
| SL3, SL7 | A, A | With SL3 and SL7 in Position A, the ADP1720-3.3 (U7) regulator supplies AV_{DD} with 3.3 V. With SL3 and SL7 in Position B, the ADP1720 (U4) regulator supplies AV_{DD} with 1.8 V. |
| SL5 | B | With this link in Position A, the IOV_{DD} supply is provided from an external source via Connector J9. With this link in Position B, the 3.3 V supply is generated by the ADP1720-3.3 (U10) regulator. The evaluation system operates with 3.3 V logic. |
| AV_{SS} to AGND | | Inserting these links ties AV_{SS} to AGND. When setting AV_{SS} to -1.8 V, remove these links. |

On-Board Connectors

Table 2 provides information about the external connectors on the [EVAL-AD7124-8SDZ](#).

Table 2. On-Board Connectors

| Connector | Function |
|-----------|--|
| J1 | A 120-pin connector that mates with the EVAL-SDP-CB1Z (black colored controller board). |
| J2 | Straight PCB mount SMB/SMA jack for master clock (not inserted). The EVAL-AD7124-8SDZ has the footprint to include an SMA/SMB connector, if using an external clock source to provide the master clock to the ADC. |
| J3 | Bench top power supply voltage input. Apply 7 V to 9 V and GND (0 V) to this connector to power the evaluation board. |
| J5 | Wall wart (dc plug) power supply voltage input. Apply 7 V to 9 V and GND (0 V) to this connector to power the evaluation board. |
| J6 | Analog input connector. Connections to AIN0 to AIN5 are available along with REFIN1(±) connections. Use this connector to connect an RTD to the AD7124-8 . |
| J9 | Optional external connector, allowing external bench top or alternative supply for AV _{DD} and IOV _{DD} . Connector J9 supplies AV _{SS} externally when split supplies are used. |
| J11 | Analog input connector. Connections to AIN6 to AIN7 are available along with REFIN1(±) and analog power supply connections. Use this connector to connect a load cell to the AD7124-8 . |
| J12 | 6-pin connector. Provides an I ² C interface to allow the SDP to interface with a digital temperature sensor. This is required if a thermocouple is interfaced with the AD7124-8 using connector A2. |
| J13 | 7-pin connector. Connects an external amplifier to channel AIN4/AIN5. |
| J14 | 7-pin connector. Allows connection to pins AIN4 and AIN5. |
| A0 | Straight PCB mount SMB/SMA jack. The footprint for an SMA/SMB connector is included on the evaluation board to provide the signal to analog input AIN4. |
| A1 | Straight PCB mount SMB/SMA jack. The footprint for an SMA/SMB connector is included on the evaluation board to provide the signal to analog input AIN5. |
| A2 | Thermocouple connector. This connector is required if a thermocouple is being interfaced to the evaluation board. |
| A5 | Straight PCB mount SMB/SMA jack. The footprint for an SMA/SMB connector is included on the evaluation board to provide the signal REFIN1(+). |
| A6 | Straight PCB mount SMB/SMA jack. The footprint for an SMA/SMB connector is included on the evaluation board to provide the signal REFIN1(–). |

POWER SUPPLIES

The evaluation board requires applying an external power supply—either a bench top supply or a wall wart (dc plug) supply—to J3 or J5 (see Table 3). Linear regulators generate the required power supply levels from the applied V_{IN} rail. The regulators used are the [ADP1720-3.3](#) (U7) and the [ADP1720](#) (U4), which supply 3.3 V and 1.8 V, respectively, to AV_{DD} of the ADC. The 3.3 V [ADP1720](#) (U10) delivers 3.3 V to the IOV_{DD} pin of the [AD7124-8](#).

When a split power supply is used, apply the AV_{SS} voltage from an external source via Connector J9. Connector J9 can also provide AV_{DD} and IOV_{DD} . However, the 7 V to 9 V supply is still required because the on-board reference ([ADR4525](#)) is supplied from this power supply.

Each supply is decoupled at the point where it enters the board and again at the point where it connects to each device (see the schematics shown in Figure 26 to Figure 34 to identify decoupling points).

SERIAL INTERFACE

The [EVAL-AD7124-8SDZ](#) evaluation board connects via the serial peripheral interface (SPI) to the Blackfin® [ADSP-BF527](#) on the [EVAL-SDP-CB1Z](#).

There are four primary signals: CS, \overline{SCLK} , DIN, and $DOUT/\overline{RDY}$ (all are inputs, except for $DOUT/\overline{RDY}$, which is an output).

To operate the [EVAL-AD7124-8SDZ](#) in standalone mode, the [AD7124-8](#) serial interface lines can be disconnected from the 120-pin header by removing the 0 Ω links, R9 through R13. The test points can then be used to fly-wire the signals to an alternative digital capture setup.

ANALOG INPUTS

Apply the [EVAL-AD7124-8SDZ](#) primary analog inputs voltages in two ways:

- Using J6 and J11, the green, screw-in terminal connectors.
- Using the A0 and A1 SMB/SMA footprints on the evaluation board that connect to AIN4 and AIN5 analog inputs.

The [AD7124-8 EVAL+ Software](#) is set up to analyze dc inputs to the ADC.

Table 3. Required External Power Supply¹

| Power Supply (V_{IN}) Applied To | Voltage Range | Function |
|--------------------------------------|---------------|---|
| J3 | 7 V to 9 V | Bench top supply to the evaluation board. Supplies LDOs that create the 3.3 V and 1.8 V rails. It also supplies the ADR4525 external reference. Ensure that LK2 is set to Position A when the external power supply is applied to this connector. |
| J5 | 7 V to 9 V | Wall wart (dc plug) supply to the evaluation board. Supplies LDOs that create the 3.3 V and 1.8 V rails. It also supplies the ADR4525 external reference. Set LK2 to Position B when the external power supply is applied to this connector. |

¹Only a single supply is required, for either J3 or J5. This can be selected using LK2.

REFERENCE OPTIONS

The [EVAL-AD7124-8SDZ](#) includes an external 2.5 V reference (the [ADR4525](#)) and an internal 2.5 V reference. The default operation uses the external reference input, which accepts the 2.5 V [ADR4525](#) on the evaluation board.

Select the reference used for a conversion by choosing the reference in the configuration registers associated with Setup 0 to Setup 7. Switch between using the internal reference and external reference by accessing the [AD7124-8](#) registers through the pop-up windows (discussed in more detail in the following sections) via the evaluation software. Figure 3 shows how to select the reference source for Setup 0 to Setup 7. Figure 4 shows the ADC Control register setting that enables the internal reference.

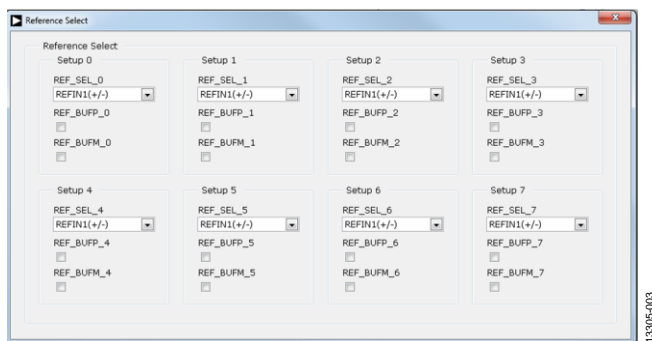


Figure 3. Selecting the Reference Source Using Pop-Up Windows

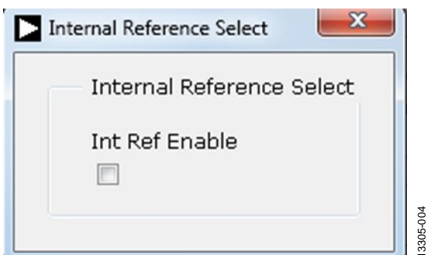


Figure 4. Enabling the Internal 2.5 V Reference Using Pop-Up Windows

EVALUATION BOARD SETUP PROCEDURE

After following the instructions in the Software Installation Procedures section, set up the evaluation and SDP boards as detailed in this section.

Warning

The evaluation software and drivers must be installed before connecting the [EVAL-AD7124-8SDZ](#) evaluation board and [EVAL-SDP-CB1Z](#) board to the USB port of the PC to ensure the PC correctly recognizes the evaluation system.

Configuring the Evaluation and SDP Boards

1. Connect the [EVAL-SDP-CB1Z](#) board to Connector A or Connector B on the [EVAL-AD7124-8SDZ](#) board. Screw the two boards together using the plastic screw and washer set included in the evaluation board kit to connect the boards firmly together.
2. Connect the power supplies to the [EVAL-AD7124-8SDZ](#) board. The [EVAL-AD7124-8SDZ](#) board, by default, uses the wall wart (dc plug) supply that accompanies the evaluation kit. Connect the wall wart (dc plug) supply to Connector J5 on the [EVAL-AD7124-8SDZ](#) board. (For more information about the required connections and available options, refer to the Power Supplies section.)
3. Connect the [EVAL-SDP-CB1Z](#) board to the PC using the supplied USB cable.

EVALUATION BOARD SOFTWARE

SOFTWARE INSTALLATION PROCEDURES

The EVAL-AD7124-8SDZ evaluation kit includes a CD containing software that needs to be installed before using the EVAL-AD7124-8SDZ evaluation board.

There are two parts to the installation:

- EVAL-AD7124-8SDZ EVAL+ Software installation
- EVAL-SDP-CB1Z SDP board drivers installation

Warning

The evaluation software and drivers must be installed before connecting the EVAL-AD7124-8SDZ evaluation board and EVAL-SDP-CB1Z board to the USB port of the PC to ensure the PC correctly recognizes the evaluation system.

Installing the AD7124-8 EVAL+ Software

To install the AD7124-8 EVAL+ Software:

1. With the EVAL-SDP-CB1Z disconnected from the USB port of the PC, insert the installation CD into the CD-ROM drive.
2. Double-click the **setup.exe** file to begin the evaluation board software installation. The software then installs to the following default location: **C:\Program Files\Analog Devices\AD7124 EVAL+**.
3. A dialog box appears asking for permission to allow the program to make changes to your PC. Click **Yes**.



Figure 5. AD7124-8 EVAL+ Software Installation: Granting Permission for the Program to Make Changes to Your PC

4. Select a location to install the software and then click **Next**. (Figure 6 shows the default locations, which are displayed when the dialogue box opens, but you can select another location by clicking **Browse**.)

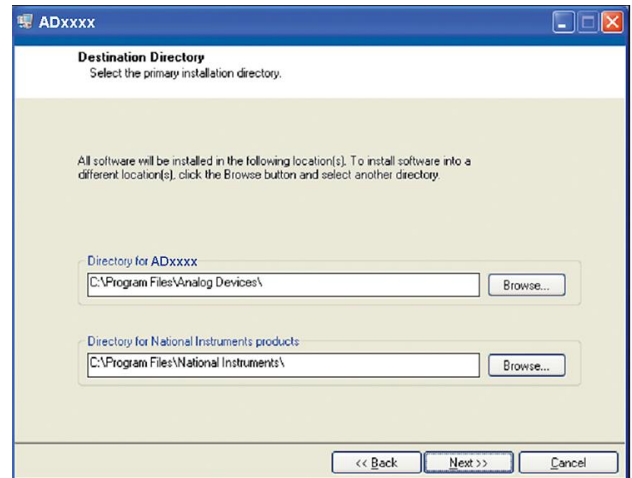


Figure 6. AD7124-8 EVAL+ Software Installation: Selecting the Location for Software Installation

5. A license agreement appears. Read the agreement and then select **I accept the License Agreement** and click **Next**.

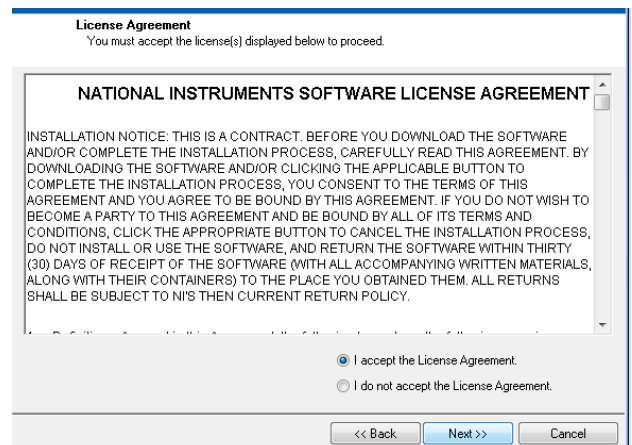


Figure 7. AD7124-8 EVAL+ Software Installation: Accepting the License Agreement

6. A summary of the installation displays. Click **Next** to continue.

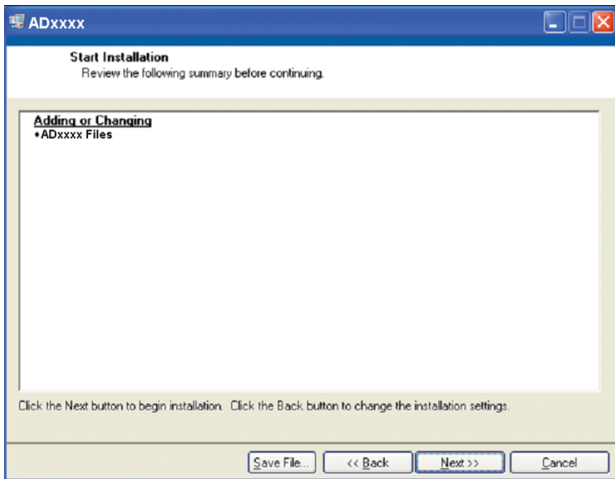


Figure 8. AD7124-8 EVAL+ Software Installation: Reviewing a Summary of the Installation

7. The message in Figure 9 appears when the installation is complete. Click **Next**.

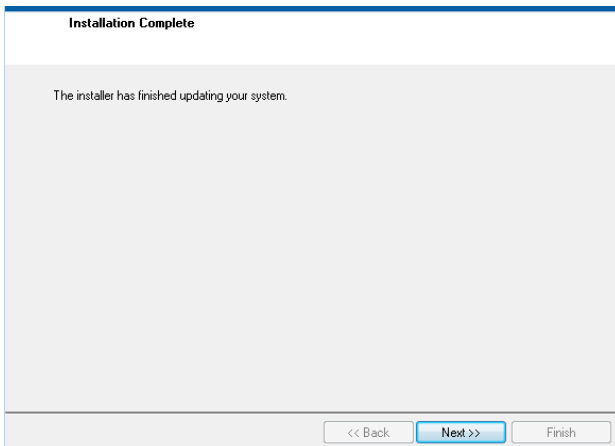


Figure 9. AD7124-8 EVAL+ Software Installation: Indicating When the Installation Is Complete

Installing the EVAL-SDP-CB1Z System Demonstration Platform Board Drivers

After the installation of the evaluation software is complete, a welcome window displays for the installation of the EVAL-SDP-CB1Z SDP board drivers.

1. With the EVAL-SDP-CB1Z board still disconnected from the USB port of the PC, make sure that all other applications are closed, and then click **Next**.



Figure 10. EVAL-SDP-CB1Z Drivers Setup: Beginning the Drivers Installation

2. Select the location to install the drivers and then click **Next**.

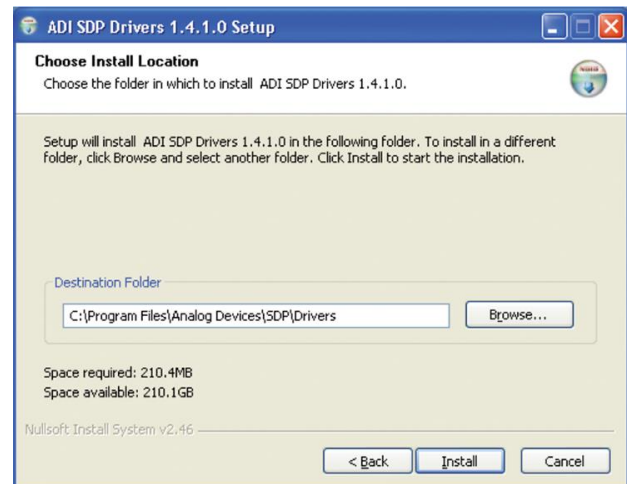


Figure 11. EVAL-SDP-CB1Z Drivers Setup: Selecting the Location for Drivers Installation

- Click **Install** to install the drivers.

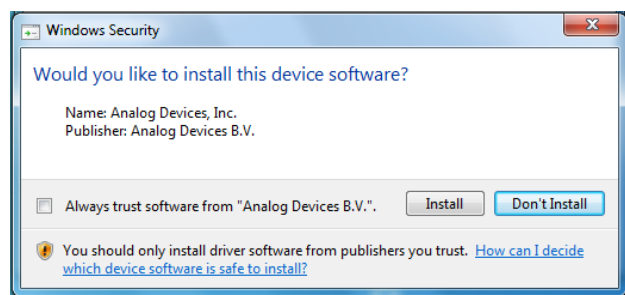


Figure 12. EVAL-SDP-CB1Z Drivers Setup: Granting Permission to Install Drivers

- To complete the drivers installation, click **Finish**, which closes the installation Setup Wizard.

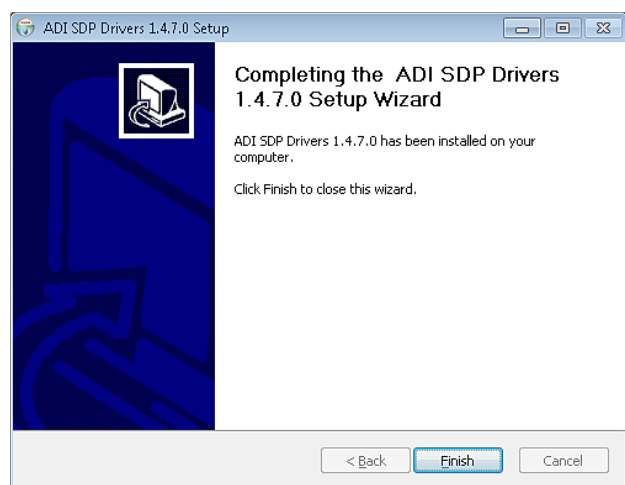


Figure 13. EVAL-SDP-CB1Z Drivers Setup: Completing the Drivers Setup Wizard

- Before using the evaluation board, you must restart the PC.

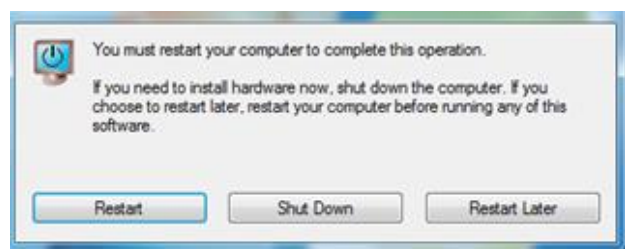


Figure 14. EVAL-SDP-CB1Z Drivers Setup: Restarting the PC

Setting Up the System for Data Capture

After completing the steps in the Software Installation Procedures section and the Evaluation Board Hardware section, set up the system for data capture as follows:

- Allow the Found New Hardware Wizard to run after you connect the EVAL-SDP-CB1Z board to your PC. (If you are using Windows XP, you may need to search for the EVAL-SDP-CB1Z drivers. Choose to automatically search for the drivers for the EVAL-SDP-CB1Z board if prompted by the operating system.)
- Check the board is connecting to the PC correctly using the **Device Manager** of the PC.
- Access the **Device Manager** as follows:
 - Right-click **My Computer** and then click **Manage**.
 - A dialog box appears asking for permission to allow the program to make changes to your PC. Click **Yes**.
 - The **Computer Management** box appears. Click **Device Manager** from the list of System Tools (see Figure 15).
 - The EVAL-SDP-CB1Z board then appears under **ADI Development Tools**. This indicates the driver software is installed and the board is connecting to the PC correctly.

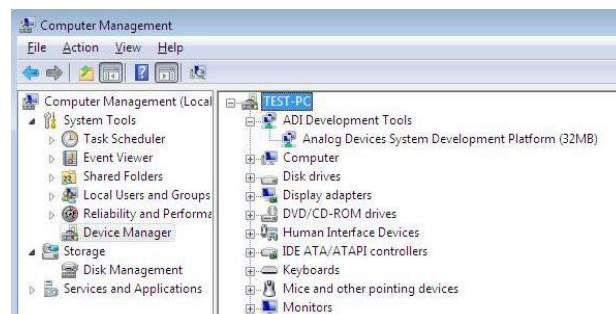


Figure 15. Device Manager: Checking the Board Is Connected to the PC Correctly

Launching the Software

After completing the steps in the Setting Up the System for Data Capture section, launch the [AD7124-8 EVAL+ Software](#) as follows:

1. From the Start menu, click **Programs > Analog Devices > AD7124 Eval+ > AD7124 Eval+**. The dialog box in Figure 19 appears; select **EVAL-AD7124-8SDZ**, and the main window of the software then displays as shown in Figure 20.
2. If the [AD7124-8](#) evaluation system is not connected to the USB port via the [EVAL-SDP-CB1Z](#) when the software is launched, a connectivity error displays (see Figure 16). Connect the evaluation board to the USB port of the PC, wait a few seconds, click **Rescan**, and then follow the on-screen instructions.

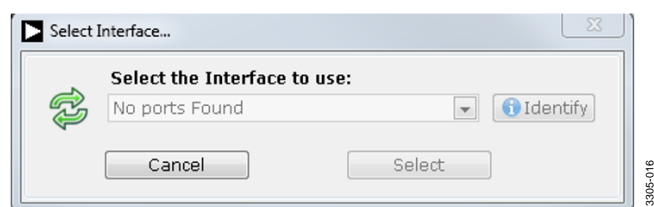


Figure 16. Connectivity Error Alert

When the software starts running, it searches for hardware connected to the PC. A dialog box indicates when the generic SDP attached to the PC is detected; the main window appears (see Figure 18). Press the RESET button on the SDP board as highlighted in Figure 17.



Figure 17. SDP Connectivity Board—RESET Button

Clicking the RESET button enables the software to rescan for a connected SDP board. If found, the message shown in Figure 18 displays.

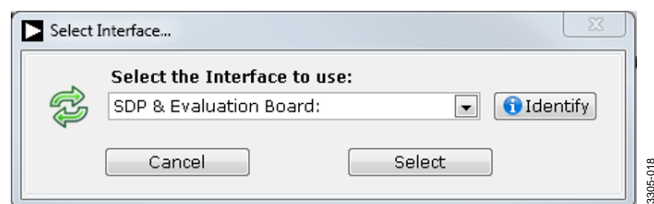


Figure 18. Connectivity when SDP and Evaluation Boards are Found

SOFTWARE OPERATION

Overview of the Main Window

The evaluation software supports both the [AD7124-4](#) and the [AD7124-8](#) devices.

When running the software, the specific evaluation board connected to the pc can be selected as shown in Figure 19. For the [AD7124-8](#), select **EVAL-AD7124-8SDZ** from the drop-down menu as shown in Figure 19.

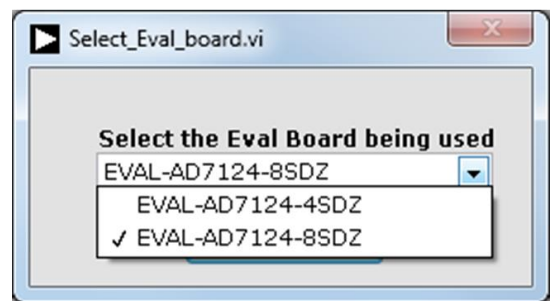


Figure 19. AD7124 Evaluation Board Selection

When selecting [EVAL-AD7124-8SDZ](#), the main window of the evaluation software displays, as shown in Figure 20. Figure 20 shows the control buttons and analysis indicators of the [AD7124-8 EVAL+ Software](#). The main window of the [AD7124-8 EVAL+ Software](#) contains four tabs:

- Configuration
- Waveform
- Histogram
- Register Map

CONFIGURATION TAB

The **Configuration** tab shows a block diagram of the [AD7124-8](#). It allows the user to set up the ADC, reset the ADC, read the diagnostics to view errors present, as well as configure the device for different demo modes. Figure 20 shows the **Configuration** tab in more detail, and the following sections discuss the different elements on the **Configuration** tab of the software window.

ADC Reset

Click **ADC RESET** (Label 2) to perform a software reset of the [AD7124-8](#). There is no hardware reset pin on the [AD7124-8](#).

To perform a hard reset, remove power from the board. However, the software reset has the same effect as a hard reset.

Selecting External Reference

There are two options to select the external reference on the [AD7124-8 EVAL+ Software](#): **AVdd** and **Refin1(+/-)** (Label 3). The **Refin1(+/-)** field sets the external reference voltage that is connected between REFIN1+ and REFIN1-. The **AVdd** field sets the AV_{DD} voltage level for the [AD7124-8](#). Using [EVAL-AD7124-8SDZ](#) evaluation board, the AV_{DD} voltage is 3.3 V. Either of these voltage levels can be used to calculate the results on the **Waveform** and **Histogram** tabs. The evaluation board has an external 2.5 V [ADR4525](#) reference; this reference selection can be bypassed on the evaluation board. If bypassing the [ADR4525](#) on board, change the external reference voltage value in **Refin1(+/-)** to ensure correct calculation of results in the **Waveform** and **Histogram** tabs.

Tutorial Button

Click the **TUTORIAL** button (Label 4) to open a tutorial on using the software and additional information on using the [AD7124-8 EVAL+ Software](#).

Functional Block Diagram

The functional block diagram of the ADC (Label 5) shows each of the functional blocks within the ADC. Clicking a configuration button on this graph opens the configuration pop-up window for that block.

Configuration Pop-Up Button

Each configuration pop-up button (Label 6) opens a different window to configure the relevant functional block.

Config Summary

Clicking the **CONFIG SUMMARY** button (Label 7) displays the channel configuration information on each of the individual setups as well as information on any error present. These tabs can be used to quickly check how the ADC channels are configured, as well as any errors that are present.

Demo Modes

The [AD7124-8 EVAL+ Software](#) supports a number of demo modes (Label 8); these demo modes configure the [AD7124-8](#) for each of the modes shown. A help file is available for each demo mode; to access this help file, click the question mark button.

Status Bar

The status bar (Label 9) displays status updates such as **Analysis Completed**, **Reset Completed**, and **Configuring Demo Mode** during software use, as well as the software version and the **Busy** indicator.

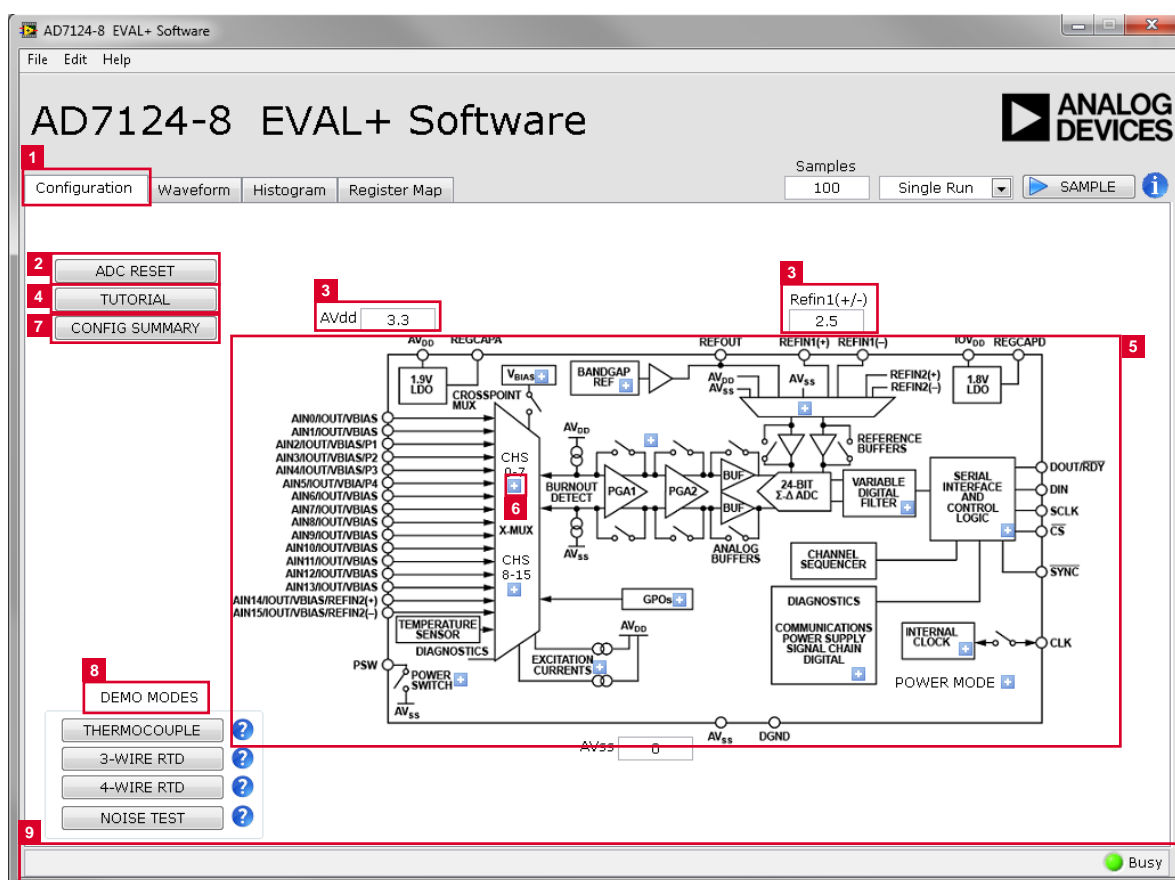


Figure 20. Configuration Tab of the [AD7124-8 EVAL+ Software](#)

WAVEFORM TAB

The **Waveform** tab graphs the conversions gathered and processes the data, calculating the peak-to-peak noise, rms noise, and resolution (see Figure 21).

Waveform Graph and Controls

The data waveform graph (Label 1) shows each successive sample of the ADC output. Zoom in on the data in the graph using the control toolbar (Label 2). Change the scales on the graph by typing values into the x-axis and y-axis.

Analysis Channel

The **Noise Analysis** section and histogram graph show the analysis of the channel selected via the **Analysis Channel** control (Label 3).

Samples

The **Samples** numeric control (Label 4) and batch control (Label 5) set the number of samples gathered per batch. Batch control sets whether a single batch or multiple batches of samples are gathered. This control is unrelated to the ADC mode. You can capture a defined sample set or continuously gather batches of samples. In both cases, the number of samples set in the **Samples** (Label 4) numeric input dictates the number of samples.

Sample

Click the **SAMPLE** button (Label 6) to start gathering ADC results. Results appear in the waveform graph (Label 1).

Channel Selection

The channel selection control (Label 7) selects which channels display on the data waveform and shows the analog inputs for the channel labeled next to the on and off controls.

These controls only affect the display of the channels and have no effect on the channel settings in the ADC register map.

Display Units and Axis Controls

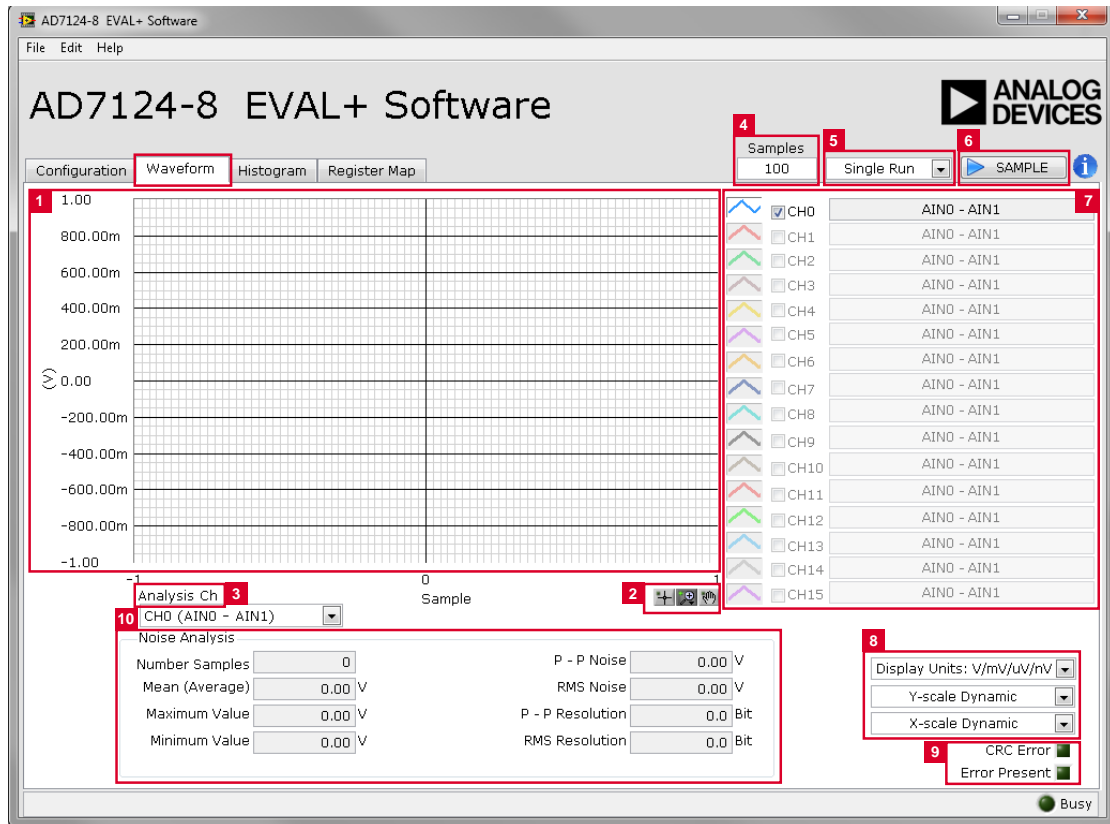
Click the **Display Units** drop-down menu (Label 8) to select whether the data graph displays in units of voltages or codes. This control affects both the waveform graph and the histogram graph. The axis controls switch between dynamic and fixed. When dynamic is selected, the axis automatically adjusts to show the entire range of the ADC results after each batch of samples. When selecting **Fixed**, the axis ranges can be programmed; however, these ranges do not automatically adjust after each batch of samples.

CRC Error and Overall Error

The **CRC Error** LED indicator (Label 9) illuminates on the **Waveform** tab when a cyclic redundancy check (CRC) error is detected in the communications between the software and the [AD7124-8](#). The CRC functionality on the [AD7124-8](#) is disabled by default and must be enabled for this indicator to work. The **Error Present** LED indicates if an overall error is present in the diagnostics register. For this indicator to work, the check for the different diagnostic errors must be enabled in the Error_EN register.

Noise Analysis

The **Noise Analysis** (Label 10) section displays the results of the noise analysis for the selected analysis channel, including both noise and resolution measurements.

Figure 21. **Waveform** Tab of the AD7124-8 EVAL+ Software

HISTOGRAM TAB

The **Histogram** tab generates a histogram using the gathered samples and processes the data, calculating the peak-to-peak noise, rms noise, and resolution (Figure 22).

Histogram Graph and Controls

The data histogram graph (Label 1) shows the number of times each sample of the ADC output occurs. Zoom in on the data using the control toolbar (Label 6) in the graph. Change the scales on the graph by typing values into the x-axis and y-axis.

Analysis Channel

The **Noise Analysis** section and histogram graph show the analysis of the channel selected via the **Analysis Channel** (Label 2) control.

Noise Analysis

The **Noise Analysis** section (Label 3) displays the results of the noise analysis for the selected analysis channel, including both noise and resolution measurements.

Display Units and Axis Controls

Click the **Display Units** drop-down box (Label 4) to select whether the data graph displays in units of voltages or codes.

This control affects both the waveform graph and the histogram graph. The axis controls can be used to switch between dynamic and fixed range. When **Dynamic** is selected, the axis automatically adjusts to show the entire range of the ADC results after each batch of samples. When selecting **Fixed**, the user can program the axis ranges; the axis ranges do not automatically adjust after each batch of samples.

CRC Error and Overall Error

The **CRC Error** LED indicator (Label 5) illuminates when detecting a cyclic redundancy check (CRC) error in the communications between the software and the [AD7124-8](#). The CRC functionality on the [AD7124-8](#) is disabled by default and must be enabled for this indicator to work. The **Error Present** LED (Label 5) indicates if an overall error is present in the diagnostics register. For this indicator to work, the check for the different diagnostic errors must be enabled in the Error_EN register.

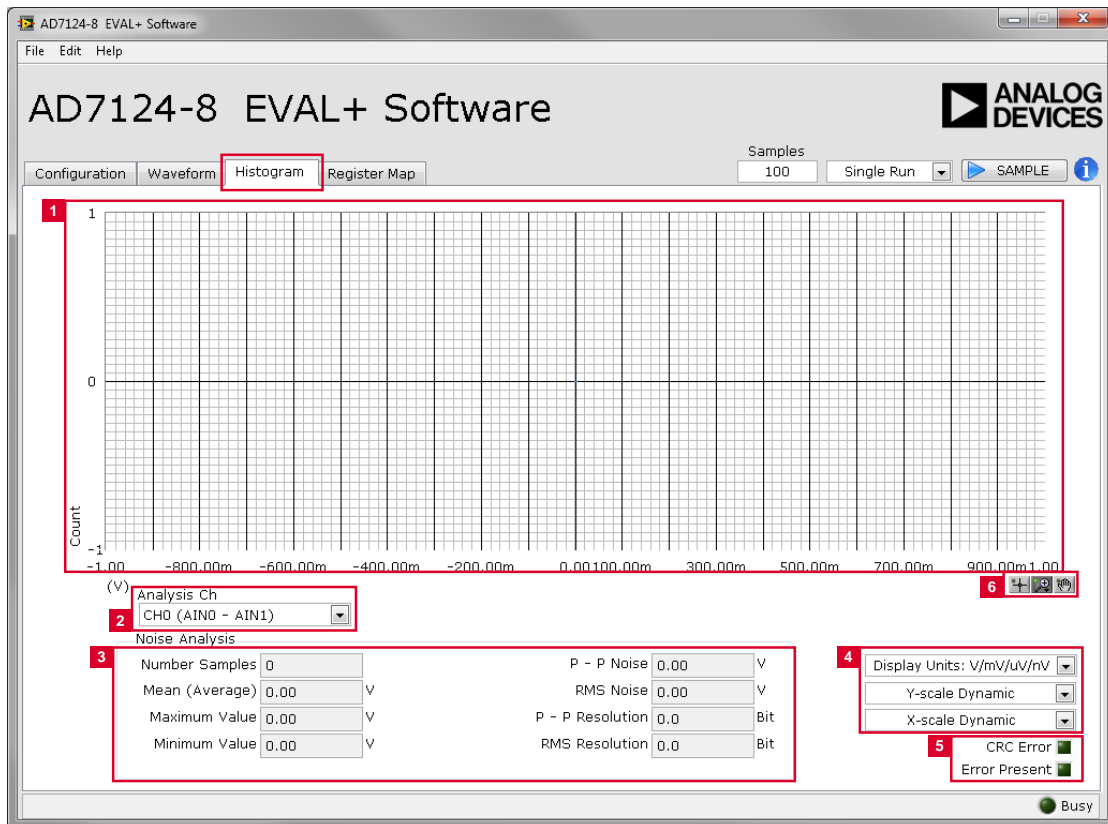


Figure 22. Histogram Tab of the [AD7124-8 EVAL+ Software](#)

NOISE TEST—QUICK START DEMONSTRATION

Click the **NOISE TEST** demo button (Figure 20) to configure the device for the noise test. The AD7124-8 is now configured for the noise test demo, where the output data rate is 9.38 SPS, where the sinc⁴ digital filter, full power mode of operation, and external reference REFIN1(±) is selected. Gain and offset are the default factory values following a reset.

To gather samples, change the **Samples** field to the number of samples required, then click the **SAMPLE** button to acquire the samples from the ADC. Figure 24 shows an example of the main window after running a noise test.

Reading Samples from the ADC

The evaluation board is set up to use the external 2.5 V on-board reference (ADR4525). To read samples from the ADC, do the following:

1. The value in the **Refin1(+/-)** field on the **Configuration** tab is set to 2.5 V by default to use the external 2.5 V on-board reference (ADR4525). If a different reference is used to the AD7124-8, the **Refin1(+/-)** field should be updated accordingly. (The analysis results are based on the value set in this input field.)
 - a. When selecting **Single Run**, a batch of samples is read when clicking the **SAMPLE** button; the batch size is set by the value in the **Samples** field.

- b. When selecting **Continuous Read**, the software performs a continuous capture from the ADC by clicking the **SAMPLE** button. Click the **SAMPLE** button again to stop capturing data.
2. Use the navigation tools within each graph to control the cursor, zooming, and panning.

Waveform

Find the waveforms resulting from the gathered samples in the **Waveform** tab. The waveform graph shows each successive sample of the ADC output (input referred). The indicators beside this graph show the channels converting. The navigation tools allow you to control the cursor, zooming, and panning. You can also display the conversions as voltages or codes.

Below the graph are parameters, such as peak-to-peak noise and rms noise, in the **Analysis** section for the current batch of samples. If there are several enabled analog input channels, you can select each enabled channel and the conversions through the analyzed channel using the **Analysis Channel**.

Save the conversion data in a text file using File at the top of the window. To save the data into an Excel file, right-click the waveform graph and select **Export Data** from the drop-down menu that appears. A **Save** dialog box is displayed, prompting you to save the data to an appropriate folder location.

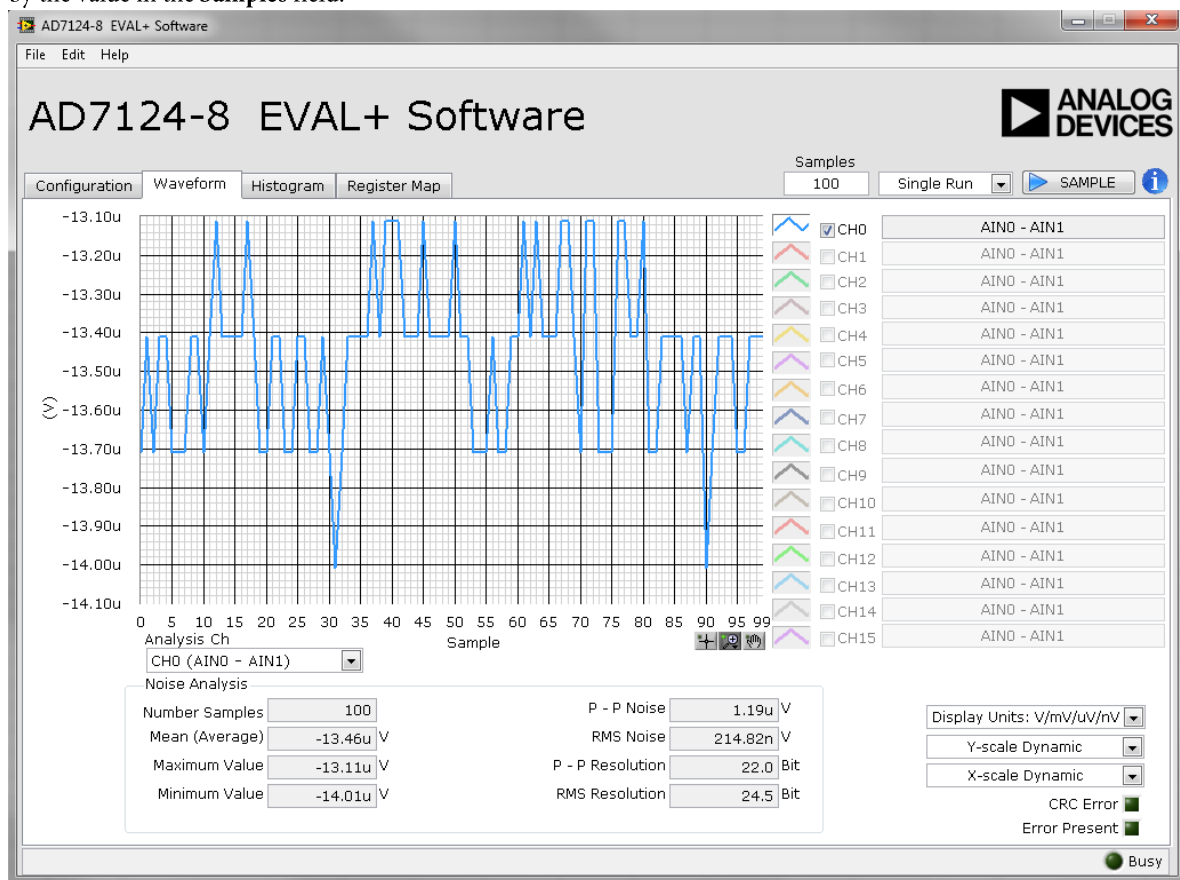


Figure 24. Example of the **Waveform** Tab After Running a Noise Test

Histogram

This tab shows the histogram analysis. The indicators beside this graph show the channels converting. The navigation tools allow you to control the cursor, zooming, and panning. You can also display the conversions as voltages or codes.

Parameters such as peak-to-peak noise and rms noise are displayed in the **Analysis Results** section for the current batch of samples.

Save the conversion data in a text file using **File** at the top of the window. To save the data into an Excel file, right-click the waveform graph and select **Export Data** from the drop-down menu that appears. A **Save** dialog box is displayed, prompting you to save the data to an appropriate folder location.

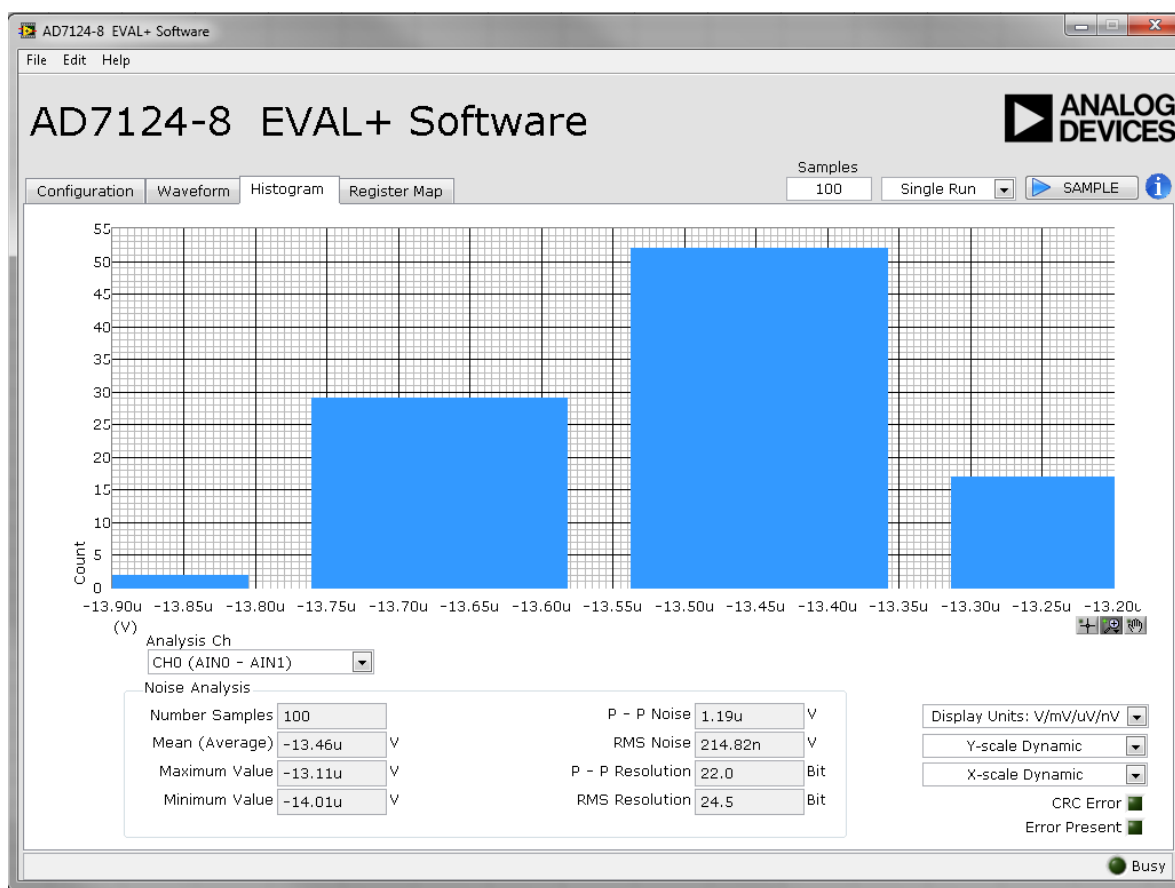
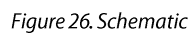


Figure 25. Example of the **Histogram** Tab After Running a Noise Test

13305-026



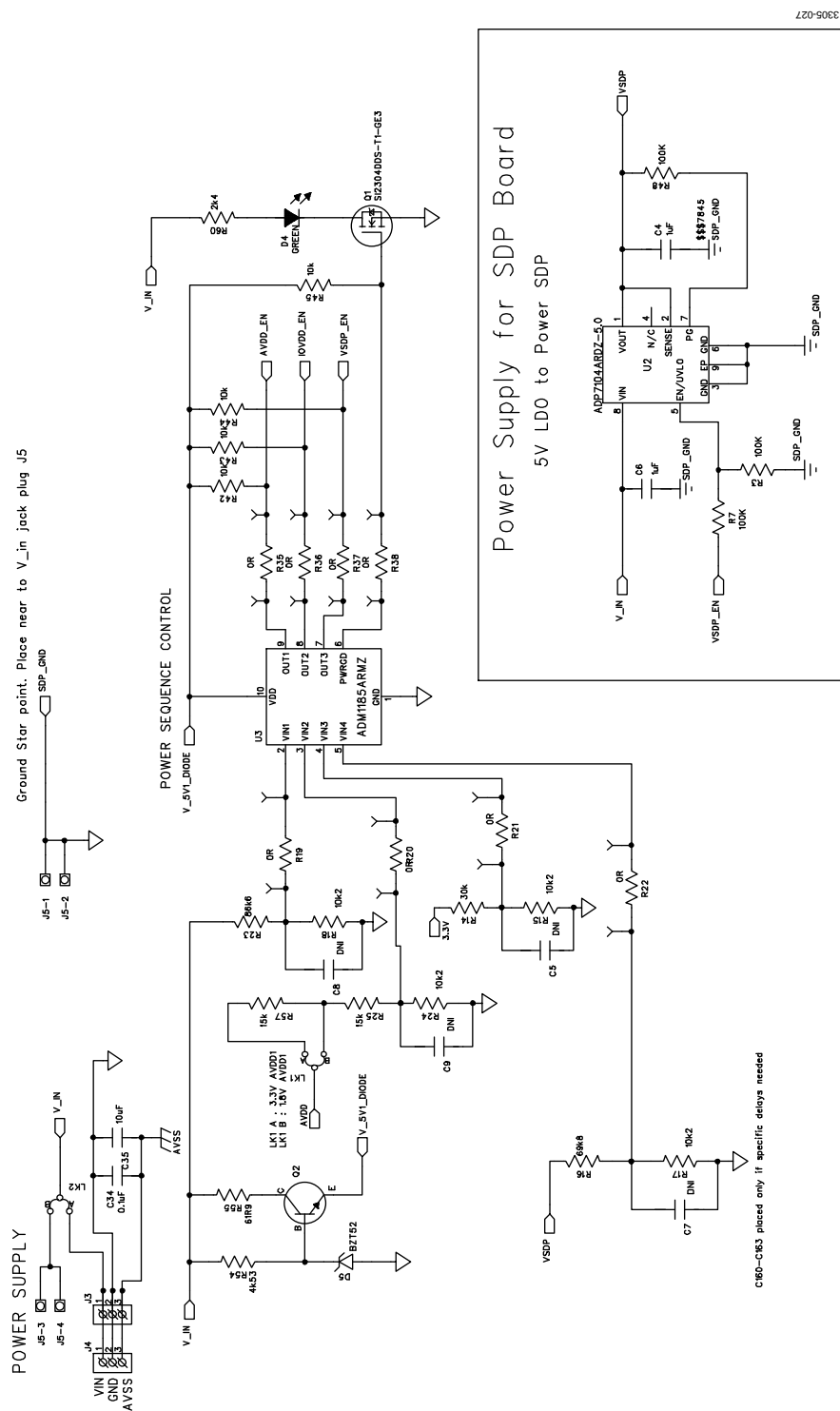


Figure 27. Schematic—Power Supply

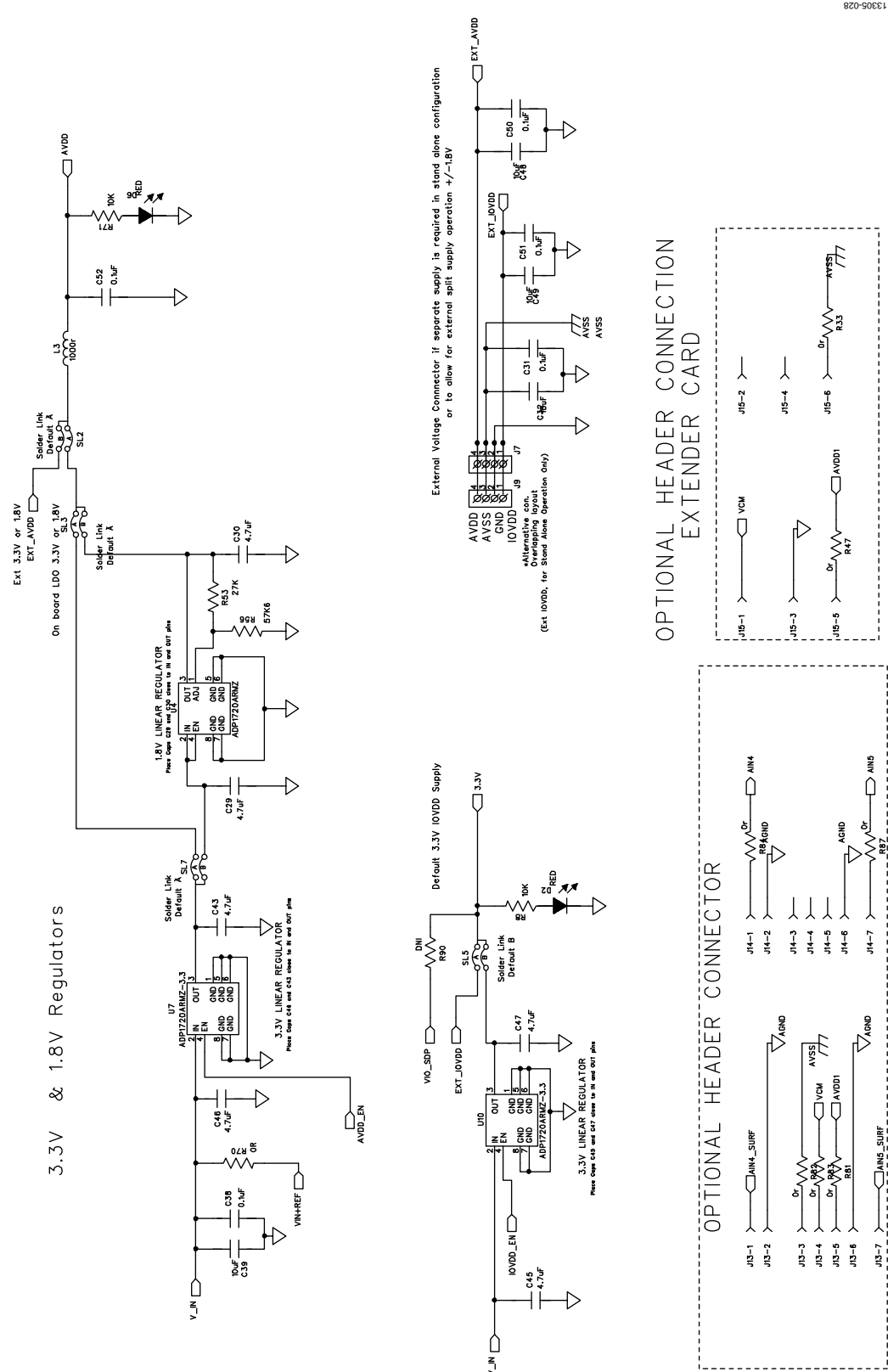


Figure 28. Schematic—Regulators

SDP CONNECTOR EEPROM-SW/USB ID

VIO: USE to set IO voltage max draw 20mA

VIN: Use this pin to power the SDP requires 4-7V 200mA

BMODE: Pull up with a 10K resistor to set SDP to boot from a SPI FLASH on the daughter board

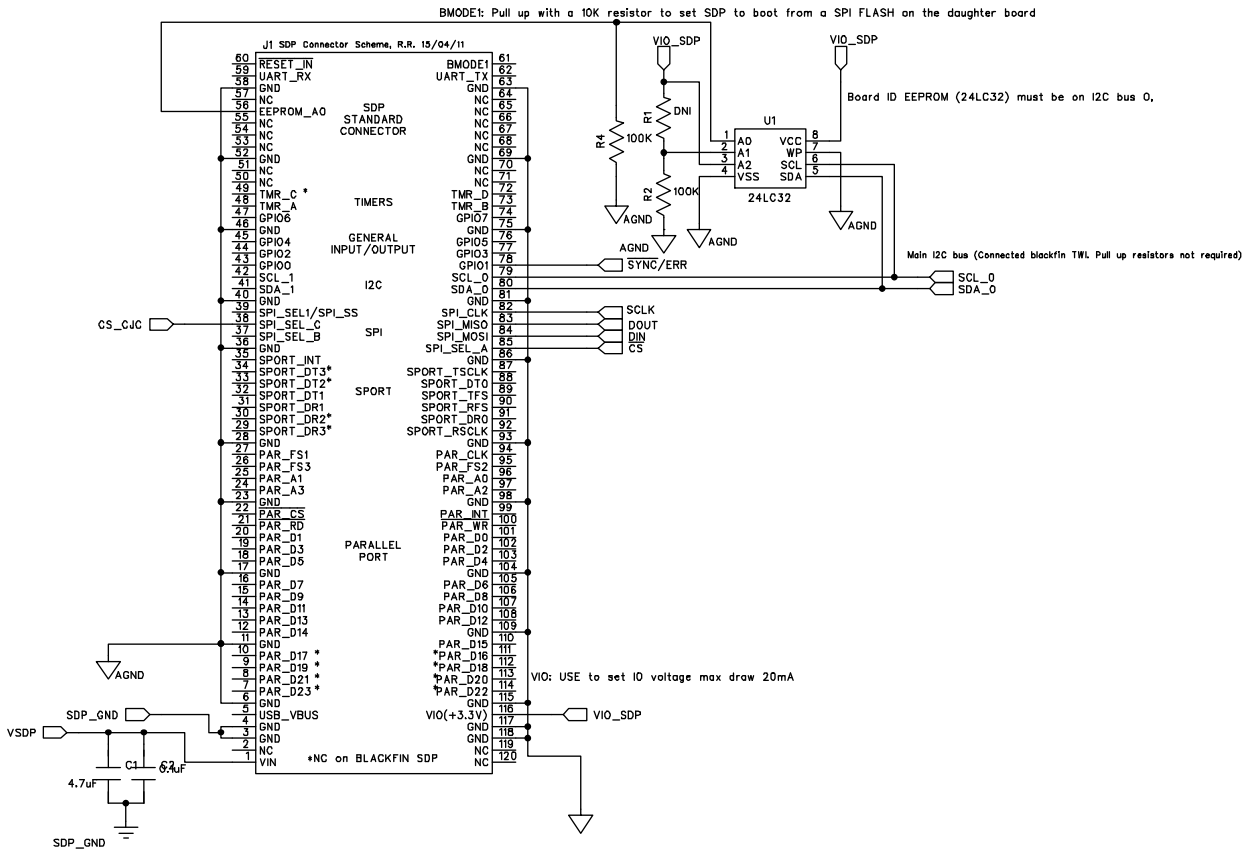


Figure 29. Schematic—SDP

13305-029

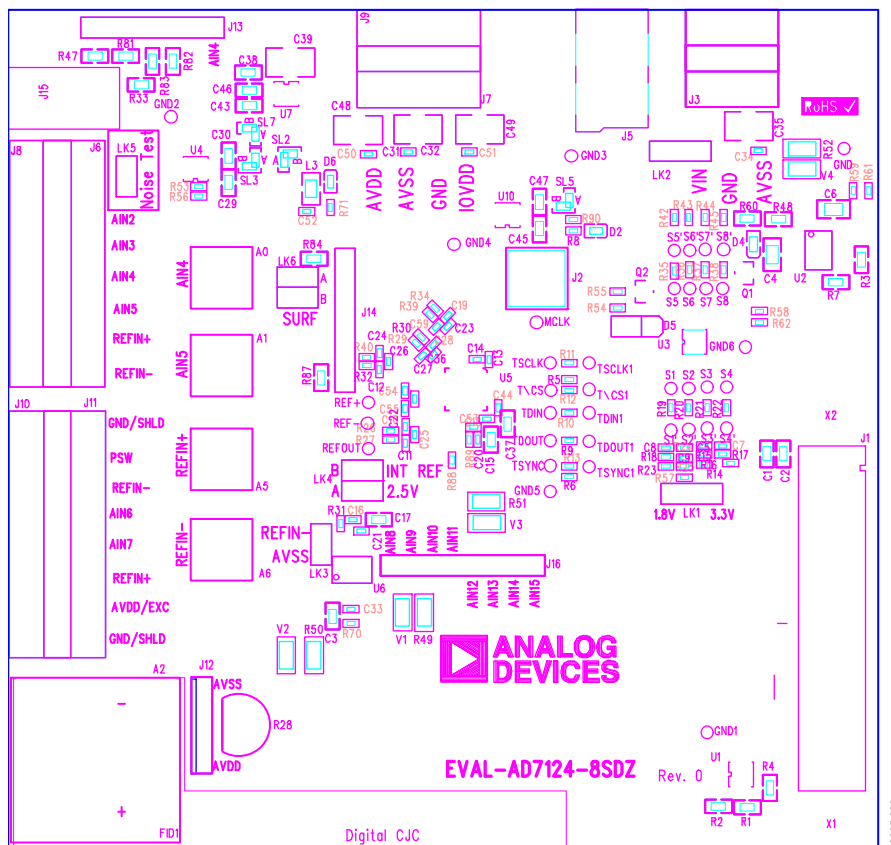


Figure 30. Top Printed Circuit Board (PCB) Silkscreen

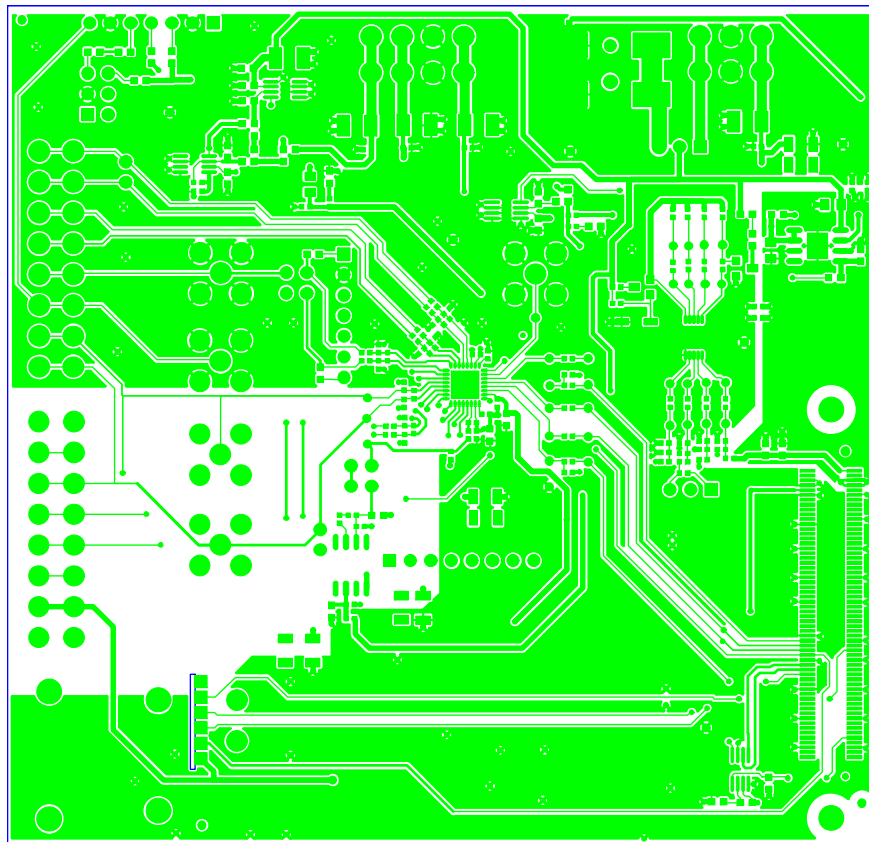


Figure 31. Layer 1 Component Side

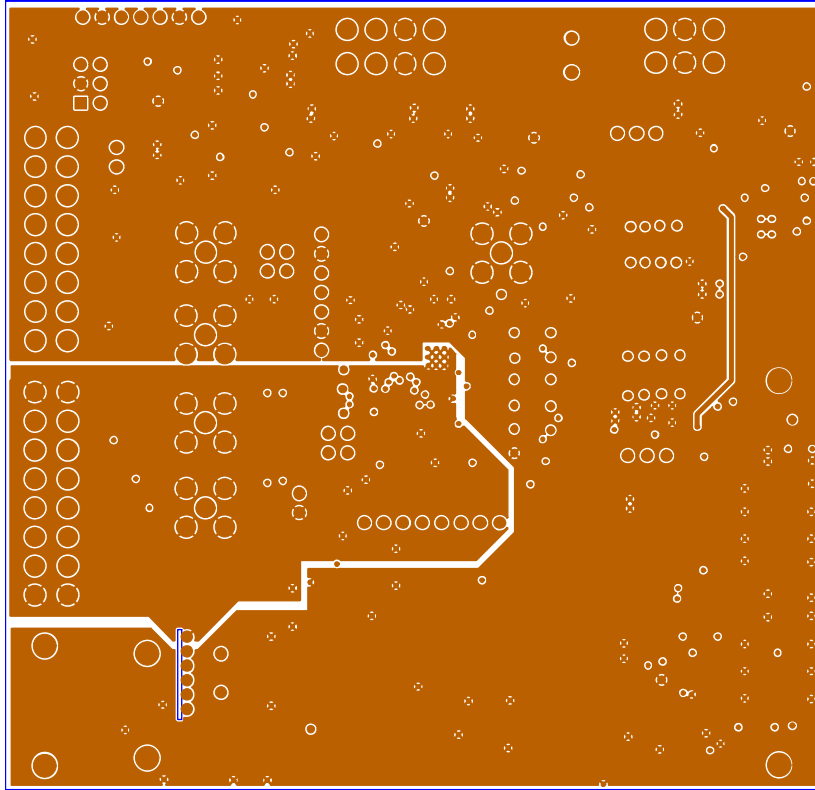


Figure 32. Layer 2 Ground Plane

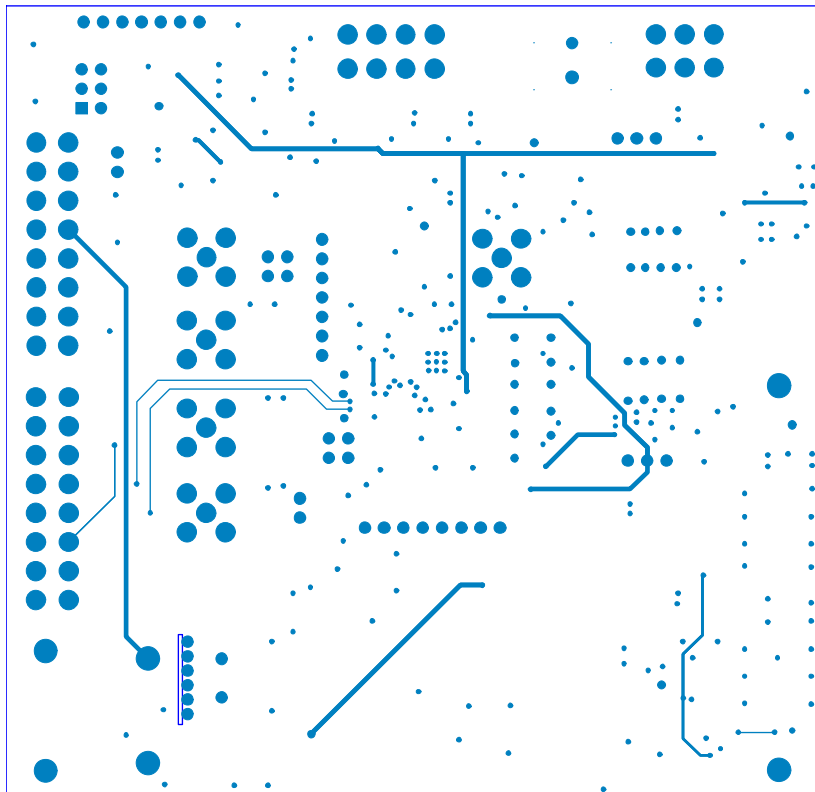


Figure 33. Layer 3 Power/Ground Plane

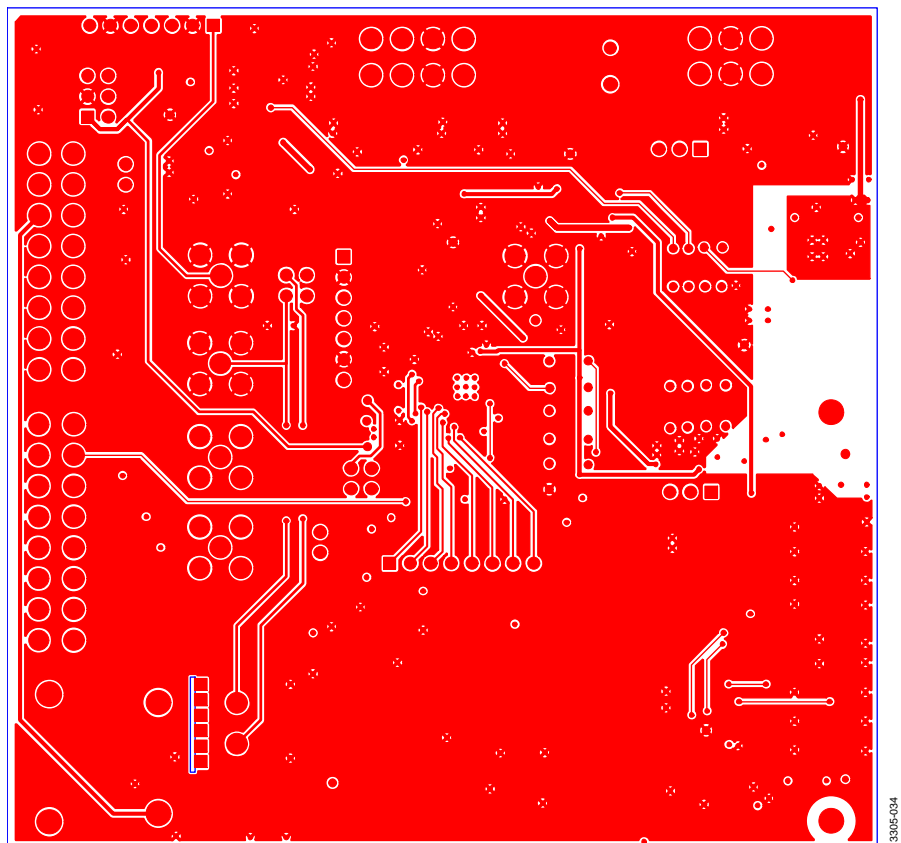


Figure 34. Layer 4 Component Side

BILL OF MATERIALS

Table 4.¹

| Reference Designator | Description | Manufacturer | Part Number | Stock Code |
|---|---|--------------------|-------------------------------|---------------------------|
| A0, A1, A5, A6, J2 | Straight PCB mount SMB jack, keep hole clear of solder | Tyco | 1-1337482-0 | Do Not Insert |
| A2 | Miniature thermocouple connector | Omega | PCC-SMP-U-50 | Do Not Insert |
| C1, C17, C29, C30, C43, C47 | Ceramic capacitor, 6.3 V, X5R, 0603, 4.7 μ F, \pm 10% | Murata | GRM188R60J475K | FEC 173-5527 |
| C2, C22, C25, C26, C36, C38, C54, C55 | Ceramic capacitor, 50 V, X7R, 0603, 0.1 μ F, \pm 10% | Murata | GRM188R71H104K | FEC 882-0023 |
| C3, C45, C46 | Ceramic capacitor, 10 V, X5R, 0603, 4.7 μ F, \pm 10% | KEMET | C0603C475K8PACTU | FEC 157-2625 |
| C4, C6 | Capacitor, 0805, 1 μ F, 50V, X7R, 1 μ F, \pm 10% | Murata | GRM21BR71H105KA12L | FEC 173-5541 |
| C5, C7, C8, C9, C16 | Ceramic capacitor, not inserted, 0402 | N/A | N/A | Do Not Insert |
| C10-C12, C24, C27, C28 | Ceramic capacitor, 50 V, NPO, 0603, 0.01 μ F | Phycomp | 2238 586 15636 | FEC 722-236 |
| C13, C14, C18, C20, C21, C31, C33, C34, C44, C50 to C53 | Ceramic capacitor, 16 V, X7R, 0402, 0.1 μ F, \pm 10% | Murata | GRM155R71C104K | FEC 881-9742 |
| C15, C37 | Capacitor, 6.3 V, 1 μ F, \pm 10% | Murata | GRM188R70J105KA01D | FEC 184-5765 |
| C19, C59 | Ceramic capacitor, 25 V, NPO, 0603, 0.01 μ F | N/A | N/A | Do Not Insert |
| C23 | Ceramic capacitor, 50 V, NPO, 0603, 0.1 μ F | N/A | N/A | Do Not Insert |
| C32, C35, C39, C48, C49 | Ceramic capacitor, 50 V, X5R, 1210, 10 μ F | Murata | GRM32ER61H106K | FEC 184-5764 |
| D2, D6 | Red LED, high intensity (>90 mCd), 0603 | Avago Technologies | HSMC-C191 | FEC 855-8528 |
| D4 | LED, SMD green | OSRAM | LGQ971 | Digikey 475-1409-1-ND |
| D5 | Zener diode, 0.5 W, 5.1 V, BZT52 | Vishay | BZT52B5V1-V-GS08 | FEC 161-7767 |
| GND to GND6, MCLK, REF+, REF-, REFOUT, S1-S8, TDIN, TDIN1, TDOUT, TDOUT1, TSCLK, TSCLK1, TSYNC, TSYNC1, TVCS, TVCS1 | Test point, not inserted, keep hole clear of solder | N/A | N/A | Do Not Insert |
| J1 | 120-way connector, 0.6 mm pitch | Hirose | FX8-120S-SV(21) | FEC 132-4660 |
| J3 | Socket terminal block, pitch 3.81 mm | Phoenix Contact | MC 1.5/3-G-3.81 | FEC 370-4737 |
| J4 | Screw terminal block, pitch 3.81 mm | Phoenix Contact | 1727023 | Do Not Insert |
| J5 | DC power connectors 2 mm SMT power jack | Kycon | KLDX-SMT2-0202-A | MOUSER 806-KLDX-SMT20202A |
| J6, J11 | 8-pin terminal header, pitch 3.81 mm, vertical | Phoenix Contact | MC 1,5/ 8-G-3,81 | FEC 370-4774 |
| J7 | Connector, pitch 3.81 mm, right angle, 1 \times 4-pin | Phoenix Contact | MC 1,5/ 4-G-3,81 and 180-3594 | Do Not Insert |
| J8, J10 | 8-pin terminal header, pitch 3.81 mm, vertical | Phoenix Contact | 1727078 | Do Not Insert |
| J9 | Screw terminal block, pitch 3.81 mm, 1 \times 4-pin | Phoenix Contact | 1727036 | FEC 370-4592 |
| J12 | PCB pads, 6-way solder slot for Analog Devices PCB, 6-way | Aragorn | ADT7320-CJC-PCB | ADT7320-CJC-PCB |
| J13 | 7-way SSW 2.54 mm vertical socket | Samtec | SSW-107-01-T-S | FEC 180-3478 |

| Reference Designator | Description | Manufacturer | Part Number | Stock Code |
|--|--|------------------|--------------------------|--|
| J14 | 7-way sip 2.54 mm TH header | Samtec | TLW-107-05-G-S | FEC 166-8499 |
| J15 | Do not insert | N/A | N/A | Do Not Insert |
| L3 | Ferrite bead, 0.3 Ω at DC, 1000 Ω at 100 MHz, 350 mA, 0805 | Tyco | BMB2A1000LN2 | FEC 119-3421 |
| LK1, LK2 | 3-pin (3 \times 1) 0.1" header and shorting block in Position A | Harwin | M20-9990346 and M7566-05 | FEC 102-2249 and 150-411 |
| LK3, LK5 | 2-pin (0.1" pitch) header and shorting shunt | Harwin | M20-9990246 | FEC 102-2247 and 150-411 |
| LK4, LK6 | 4-pin (2 \times 2) 0.1" header and shorting block | Harwin | M20-9983646 and M7566-05 | FEC 1022244 and 150-411 (36 Pin Strip) |
| Q1 | MOSFET transistor | Vishay Siliconix | SI2304DDS-T1-GE3 | FEC 185-8939 |
| Q2 | Transistor, NPN, SOT-23 | ON Semiconductor | MMBT3904LT1G | FEC 145-9100 |
| R1 | Resistor, not inserted, 0603 | N/A | N/A | Do Not Insert |
| R2 to R4, R7, R48 | SMD resistor, 100 k Ω , 1% | Multicomp | MC 0.063W 0603 1% 100K | FEC 933-0402 |
| R5, R6, R8, R71 | Resistor, 1%, 0402, 10 k Ω | Phycomp | CRCW040210K0 FKEAHP | FEC 173-8864 |
| R9 to R13, R19 to R22, R35 to R38, R58, R59, R61, R62, R70 | Resistor, 0402, 0 Ω , 1% | Vishay | CRCW04020000 Z0ED | FEC 146-9661 |
| R14 | Resistor, 0402, 1%, 30 k Ω | Multicomp | MC 0.0625W 0402 1% 30K | FEC 135-8082 |
| R15, R17, R18, R24 | SMD Resistor, 10.2 k Ω , 1% | Multicomp | MC 0.0625W 0402 1% 10K2 | FEC 180-3137 |
| R16 | Resistor, 0402, 1%, 69.8 k Ω | Multicomp | MC 0.0625W 0402 1% 69K8 | FEC 180-3735 |
| R23 | Resistor, 0402, 1%, 86.6 k Ω | Multicomp | MC 0.0625W 0402 1% 86K6 | FEC 180-3744 |
| R25, R57 | Resistor, 0402, 1%, 15 k Ω | Multicomp | MC 0.0625W 0402 1% 15k | FEC 1358073 |
| R26, R27, R29, R30, R32, R40 | Resistor, 0603, 1 Ω , 1% | Multicomp | MC 0.063W 0603 1% 1K | FEC 933-0380 |
| R28 | Thermistor, 1950 Ω to 1990 Ω | Infineon | Q62705-K110 | Philips (Arrow) KTY81/110 |
| R3, R901 | Resistor, not inserted, 0402 | N/A | N/A | Do Not Insert |
| R33, R34, R39, R47, R81 to R84, R87, R89 | Resistor, 0603, 0 Ω , 1% | Vishay Draloric | CRCW06030000 Z0EA | FEC 146-9739 |
| R42 to R45 | Resistor, thick film, 10 k Ω , 62.5 mW, 5% | Yageo | RC0402JR-1310KL | FEC 179-9316 |
| R49 to R52 | Resistor, 1206, 0 Ω , 5% | Multicomp | MC 0.125W 1206 0R | FEC 933-6974 |
| R53 | Resistor, 0402, 27 k Ω , 1% | Multicomp | MC 0.0625W 0402 1% 27K | FEC 135-8081 |
| R54 | Resistor, thick film, 4.53 k Ω , 63 mW, 1% | Vishay Dale | CRCW04024K53 FKED | FEC 115-1244 |
| R55 | Resistor, 0402, 1%, 61.9 Ω | Multicomp | MC 0.0625W 0402 1% 61R9 | FEC 180-2915 |
| R56 | Resistor, 0402, 57.6 k Ω , 1% | Multicomp | MC 0.0625W 0402 1% 57K6 | FEC 185-1295 |
| R60 | Resistor, thick film, 2.4 k Ω , 0603, 100 mW, 1% | Yageo | RC0603FR-072K4L | FEC 179-9329 |
| R88 | Resistor, 0603, not inserted | N/A | N/A | Do Not Insert |

| Reference Designator | Description | Manufacturer | Part Number | Stock Code |
|----------------------|--|----------------|------------------------------------|------------------------------------|
| SL2, SL3, SL7 | 2-way solder link (use 0 Ω , 0603 resistor) | N/A | Insert in Link Position "A" | FEC 933-1662 |
| SL5 | 2-way solder link (use 0 Ω , 0603 resistor) | N/A | Insert in Link Position "B" | FEC 933-1662 |
| STAR3 | Ground link | N/A | N/A | N/A |
| U1 | 32 k I ² C serial EEPROM | Microchip | 24LC32A-I/MS | FEC133-1330 |
| U2 | Linear regulator 5 V, 20 V, 500 mA, ultralow noise, CMOS | Analog Devices | ADP7104ARDZ-5.0 | ADP7104ARDZ-5.0 |
| U3 | Quad voltage monitor and sequencer | Analog Devices | ADM1185ARMZ-1 | ADM1185ARMZ-1 |
| U4 | 50 mA, high voltage, micropower linear regulator, ADJ | Analog Devices | ADP1720ARMZ-R7 | ADP1720ARMZ-R7 |
| U5 | 8-channel, low power, low noise, Σ - Δ ADC | Analog Devices | AD7124-8BCPZ | AD7124-8BCPZ |
| U6 | 2.5 V low noise reference | Analog Devices | ADR4525BRZ | ADR4525BRZ |
| U7, U10 | 50 mA, high voltage, micropower linear regulator 3.3 V | Analog Devices | ADP1720ARMZ-3.3-R7 | ADP1720ARMZ-3.3-R7 |
| V1 to V4 | 1206, place holder | N/A | N/A | Do Not Insert |

¹ N/A means not applicable.

NOTES

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

**ESD Caution**

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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