S-19502/19503 Series

AUTOMOTIVE, 125°C OPERATION, 36 V INPUT, 400 mA, BUILT-IN WATCHDOG TIMER VOLTAGE REGULATOR WITH RESET FUNCTION

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The S-19502/19503 Series, developed by using high-withstand voltage CMOS technology, is a low dropout positive voltage regulator with the watchdog timer and the reset function, which has high-withstand voltage. The monitoring time of watchdog timer can be adjusted by an external capacitor. Moreover, a voltage detection circuit which monitors the output voltage is also prepared.

ABLIC Inc. offers a "thermal simulation service" which supports the thermal design in conditions when our power management ICs are in use by customers. Our thermal simulation service will contribute to reducing the risk in the thermal design at customers' development stage.
ABLIC Inc. also offers FIT rate calculated based on actual customer usage conditions in order to support customer functional safety design.
Contact our sales representatives for details.

Caution **This product can be used in vehicle equipment and in-vehicle equipment. Before using the product for these purposes, it is imperative to contact our sales representatives.**

■ Features

Regulator block

- Output voltage: 3.0 V to 5.3 V, selectable in 0.1 V step
- Input voltage: 4.0 V to 36.0 V
- Output voltage accuracy: ±2.0% (T_j = –40°C to +150°C)
- Dropout voltage: 120 mV typ. (5.0 V output product, I_{OUT} = 100 mA)
- Output current: Possible to output 400 mA (V_{IN} = $V_{OUT(S)}$ + 1.0 V)*1
- Input and output capacitors: A ceramic capacitor of 2.2 µF or more can be used.
- Ripple rejection: 70 dB typ. (f = 100 Hz)
- Built-in overcurrent protection circuit: Limits overcurrent of output transistor.
- Built-in thermal shutdown circuit: Detection temperature 170°C typ.

Detector block

- Detection voltage: 2.6 V to 5.0 V, selectable in 0.1 V step
- Detection voltage accuracy: ±100 mV (T_j = –40°C to +150°C)
- Hysteresis width: 0.12 V min.
- Release delay time is adjustable*2: 18 ms typ. (C_{DLY} = 47 nF)

Watchdog timer block

- Watchdog activation current is adjustable: 1.5 mA typ. (WADJ pin is open)
- Watchdog trigger time is adjustable*2: 43 ms typ. (C_{DLY} = 47 nF)
- Product type is selectable: S-19502 Series (Product with WEN pin (Output: WO / RO pin))
  S-19503 Series (Product without WEN pin (Output: WO pin and RO pin))
- Autonomous watchdog operation function: Watchdog timer operates due to detection of load current.
- Watchdog mode: Time-out mode

Overall

- Current consumption: 60 µA typ. (I_{OUT} = 0 mA, During the watchdog timer deactivation)
  75 µA typ. (I_{OUT} ≤ 5 mA, During the watchdog timer activation)
- Operation temperature range: Ta = –40°C to +125°C
- Lead-free (Sn 100%), halogen-free
- Withstand 45 V load dump
- AEC-Q100 qualified*3

***1.** Please make sure that the loss of the IC will not exceed the power dissipation when the output current is large.
***2.** The release delay time and the watchdog trigger time can be adjusted by connecting C_{DLY} to the DLY pin.
***3.** Contact our sales representatives for details.

■ Applications

- Constant-voltage power supply for automotive electric component, monitoring of microcontroller

■ Packages

- TO-252-9S
- HSOP-8A

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■ Block Diagrams

1. S-19502 Series (Product with WEN pin)

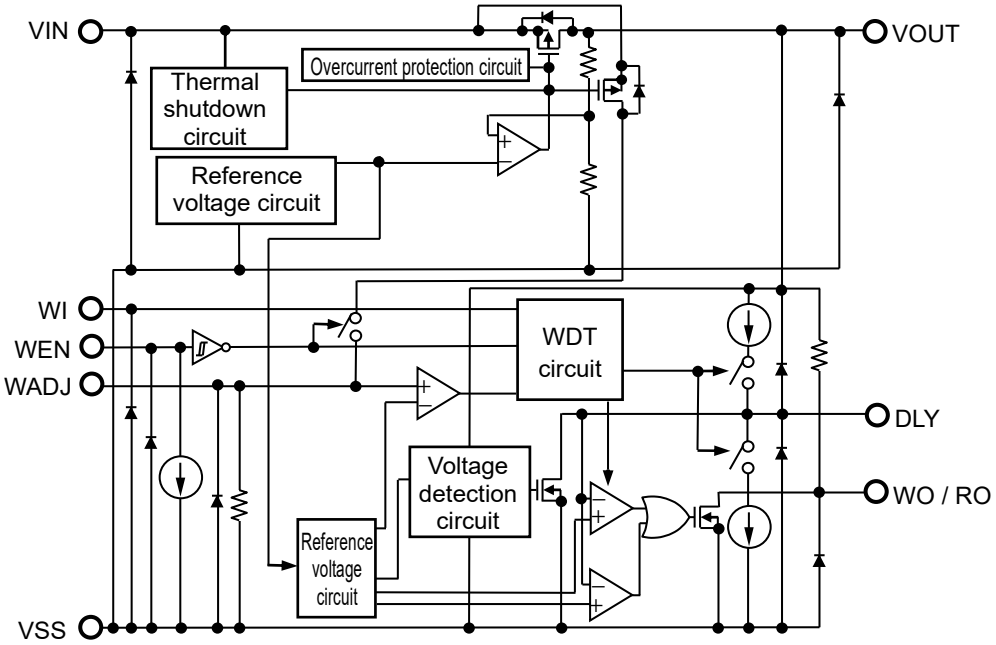


Figure 1

2. S-19503 Series (Product without WEN pin)

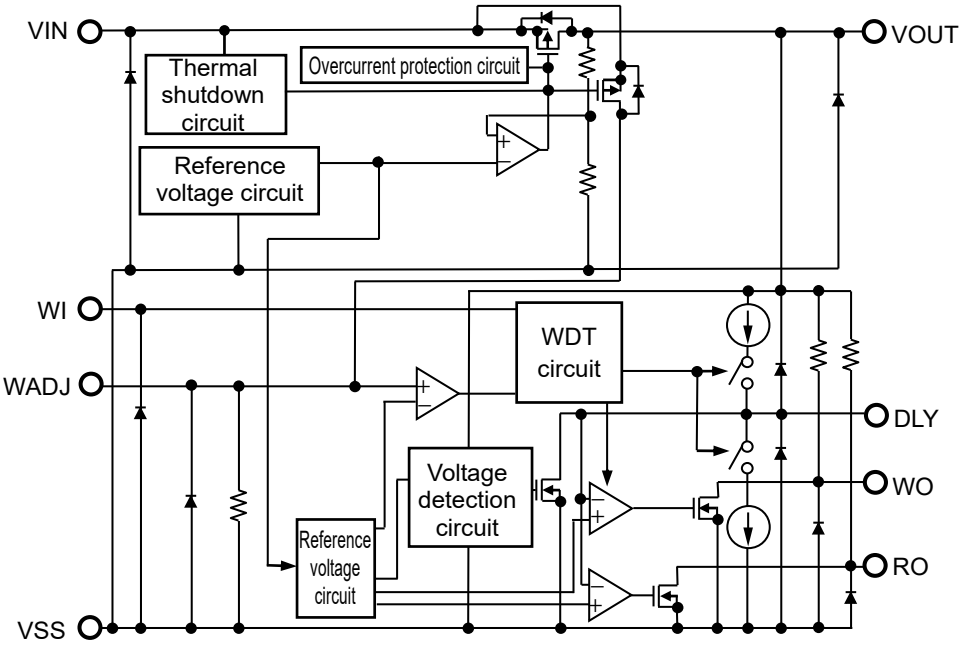


Figure 2

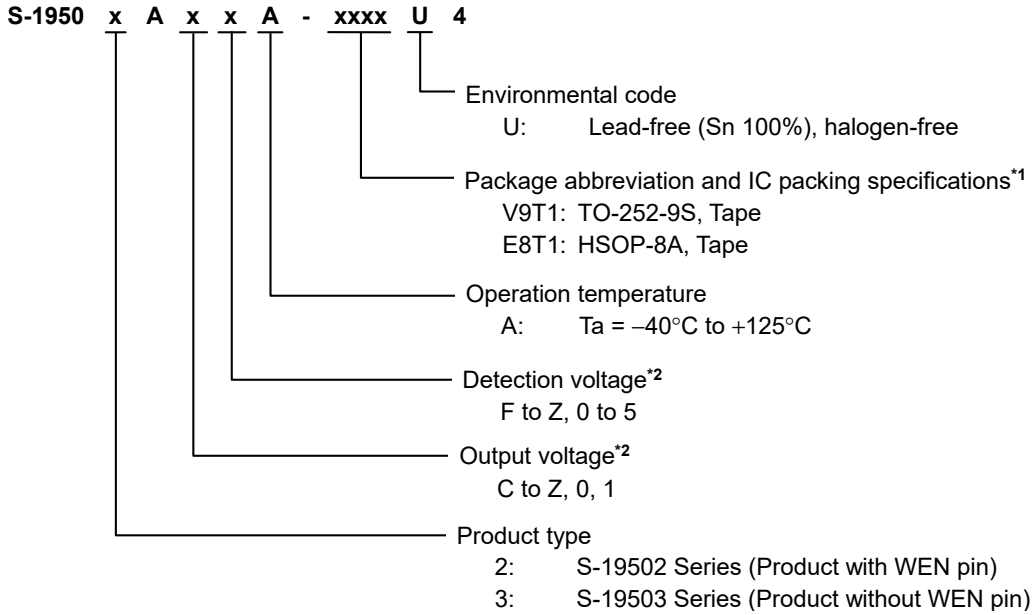
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■ AEC-Q100 Qualified

This IC supports AEC-Q100 for the operation temperature grade 1.
Contact our sales representatives for details of AEC-Q100 reliability specification.

■ Product Name Structure

1. Product name



***1.** Refer to the tape drawing.
***2.** Refer to "**2. Product option list**".

2. Product option list

Table 1 Output Voltage

Set Output Voltage	Symbol
5.3 V	C
5.2 V	D
5.1 V	E
5.0 V	F
4.9 V	G
4.8 V	H
4.7 V	J
4.6 V	K
4.5 V	L
4.4 V	M
4.3 V	N
4.2 V	P

Set Output Voltage	Symbol
4.1 V	Q
4.0 V	R
3.9 V	S
3.8 V	T
3.7 V	U
3.6 V	V
3.5 V	W
3.4 V	X
3.3 V	Y
3.2 V	Z
3.1 V	0
3.0 V	1

Table 2 Detection Voltage

Set Detection Voltage	Symbol
5.0 V	F
4.9 V	G
4.8 V	H
4.7 V	J
4.6 V	K
4.5 V	L
4.4 V	M
4.3 V	N
4.2 V	P
4.1 V	Q
4.0 V	R
3.9 V	S
3.8 V	T

Set Detection Voltage	Symbol
3.7 V	U
3.6 V	V
3.5 V	W
3.4 V	X
3.3 V	Y
3.2 V	Z
3.1 V	0
3.0 V	1
2.9 V	2
2.8 V	3
2.7 V	4
2.6 V	5

Remark Set output voltage ≥ Set detection voltage + 0.3 V

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3. Packages

Table 3 Package Drawing Codes

Package Name	Dimension	Tape	Reel	Land
TO-252-9S	VA009-A-P-SD	VA009-A-C-SD	VA009-A-R-SD	VA009-A-L-SD
HSOP-8A	FH008-A-P-SD	FH008-A-C-SD	FH008-A-R-SD	FH008-A-L-SD

4. Product name list

4. 1 S-19502 Series (Product with WEN pin)

Table 4

Output Voltage	Detection Voltage	TO-252-9S	HSOP-8A
3.3 V ± 2.0%	2.8 V ± 0.1 V	S-19502AY3A-V9T1U4	–
3.3 V ± 2.0%	2.9 V ± 0.1 V	S-19502AY2A-V9T1U4	S-19502AY2A-E8T1U4
5.0 V ± 2.0%	4.6 V ± 0.1 V	S-19502AFKA-V9T1U4	S-19502AFKA-E8T1U4
5.0 V ± 2.0%	4.7 V ± 0.1 V	S-19502AFJA-V9T1U4	–

Remark Please contact our sales representatives for products other than the above.

4. 2 S-19503 Series (Product without WEN pin)

Table 5

Output Voltage	Detection Voltage	TO-252-9S	HSOP-8A
3.3 V ± 2.0%	2.8 V ± 0.1 V	S-19503AY3A-V9T1U4	–
3.3 V ± 2.0%	2.9 V ± 0.1 V	S-19503AY2A-V9T1U4	S-19503AY2A-E8T1U4
5.0 V ± 2.0%	4.6 V ± 0.1 V	S-19503AFKA-V9T1U4	S-19503AFKA-E8T1U4
5.0 V ± 2.0%	4.7 V ± 0.1 V	S-19503AFJA-V9T1U4	–

Remark Please contact our sales representatives for products other than the above.

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■ Pin Configurations

1. TO-252-9S

Top view

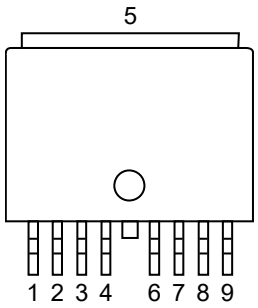


Figure 3

Table 6 S-19502 Series (Product with WEN pin)

Pin No.	Symbol	Description	
1	VOUT	Voltage output pin (Regulator block)	
2	WADJ	Connection pin for watchdog activation threshold current adjustment resistor	
3	DLY	Connection pin for release delay time and monitoring time adjustment capacitor	
4	NC*1	No connection	
5	VSS	GND pin	
6	WO / RO*2	WO	Watchdog output pin
		RO	Reset output pin
7	WEN	Watchdog enable pin	
8	WI	Watchdog input pin	
9	VIN	Voltage input pin (Regulator block)	

Table 7 S-19503 Series (Product without WEN pin)

Pin No.	Symbol	Description
1	VOUT	Voltage output pin (Regulator block)
2	WADJ	Connection pin for watchdog activation threshold current adjustment resistor
3	DLY	Connection pin for release delay time and monitoring time adjustment capacitor
4	NC*1	No connection
5	VSS	GND pin
6	RO	Reset output pin
7	WO	Watchdog output pin
8	WI	Watchdog input pin
9	VIN	Voltage input pin (Regulator block)

***1.** The NC pin is electrically open.
The NC pin can be connected to the VIN pin or the VSS pin.
***2.** The WO / RO pin combines the watchdog output pin and the reset output pin.

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2. HSOP-8A

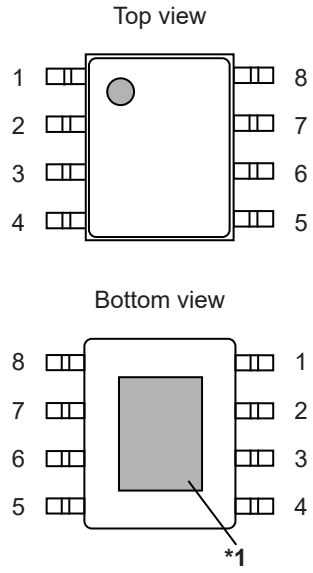


Figure 4

Table 8 S-19502 Series (Product with WEN pin)

Pin No.	Symbol	Description	
1	VOUT	Voltage output pin (Regulator block)	
2	WADJ	Connection pin for watchdog activation threshold current adjustment resistor	
3	VSS	GND pin	
4	DLY	Connection pin for release delay time and monitoring time adjustment capacitor	
5	WO / RO*2	WO	Watchdog output pin
		RO	Reset output pin
6	WEN	Watchdog enable pin	
7	WI	Watchdog input pin	
8	VIN	Voltage input pin (Regulator block)	

Table 9 S-19503 Series (Product without WEN pin)

Pin No.	Symbol	Description
1	VOUT	Voltage output pin (Regulator block)
2	WADJ	Connection pin for watchdog activation threshold current adjustment resistor
3	VSS	GND pin
4	DLY	Connection pin for release delay time and monitoring time adjustment capacitor
5	RO	Reset output pin
6	WO	Watchdog output pin
7	WI	Watchdog input pin
8	VIN	Voltage input pin (Regulator block)

***1.** Connect the heat sink of backside at shadowed area to the board, and set electric potential GND.
However, do not use it as the function of electrode.

***2.** The WO / RO pin combines the watchdog output pin and the reset output pin.

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■ Absolute Maximum Ratings

Table 10

(T_j = –40°C to +150°C unless otherwise specified)

Item	Symbol	Absolute Maximum Rating	Unit
VIN pin voltage	V_{IN}	V_{SS} – 0.3 to V_{SS} + 45.0	V
VOUT pin voltage	V_{OUT}	V_{SS} – 0.3 to V_{IN} + 0.3 ≤ V_{SS} + 7.0	V
DLY pin voltage	V_{DLY}	V_{SS} – 0.3 to V_{OUT} + 0.3 ≤ V_{SS} + 7.0	V
RO pin voltage	V_{RO}	V_{SS} – 0.3 to V_{OUT} + 0.3 ≤ V_{SS} + 7.0	V
WADJ pin voltage	V_{WADJ}	V_{SS} – 0.3 to V_{IN} + 0.3 ≤ V_{SS} + 7.0	V
WEN pin voltage	V_{WEN}	V_{SS} – 0.3 to V_{SS} + 7.0	V
WI pin voltage	V_{WI}	V_{SS} – 0.3 to V_{SS} + 7.0	V
WO pin voltage	V_{WO}	V_{SS} – 0.3 to V_{OUT} + 0.3 ≤ V_{SS} + 7.0	V
WO / RO pin voltage	$V_{WO / RO}$	V_{SS} – 0.3 to V_{OUT} + 0.3 ≤ V_{SS} + 7.0	V
Output current	I_{OUT}	520	mA
Junction temperature	T_j	–40 to +150	°C
Operation ambient temperature	T_{opr}	–40 to +125	°C
Storage temperature	T_{stg}	–40 to +150	°C

Caution **The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.**

■ Thermal Resistance Value

Table 11

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Junction-to-ambient thermal resistance*1	θ_{JA}	TO-252-9S	Board A	–	88	–	°C/W
			Board B	–	63	–	°C/W
			Board C	–	37	–	°C/W
			Board D	–	31	–	°C/W
			Board E	–	28	–	°C/W
		HSOP-8A	Board A	–	104	–	°C/W
			Board B	–	74	–	°C/W
			Board C	–	39	–	°C/W
			Board D	–	37	–	°C/W
			Board E	–	31	–	°C/W

***1.** Test environment: compliance with JEDEC STANDARD JESD51-2A

Remark Refer to "■ **Power Dissipation**" and "**Test Board**" for details.

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■ Recommended Operation Conditions

Table 12

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
VIN pin voltage	V_{IN}	–		4.0	–	36.0	V
		When using autonomous watchdog operation function*1		$V_{OUT(S)}$ + 1.0	–	36.0	V
VOUT pin voltage	V_{OUT}	Detector block		1.0	–	–	V
		Watchdog timer block		$+V_{DET}$	–	–	V
Watchdog input voltage "H"*2	V_{WIH}	–		2	–	–	V
Watchdog input voltage "L"*2	V_{WIL}	–		–	–	0.8	V
Watchdog input "H" time*2	t_{high}	$V_{WI} \geq V_{WIH}$		5.0	–	–	µs
Watchdog input "L" time*2	t_{low}	$V_{WI} \leq V_{WIL}$		5.0	–	–	µs
Slew rate*2	$\frac{dV_{WI}}{dt}$	$V_{WI} = V_{WIL} + (V_{WIH} - V_{WIL}) \times 0.1$ to $V_{WIL} + (V_{WIH} - V_{WIL}) \times 0.9$		1	–	–	V/µs
Watchdog input frequency	f_{WI}	Duty ratio 50%		–	–	0.2	MHz
WEN pin input voltage "H"	V_{WENH}	S-19502 Series		2.0	–	$V_{OUT(S)}$	V
WEN pin input voltage "L"	V_{WENL}	S-19502 Series		0	–	0.8	V
Input capacitance	C_{IN}	–		2.2	–	–	µF
Output capacitance	C_L	–		2.2	–	–	µF
Equivalent series resistance	R_{ESR}	Output capacitor (C_L)		–	–	50	Ω
Release delay time and monitoring time adjustment capacitance*3	C_{DLY}	–		1	47	–	nF
Watchdog activation threshold current adjustment resistance*4	$R_{WADJ,ext}$	Connected to WADJ pin		10	–	–	kΩ
External pull-up resistances for output pins	R_{extW}	S-19503 Series	Connected to WO pin	3	–	–	kΩ
	R_{extR}	S-19502 Series	Connected to WO / RO pin	3	–	–	kΩ
		S-19503 Series	Connected to RO pin	3	–	–	kΩ

***1.** Refer to "**3. Watchdog timer block**" in "**■ Operation**" for the autonomous watchdog operation function.

***2.** When inputting a rising edge that satisfies the condition of **Figure 5** to the WI pin, the watchdog timer detects a trigger.
The signal input from the monitored object by the watchdog timer should satisfy the condition of **Figure 5**.

***3.** Refer to "**2. Release delay time and monitoring time adjustment capacitor (C_{DLY})**" in "**■ Selection of External Parts**" for the details.

***4.** Refer to "**3. Watchdog activation threshold current adjustment resistor ($R_{WADJ,ext}$)**" in "**■ Selection of External Parts**" for the details.

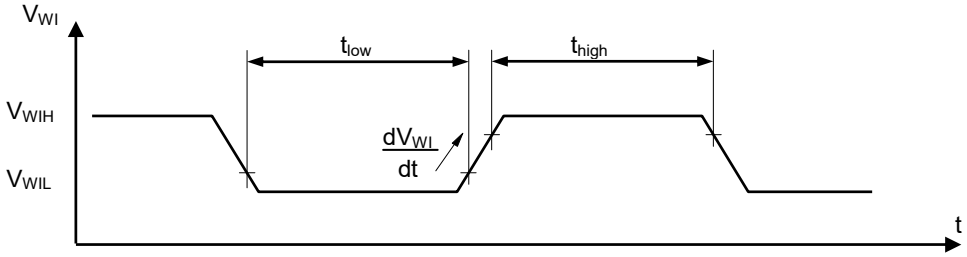


Figure 5

Caution 1. Generally a series regulator may cause oscillation, depending on the selection of external parts. Confirm that no oscillation occurs in the actual application using capacitors that meet the above C_{IN}, C_L, and R_{ESR}.
2. Define the external pull-up resistance by sufficient evaluation including the temperature characteristics under the actual usage conditions.

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■ Electrical Characteristics

1. Regulator block

Table 13

(V_{IN} = 13.5 V, T_j = –40°C to +150°C unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
Output voltage*1	$V_{OUT(E)}$	V_{IN} = 13.5 V, I_{OUT} = 30 mA	$V_{OUT(S)}$ – 2.0%	$V_{OUT(S)}$	$V_{OUT(S)}$ + 2.0%	V	1
Output current*2	I_{OUT}	$V_{IN} \geq V_{OUT(S)}$ + 1.0 V	400*7	–	–	mA	2
Dropout voltage*3	V_{drop}	I_{OUT} = 100 mA, Ta = +25°C, $V_{OUT(S)}$ = 3.0 V to 5.3 V	–	120	200	mV	1
		I_{OUT} = 200 mA, Ta = +25°C, $V_{OUT(S)}$ = 3.0 V to 5.3 V	–	240	400	mV	1
Line regulation*4	$\frac{\Delta V_{OUT1}}{\Delta V_{IN} \bullet V_{OUT}}$	$V_{OUT(S)}$ + 1.0 V ≤ V_{IN} ≤ 36.0 V, I_{OUT} = 30 mA, Ta = +25°C	–	0.02	0.10	%/V	1
Load regulation*5	ΔV_{OUT2}	V_{IN} = 13.5 V, 100 µA ≤ I_{OUT} ≤ 100 mA, Ta = +25°C	–	20	40	mV	1
Input voltage	V_{IN}	–	4.0	–	36.0	V	–
Ripple rejection	|RR|	V_{IN} = 13.5 V, I_{OUT} = 30 mA, f = 100 Hz, ΔV_{rip} = 1.0 V_{p-p}	–	70	–	dB	3
Limit current*6	I_{LIM}	V_{IN} = $V_{OUT(S)}$ + 1.0 V, V_{OUT} = 1.2 V, Ta = +25°C	480	700	950	mA	2
Short-circuit current	I_{short}	V_{IN} = 13.5 V, V_{OUT} = 0 V, Ta = +25°C	55	105	145	mA	2
Thermal shutdown detection temperature	T_{SD}	Junction temperature	–	170	–	°C	–
Thermal shutdown release temperature	T_{SR}	Junction temperature	–	135	–	°C	–

***1.** The accuracy is guaranteed when the input voltage, output current, and temperature satisfy the conditions listed above.
$V_{OUT(S)}$: Set output voltage
$V_{OUT(E)}$: Actual output voltage

***2.** The output current when increasing the output current gradually until the output voltage has reached the value of 95% of $V_{OUT(E)}$.

***3.** The difference between input voltage (V_{IN1}) and the output voltage when decreasing input voltage (V_{IN}) gradually until the output voltage has dropped out to the value of 98% of output voltage (V_{OUT3}).
V_{drop}: V_{IN1} – (V_{OUT3} × 0.98)
V_{OUT3}: Output voltage when V_{IN} = $V_{OUT(S)}$ + 1.0 V

***4.** The dependency of the output voltage against the input voltage. The value shows how much the output voltage changes due to a change in the input voltage while keeping output current constant.

***5.** The dependency of the output voltage against the output current. The value shows how much the output voltage changes due to a change in the output current while keeping input voltage constant.

***6.** The current limited by overcurrent protection circuit.

***7.** Due to limitation of the power dissipation, this value may not be satisfied. Attention should be paid to the power dissipation when the output current is large.
This specification is guaranteed by design.

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2. Detector block

Table 14

(V_{IN} = 13.5 V, T_j = –40°C to +150°C unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
Detection voltage*1	$-V_{DET}$	–	$-V_{DET(S)} - 0.1$	$-V_{DET(S)}$	$-V_{DET(S)} + 0.1$	V	4
Hysteresis width*2	V_{HYS}	–	120	150	–	mV	4
Reset output voltage "H"	V_{ROH}	–	$V_{OUT(S)} \times 0.9$	–	–	V	4
Reset output voltage "L"	V_{ROL}	$V_{OUT} \geq 1.0$ V, $R_{extR} \geq 3$ kΩ, Connected to VOUT pin	–	0.2	0.4	V	4
Reset pull-up resistance	R_{RO}	VOUT pin internal resistance	20	30	45	kΩ	–
Reset output current	I_{RO}	V_{RO} = 0.4 V, $V_{OUT} = -V_{DET(S)} - 0.1$ V	3.0	–	–	mA	5
Release delay time*3	t_{rd}	C_{DLY} = 47 nF	11	18	25	ms	4
Reset reaction time*4	t_{rr}	C_{DLY} = 47 nF	–	–	50*5	µs	4

***1.** The voltage at which the output of the RO pin turns to "L". The accuracy is guaranteed when the input voltage and temperature satisfy the listed conditions above.

$-V_{DET(S)}$: Set detection voltage
$-V_{DET}$: Actual detection voltage

***2.** The voltage difference between the detection voltage ($-V_{DET}$) and the release voltage ($+V_{DET}$). The relation between the actual output voltage ($V_{OUT(E)}$) of the regulator block and the actual release voltage ($+V_{DET} = -V_{DET} + V_{HYS}$) of the detector block is as follows.

$V_{OUT(E)} > +V_{DET}$

***3.** The time from when V_{OUT} exceeds $+V_{DET}$ to when the RO pin output inverts (Refer to **Figure 6**). This value changes according to the release delay time and monitoring time adjustment capacitor (C_{DLY}).
The time period from when V_{OUT} changes to $+V_{DET} \rightarrow V_{OUT(S)}$ to when V_{RO} reaches V_{OUT} / 2.

***4.** The time from when V_{OUT} falls below $-V_{DET}$ to when the RO pin output inverts (Refer to **Figure 7**). The time period from when V_{OUT} changes to $V_{OUT(S)} \rightarrow -V_{DET}$ to when V_{RO} reaches V_{OUT} / 2.

***5.** The guaranteed value when the watchdog timer is deactivated. t_{rr} may shorten since the discharge operation of C_{DLY} may be performed while the watchdog timer is activated.

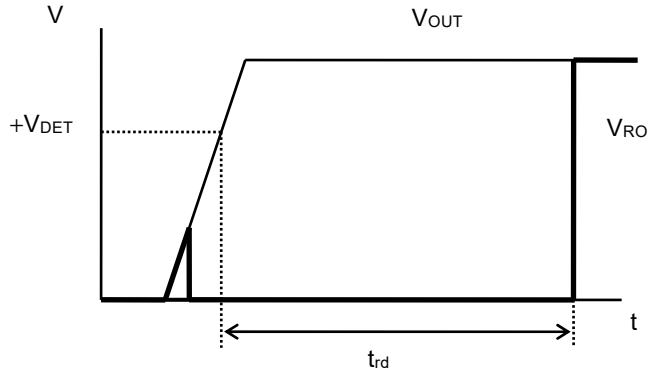


Figure 6 Release Delay Time

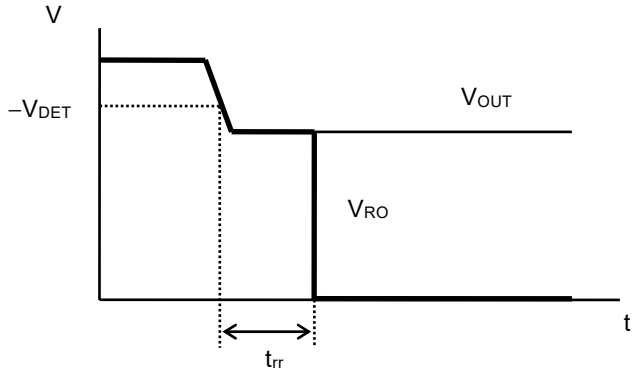


Figure 7 Reset Reaction Time

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3. Watchdog timer block

3. 1 S-19502 Series (Product with WEN pin)

Table 15

(V_{IN} = 13.5 V, T_j = –40°C to +150°C unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
Watchdog activation threshold current	$I_{O,WDact}$	WADJ pin is open	1.1	1.5	1.9	mA	6
Watchdog deactivation threshold current	$I_{O,WDdeact}$	WADJ pin is open	–	1.3	–	mA	6
Watchdog activation hysteresis current	$I_{O,WDhys}$	WADJ pin is open	0.1	0.2	–	mA	6
Watchdog activation threshold voltage	$V_{WADJ,th}$	–	1.28	1.35	1.45	V	7
WADJ pin current ratio	$\frac{I_{OUT}}{I_{WADJ}}$	V_{WADJ} = 0 V, I_{OUT} = 10 mA	–	750	–	–	7
WADJ pin internal resistance	$R_{WADJ,int}$	–	490	650	845	kΩ	–
Watchdog output pulse period*1	$t_{WD,p}$	C_{DLY} = 47 nF	38	54	72	ms	6
Watchdog output "L" time*2	$t_{WD,L}$	V_{OUT} > –V_{DET}, C_{DLY} = 47 nF Watchdog timer is activated	6	11	16	ms	6
Watchdog trigger time*3	$t_{WI,tr}$	C_{DLY} = 47 nF	32	43	56	ms	6
WEN pin input voltage "H"	V_{SH}	–	2	–	–	V	8
WEN pin input voltage "L"	V_{SL}	–	–	–	0.8	V	8
WEN pin input current "H"	I_{SH}	V_{WEN} = $V_{OUT(S)}$	–	0.1	1	µA	8
WEN pin input current "L"	I_{SL}	V_{WEN} = 0 V	–0.1	–	0.1	µA	8

***1.** The period of the continuous rectangular wave that appears in the WO / RO pin when the watchdog timer repeats the detection of a time-out (Refer to **Figure 8**). It is calculated by using the following equation.

$$t_{WD,p} = t_{WI,tr} + t_{WD,L}$$

***2.** The time when the WO / RO pin continues "L" after the watchdog timer detects a time-out (Refer to **Figure 8**).

***3.** The time from when the watchdog timer initiates the detection of a trigger signal to when a time-out is detected and the WO / RO pin output changes to "L" (Refer to **Figure 8**). This value changes according to C_{DLY}.
This is the guaranteed value when V_{OUT} increases to +V_{DET} or higher and the discharge operation of C_{DLY} due to the detector operation is not performed. The discharge operation of C_{DLY} may be performed when V_{OUT} decreases to –V_{DET} or lower. At that time, $t_{WI,tr}$, $t_{WD,L}$ and $t_{WD,p}$ may be changed.

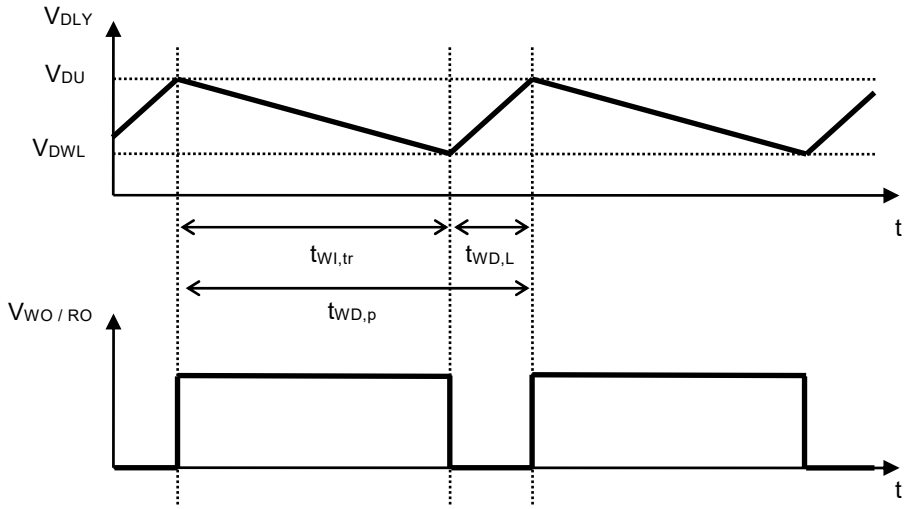


Figure 8

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3. 2 S-19503 Series (Product without WEN pin)

Table 16

(V_{IN} = 13.5 V, T_j = –40°C to +150°C unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
Watchdog activation threshold current	$I_{O,WDact}$	WADJ pin is open	1.1	1.5	1.9	mA	6
Watchdog deactivation threshold current	$I_{O,WDdeact}$	WADJ pin is open	–	1.3	–	mA	6
Watchdog activation hysteresis current	$I_{O,WDhys}$	WADJ pin is open	0.1	0.2	–	mA	6
Watchdog activation threshold voltage	$V_{WADJ,th}$	–	1.28	1.35	1.45	V	7
WADJ pin current ratio	$\frac{I_{OUT}}{I_{WADJ}}$	V_{WADJ} = 0 V, I_{OUT} = 10 mA	–	750	–	–	7
WADJ pin internal resistance	$R_{WADJ,int}$	–	490	650	845	kΩ	–
Watchdog output voltage "H"	V_{WOH}	–	$V_{OUT(S)} \times 0.9$	–	–	V	11
Watchdog output voltage "L"	V_{WOL}	$R_{extW} \geq 3$ kΩ, Connected to VOUT pin	–	0.2	0.4	V	11
Watchdog pull-up resistance	R_{WO}	VOUT pin internal resistance	20	30	45	kΩ	–
Watchdog output current	I_{WO}	V_{WO} = 0.4 V, $V_{OUT} = -V_{DET(S)} - 0.1$ V	3.0	–	–	mA	12
Watchdog output pulse period*1	$t_{WD,p}$	C_{DLY} = 47 nF	38	54	72	ms	6
Watchdog output "L" time*2	$t_{WD,L}$	$V_{OUT} > -V_{DET}$, C_{DLY} = 47 nF Watchdog timer is activated	6	11	16	ms	6
Watchdog trigger time*3	$t_{WI,tr}$	C_{DLY} = 47 nF	32	43	56	ms	6

***1.** The period of the continuous rectangular wave that appears in the WO pin when the watchdog timer repeats the detection of a time-out (Refer to **Figure 9**). It is calculated by using the following equation.

$$t_{WD,p} = t_{WI,tr} + t_{WD,L}$$

***2.** The time when the WO pin continues "L" after the watchdog timer detects a time-out (Refer to **Figure 9**).

***3.** The time from when the watchdog timer initiates the detection of a trigger signal to when a time-out is detected and the WO pin output changes to "L" (Refer to **Figure 9**). This value changes according to C_{DLY}.
This is the guaranteed value when V_{OUT} increases to $+V_{DET}$ or higher and the discharge operation of C_{DLY} due to the detector operation is not performed. The discharge operation of C_{DLY} may be performed when V_{OUT} decreases to $-V_{DET}$ or lower. At that time, $t_{WI,tr}$, $t_{WD,L}$ and $t_{WD,p}$ may be changed.

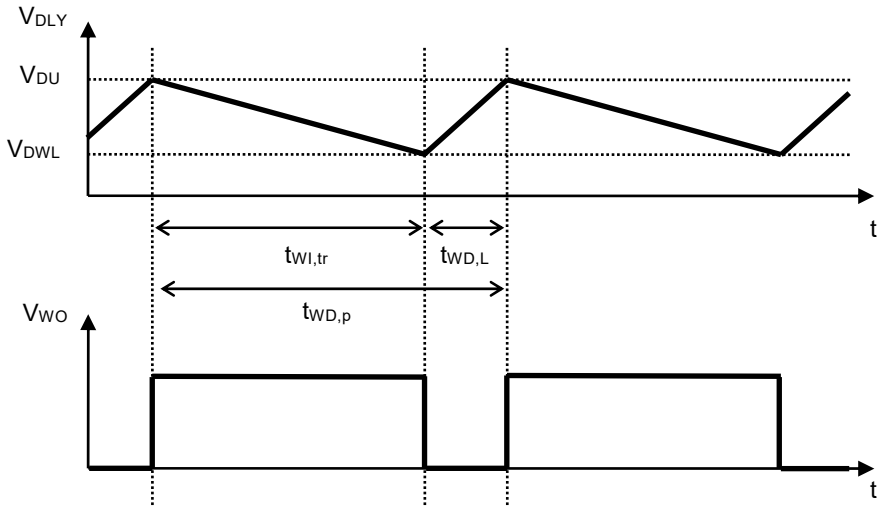


Figure 9

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4. Overall

Table 17

(V_{IN} = 13.5 V, T_j = −40°C to +150°C unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
Current consumption during operation	I_{SS1}	I_{OUT} ≤ 5 mA, WADJ pin is open, during watchdog timer activation, WO pin = "H"	–	75	115	µA	9
		I_{OUT} = 50 mA, WADJ pin is open, during watchdog timer activation, WO pin = "H"	–	80	125	µA	9
		I_{OUT} = 200 mA, WADJ pin is open, during watchdog timer activation, WO pin = "H"	–	100	150	µA	9
Current consumption during watchdog timer deactivation	I_{SS2}	I_{OUT} = 0 mA, during watchdog timer deactivation	–	60	95	µA	10

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■ Test Circuits

1. S-19502 Series (Product with WEN pin)

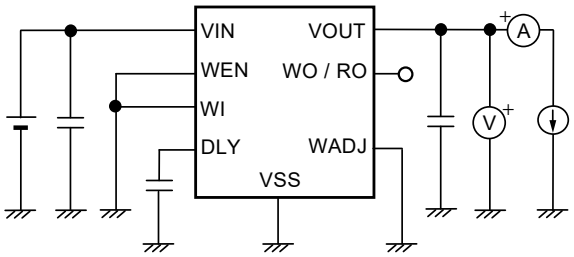


Figure 10 Test Circuit 1

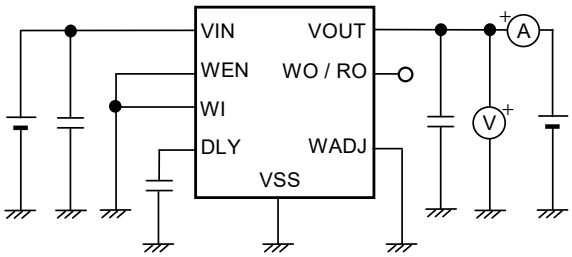


Figure 11 Test Circuit 2

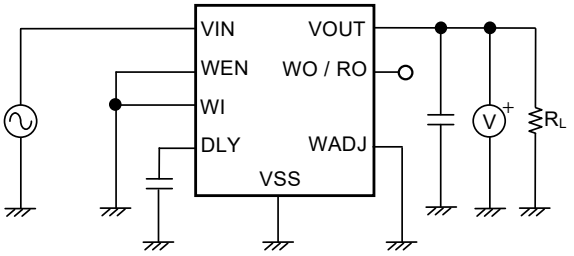


Figure 12 Test Circuit 3

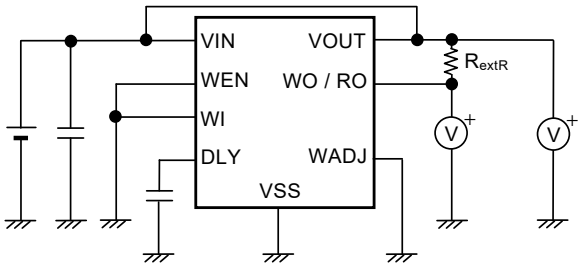


Figure 13 Test Circuit 4

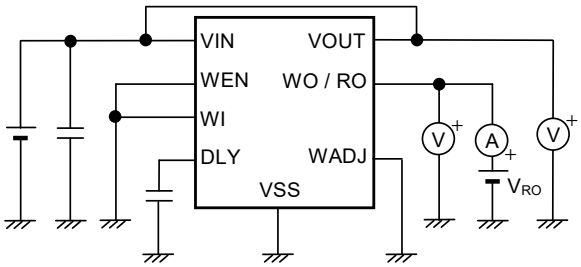


Figure 14 Test Circuit 5

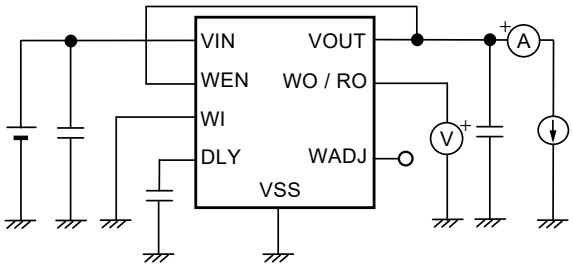


Figure 15 Test Circuit 6

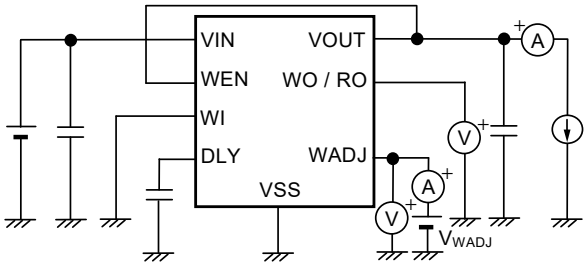


Figure 16 Test Circuit 7

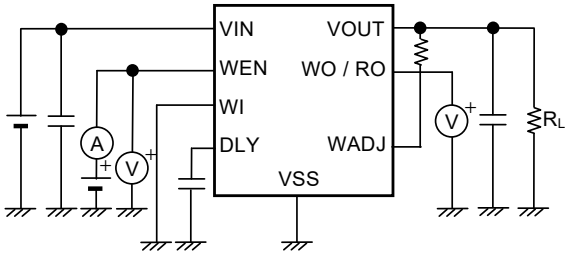


Figure 17 Test Circuit 8

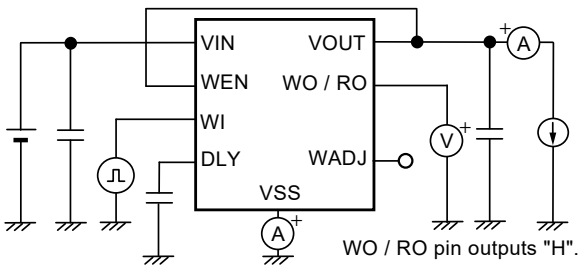


Figure 18 Test Circuit 9

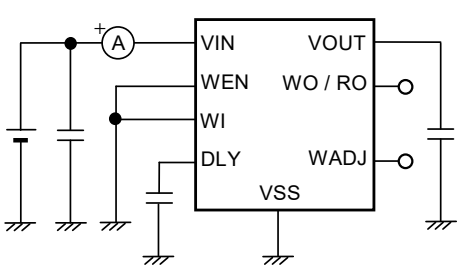


Figure 19 Test Circuit 10

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2. S-19503 Series (Product without WEN pin)

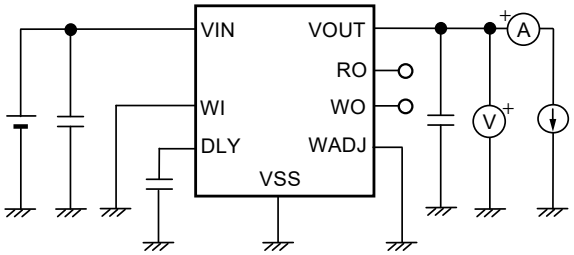


Figure 20 Test Circuit 1

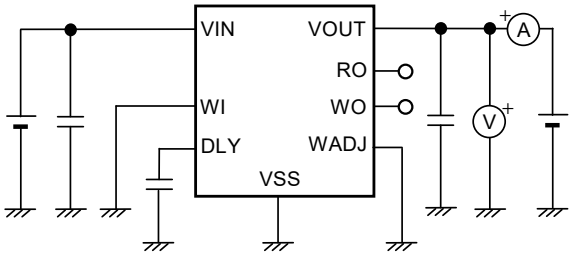


Figure 21 Test Circuit 2

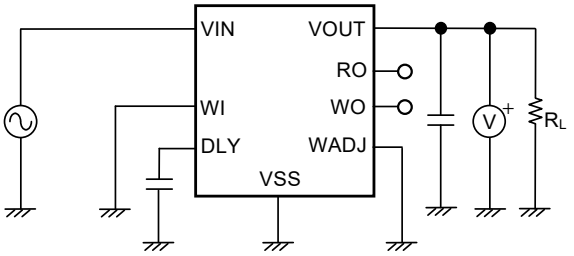


Figure 22 Test Circuit 3

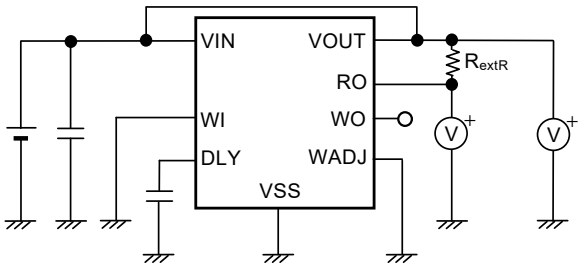


Figure 23 Test Circuit 4

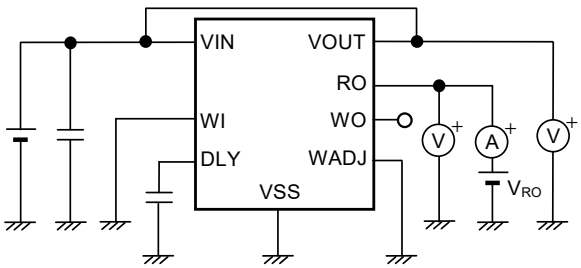


Figure 24 Test Circuit 5

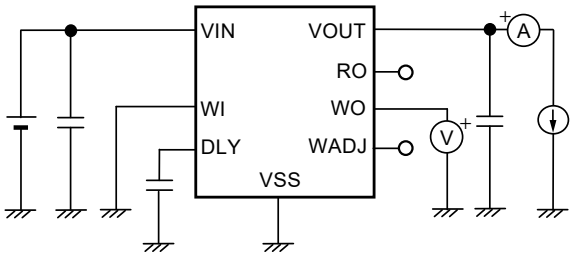


Figure 25 Test Circuit 6

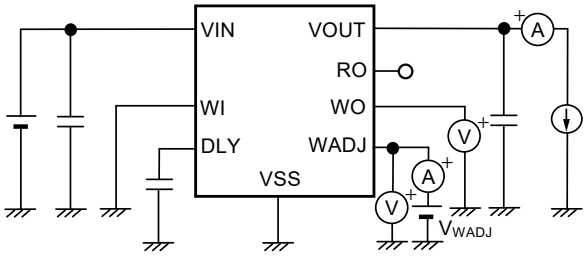


Figure 26 Test Circuit 7

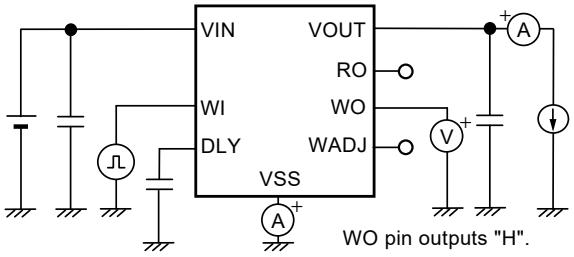


Figure 27 Test Circuit 8

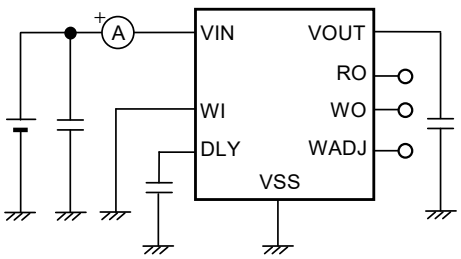


Figure 28 Test Circuit 9

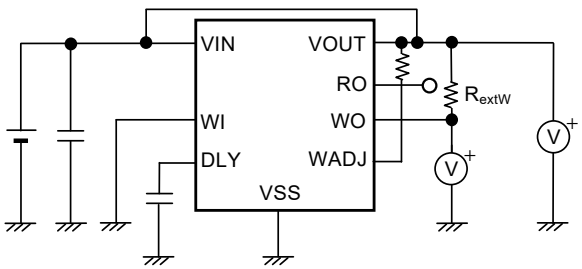


Figure 29 Test Circuit 10

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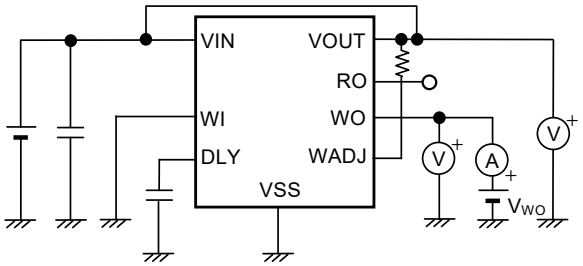


Figure 30 Test Circuit 11

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■ Standard Circuits

1. S-19502 Series (Product with WEN pin)

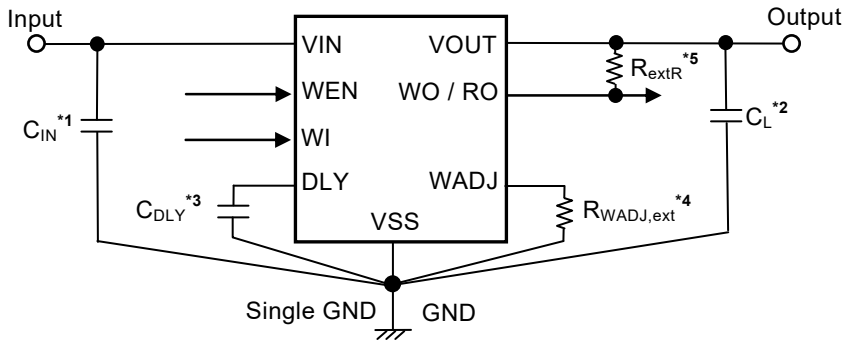


Figure 31

2. S-19503 Series (Product without WEN pin)

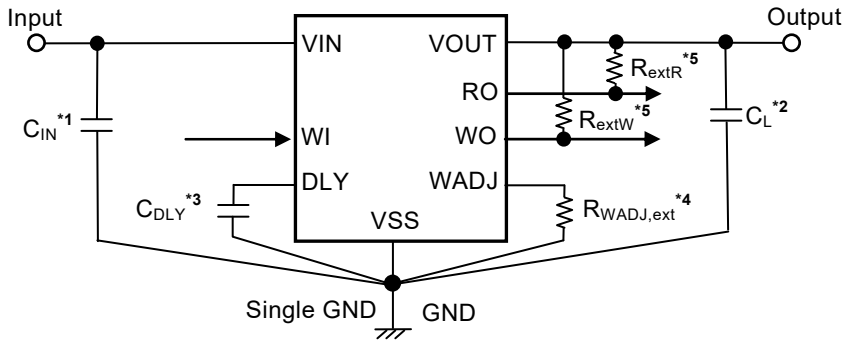


Figure 32

***1.** C_{IN} is a capacitor for stabilizing the input.

***2.** C_L is a capacitor for stabilizing the output. A ceramic capacitor of 2.2 μF or more can be used.

***3.** C_{DLY} is the release delay time and monitoring time adjustment capacitor.

***4.** $R_{WADJ,ext}$ is the watchdog activation threshold current adjustment resistor.

***5.** R_{extR} and R_{extW} are the external pull-up resistors for the reset output pin and the watchdog output pin, respectively. Connection of the external pull-up resistor is not absolutely essential since the S-19502/19503 Series has a built-in pull-up resistor.

Caution The above connection diagram and constants will not guarantee successful operation. Perform thorough evaluation using an actual application to set the constants.

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■ Selection of External Parts

1. Input and output capacitors (C_{IN}, C_L)

The S-19502/19503 Series requires C_L between the VOUT pin and the VSS pin for phase compensation. Operation is stabilized by a ceramic capacitor with an output capacitance of 2.2 μF or more over the entire temperature range. When using an OS capacitor, a tantalum capacitor, or an aluminum electrolytic capacitor, the capacitance must be 2.2 μF or more, and the ESR must be 50 Ω or less.
The values of output overshoot and undershoot, which are transient response characteristics, vary depending on the value of the output capacitor.
The required value of capacitance for the input capacitor differs depending on the application.

Caution Define the capacitance of C_{IN} and C_L by sufficient evaluation including the temperature characteristics under the actual usage conditions.

2. Release delay time and monitoring time adjustment capacitor (C_{DLY})

In the S-19502/19503 Series, the release delay time and monitoring time adjustment capacitor (C_{DLY}) is necessary between the DLY pin and the VSS pin to adjust the release delay time (t_{rd}) of the detector and the monitoring time of the watchdog timer.
The set release delay time ($t_{rd(S)}$), the set watchdog trigger time ($t_{WI,tr(S)}$), the set watchdog output "L" time ($t_{WD,L(S)}$) and the set watchdog output pulse period ($t_{WD,p(S)}$) are calculated by using following equations, respectively.
The release delay time (t_{rd}), the watchdog trigger time ($t_{WI,tr}$), the watchdog output "L" time ($t_{WD,L}$) and the watchdog output pulse period ($t_{WD,p}$) at the time of the condition of C_{DLY} = 47 nF are shown in "■ **Electrical Characteristics**".

$$t_{rd(S)}\ [\mathrm{ms}] = t_{rd}\ [\mathrm{ms}] \times \frac{C_{DLY}\ [\mathrm{nF}]}{47\ [\mathrm{nF}]}$$

$$t_{WI,tr(S)}\ [\mathrm{ms}] = t_{WI,tr}\ [\mathrm{ms}] \times \frac{C_{DLY}\ [\mathrm{nF}]}{47\ [\mathrm{nF}]}$$

$$t_{WD,L(S)}\ [\mathrm{ms}] = t_{WD,L}\ [\mathrm{ms}] \times \frac{C_{DLY}\ [\mathrm{nF}]}{47\ [\mathrm{nF}]}$$

$$t_{WD,p(S)}\ [\mathrm{ms}] = t_{WI,tr(S)}\ [\mathrm{ms}] + t_{WD,L(S)}\ [\mathrm{ms}]$$

Caution 1. The above equations will not guarantee successful operation. Perform thorough evaluation including the temperature characteristics using an actual application to set the constants.
2. Mounted board layout should be made in such a way that no current flows into or flows from the DLY pin since the impedance of the DLY pin is high, otherwise correct delay time and monitoring time may not be provided.
3. Select C_{DLY} whose leakage current can be ignored against the built-in constant current (5.0 μA typ.). The leakage current may cause deviation in delay time and monitoring time. When the leakage current is larger than the built-in constant current, no release takes place.
4. Deviations of C_{DLY} are not included in the equations mentioned above. Be sure to determine the constants considering the deviation of C_{DLY} to be used.

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3. Watchdog activation threshold current adjustment resistor ($R_{WADJ,ext}$)

In the S-19502/19503 Series, the watchdog activation threshold current adjustment resistor ($R_{WADJ,ext}$) can be connected between the WADJ pin and the VSS pin to adjust the watchdog timer activation threshold current.
The set watchdog activation threshold current ($I_{O,WDact(S)}$), the set watchdog deactivation threshold current ($I_{O,WDdeact(S)}$) and the set watchdog activation hysteresis current ($I_{O,WDhys(s)}$) are calculated by using following equations, respectively.
The watchdog activation threshold current ($I_{O,WDact}$), the watchdog deactivation threshold current ($I_{O,WDdeact}$) and the watchdog activation hysteresis current ($I_{O,WDhys}$) when the WADJ pin is open are shown in "■ **Electrical Characteristics**".

$$I_{O,WDact(S)}\ [mA] = I_{O,WDact}\ [mA] \times \left(1 + \frac{R_{WADJ,int}\ [k\Omega]}{R_{WADJ,ext}\ [k\Omega]}\right)$$

$$I_{O,WDdeact(S)}\ [mA] = I_{O,WDdeact}\ [mA] \times \left(1 + \frac{R_{WADJ,int}\ [k\Omega]}{R_{WADJ,ext}\ [k\Omega]}\right)$$

$$I_{O,WDhys(S)}\ [mA] = I_{O,WDact(S)}\ [mA] - I_{O,WDdeact(S)}\ [mA]$$

Caution 1. The above equations will not guarantee successful operation. Perform thorough evaluation including the temperature characteristics using an actual application to set the constants.
2. Mounted board layout should be made in such a way that no current flows into or flows from the WADJ pin since the impedance of the WADJ pin is high, otherwise correct $I_{O,WDact}$ and $I_{O,WDdeact}$ may not be provided.
3. Refer to "3. 2 Autonomous watchdog operation function (Output current detection circuit)" in "■ Operation" for the details.

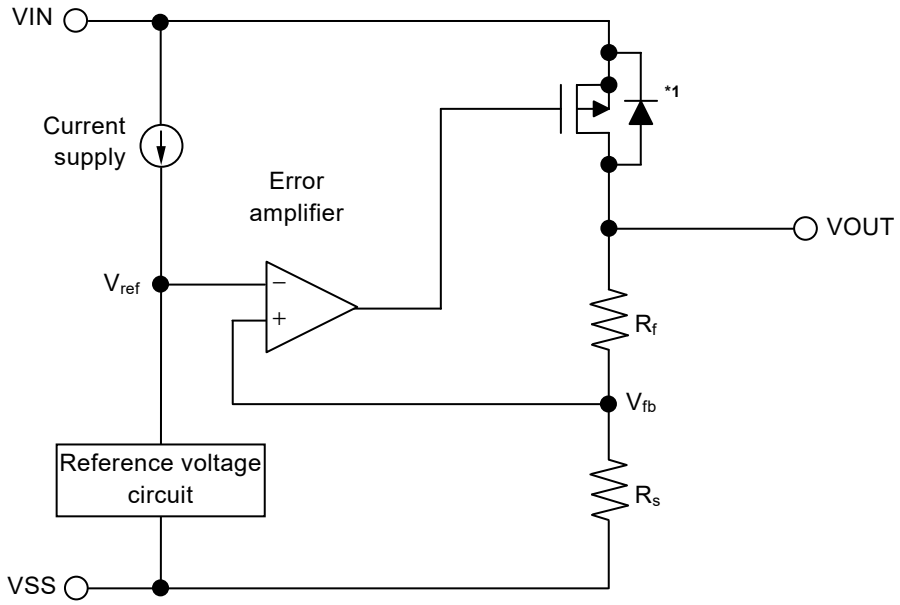
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■ Operation

1. Regulator block

1. 1 Basic operation

Figure 33 shows the block diagram of the regulator in the S-19502/19503 Series.
The error amplifier compares the reference voltage (V_{ref}) with feedback voltage (V_{fb}), which is the output voltage resistance-divided by feedback resistors (R_s and R_f). It supplies the gate voltage necessary to maintain the constant output voltage which is not influenced by the input voltage and temperature change, to the output transistor.



1. Parasitic diode

Figure 33

1. 2 Output transistor

In the S-19502/19503 Series, a low on-resistance P-channel MOS FET is used as the output transistor.
Be sure that V_{OUT} does not exceed $V_{IN} + 0.3$ V to prevent the voltage regulator from being damaged due to reverse current flowing from the VOUT pin through a parasitic diode to the VIN pin, when the potential of V_{OUT} became higher than V_{IN}.

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1. 3 Overcurrent protection circuit

The S-19502/19503 Series includes an overcurrent protection circuit which having the characteristics shown in "**1. 1 Output voltage vs. Output current (When load current increases) (Ta = +25°C)"** of "**1. Regulator block**" in "**■ Characteristics (Typical Data)**", in order to limit an excessive output current and overcurrent of the output transistor due to short-circuiting between the VOUT pin and the VSS pin. The current when the output pin is short-circuited (I_{short}) is internally set at 105 mA typ., and the load current when short-circuiting is limited based on this value. The output voltage restarts regulating if the output transistor is released from overcurrent status.

Caution This overcurrent protection circuit does not work as for thermal protection. If this IC long keeps short circuiting, pay attention to the conditions of input voltage and load current so that, under the usage conditions including short circuit, the loss of the IC will not exceed power dissipation.

1. 4 Thermal shutdown circuit

The S-19502/19503 Series has a thermal shutdown circuit to limit self-heating. When the junction temperature rises to 170°C typ., the thermal shutdown circuit operates to stop regulating. After that, when the junction temperature drops to 135°C typ., the thermal shutdown circuit is released to restart regulating.
Due to self-heating of the S-19502/19503 Series, if the thermal shutdown circuit starts operating, it stops regulating so that the output voltage drops. For this reason, self-heating is limited and the IC's temperature drops. When the temperature drops, the thermal shutdown circuit is released to restart regulating, thus self-heating is generated again due to rising of the output voltage. Repeating this procedure makes the waveform of the VOUT pin output into a pulse-like form. This phenomenon continues unless decreasing either or both of the input voltage and the output current in order to reduce the internal power consumption, or decreasing the ambient temperature. Note that the product may suffer physical damage such as deterioration if the above phenomenon occurs continuously.

Table 18

Thermal Shutdown Circuit	VOUT Pin Voltage
Detect: 170°C typ.*1	V_{SS} level
Release: 135°C typ.*1	Set value

***1.** Junction temperature

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2. Detector block

2. 1 Basic operation

(1) When the output voltage (V_{OUT}) of the regulator is release voltage ($+V_{DET}$) of the detector or higher, the Nch transistor (N1 and N2) are turned off and "H" is output to the RO pin. Since the Pch transistor (P1) is turned on, the input voltage to the comparator (C1) is $\frac{R_B \bullet V_{OUT}}{R_A + R_B}$.

(2) Even if V_{OUT} decreases to $+V_{DET}$ or lower, "H" is output to the RO pin when V_{OUT} is the detection voltage ($-V_{DET}$) or higher. When V_{OUT} decreases to $-V_{DET}$ (point A in **Figure 35**) or lower, N1 which is controlled by C1 is turned on, and C_{DLY} is discharged. If the DLY pin voltage (V_{DLY}) decreases to the lower reset timing threshold voltage (V_{DRL}) or lower, N2 of output stage of C2 is turned on, and then "L" is output to the RO pin. At this time, P1 is turned off, and the input voltage to C1 is $\frac{R_B \bullet V_{OUT}}{R_A + R_B + R_C}$.

(3) If V_{OUT} further decreases to the IC's minimum operation voltage or lower, the RO pin output is "H".

(4) When V_{OUT} increases to the IC's minimum operation voltage or higher, "L" is output to the RO pin. Moreover, even if V_{OUT} exceeds $-V_{DET}$, the output is "L" when V_{OUT} is lower than $+V_{DET}$.

(5) When V_{OUT} increases to $+V_{DET}$ (point B in **Figure 35**) or higher, N1 is turned off and C_{DLY} is charged. N2 is turned off if V_{DLY} increases to the upper timing threshold voltage (V_{DU}) or higher, and "H" is output to the RO pin.

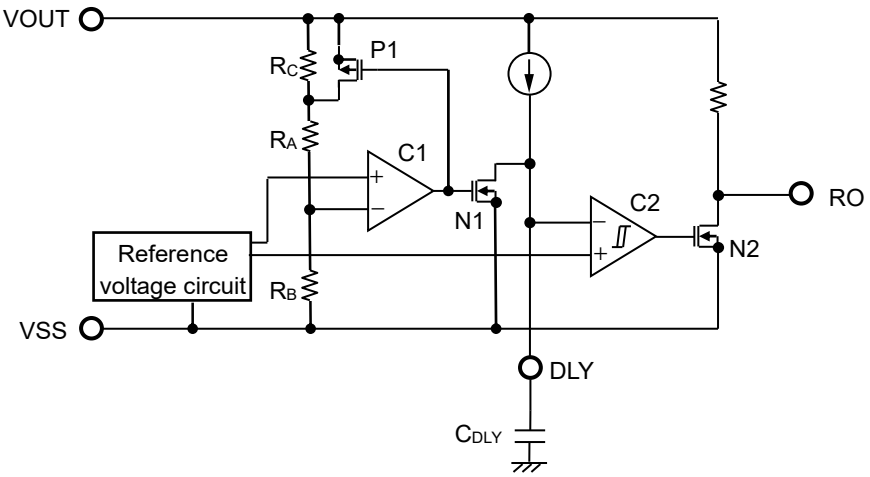


Figure 34 Operation of Detector Block

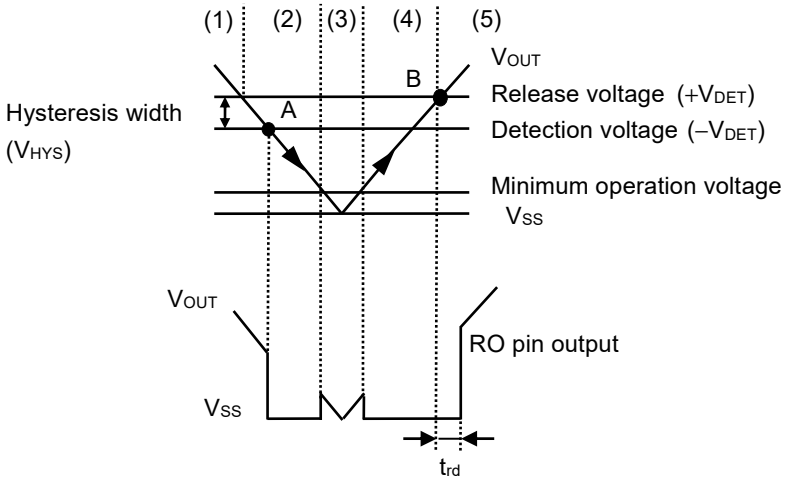


Figure 35 Timing Chart of Detector Block

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2. 2 Delay circuit

When the output voltage (V_{OUT}) of the regulator rises under the status that "L" is output to the RO pin, the reset release signal is output to the RO pin later than when V_{OUT} becomes $+V_{DET}$. The release delay time (t_{rd}) changes according to C_{DLY}. Refer to "**2. Release delay time and monitoring time adjustment capacitor (C_{DLY})**" in "**■ Selection of External Parts**" for details.
In addition, if the time from when V_{OUT} decreases to $-V_{DET}$ or lower to when V_{OUT} increases to $+V_{DET}$ or higher is significantly shorter compared to the length of the reset reaction time (t_{rr}), V_{DLY} may not decrease to V_{DRL} or lower. In that case, "H" output remains in the RO pin. Refer to "**2. 9 Reset reaction time vs. Release delay time and monitoring time adjustment capacitance**" in "**■ Characteristics (Typical Data)**" for the details.

Caution Since t_{rd} depends on the charge time of C_{DLY}, t_{rd} may be shorter than the set value if the charge operation is initiated under the condition that a residual electric charge is left in C_{DLY}.

2. 3 Output circuit

Since the RO pin has a built-in resistor to pull up to the VOUT pin internally, the RO pin can output a signal without an external pull-up resistor
Do not connect to the pin other than VOUT pin when connecting an external pull-up resistor.
In the S-19502 Series, the reset output pin and the watchdog output pin are prepared as the WO / RO pin.
The output level of the WO / RO pin is applied by the AND logic of the reset output pin and the watchdog output pin.

Example: When the WO pin is "L" and the RO pin is "H", the WO / RO pin is "L".

In the S-19503 Series, the reset output pin is prepared as the RO pin.

Caution Define the external pull-up resistance by sufficient evaluation including the temperature characteristics under the actual usage conditions.

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3. Watchdog timer block

3. 1 Basic operation

The watchdog timer operates as follows during monitoring operation.

(1) When the WO pin outputs "H", C_{DLY} is discharged by an internal constant current source, and the DLY pin voltage (V_{DLY}) decreases. The watchdog timer detects a trigger and the C_{DLY} is charged by an internal constant current source if a rising edge is input to the WI pin from a monitored object by the watchdog timer, and then V_{DLY} rises. The discharge operation is restarted if V_{DLY} reaches the upper timing threshold voltage (V_{DU}), and V_{DLY} decreases again. By inputting a rising edge to the WI pin again during the discharge operation, the similar operation is repeated. At this time, the WO pin outputs "H" continuously.
(2) The watchdog timer does not detect a trigger if the rising edge is not input to the WI pin from a monitored object by the watchdog timer when the C_{DLY} is discharged and V_{DLY} decreases. The WO pin outputs "L" if the discharge operation continues not detecting a trigger when V_{DLY} reaches the lower watchdog timing threshold voltage (V_{DWL}). This operation is called the time-out detection.
(3) After the time-out detection, C_{DLY} is charged while the WO pin outputs "L", and V_{DLY} increases. The WO pin outputs "H" and restarts the discharge operation if V_{DLY} reaches V_{DU}.
(4) By the operation of (3), a monitored object by the watchdog timer is reset. If a rising edge is input to the WI pin again, the operation similar to (1) is continued since the watchdog timer detects a trigger.
(5) After the operation of (3), if the status in which a rising edge is not input to the WI pin continues, the watchdog timer repeats the operation of (5) → (3) → (5) →...

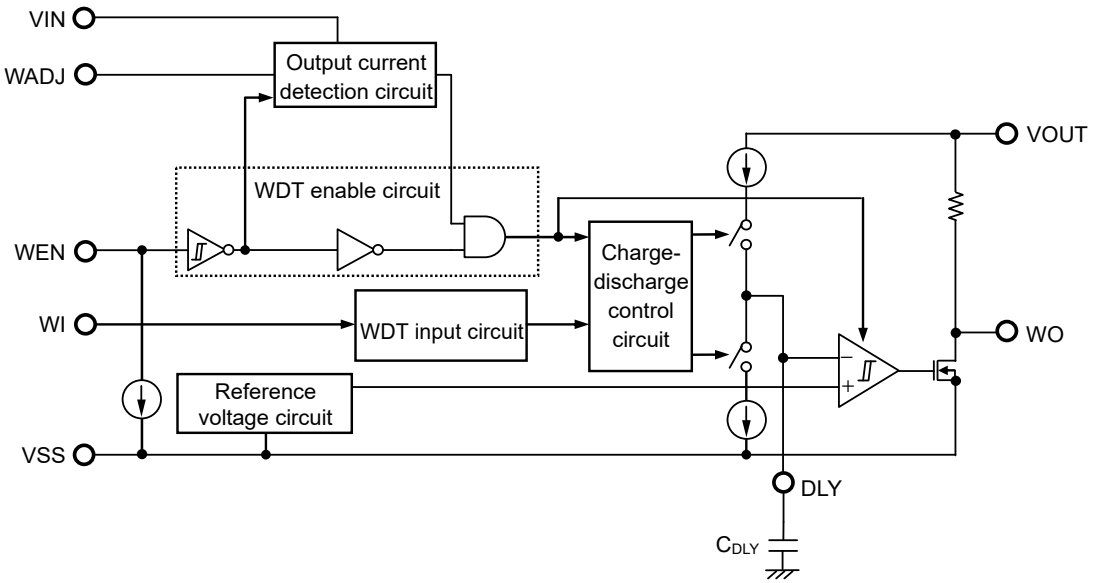


Figure 36

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The time period from when the watchdog timer detects a trigger to when it detects a time-out ($t_{WD,TO}$) is indicated as the following expression. **Figure 37** shows a timing chart of the watchdog timer.

$t_{WI,tr} \leq t_{WD,TO} \leq t_{WD,p}$

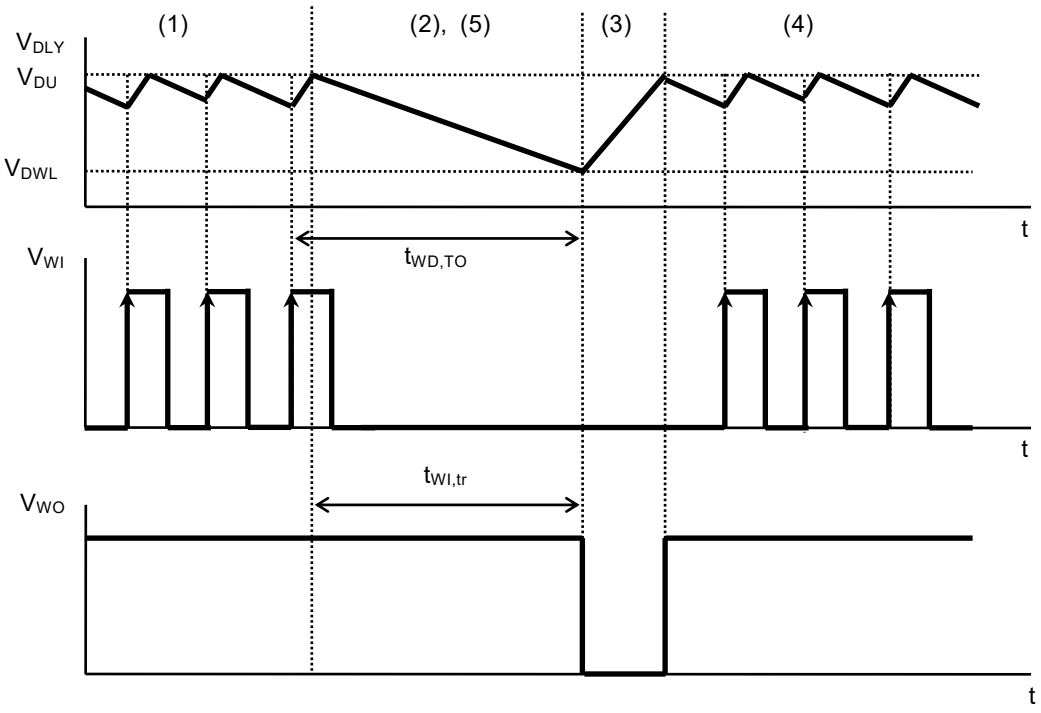


Figure 37

Regardless of the status of the watchdog timer, the capacitance of C_{DLY} could be discharged by the detector operation. Even if watchdog timer detects a trigger of signal input to the WI pin, the WO pin outputs "L" when V_{DLY} reaches V_{DWL}. After that, the watchdog timer restarts the monitoring operation if the WO pin outputs "H" when V_{DLY} reaches V_{DU}.

3. 2 Autonomous watchdog operation function (Output current detection circuit)

Since the S-19502/19503 Series has a built-in output current detection circuit, the watchdog timer operates autonomously. When using the autonomous watchdog operation function, the current flows in the load is detected by the output current of the regulator, the watchdog timer initiates the activation when the output current is the watchdog activation threshold current ($I_{O,WDact}$) or more, the watchdog timer is deactivated when the output current is the watchdog deactivation threshold current ($I_{O,WDdeact}$) or less.
Table 19 shows the connection of WADJ pin depending on the usage of the watchdog timer.
In the S-19502 Series, the watchdog timer is deactivated regardless of the connection of the WADJ pin if the watchdog timer is set to Disable by the WEN pin.

Table 19

Usage of Watchdog Timer	Connection of WADJ Pin	Status of WADJ Pin
Watchdog timer is not in use	Connect to the VSS pin	"L"
Watchdog timer is always activated	Connect to the VOUT pin via a 270 kΩ (recommended) resistor*1	"H"
Watchdog timer turns on and off autonomously depending on the load current (Autonomous watchdog operation function)	Open or connect to the VSS pin via an external resistor*2	"H": $I_{OUT} > I_{O,WDact}$ "L": $I_{OUT} < I_{O,WDdeact}$

***1.** Even if the WADJ pin is directly connected to the VOUT pin, the watchdog timer is always activated. Note that the current consumption will increase by as many resistors as unconnected.

***2.** Refer to "**3. Watchdog activation threshold current adjustment resistor ($R_{WADJ,ext}$)**" in "**■ Selection of External Parts**" for details.

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Depending on the output current (I_{OUT}) of the regulator, the watchdog timer monitoring activation is as follows.

(1) When I_{OUT} of the regulator is the watchdog activation threshold current ($I_{O,WDact}$) or more, the WADJ pin voltage (V_{WADJ}) is higher than the reference voltage (V_{ref}), and the output of the comparator (C1) is "H". At this time, the watchdog timer initiates the monitoring activation.
(2) When I_{OUT} decreases to the watchdog deactivation threshold current ($I_{O,WDdeact}$) (point A in **Figure 39**) or less, V_{WADJ} decreases to V_{ref} or less and the output of C1 is "L". At this time, the watchdog timer deactivates the monitoring. Even if I_{OUT} increases, the watchdog timer continues the monitoring deactivation when I_{OUT} is within less than $I_{O,WDact}$
(3) If I_{OUT} further increases to $I_{O,WDact}$ (point B in **Figure 39**) or more, V_{WADJ} increases to V_{ref} or higher and the output of C1 is "H". And then, the watchdog timer initiates the monitoring activation.

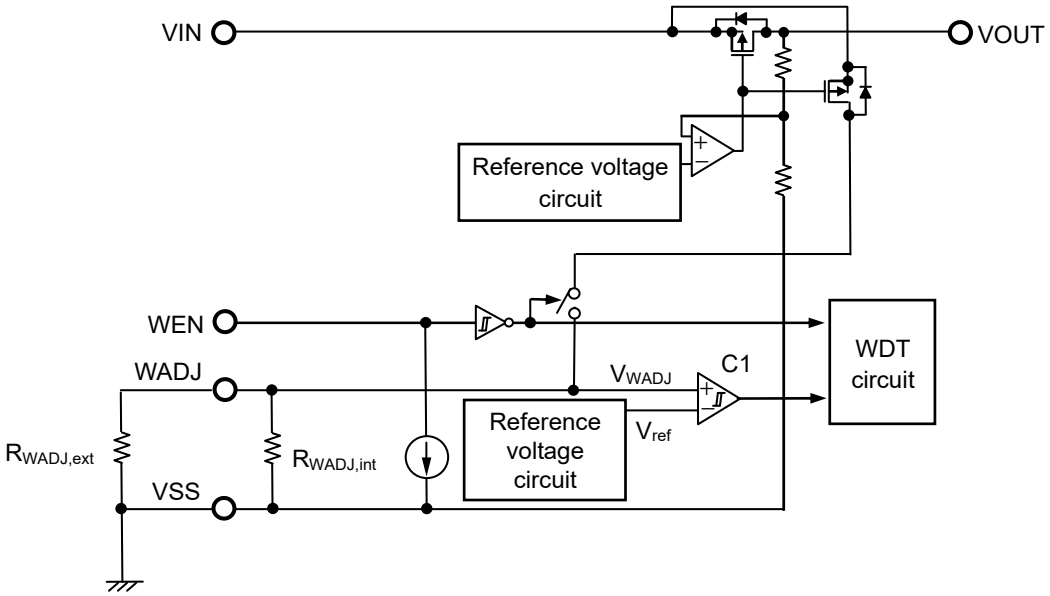


Figure 38 Operation of Output Current Detection Circuit

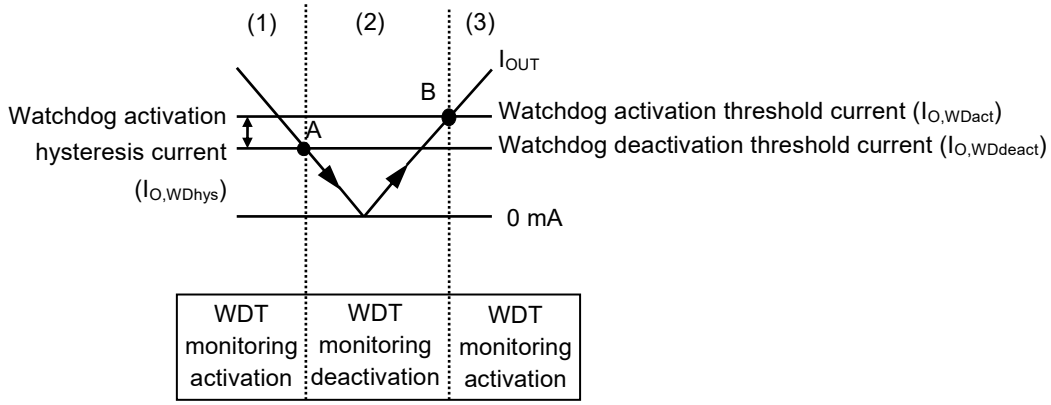


Figure 39 Autonomous Watchdog Operation Function

Caution **Due to detecting I_{OUT} of the regulator, current flows through the resistors connected to the WADJ pin ($R_{WADJ,ext}$ and $R_{WADJ,int}$). Therefore, the WADJ pin voltage (V_{WADJ}) may fluctuate since the current flowing through $R_{WADJ,ext}$ and $R_{WADJ,int}$ also changes in the same way if the output current changes transiently. V_{WADJ} at that time should be evaluated with the actual device**.

Remark $I_{O,WDact}$, $I_{O,WDdeact}$ and $I_{O,WDhys}$ can be adjusted by connecting $R_{WADJ,ext}$ to the WADJ pin. Refer to "**3. Watchdog activation threshold current adjustment resistor ($R_{WADJ,ext}$)**" in "**■ Selection of External Parts**" for the detail.

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3. 3 Watchdog enable circuit (only S-19502 Series)

When inputting "L" to the WEN pin, the watchdog timer becomes Disable and stops the output current detection operation and monitoring activation. When inputting "H" to the WEN pin, the watchdog timer becomes Enable. The watchdog timer monitoring activation is performed depending on the connection of the WADJ pin.
The WEN pin is pulled down internally by the constant current source. For this reason, the WEN pin is set to "L" when using the WEN pin in the floating status, and the watchdog timer becomes Disable. However, in order that the watchdog timer become Disable certainly, connect the WEN pin to GND so that "L" is input to the WEN pin certainly, since the impedance of the WEN pin becomes high when using the WEN pin in the floating status.
In order to fix the watchdog timer to Enable, connect the WEN pin to the VOUT pin so that "H" is input to the WEN pin.
Table 20 and **Table 21** show the relation between each pin status and the watchdog timer.

3. 4 Watchdog input circuit

By inputting a rising edge to the WI pin, the watchdog timer detects a trigger. The S-19502/19503 Series has a built-in watchdog input circuit which contains a band pass filter in the WI pin, and detects a rising edge which satisfies an input condition as a trigger signal. Refer to ***2** of **Table 12** and **Figure 5** in "**■ Recommended Operation Conditions**".
During the operation of the watchdog timer, a trigger is detected only when the DLY pin voltage is in V_{DU} to V_{DWL} and while the discharge operation of C_{DLY} is being performed. Refer to "**3. Watchdog timer block**" in "**■ Operation**" for details. The signal input from a monitored object by the watchdog timer to the watchdog timer should be input with a time interval which is sufficiently shorter than the watchdog trigger time ($t_{WI,tr}$).
Table 20 and **Table 21** show the relation between each pin status and the watchdog timer.

Caution Under a noisy environment, the watchdog input circuit may detect the noise as a trigger signal. Sufficiently evaluate with the actual application to confirm that a trigger is detected only in the intended signal.

3. 5 Watchdog output circuit

Since the WO pin has a built-in resistor to pull up to the VOUT pin internally, the WO pin can output a signal without an external pull-up resistor
Do not connect to the pin other than VOUT pin when connecting an external pull-up resistor.
In the S-19502 Series, the reset output pin and the watchdog output pin are prepared as the WO / RO pin.
The output level of the WO / RO pin is applied by the AND logic of the reset output pin and the watchdog output pin.

Example: When the WO pin is "L" and the RO pin is "H", the WO / RO pin is "L".

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3. 6 Each pin status and output logic

Table 20 and **Table 21** show each pin status and output logic in truth table.

3. 6. 1 S-19502 Series (Product with WEN pin)

Table 20

Status	Each Pin Status				Output Logic
	WEN Input	WADJ Status*1	WI Input	VOUT Output	WO / RO Output
WDT monitoring activation	"H"	"H"	Trigger	≥ +V_{DET}	"H"
WDT abnormal detection	"H"	"H"	No trigger	≥ +V_{DET}	"L"
WDT monitoring deactivation	"H"	"L"	Don't care	≥ +V_{DET}	"H"
WDT Disable	"L"	Don't care	Don't care	≥ +V_{DET}	"H"
Low voltage detection	Don't care	Don't care	Don't care	≤ –V_{DET}	"L"

***1.** Refer to **Table 19** for the status of WADJ pin.

3. 6. 2 S-19503 Series (Product without WEN pin)

Table 21

Status	Each Pin Status			Output Logic	
	WADJ Status*1	WI Input	VOUT Output	WO Output	RO Output
WDT monitoring activation	"H"	Trigger	≥ +V_{DET}	"H"	"H"
WDT abnormal detection	"H"	No trigger	≥ +V_{DET}	"L"	"H"
WDT monitoring deactivation	"L"	Don't care	≥ +V_{DET}	"H"	"H"
Low voltage detection	"H"	Don't care	≤ –V_{DET}	"L"	"L"
	"L"	Don't care	≤ –V_{DET}	"H"	"L"

***1.** Refer to **Table 19** for the status of WADJ pin.

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■ Timing Charts

1. S-19502 Series (Product with WEN pin)

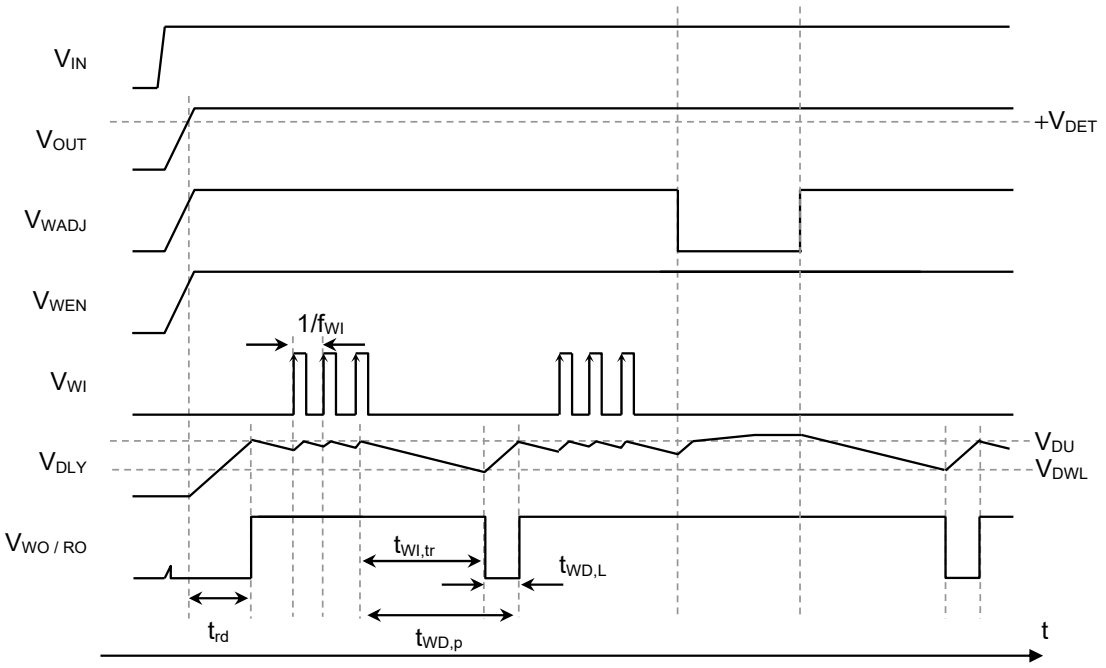


Figure 40 Example of Watchdog Timer Monitoring Operation 1

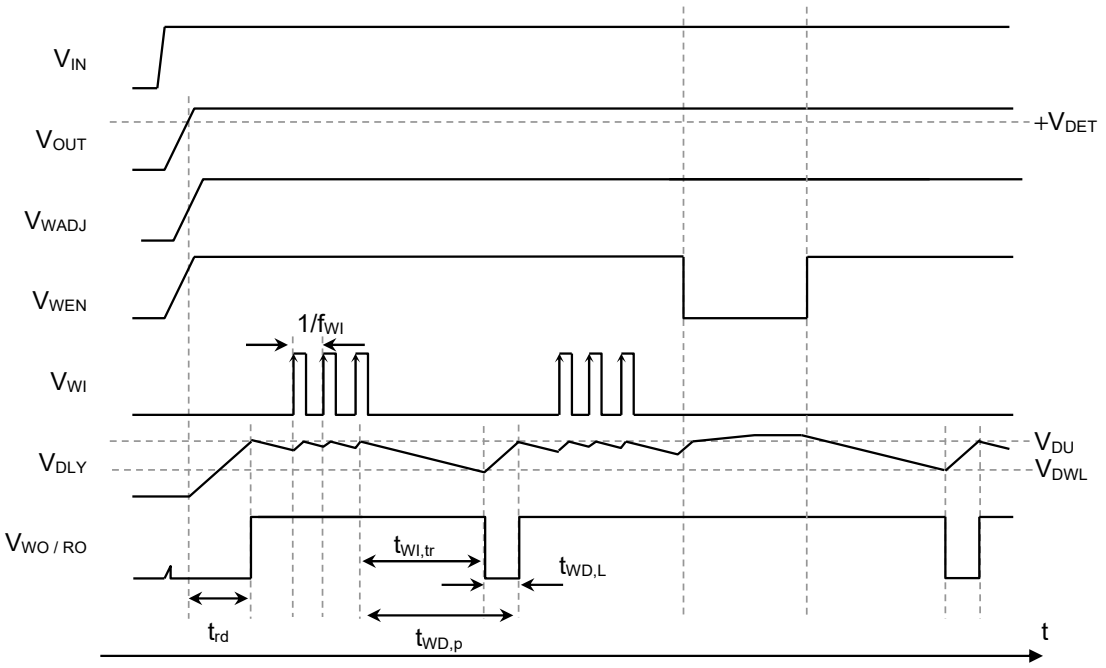


Figure 41 Example of Watchdog Timer Monitoring Operation 2

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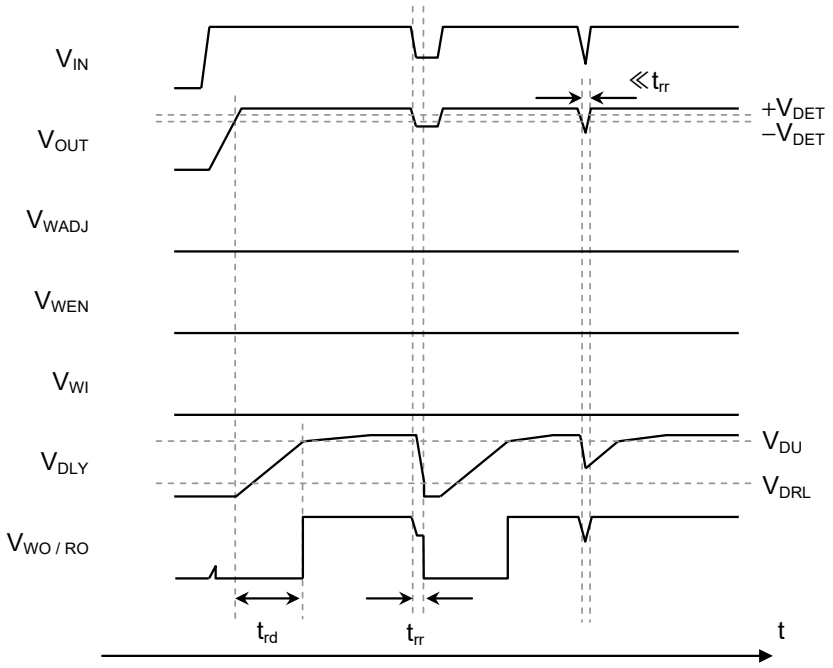


Figure 42 Example of Detector Operation

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2. S-19503 Series (Product without WEN pin)

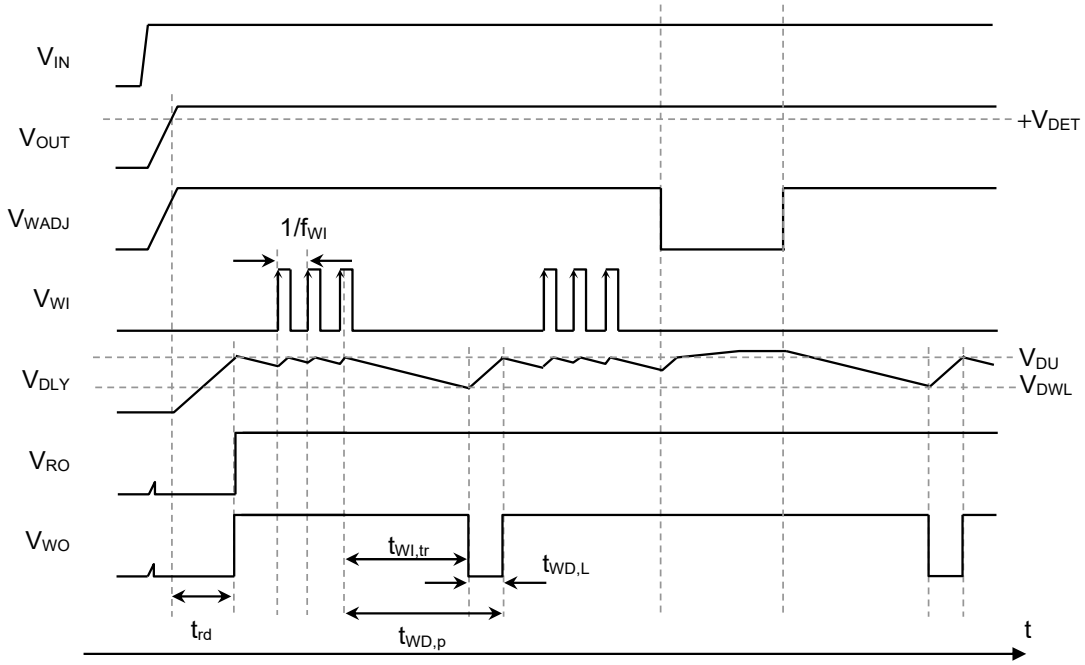


Figure 43 Example of Watchdog Timer Monitoring Operation

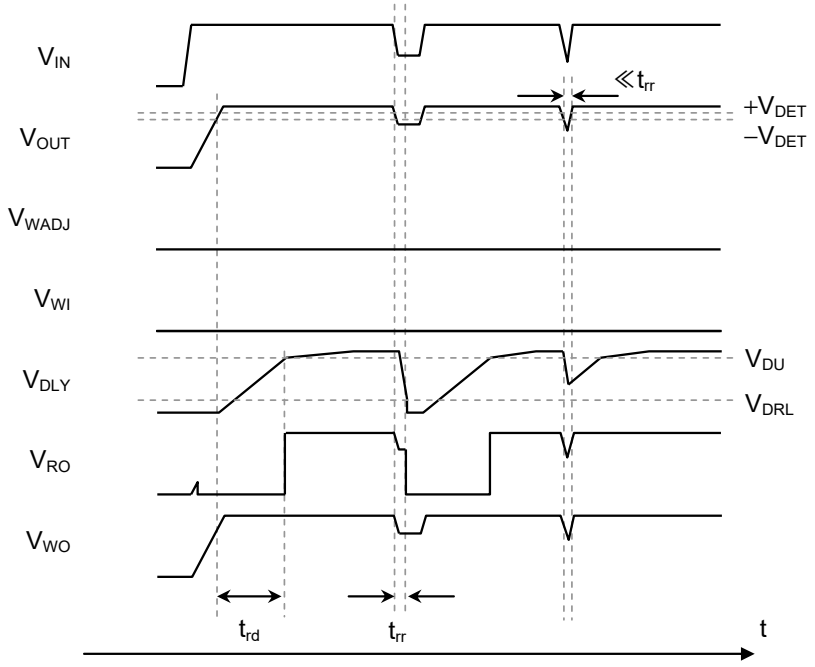


Figure 44 Example of Detector Operation

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■ Precautions

- Wiring patterns for the VIN pin, the VOUT pin and GND should be designed so that the impedance is low. When mounting an output capacitor between the VOUT pin and the VSS pin (C_L) and an input capacitor between the VIN pin and the VSS pin (C_{IN}), the distance from the capacitors to these pins should be as short as possible.
- Note that generally the output voltage may increase when a series regulator is used at low load current (0.1 mA or less).
- Note that generally the output voltage may increase due to the leakage current from an output transistor when a series regulator is used at high temperature.
- Generally a series regulator may cause oscillation, depending on the selection of external parts. The following conditions are recommended for the S-19502/19503 Series. However, be sure to perform sufficient evaluation under the actual usage conditions for selection, including evaluation of temperature characteristics. Refer to "**4. Example of equivalent series resistance vs. Output current characteristics (Ta = –40°C to +125°C)**" in "**■ Reference Data**" for the equivalent series resistance (R_{ESR}) of the output capacitor.

  Input capacitor (C_{IN}): 2.2 μF or more
  Output capacitor (C_L): 2.2 μF or more

- In a series regulator, generally the values of overshoot and undershoot in the output voltage vary depending on the variation factors of power-on, power supply fluctuation and load fluctuation, or output capacitance.
  Determine the conditions of the output capacitor after sufficiently evaluating the temperature characteristics of overshoot or undershoot in the output voltage with the actual device.
- The voltage regulator may oscillate when the impedance of the power supply is high and the input capacitance is small or an input capacitor is not connected.
- Overshoot may occur in the output voltage momentarily if the voltage is rapidly raised at power-on or when the power supply fluctuates. Sufficiently evaluate the output voltage at that time with the actual device.
- If the VOUT pin is steeply shorted with GND, a negative voltage exceeding the absolute maximum ratings may occur to the VOUT pin due to resonance of the wiring inductance and the output capacitance in the application. The negative voltage can be limited by inserting a protection diode between the VOUT pin and the VSS pin or inserting a series resistor to the output capacitor.
- The application conditions for the input voltage, the output voltage, and the load current should not exceed the power dissipation.
- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.
- In determining the output current, attention should be paid to the output current value specified in **Table 13** in "**■ Electrical Characteristics**" and footnote ***7** of the table.
- ABLIC Inc. claims no responsibility for any disputes arising out of or in connection with any infringement by products including this IC of patents owned by a third party.

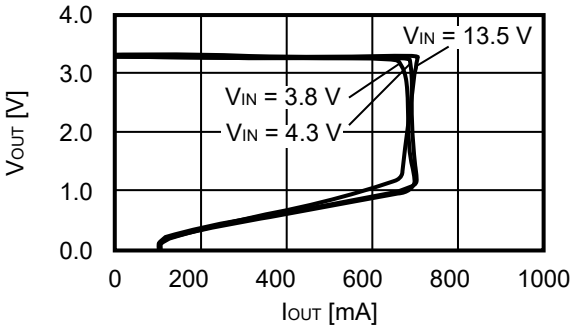
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■ Characteristics (Typical Data)

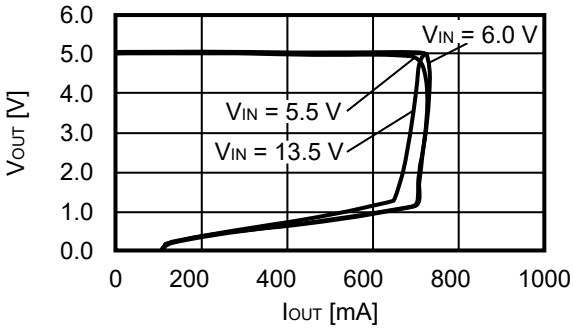
1. Regulator block

1. 1 Output voltage vs. Output current (When load current increases) (Ta = +25°C)

1. 1. 1 V_{OUT} = 3.3 V

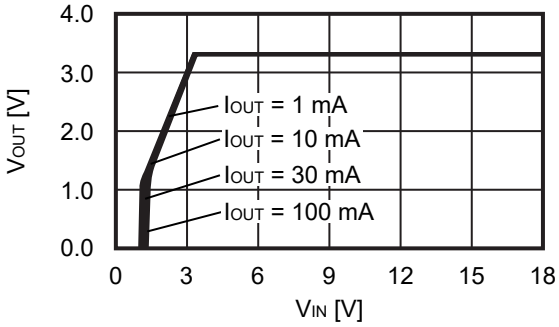


1. 1. 2 V_{OUT} = 5.0 V

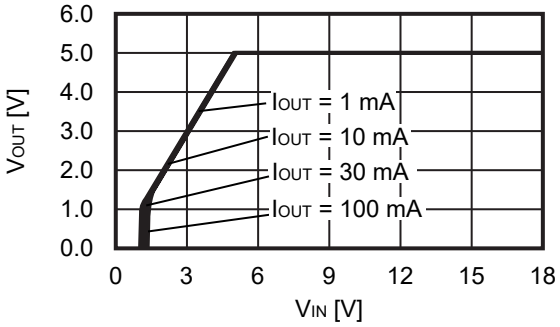


1. 2 Output voltage vs. Input voltage (Ta = +25°C)

1. 2. 1 V_{OUT} = 3.3 V

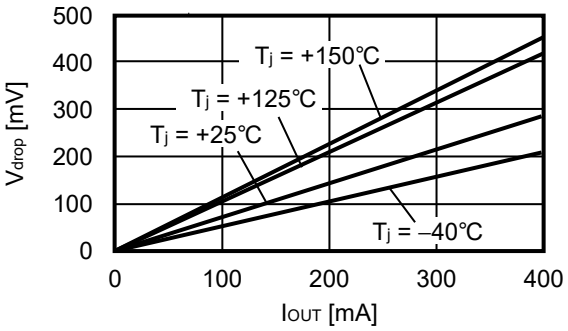


1. 2. 2 V_{OUT} = 5.0 V

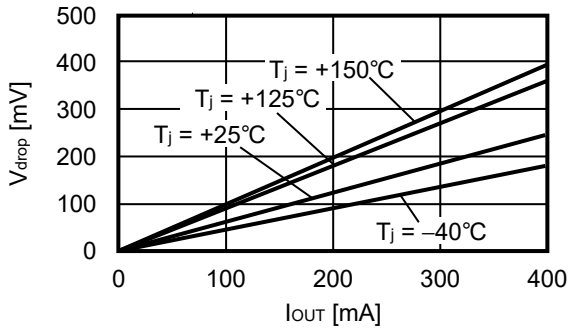


1. 3 Dropout voltage vs. Output current

1. 3. 1 V_{OUT} = 3.3 V

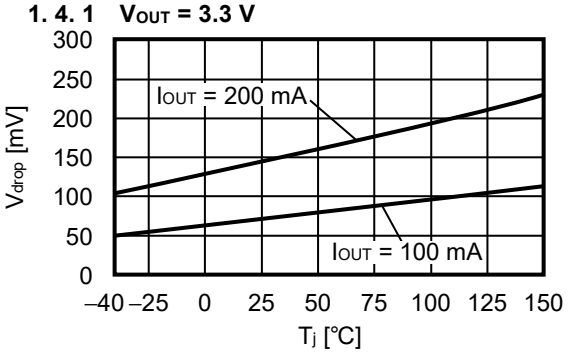


1. 3. 2 V_{OUT} = 5.0 V

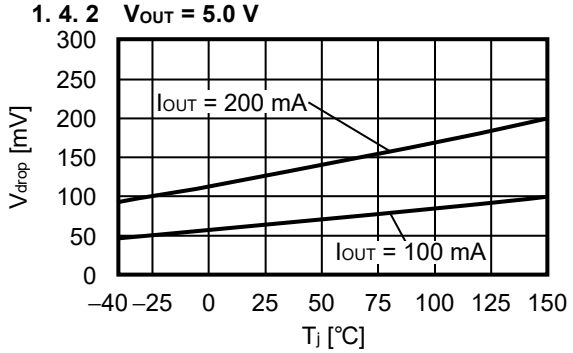


1. 4 Dropout voltage vs. Junction temperature

1. 4. 1 V_{OUT} = 3.3 V



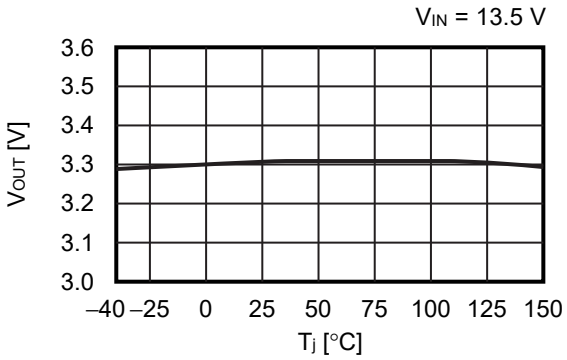
1. 4. 2 V_{OUT} = 5.0 V



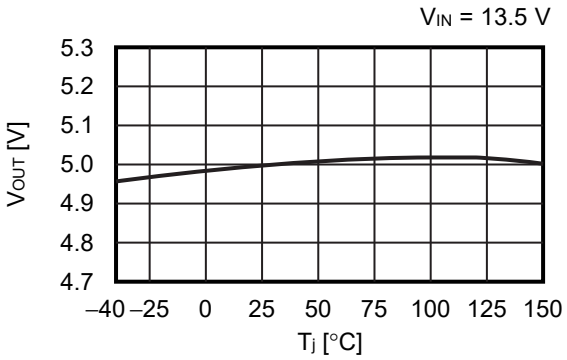
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1. 5 Output voltage vs. Junction temperature

1. 5. 1 V_{OUT} = 3.3 V

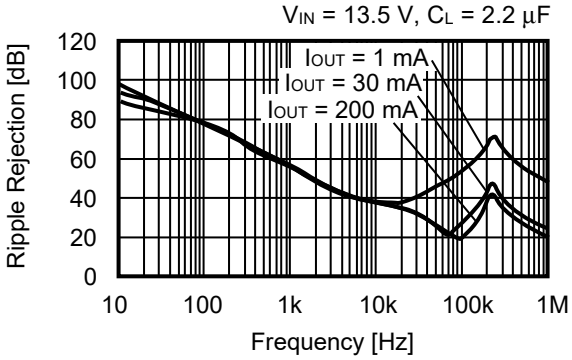


1. 5. 2 V_{OUT} = 5.0 V

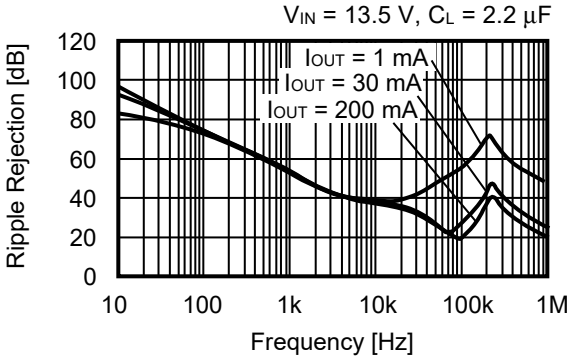


1. 6 Ripple rejection (Ta = +25°C)

1. 6. 1 V_{OUT} = 3.3 V



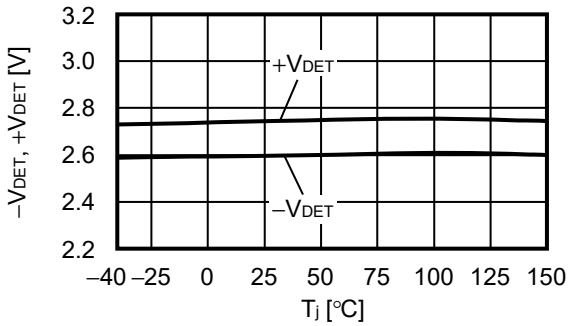
1. 6. 2 V_{OUT} = 5.0 V



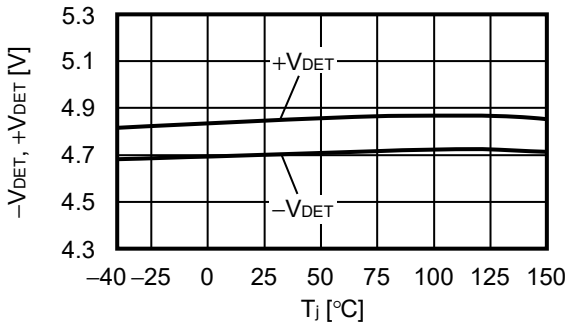
2. Detector block

2. 1 Detection voltage, Release voltage vs. Junction temperature

2. 1. 1 $-V_{DET}$ = 2.6 V

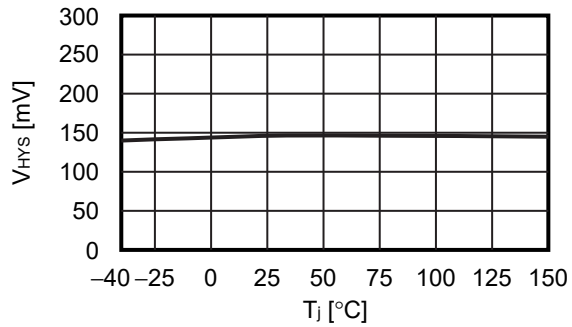


2. 1. 2 $-V_{DET}$ = 4.7 V

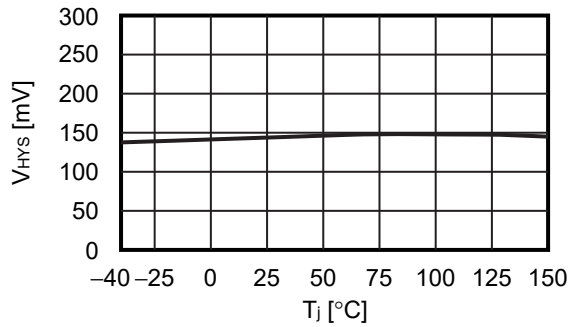


2. 2 Hysteresis width vs. Junction temperature

2. 2. 1 $-V_{DET}$ = 2.6 V



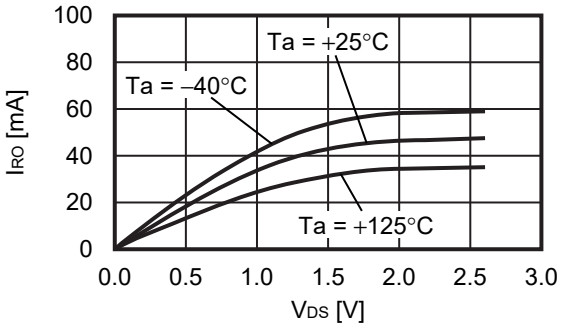
2. 2. 2 $-V_{DET}$ = 4.7 V



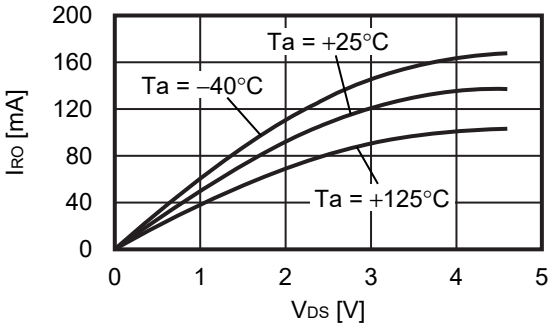
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2. 3 Reset output current vs. V_{DS}

2. 3. 1 $-V_{DET}$ = 2.6 V

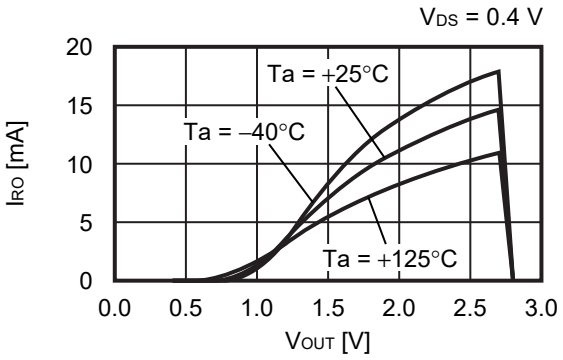


2. 3. 2 $-V_{DET}$ = 4.7 V

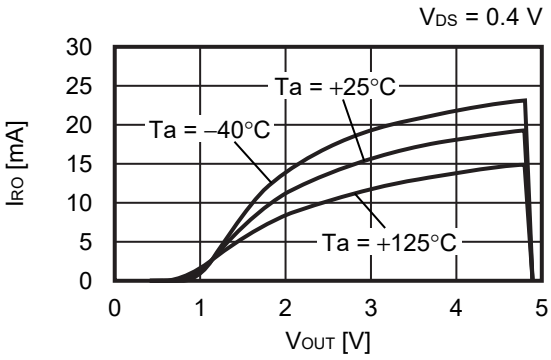


2. 4 Reset output current vs. Output voltage

2. 4. 1 $-V_{DET}$ = 2.6 V

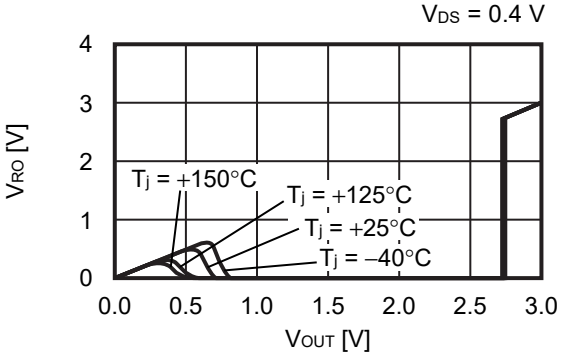


2. 4. 2 $-V_{DET}$ = 4.7 V

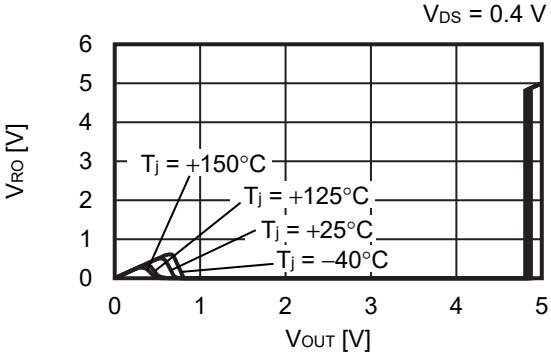


2. 5 RO pin voltage vs. Output voltage

2. 5. 1 $-V_{DET}$ = 2.6 V



2. 5. 2 $-V_{DET}$ = 4.7 V

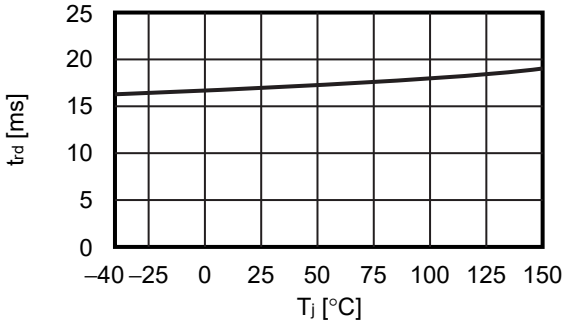


Remark I_{RO}: Nch transistor output current
V_{RO}: Nch transistor output voltage
V_{DS}: Drain-to-source voltage of Nch transistor

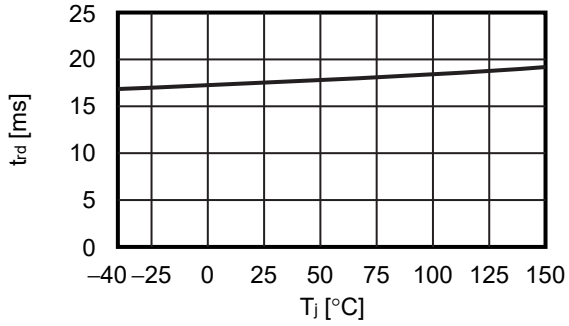
Downloaded from Arrow.com.

2. 6 Release delay time vs. Junction temperature

2. 6. 1 $-V_{DET}$ = 2.6 V

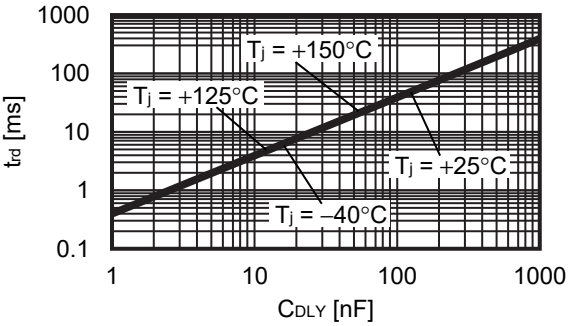


2. 6. 2 $-V_{DET}$ = 4.7 V

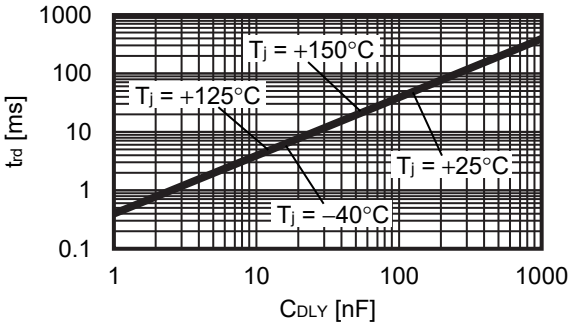


2. 7 Release delay time vs. Release delay time and monitoring time adjustment capacitance

2. 7. 1 $-V_{DET}$ = 2.6 V

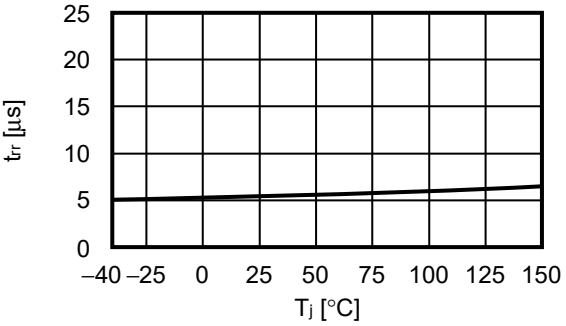


2. 7. 2 $-V_{DET}$ = 4.7 V

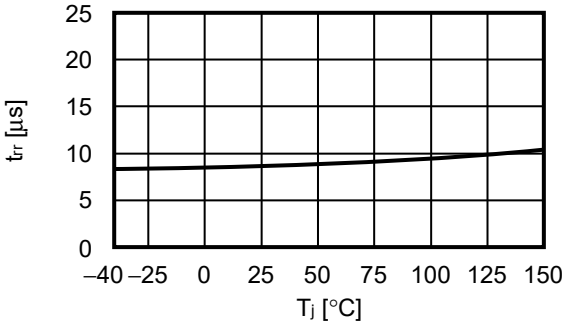


2. 8 Reset reaction time vs. Junction temperature

2. 8. 1 $-V_{DET}$ = 2.6 V

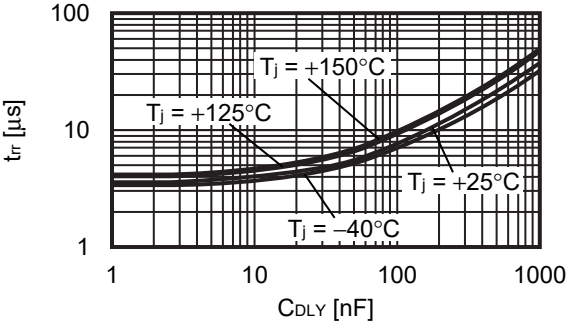


2. 8. 2 $-V_{DET}$ = 4.7 V

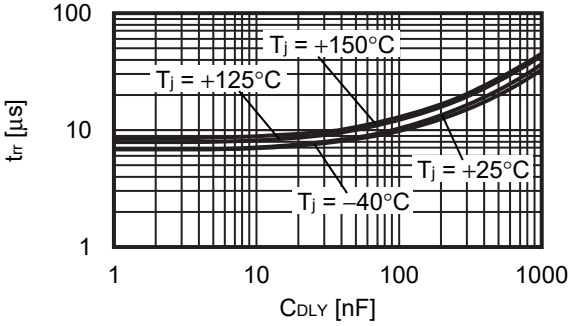


2. 9 Reset reaction time vs. Release delay time and monitoring time adjustment capacitance

2. 9. 1 $-V_{DET}$ = 2.6 V



2. 9. 2 $-V_{DET}$ = 4.7 V

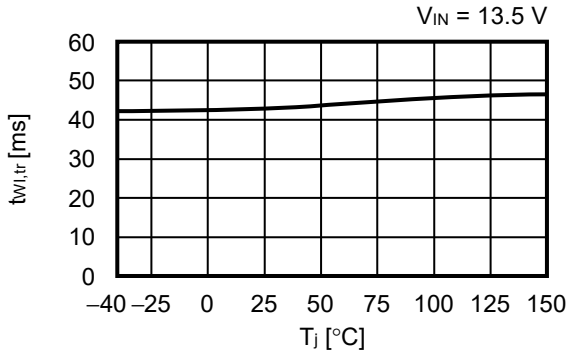


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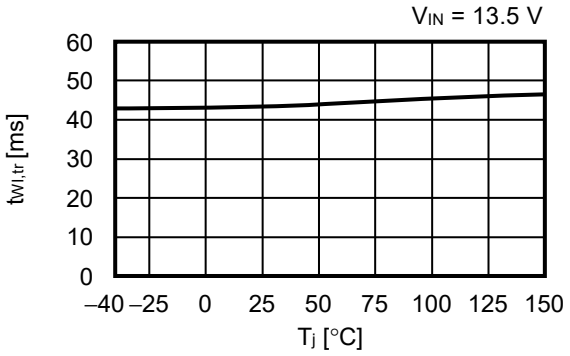
3. Watchdog timer block

3. 1 Watchdog trigger time vs. Junction temperature

3. 1. 1 V_{OUT} = 3.3 V

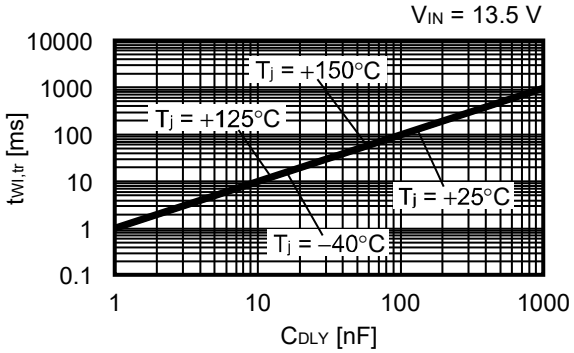


3. 1. 2 V_{OUT} = 5.0 V

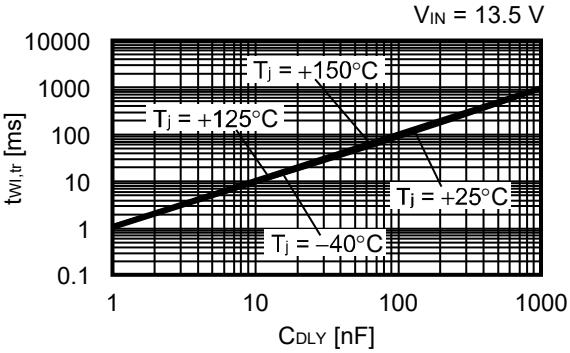


3. 2 Watchdog trigger time vs. Release delay time and monitoring time adjustment capacitance

3. 2. 1 V_{OUT} = 3.3 V

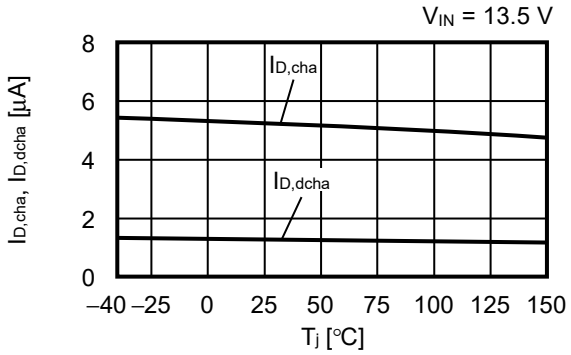


3. 2. 2 V_{OUT} = 5.0 V

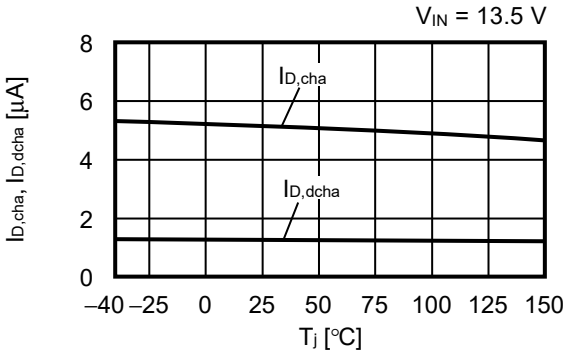


3. 3 Charge current, discharge current vs. Junction temperature

3. 3. 1 V_{OUT} = 3.3 V

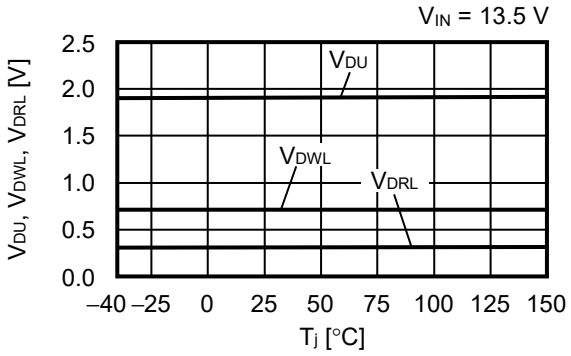


3. 3. 2 V_{OUT} = 5.0 V

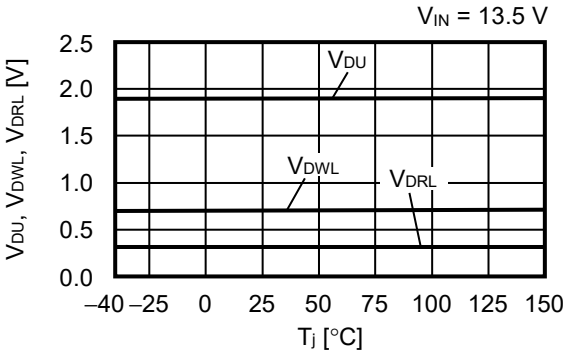


3. 4 Upper timing threshold voltage, lower watchdog timing threshold voltage, lower reset timing threshold voltage vs. Junction temperature

3. 4. 1 V_{OUT} = 3.3 V



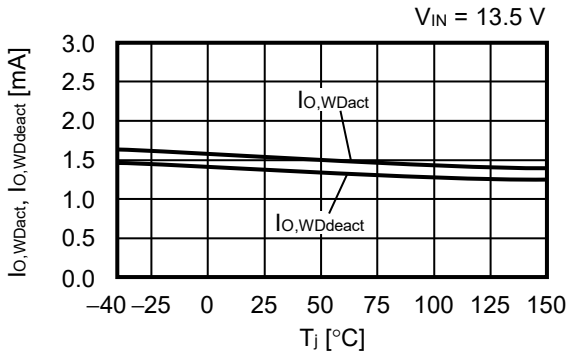
3. 4. 2 V_{OUT} = 5.0 V



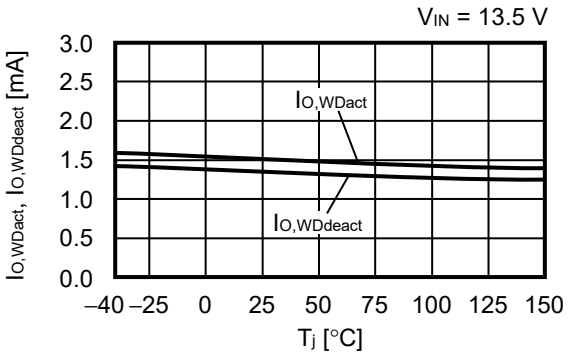
Downloaded from Arrow.com.

3. 5 Watchdog activation threshold current, watchdog deactivation threshold current vs. Junction temperature

3. 5. 1 V_{OUT} = 3.3 V

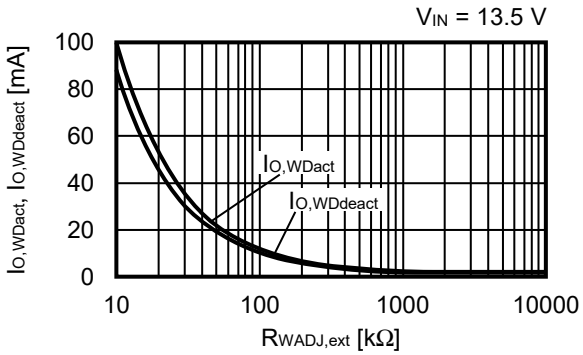


3. 5. 2 V_{OUT} = 5.0 V

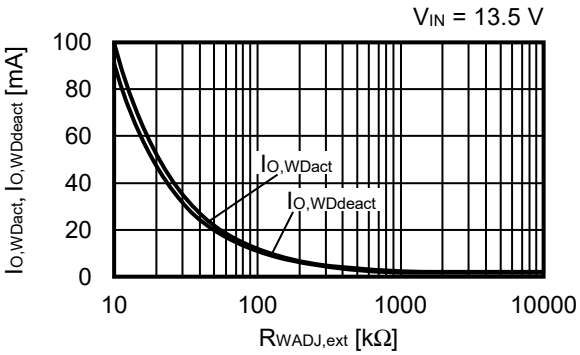


3. 6 Watchdog activation threshold current, Watchdog deactivation threshold current vs. Watchdog activation threshold current adjustment resistance (Ta = +25°C)

3. 6. 1 V_{OUT} = 3.3 V



3. 6. 2 V_{OUT} = 5.0 V



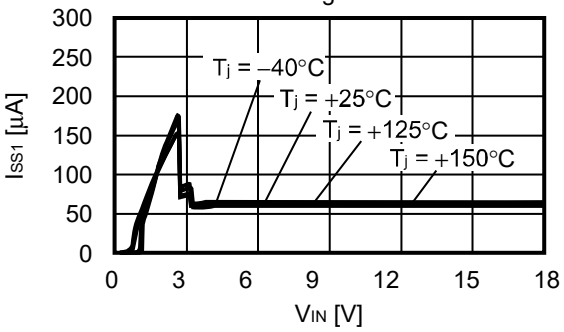
Downloaded from Arrow.com.

4. Overall

4. 1 Current consumption during operation vs. Input voltage

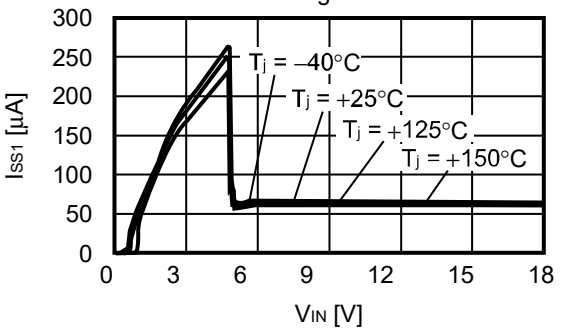
4. 1. 1 V_{OUT} = 3.3 V, $-V_{DET}$ = 2.6 V

When watchdog timer is deactivated



4. 1. 2 V_{OUT} = 5.0 V, $-V_{DET}$ = 4.7 V

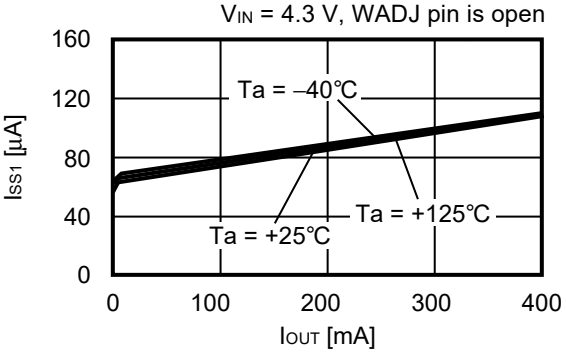
When watchdog timer is deactivated



4. 2 Current consumption during operation vs. Output current

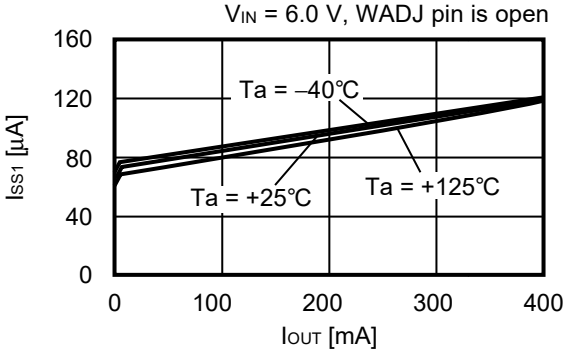
4. 2. 1 V_{OUT} = 3.3 V, $-V_{DET}$ = 2.6 V

V_{IN} = 4.3 V, WADJ pin is open



4. 2. 2 V_{OUT} = 5.0 V, $-V_{DET}$ = 4.7 V

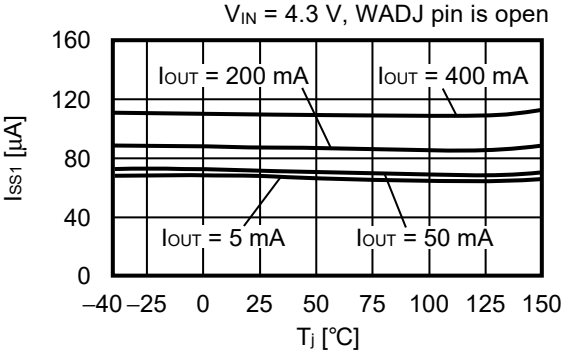
V_{IN} = 6.0 V, WADJ pin is open



4. 3 Current consumption during operation vs. Junction temperature

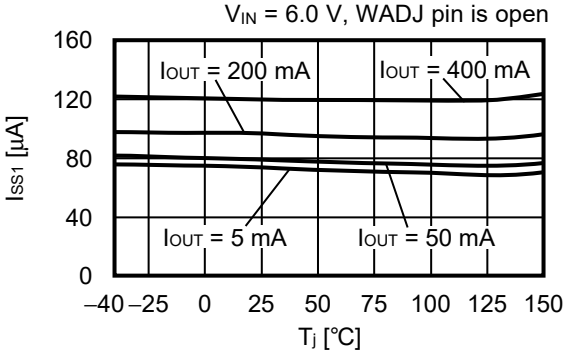
4. 3. 1 V_{OUT} = 3.3 V, $-V_{DET}$ = 2.6 V

V_{IN} = 4.3 V, WADJ pin is open



4. 3. 2 V_{OUT} = 5.0 V, $-V_{DET}$ = 4.7 V

V_{IN} = 6.0 V, WADJ pin is open



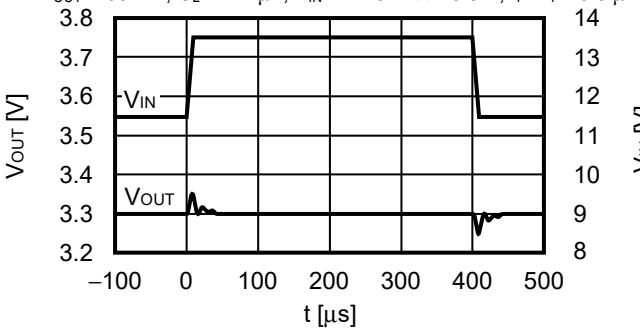
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■ Reference Data

1. Characteristics of input transient response (Ta = +25°C)

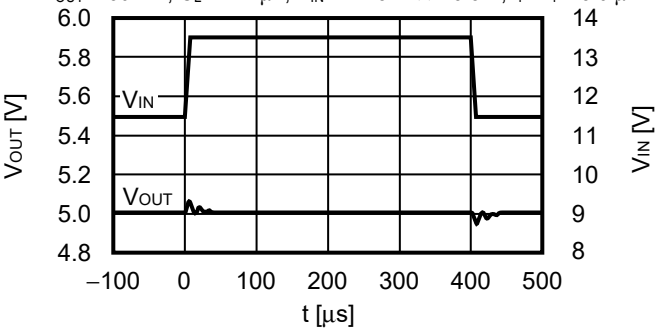
1. 1 V_{OUT} = 3.3 V

I_{OUT} = 30 mA, C_L = 2.2 µF, V_{IN} = 11.5 V ↔ 13.5 V, t_r = t_f = 5.0 µs



1. 2 V_{OUT} = 5.0 V

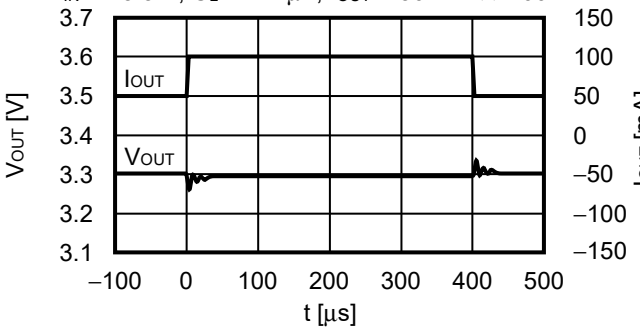
I_{OUT} = 30 mA, C_L = 2.2 µF, V_{IN} = 11.5 V ↔ 13.5 V, t_r = t_f = 5.0 µs



2. Characteristics of load transient response (Ta = +25°C)

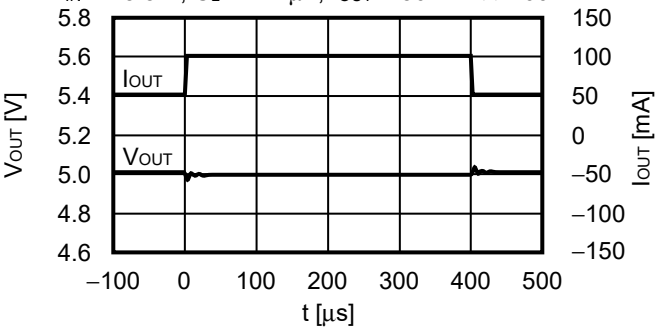
2. 1 V_{OUT} = 3.3 V

V_{IN} = 13.5 V, C_L = 2.2 µF, I_{OUT} = 50 mA ↔ 100 mA



2. 2 V_{OUT} = 5.0 V

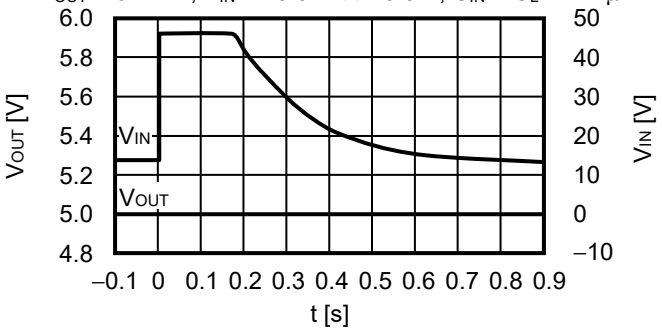
V_{IN} = 13.5 V, C_L = 2.2 µF, I_{OUT} = 50 mA ↔ 100 mA



3. Load dump characteristics (Ta = +25°C)

3. 1 V_{OUT} = 5.0 V

I_{OUT} = 0.1 mA, V_{IN} = 13.5 V ↔ 45.0 V, C_{IN} = C_L = 2.2 µF



4. Example of equivalent series resistance vs. Output current characteristics (Ta = –40°C to +125°C)

C_{IN} = C_L = 2.2 µF, C_{DLY} = 47 nF

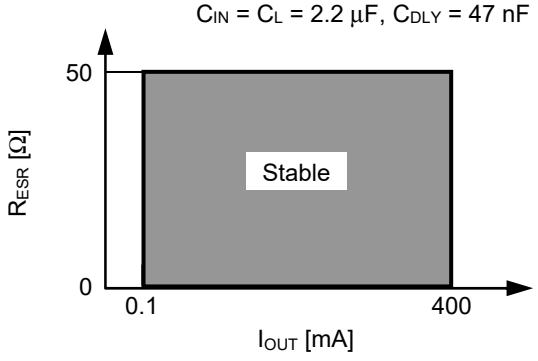
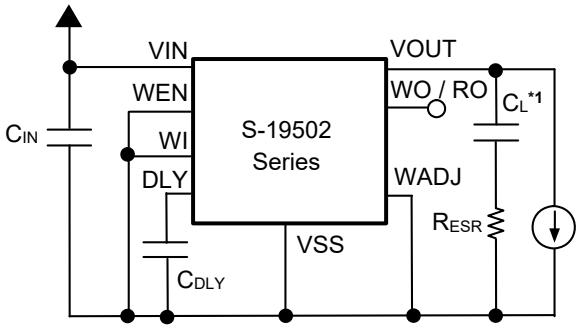


Figure 45



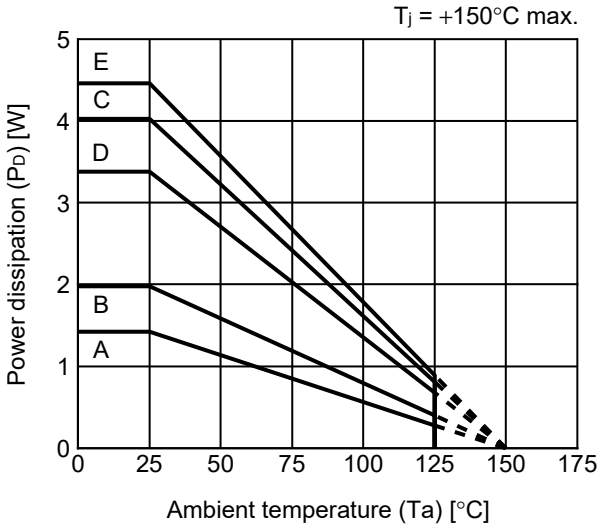
***1.** C_L: Murata Manufacturing Co., Ltd.
GCM31CR71H225K (2.2 µF)

Figure 46

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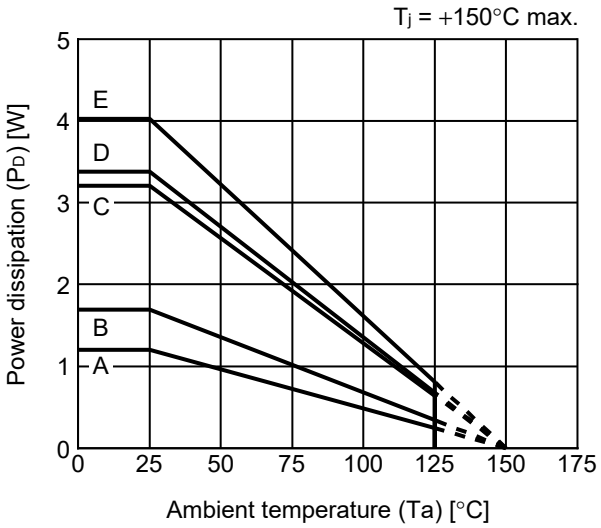
■ Power Dissipation

TO-252-9S



Board	Power Dissipation (P_D)
A	1.42 W
B	1.98 W
C	3.38 W
D	4.03 W
E	4.46 W

HSOP-8A



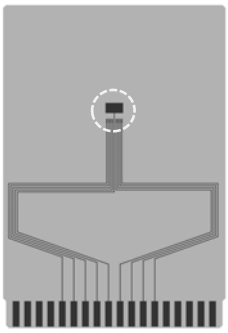
Board	Power Dissipation (P_D)
A	1.20 W
B	1.69 W
C	3.21 W
D	3.38 W
E	4.03 W

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TO-252-9S Test Board

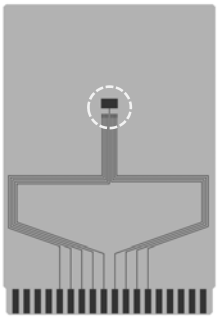
(1) Board A

IC Mount Area



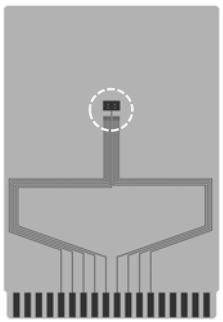
Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		2
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	-
	3	-
	4	74.2 x 74.2 x t0.070
Thermal via		-

(2) Board B



Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		-

(3) Board C



Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		Number: 4 Diameter: 0.3 mm



enlarged view

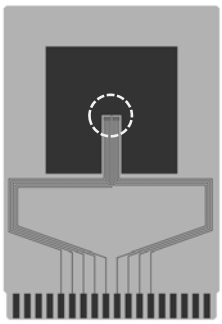
No. TO252-9S-A-Board-SD-1.0

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TO-252-9S Test Board

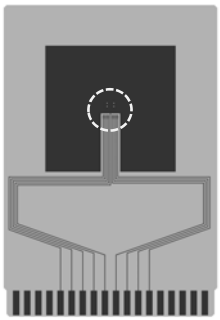
(4) Board D

IC Mount Area



Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Pattern for heat radiation: 2000mm^2 t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		-

(5) Board E



Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Pattern for heat radiation: 2000mm^2 t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		Number: 4 Diameter: 0.3 mm



enlarged view

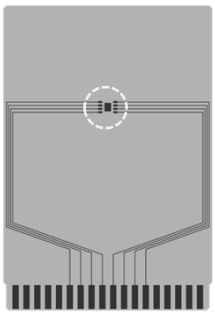
No. TO252-9S-A-Board-SD-1.0

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HSOP-8A Test Board

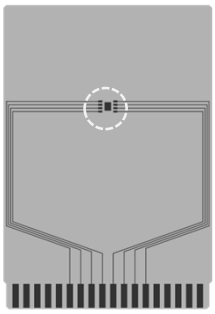
(1) Board A

IC Mount Area



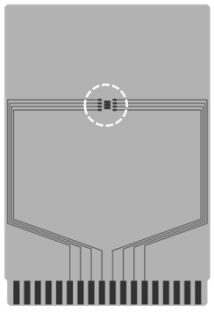
Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		2
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	-
	3	-
	4	74.2 x 74.2 x t0.070
Thermal via		-

(2) Board B

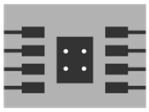


Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		-

(3) Board C



Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		Number: 4 Diameter: 0.3 mm



enlarged view

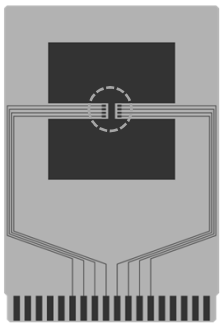
No. HSOP8A-A-Board-SD-1.0

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HSOP-8A Test Board

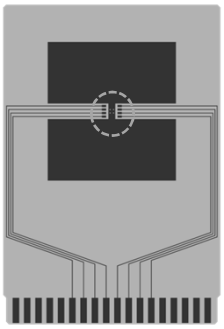
(4) Board D

IC Mount Area

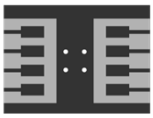


Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Pattern for heat radiation: 2000mm2 t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		-

(5) Board E



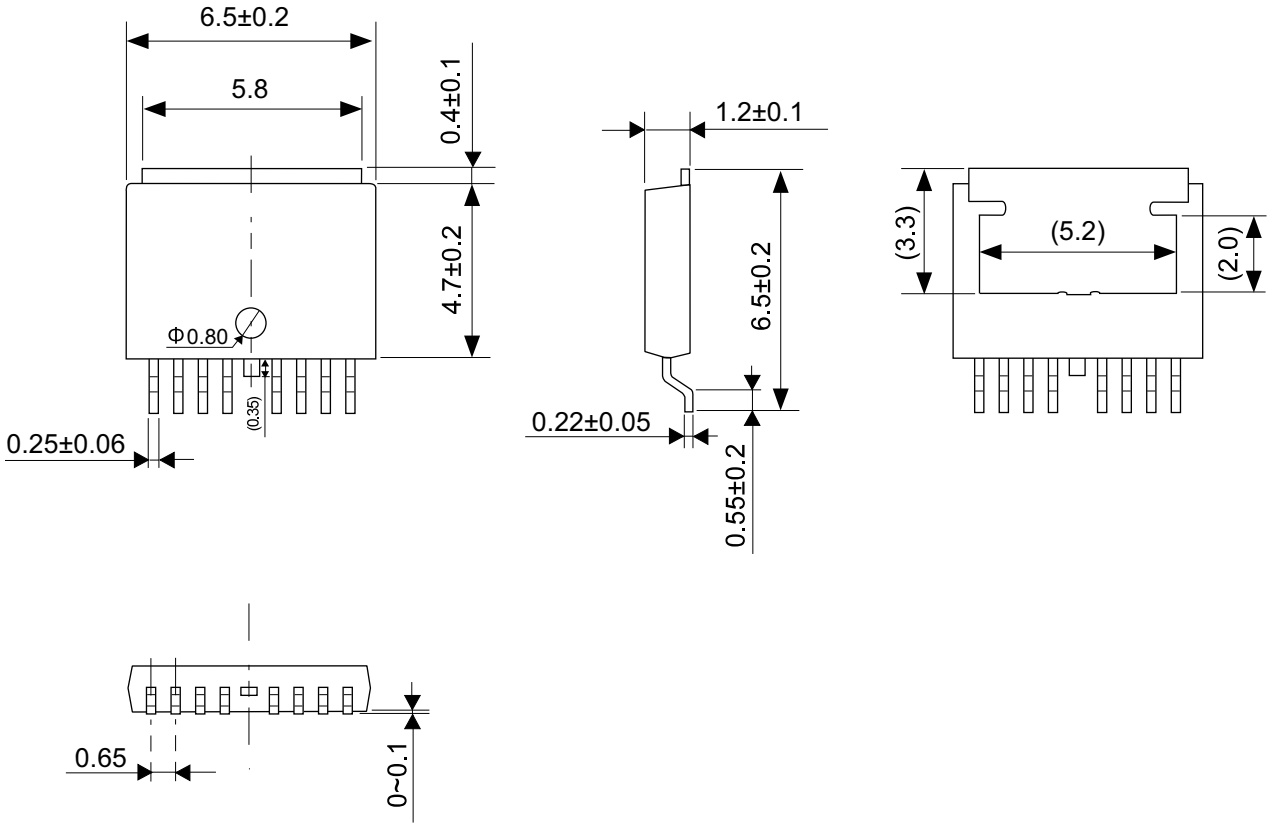
Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Pattern for heat radiation: 2000mm^2 t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		Number: 4 Diameter: 0.3 mm



enlarged view

No. HSOP8A-A-Board-SD-1.0

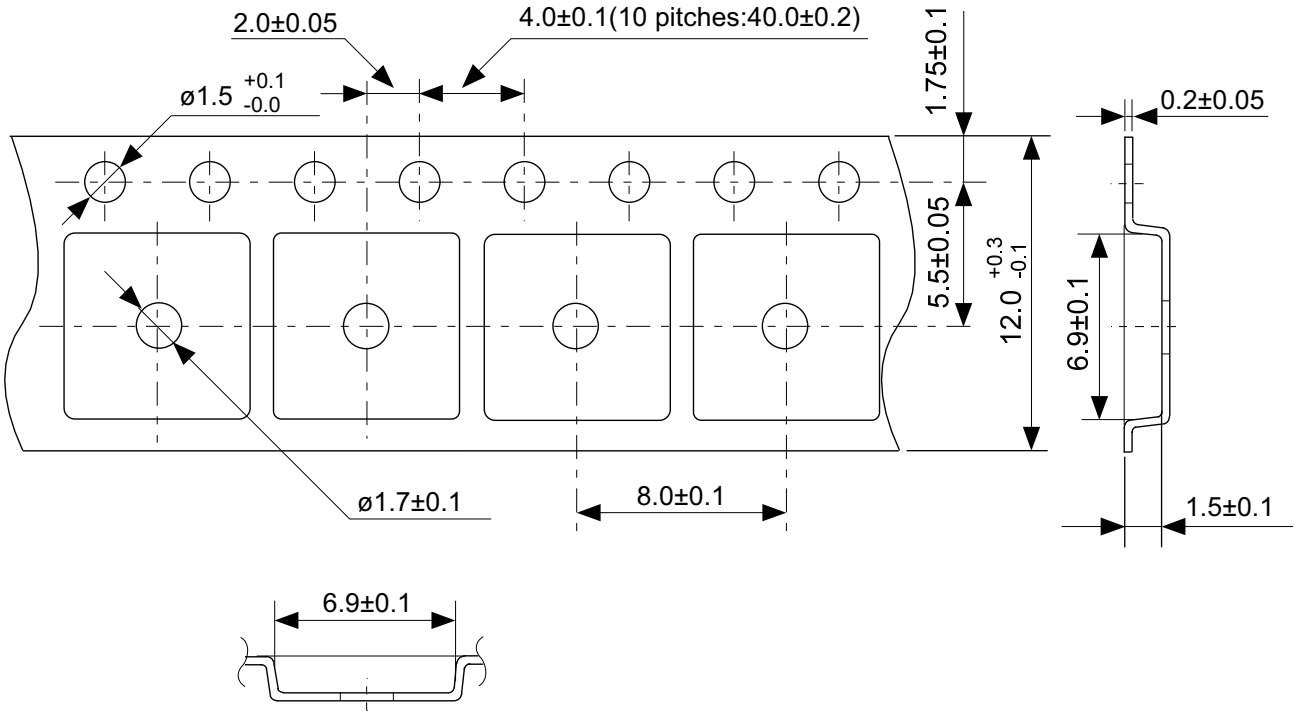
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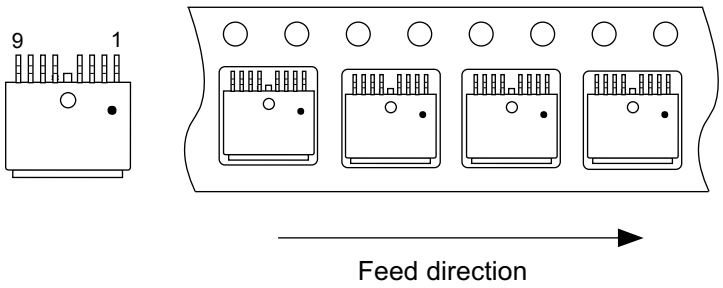


No. VA009-A-P-SD-2.0

TITLE	TO252-9S-A-PKG Dimensions
No.	VA009-A-P-SD-2.0
ANGLE	
UNIT	mm
ABLIC Inc.	

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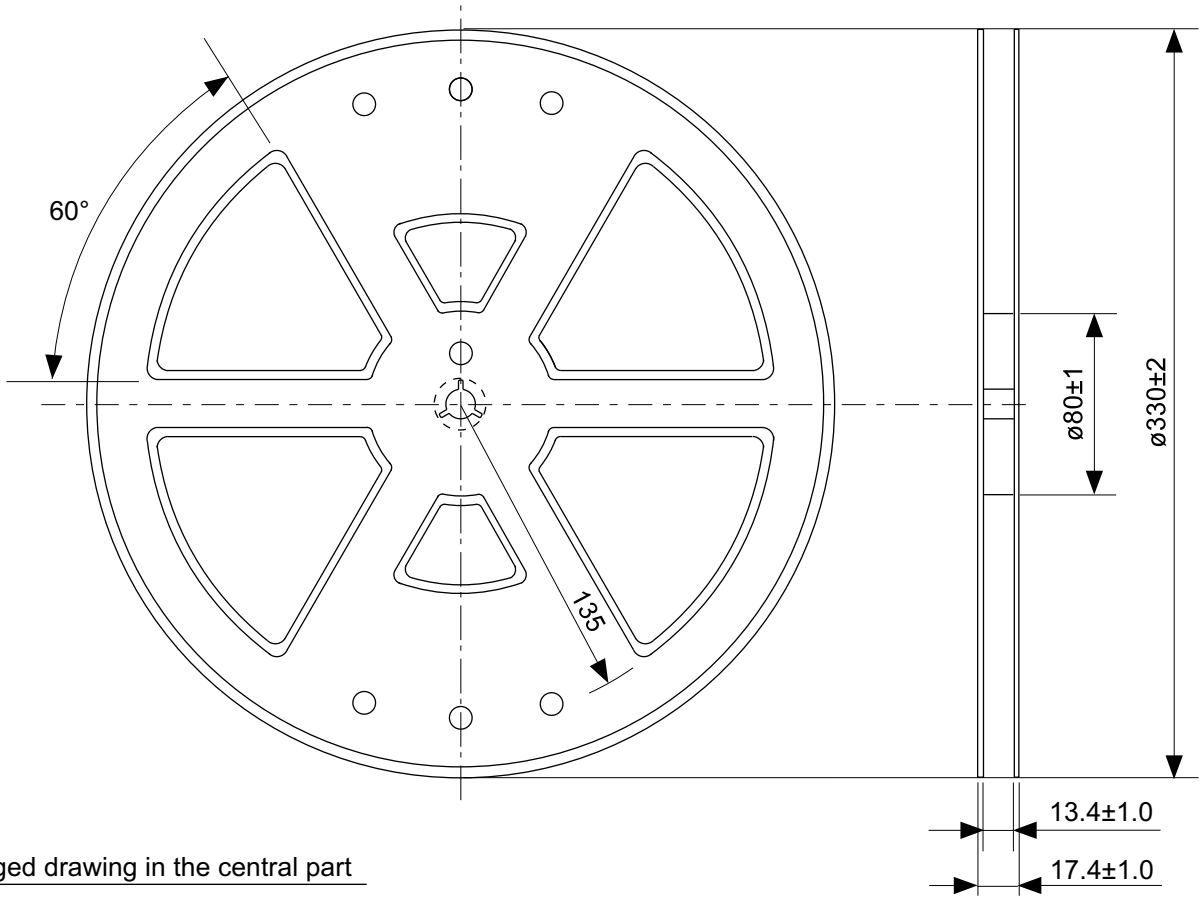




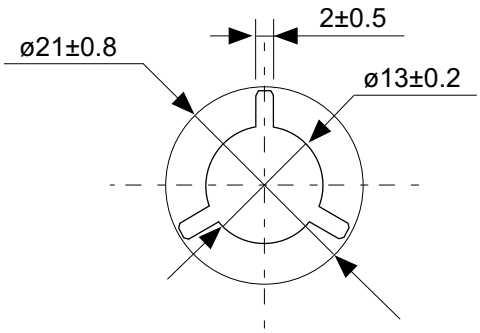
No. VA009-A-C-SD-1.0

TITLE	TO252-9S-A-Carrier Tape
No.	VA009-A-C-SD-1.0
ANGLE	
UNIT	mm
ABLIC Inc.	

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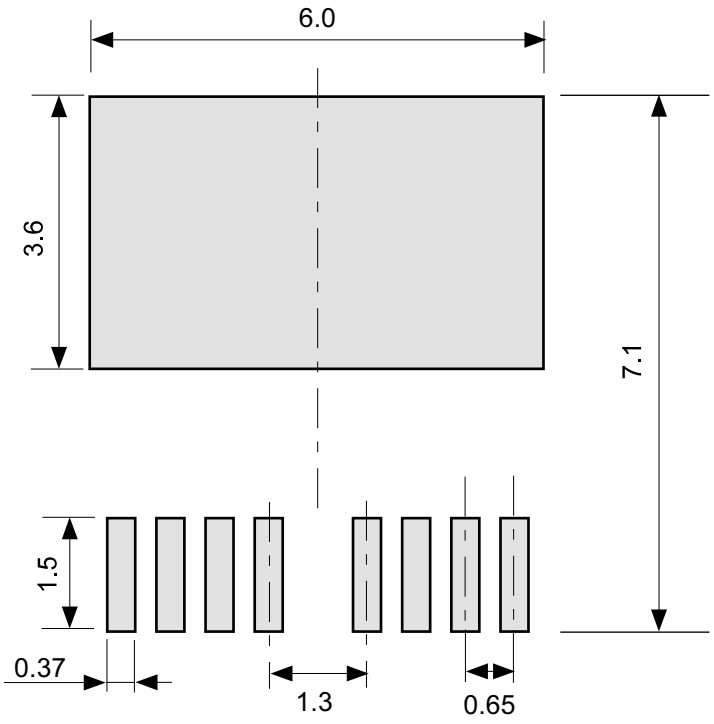
Enlarged drawing in the central part



No. VA009-A-R-SD-1.0

TITLE	TO252-9S-A-Reel		
No.	VA009-A-R-SD-1.0		
ANGLE		QTY.	4,000
UNIT	mm		
ABLIC Inc.			

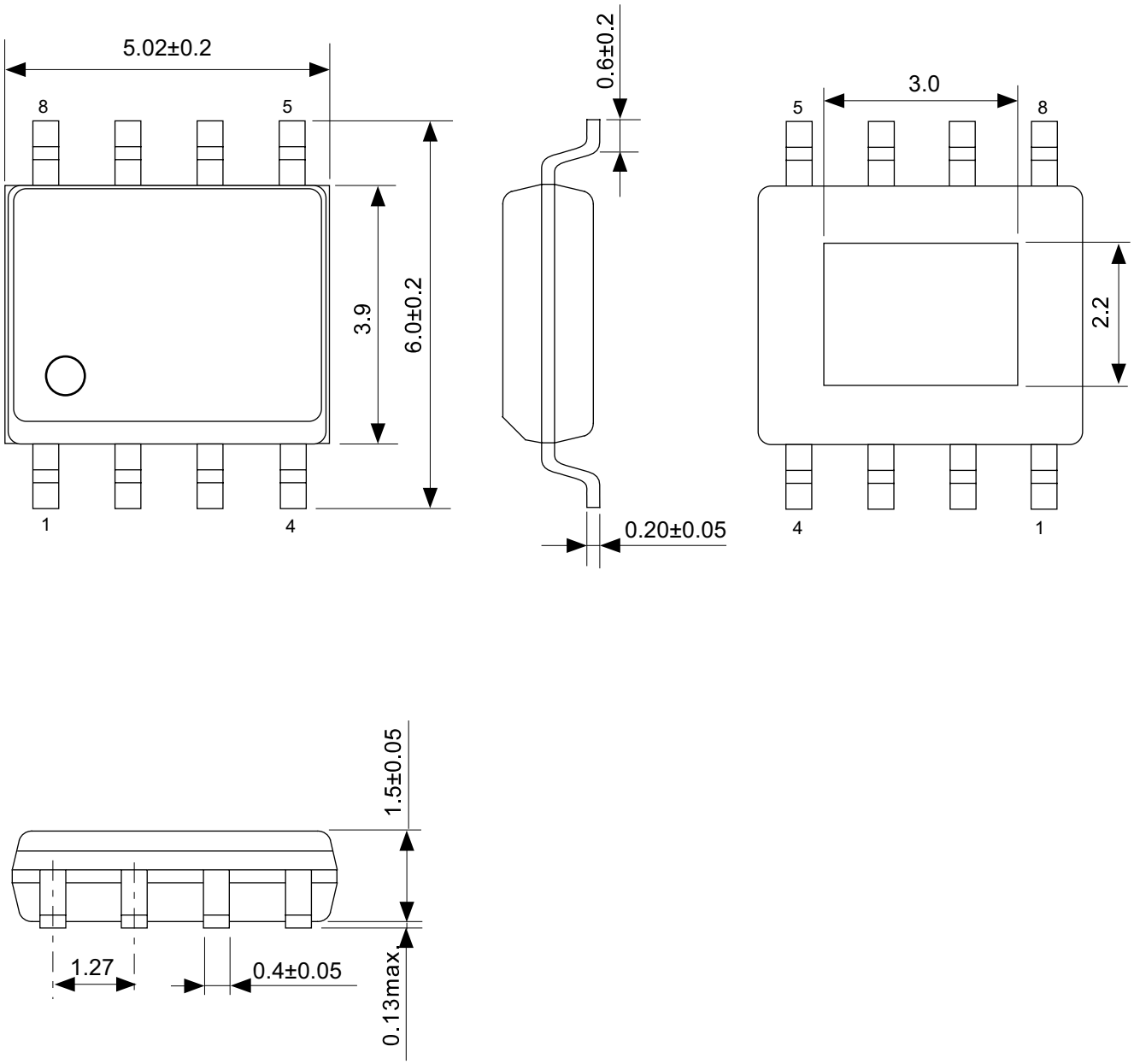
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No. VA009-A-L-SD-1.0

TITLE	TO252-9S-A -Land Recommendation
No.	VA009-A-L-SD-1.0
ANGLE	
UNIT	mm
ABLIC Inc.	

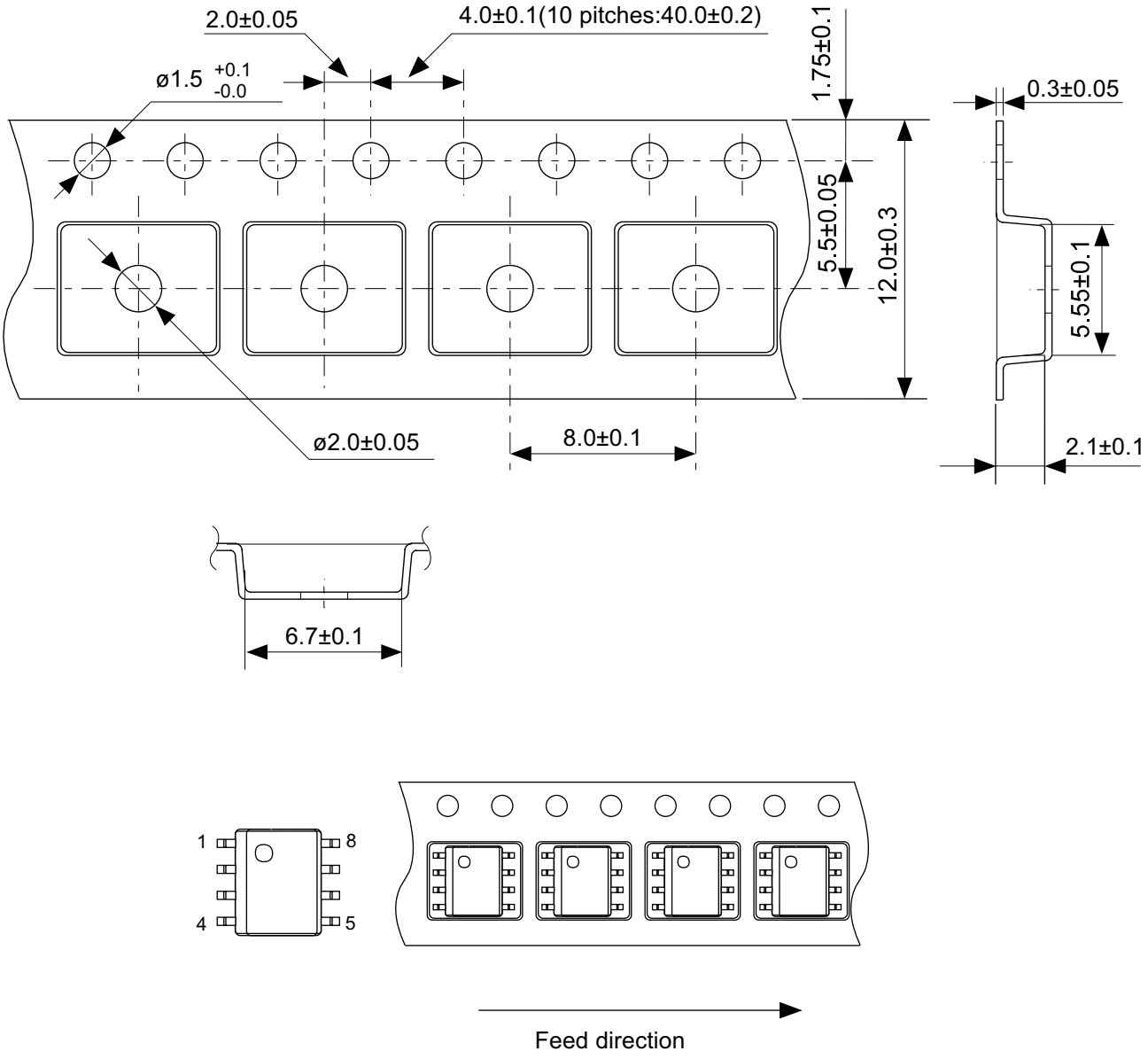
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No. FH008-A-P-SD-2.0

TITLE	HSOP8A-A-PKG Dimensions
No.	FH008-A-P-SD-2.0
ANGLE	
UNIT	mm
ABLIC Inc.	

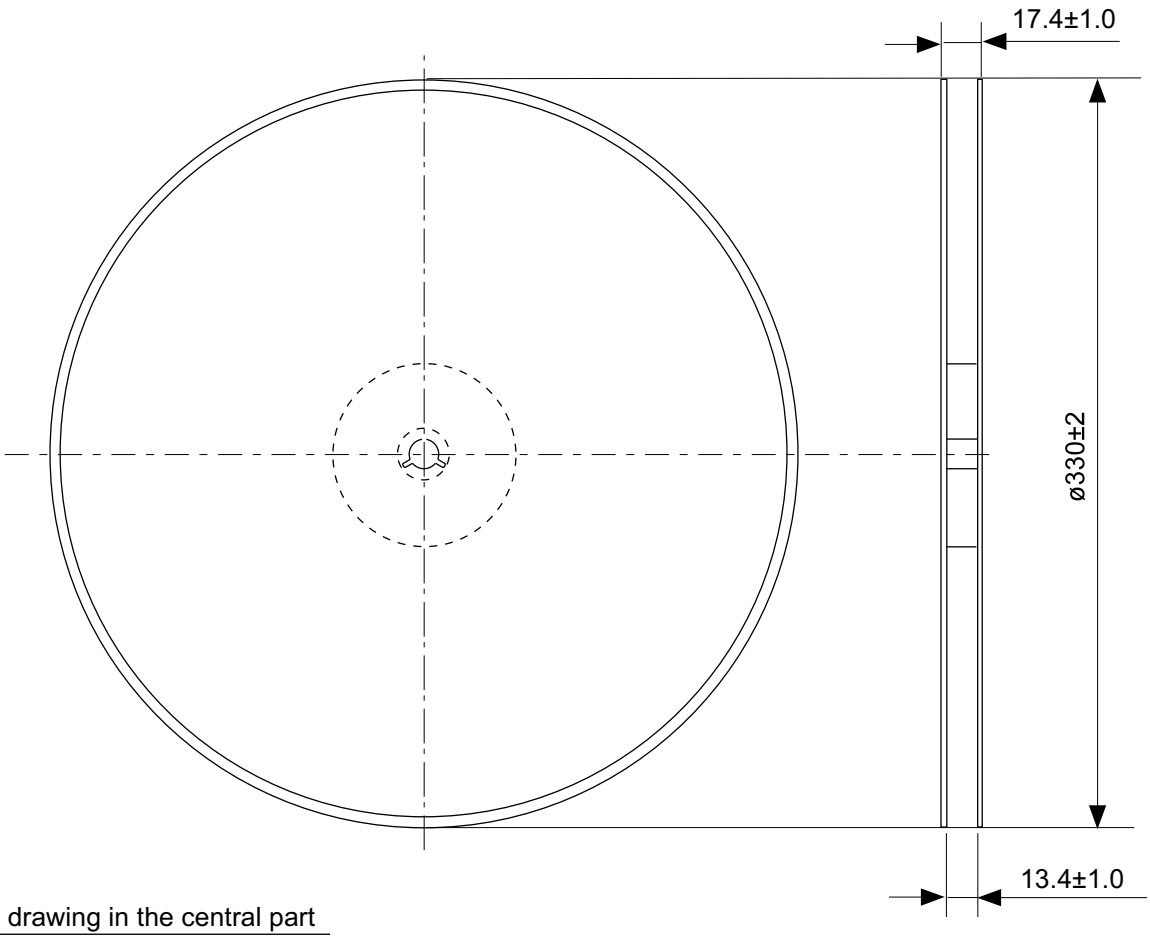
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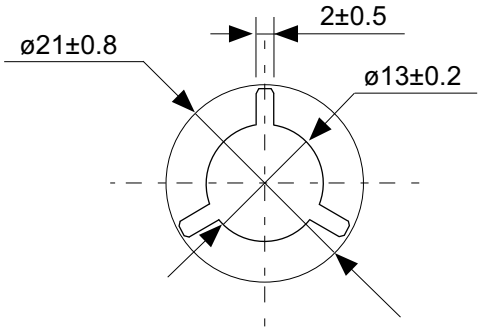
No. FH008-A-C-SD-1.0

TITLE	HSOP8A-A-Carrier Tape
No.	FH008-A-C-SD-1.0
ANGLE	
UNIT	mm
ABLIC Inc.	

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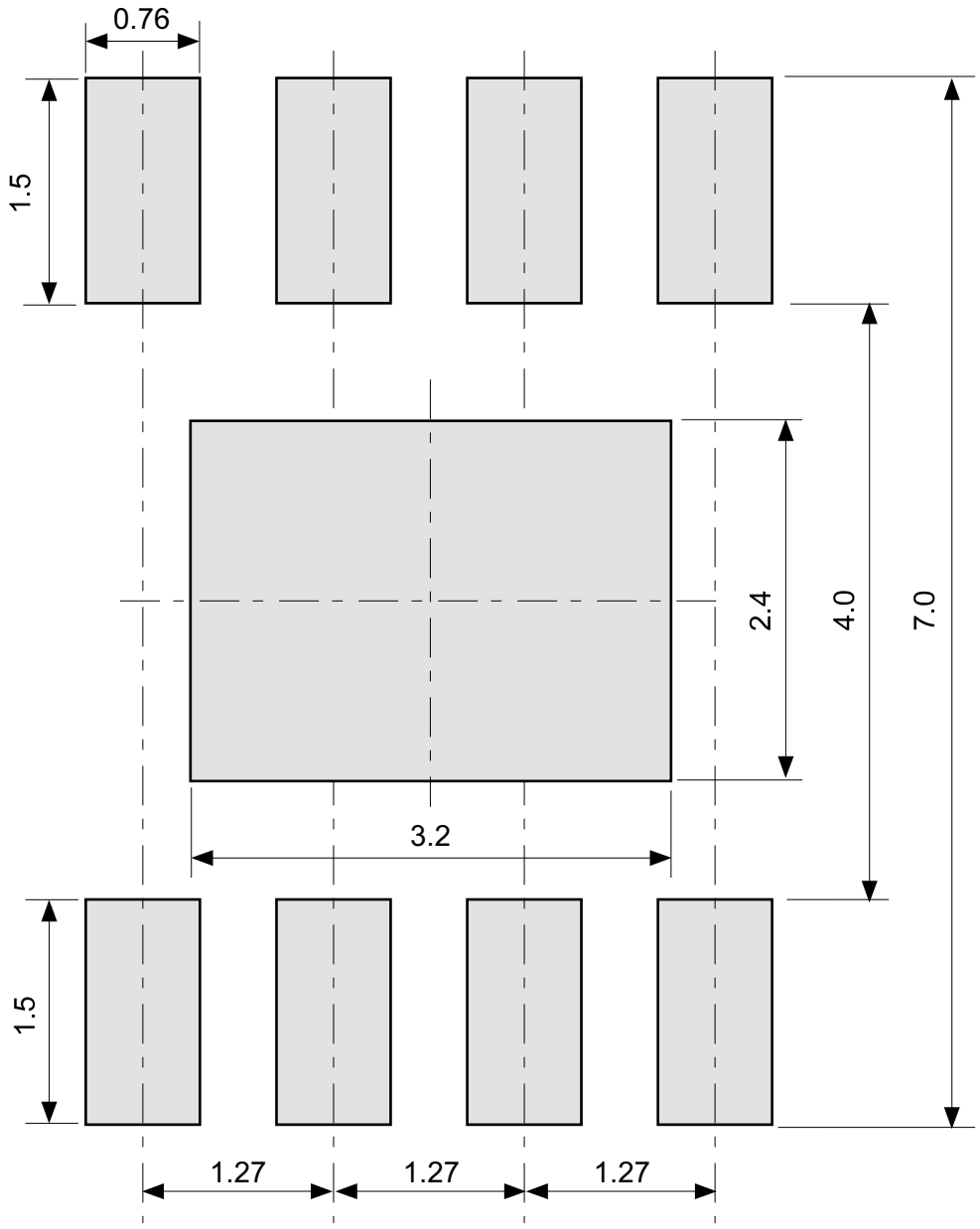
Enlarged drawing in the central part



No. FH008-A-R-SD-1.0

TITLE	HSOP8A-A-Reel		
No.	FH008-A-R-SD-1.0		
ANGLE		QTY.	4,000
UNIT	mm		
ABLIC Inc.			

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No. FH008-A-L-SD-1.0

TITLE	HSOP8A-A -Land Recommendation
No.	FH008-A-L-SD-1.0
ANGLE	
UNIT	mm
ABLIC Inc.	

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