HXBUSX18

Honeywell

18 Bit Bidirectional Bus Transceiver
Radiation Hardened 3.3V SOI CMOS

Features

- 18 Bit Bidirectional Bus Interface
- Rad Hard: 300k Rad(Si) Total Dose
- Single +3.3 V Power Supply
- Supports IEEE standard 1149.1-2001 Boundary Scan
- Functional as One 18 Bit Transceiver or Two 9 Bit Transceivers
- Temperature Range: -55°C to 125°C
- Maximum Operating Frequency: 100MHz
- Packaged in 68 lead CQFP

Low Power (Standby or Quiescent)

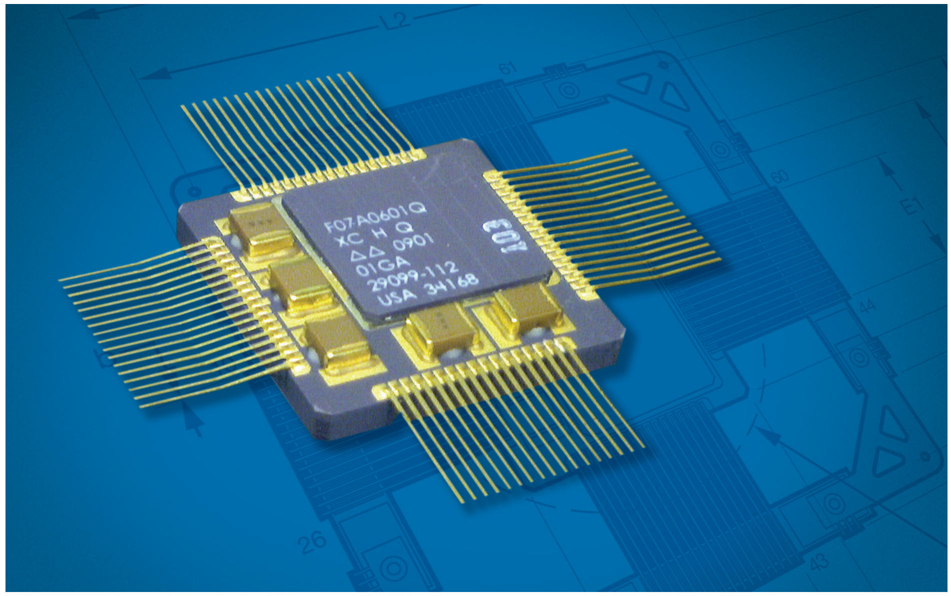
The HXBUSX18 consumes a maximum of 18mW under standby or quiescent conditions.

Flexible Operation

The HXBUSX18 combines D-type latches and D-type flip-flops to allow data to flow in transparent, latched or clocked modes.

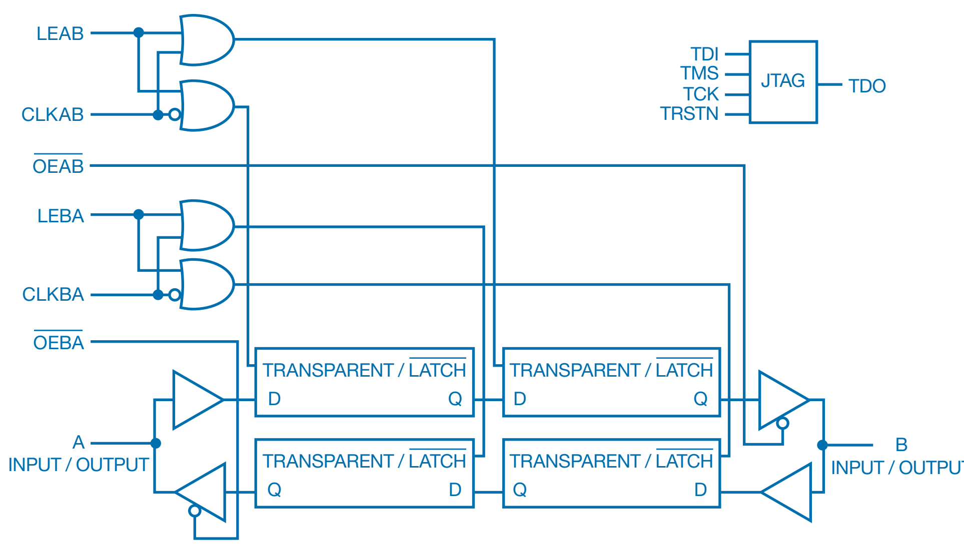
Space Qualified Package

The HXBUSX18 is packaged in a 68 lead quad ceramic flat pack.



The HXBUSX18 is a radiation hardened Silicon On Insulator (SOI) CMOS 3.3V 18-bit bidirectional bus transceiver. This part can be used as either two 9 bit transceivers or one 18 bit transceiver. This part supports the IEEE standard 1149.1-2001 boundary scan to facilitate testing of complex circuit board assemblies. This device is designed specifically for low voltage (3.3V) VDD operation, but with the capability to provide a TTL interface to a 5V system environment.

Functional Block Diagram



Signal Definition

Signal	Description
1LEAB, 2LEAB	Latch Enable Signals. These are 5V tolerant.
1LEBA, 2LEBA	
1OEAB, 2OEAB	Output Enable Signals. These are 5V tolerant.
1OEBA, 2OEBA	
1CLKAB, 2CLKAB	Clock Input Signals. These are 5V tolerant.
1CLKBA, 2CLKBA	
A1[1:9], A2[1:9]	Bidirectional Data Signals. These are 5V tolerant.
B1[1:9], B2[1:9]	
TCK, TDI, TMS	Dedicated JTAG test input signals. These are 5V tolerant.
TDO	Dedicated JTAG test CMOS output signal
IDDQ_MODE	Factory test pin only. This CMOS input needs to have a “0” applied during normal operation. A logic signal “1” on this pin puts the chip into IDDQ mode.
TRSTN	JTAG RESET Signal

Pinout Description

Pin	Symbol	Signal Type	Pin	Symbol	Signal Type
1	IDDQ_MODE (1)	I	35	TRSTN	I
2	VDD	PWR	36	VDD	PWR
3	TDO	OZ	37	TCK	I
4	1CLKAB	I	38	2CLKBA	I
5	1LEAB	I	39	2LEBA	I
6	GND	GND	40	GND	GND
7	1OEAB	I	41	2OEBA	I
8	1A1	B	42	2B9	B
9	1A2	B	43	2B8	B
10	1A3	B	44	2B7	B
11	1A4	B	45	2B6	B
12	1A5	B	46	2B5	B
13	GND	GND	47	GND	GND
14	1A6	B	48	2B4	B
15	1A7	B	49	2B3	B
16	1A8	B	50	2B2	B
17	1A9	B	51	2B1	B
18	NC (2)		52	NC (2)	
19	VDD	PWR	53	VDD	PWR
20	2A1	B	54	1B9	B
21	2A2	B	55	1B8	B
22	2A3	B	56	1B7	B
23	GND	GND	57	GND	GND
24	2A4	B	58	1B6	B
25	2A5	B	59	1B5	B
26	2A6	B	60	1B4	B
27	2A7	B	61	1B3	B
28	2A8	B	62	1B2	B
29	2A9	B	63	1B1	B
30	GND	GND	64	GND	GND
31	2OEAB	I	65	1OEBA	I
32	2LEAB	I	66	1LEBA	I
33	2CLKAB	I	67	1CLKBA	I
34	TDI	I	68	TMS	I

(1) IDDQ_MODE must be tied low for normal operation. Factory test mode is entered when IDDQ_MODE is high.
(2) NC = No Connect (internally connected to ground).

Truth Table

Inputs				
$\overline{\text{OEAB}}$	LEAB	CLKAB	A	Output B
L	L	H	X	Maintain previous output
L	L	L	X	Maintain previous output
L	L	^	L	L
L	L	^	H	H
L	H	X	L	L
L	H	X	H	H
H	X	X	X	Z

Inputs				
$\overline{\text{OEBA}}$	LEBA	CLKBA	B	Output A
L	L	H	X	Maintain previous output
L	L	L	X	Maintain previous output
L	L	^	L	L
L	L	^	H	H
L	H	X	L	L
L	H	X	H	H
H	X	X	X	Z

L = Low voltage level H = High voltage level X = Irrelevant Z = High impedance ^ = Rising clock edge

Functional Description

The HXBUSX18 is a radiation hardened 3.3V 18 bit universal bus transceiver. This part supports IEEE Standard 1149.1-2001 boundary scan to facilitate testing of complex circuit board assemblies. Scan access to the test circuitry is accomplished via the 4 wire Test Access Port (TAP) interface. This device is designed specifically for low voltage (3.3V) VDD operation, but with the capability to provide a TTL interface to a 5V system environment.

In the normal mode, this device is an 18 bit universal bus transceiver. It combines D-type latches and D-type flip-flops to allow data to flow in transparent, latched or clocked modes. It can be used as two 9 bit transceivers or one 18 bit transceiver. The test circuitry can be activated by the TAP to take snapshot samples of the data appearing at the device pins or to perform a self test on the boundary test cells.

Data flow in each direction is controlled by output enable ($\overline{\text{OEAB}}$ and $\overline{\text{OEBA}}$), latch enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. For A to B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A bus data is latched while CLKAB is held at a static low or high logic level. Otherwise, if LEAB is low, A bus data is stored on a low to high transition of CLKAB. When $\overline{\text{OEAB}}$ is low, the B outputs are active. When $\overline{\text{OEAB}}$ is high, the B outputs are in the high impedance state. The functional operation of the device is shown in the Truth Table. B to A data flow is similar to A to B data flow, but uses the $\overline{\text{OEBA}}$, LEBA and CLKBA inputs.

In the test mode, the normal operation of the universal bus transceiver is inhibited, and the test circuitry is enabled to observe and control the I/O boundary of the device. When enabled, the test circuitry performs boundary-scan test operations according to the protocol described in IEEE Standard 1149.1-2001.

Five dedicated test pins are used to observe and control the operation of the test circuitry test data input (TDI), test data output (TDO), test mode select (TMS), test reset (TSRTN) and test clock (TCK).

The functional block diagram for the HXBUSX18 shows a single channel. The HXBUSX18 has 18 single channels that may be configured into either two 9-bit transceivers or one 18-bit transceiver.

Absolute Maximum Ratings (1)

Parameter	Symbol	Conditions	Limits Min	Limits Max	Units
Supply Voltage	V_{DD}	—	-0.5	+4.6	V
DC Input Voltage	V_{IN}	—	-0.5	VDD+0.5	V
DC Output Voltage	V_{OUT}	—	-0.5	VDD+0.5	V
Input Diode Clamp Current (non-bipad inputs only)	I_{ik}	VIN < -0.5V or VIN > VDD+0.5V	-42	+42	mA
Input Diode Clamp Current (bi-directional inputs only)	I_{ik}	VIN < -0.5V or VIN > VDD+0.5V	-84	+84	mA
Output Short Circuit Current, (2)	I_{os}	1 second	-450	+680	mA
DC Output Current, Per Pin	I_o	VOUT = 0 to VDD	-50	+50	mA
Maximum Continuous Current Per Output Pin	—	—	-31.5	31.5	mA
Thermal Resistance, Junction to Case	θ_{JC}	—	—	5.7	°C/W
Storage Temperature Range	T_{STG}	—	-65	+150	°C
Lead Temperature (soldering, 10 seconds)	T_{Lmax}	—	—	260	°C
Junction Temperature	T_J	—	—	+175	°C
ESD (Human Body Model)	—	—	2000	—	V

(1) Stresses above the absolute maximum rating may cause permanent to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
(2) One output at a time should be shorted and the maximum junction temperature should not be exceeded. It should be tested for a maximum of 1 second.

Recommended Operating Conditions (1)(6)

Parameter	Symbol		Limits Min	Max	Units
Supply Voltage		V_{DD}	3.0	3.6	V
Case Temperature		T_C	-55	+125	°C
High Level Input Voltage, (4)		V_{IH}	2.0	—	V
Low Level Input Voltage, (5)		V_{IL}	—	0.8	V
Input Voltage, (3)		V_{IN}	-0.3	6.0	V
Output Voltage, (3)		V_{OUT}	-0.3	6.0	V
High Level Output Current	A Port	I_{OH}	—	-24	mA
	B Port	I_{OH}	—	-24	mA
	TDO	I_{OH}	—	-9	mA
Low Level Output Current	A Port	I_{OL}	—	48	mA
	B Port	I_{OL}	—	48	mA
	TDO	I_{OL}	—	9	mA
Input transition rise or fall rate (clock and edge sensitive inputs) (Outputs enabled)		$\Delta t/\Delta v$	—	1.7	ns/V
Input transition rise or fall rate (non-edge sensitive inputs) (Outputs enabled)		$\Delta t/\Delta v$	—	5.2	ns/V

(1) Specifications listed in datasheet apply when used under the Recommended Operating Conditions unless otherwise specified.
(2) N/A
(3) This applies to 5V tolerant I/O only. The standard CMOS I/O range is -0.3V to V_{DD}+0.3V.
(4) This applies to 5V tolerant inputs/bi-directionals only. The standard CMOS input V_{IH} is 2.52V.
(5) This applies to 5V tolerant inputs/bi-directionals only. The standard CMOS input V_{IL} is 0.9V.
(6) All unused inputs of the device must be held at V_{DD} or GND to ensure proper device operation.

Radiation-Hardness Ratings

Parameter	Symbol	Environment Conditions	Limits	Units
Total Dose	TID		300	krad(Si)
Transient Dose Rate Upset	DRU	Pulse Width = 20ns	1×10^9	rad(Si)/s
Dose Rate Survivability	DRS	Pulse Width ≤ 20ns	1×10^{12}	rad(Si)/s
Neutron Fluence		1MeV equivalent energy	1×10^{14}	N/cm^2

(1) N/A
(2) Device will not latch up due to any of the specified radiation exposure conditions.

Radiation Characteristics

Total Ionizing Dose Radiation

The device radiation hardness assurance TID level was qualified by ^{60}Co testing, including overdose and accelerated annealing, per MIL-STD-883 Method 1019. Ongoing assurance is provided by wafer level X-ray testing during manufacturing.

Transient Dose Rate Ionizing Radiation

Many aspects of product design are addressed to handle the high energy levels associated with the transient dose rate events. The device will maintain basic functional operation during exposure to a pulse up to the DRU specification. The device will meet functional, timing and parametric specifications after exposure to a pulse up to the DRS specification.

Neutron Irradiation Damage

SOI CMOS is inherently tolerant to damage from neutron irradiation. The device meets functional and timing specifications after exposure to the specified neutron fluence.

Latchup

The device will not latchup when exposed to any of the above radiation environments when applied under recommended operating conditions. SOI CMOS provides oxide isolation between adjacent PMOS and NMOS transistors and eliminates any potential SCR latchup structures.

Electrical Requirements (1)(2)(3)

Parameter	Symbol	Conditions	Limits Min	Max	Units
Output High Voltage	V_{OH5A}	V_{DD} = 3.0V, I_{OH} = -100µA	V_{DD}-0.2	—	V
(Ports A and B)	V_{OH5B}	V_{DD} = 3.0V, I_{OH} = -8mA	2.4	—	V
	V_{OH5C}	V_{DD} = 3.0V, I_{OH} = -24mA	2	—	V
(TDO only)	V_{OH3_33}	V_{DD} = 3.0V, I_{OH} = -9 mA	V_{DD}-0.5V	—	V
Output Low Voltage	V_{OL5A}	V_{DD} = 3.0V, I_{OL} = 100µA	—	0.2	V
	V_{OL5B}	V_{DD} = 3.0V, I_{OL} = 16 mA	—	0.4	V
(Ports A and B)	V_{OL5C}	V_{DD} = 3.0V, I_{OL} = 32 mA	—	0.5	V
	V_{OL5D}	V_{DD} = 3.0V, I_{OL} = 48 mA, (4)	—	0.55	V
(TDO only)	V_{OL3_33}	V_{DD} = 3.0V, I_{OL} = 9 mA	—	0.5	V
Low Level Input Voltage (5V tolerant inputs/bi-directionals)	V_{IL_T33}	V_{DD} = 3.0V	0.8	—	V
High Level Input Voltage (5V tolerant inputs/bi-directionals)	V_{IH_T33}	V_{DD} = 3.6V	—	2.0	V
Low Level Input Voltage (CMOS inputs), (4)	V_{IL_33}	V_{DD} = 3.0V	0.9	—	V
High Level Input Voltage (CMOS inputs), (4)	V_{IH_33}	V_{DD} = 3.6V	—	2.52	V
Input Current	I_{IL1_33}	V_{DD} = 3.6V, V_{IN} = GND	-10	+10	µA
(non 5V tolerant – $I_{DDQmode}$)	I_{IH1_33}	V_{DD} = 3.6V, V_{IN} = V_{DD}	-10	+10	µA
Input Current	I_{IL1_T33}	V_{DD} = 3.6V, V_{IN} = GND	-10	+10	µA
(CMOS input 5V tolerant)	I_{IL2_T33}	V_{DD} = 3.6V, V_{IN} = GND	-1	-0.2	mA
	I_{IH1_T33}	V_{DD} = 3.6V, V_{IN} = V_{DD}	-10	+10	µA
	I_{IH2_T33}	V_{DD} = 3.6V, V_{IN} = V_{DD}	-10	+10	µA
	I_{5Vi1_T33}	V_{DD} = 3.6V, V_{IN} = 5.5V	-10	+10	µA
	I_{5Vi2_T33}	V_{DD} = 3.6V, V_{IN} = 5.5V	-10	+10	µA
Three-state Output Leakage High	I_{OZH1_T33}	V_{DD} = 3.6V, V_{OUT} = V_{DD}	-20	+20	µA
	I_{OZH4_T33}	V_{DD} = 3.0V, V_{OUT} = 2.5V	-300	0	µA
(Ports A and B)	I_{5VO1_T33}	V_{DD} = 3.6V, V_{OUT} = 5.5V	-20	+20	µA
(TDO only)	I_{OZH1_33}	TDO, V_{DD} = 3.6V, V_{OUT} = V_{DD}	-10	+10	µA
	I_{OZH4_33}	TDO, V_{DD} = 3.0V, V_{OUT} = 2.5V	-300	-60	µA
	I_{5VO4_T33}	TDO, V_{DD} = 3.6V, V_{OUT} = 5.5V	-20	+20	µA
Three-state Output Leakage Low	I_{OZL1_T33}	V_{DD} = 3.6V, V_{OUT} = GND	-20	+20	µA
(Ports A and B)	I_{OZL4_T33}	V_{DD} = 3.0V, V_{OUT} = 0.5V	+100	+350	µA
(TDO only)	I_{OZL1_33}	TDO, V_{DD} = 3.6V, V_{OUT} = GND	-10	+10	µA
	I_{OZL4_33}	TDO, V_{DD} = 3.0V, V_{OUT} = 0.5V	+30	+280	µA
Standby Supply Current	I_{DDSB_33}	V_{DD} = 3.6 V, V_{IN} = V_{DD} or GND (in steady-state static current state), Clk = 0 MHz	—	+5.0	mA
Quiescent Supply Current	I_{DDQ_33}	V_{DD} = 3.6 V, V_{IN} = V_{DD} or GND,	—	+5.0	mA
Dynamic Supply Current		V_{DD} = 3.6V, all outputs toggling			
	I_{DDOP1_33}	1 MHz	—	+189	mA
	I_{DDOP2_33}	10 MHz	—	+208	mA
	I_{DDOP3_33}	100 MHz	—	+990	mA

(1) Conditions: Supply Voltage: 3.0 to 3.6V with V_{SS} = 0V (ground); Case Temperature (TC) -55°C to +125°C.
(2) Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground.
(3) All electrical requirements shall be for pre - and post radiation as guaranteed by design.
(4) Guaranteed but not tested by vendor.

Capacitance Parameters (1)

Parameter	Symbol	Conditions	Limits Min	Limits Max	Units
Input Capacitance	C_I	V_{IN} = 3 V or 0, input only pins	—	13	pF
Input – Output Capacitance	C_{IO}	V_{OUT} = 3 V or 0, A and B port pins	—	24	pF
Output Capacitance	C_O	V_{OUT} = 3 V or 0, TDO pin only	—	14.5	pF

(1) Guaranteed but not tested by vendor.

Switching Parameters

Parameter	Symbol	Conditions	Limits Min	Limits Max	Units
Clock Frequency	f_{clock}	CLKAB or CLKBA	---	100	MHz
Pulse Duration	T_{w_clkab}	CLKAB high to low	—	+4.6	ns
	T_{w_clkba}	CLKBA high to low	—	+4.6	ns
	T_{w_leab}	LEAB high	—	+3.2	ns
	T_{w_leba}	LEBA high	—	+3.2	ns
Setup Time	T_{su_clkab}	A before CLKAB↑		+4	ns
	T_{su_clkba}	B before CLKBA↑		+4	ns
	T_{su_leab}	A before LEAB↓, CLK=high or low		+3.3	ns
	T_{su_leba}	B before LEBA↓, CLK=high or low		+3.3	ns
Hold Time	T_{h_clkab}	A after CLKAB↑		+2.4	ns
	T_{h_clkba}	B after CLKBA↑		+2.4	ns
	T_{h_leab}	A after LEAB↓		+4.4	ns
	T_{h_leba}	B after LEBA↓		+4.4	ns
Propagation Delay (Transparent Mode) (3)(4)	t_{PLH}	From input A or B to output B or A	1.75	8.2	ns
Propagation Delay (Transparent Mode) (3)(4)	t_{PHL}	From input A or B to output B or A	1.75	8.0	ns
Propagation Delay Clock to Output (A/B) (3)(4)	t_{PLHC}	From input CLKAB or CLKBA to output B or A	1.75	9.1	ns
Propagation Delay Clock to Output (A/B) (3)(4)	t_{PHLC}	From input CLKAB or CLKBA to output B or A	1.75	8.9	ns
Propagation Delay LEAB to Output (A/B) (3)(4)	t_{PLHL}	From input LEAB or LEBA to output B or A	1.75	8.8	ns
Propagation Delay LEBA to Output (A/B) (3)(4)	t_{PHLL}	From input LEAB or LEBA to output B or A	1.75	7.7	ns
Disable Time (3)(4)	t_{PHZ}	From input OEAB or OEBA to output B or A		10.3	ns
Disable Time (3)(4)	t_{PLZ}	From input OEAB or OEBA to output B or A		10.0	ns
Enable Time (3)(4)	t_{PZH}	From input OEAB or OEBA to output B or A	1.75	11.4	ns
Enable Time (3)(4)	t_{PZL}	From input OEAB or OEBA to output B or A	1.75	9.6	ns

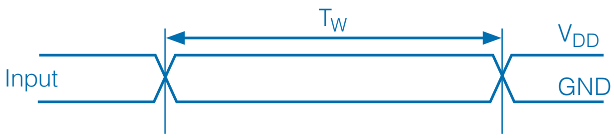
(1) Conditions: Supply Voltage: 3.0 to 3.6V with V_{SS} = 0V (ground); Case Temperature (TC) -55°C to +125°C.
(2) All electrical requirements shall be for pre - and post radiation as guaranteed by design.
(3) t_r < 2.5 ns, t_f < 2.5 ns.
(4) C_{load} = 50pF

Signal Integrity

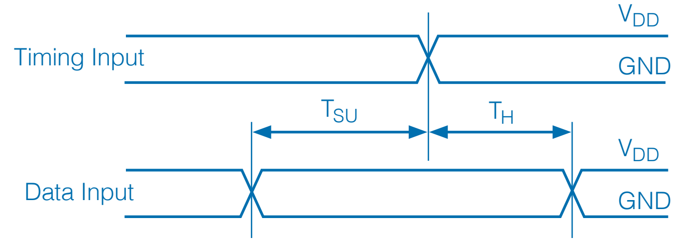
As a general design practice, for digital input signals, one should have good signal integrity which means input signals that are free of noise, glitches and ringing with rising and falling edges of ≤10ns. More specifically, an input is considered to have good signal integrity when the input voltage monotonically traverses the region between VIL and VIH in ≤10ns.

Floating inputs for an extended period of time is not recommended.

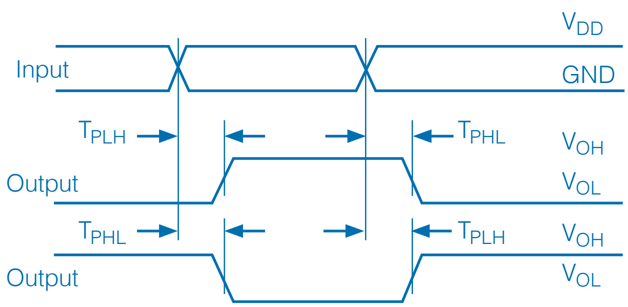
AC Timing Input and Output References



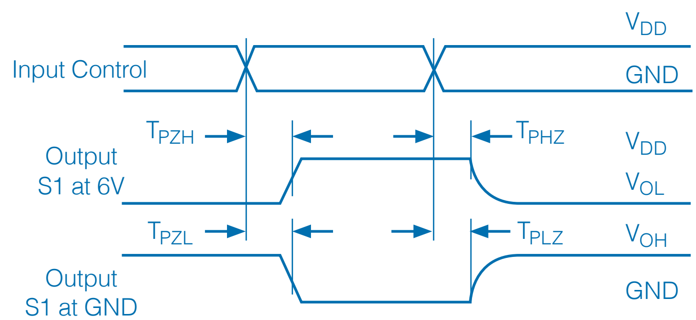
Pulse Width Waveform



Setup and Hold Waveforms

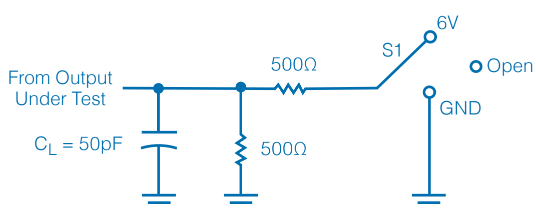


Output Propagation Waveforms



Enable Propagation Waveforms

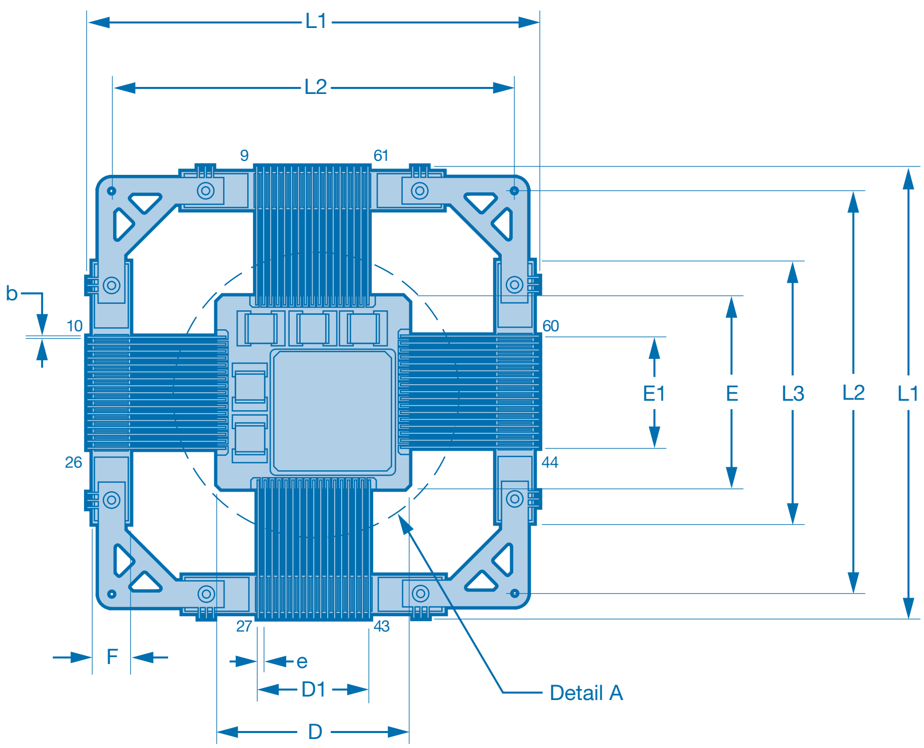
Reference Load Circuit

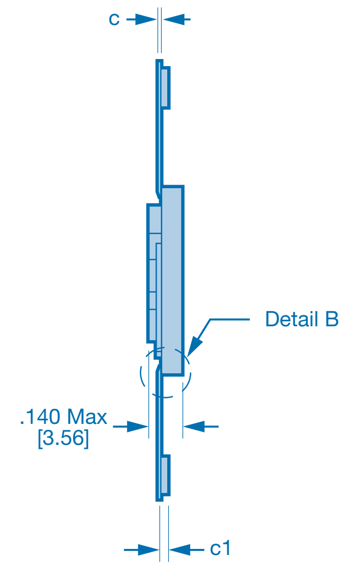


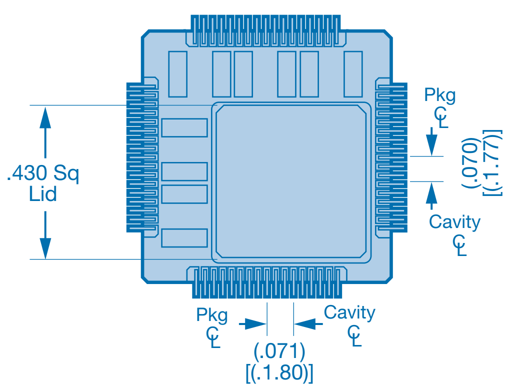
Load Circuit

Test	S1
TPLH, TPHL	OPEN
TPLZ, TPZL	6V
TPHZ, TPZH	GND

Packaging Outline Dimensions

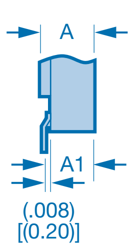






Detail A

Symbol	Dimensions - Inches Min	Nom	Max	Dimensions - Millimeters Min	Nom	Max
A	.090	.100	.111	2.29	2.54	2.82
A1	.072	.080	.088	1.83	2.03	2.23
b	.008	.010	.012	0.20	0.25	0.30
c	.005	.006	.008	0.13	0.15	0.20
c1	.030	.035	.040	0.76	0.89	1.02
D/E	.693	.700	.707	17.60	17.78	17.96
D1/E1	.395	.400	.405	10.03	10.16	10.29
e	.020	.025	.030	.505	.635	.765
F	.130	.140	.150	3.31	3.56	3.81
L1		1.641 BSC			41.68 BSC	
L2		1.460 BSC			37.08 BSC	
L3		.950 BSC			24.13 BSC	



Detail B

Reliability

For many years Honeywell has been producing integrated circuits that meet the stringent reliability requirements of space and defense systems. Honeywell has delivered hundreds of thousands of QML parts since the early 1990's. Using this proven approach Honeywell will assure the reliability of the products manufactured with the SOI CMOS process technology. This approach includes adhering to Honeywell's Quality Management Plan for:

- Designing in reliability by establishing electrical rules based on wear out mechanism characterization performed on specially designed test structures (electromigration, TDDB, hot carriers, bias temperature instability and radiation).
- Utilizing a structured and controlled design process.
- Statistically controlling wafer fabrication process with a continuous defect reduction process.
- Performing individual wafer lot acceptance through process monitor testing (includes radiation testing).
- Using characterized and qualified packages.
- Performing thorough product testing program based on MIL-PRF-38535 and MIL-STD 883.

Screening and Conformance Inspection

The product test flow includes screening units with the applicable flow (Engineering Model, QML V, QML Q, Class V and Q equivalent) and the appropriate periodic or lot conformance testing (Groups A, B, C, D, and E). Both the wafer process and the products are subject to periodic or lot based Technology Conformance Inspection (TCI) and Quality Conformance Inspection (QCI) tests as defined by Honeywell's Quality Management Plan.

Screening and Conformance Inspection

Group A	General Electrical Tests
Group B	Mechanical – Resistance to Solvents, Bond Strength, Die Shear, Solderability
Group C	Life Tests – 1000 hours at 125°C or equivalent
Group D	Package related mechanical tests – Physical Dimensions, Lead Integrity, Thermal Shock, Temp Cycle, Moisture Resistance, Seal, Mechanical Shock, Vibration, Acceleration, Salt Atmosphere, Internal Water Vapor, Adhesion of Lead Finish
Group E	Radiation Tests

Ordering Information (1)

Standard Microcircuit Drawing

The HXBUSX18 can be ordered under the SMD drawing 5962-07A06.

H	X	BUSX	18	F	V	F
Source H = Honeywell	**Process** X = SOI CMOS	**Part Number**	**Part Type**	**Package Designation** F = 68 Pin Quad Flat Pack	**Screen Level** V = QML V W = QML Q+ E = Eng. Model (2)	**Total Dose Hardness** F = 3x10^5 rad (Si) N = No Level Guaranteed (2)

(1) Orders may be faxed to 763-954-2051. Please contact our Customer Service Representative at 1-763-954-2474 for further information.
(2) Engineering Device Description: Parameters are tested -55°C to 125°C, 24 hour burn-in, no radiation guaranteed.

QCI Testing (1)

Classification	QCI Testing
QML Q+	No lot specific testing performed. (2)
QML V	Lot specific testing required in accordance with MIL-PRF-38535 Appendix B.

(1) QCI groups, subgroups and sample sizes are defined in MIL-PRF38535 and the Honeywell QM Plan. Quarterly testing is done in accordance with the Honeywell QM Plan.
(2) If customer requires lot specific testing, the purchase order must indicate specific tests and sample sizes.

Find out more

To learn more about Honeywell's radiation hardened integrated circuit products and technologies, visit www.honeywell.com/microelectronics.

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