TEXAS INSTRUMENTS

Data sheet acquired from Harris Semiconductor
SCHS098D – Revised October 2003

CD40107B Types

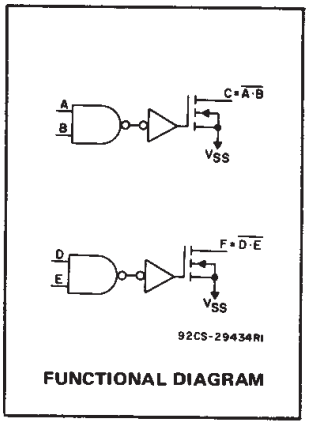
CMOS Dual 2-Input NAND Buffer/Driver

High-Voltage Type (20-Volt Rating)

The CD40107B is a dual 2-input NAND buffer/driver containing two independent 2-input NAND buffers with open-drain single n-channel transistor outputs. This device features a wired-OR capability and high output sink current capability (136 mA typ. at V_{DD} = 10 V, V_{DS} = 1 V). The CD40107B is supplied in 8-lead hermetic dual-in-line ceramic packages (F3A suffix), 8-lead dual-in-line plastic packages (E suffix), 8-lead small-outline packages (M, M96, MT, and PSR suffixes), and 8-lead thin shrink small-outline packages (PW and PWR suffixes).

Features:

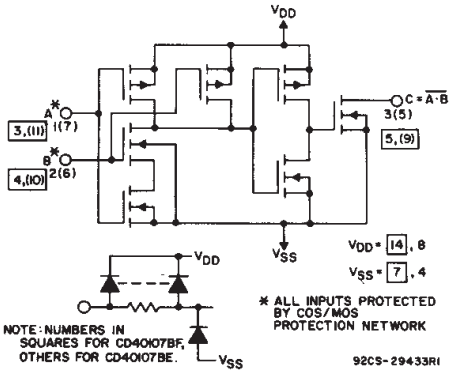
- 32 times standard B-Series output current drive sinking capability — 136 mA typ. @ V_{DD} = 10 V, V_{DS} = 1 V
- 100% tested for quiescent current at 20 V
- Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- 5-V, 10-V, and 15-V parametric ratings
- Noise margin, full package temperature range, R_L to V_{DD} = 10 kΩ:
  1 V at V_{DD} = 5 V
  2 V at V_{DD} = 10 V
  2.5 V at V_{DD} = 15 V
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"



FUNCTIONAL DIAGRAM

Applications

- Driving relays, lamps, LEDs
- Line driver
- Level shifter (up or down)



TRUTH TABLE

A	B	C	
0	0	1*	Z#
1	0	1*	Z#
0	1	1*	Z#
1	1	0	

*Requires external pull-up resistor (R_L) to V_{DD}.

#Without pull-up resistor (3-state).

Fig.1 — Schematic diagram of CD40107B (one of 2 gates)

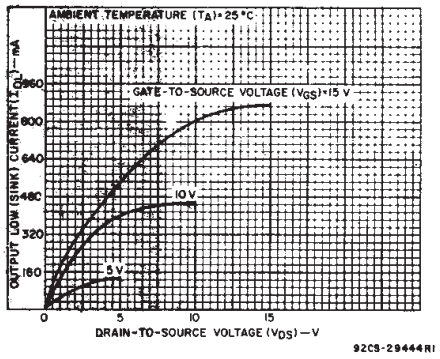


Fig.2 — Typical output low (sink) current characteristics.

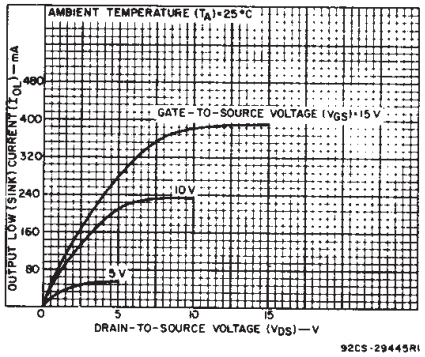


Fig.3 – Minimum output low (sink) current characteristics.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
  Voltages referenced to V_{SS} Terminal) ..... -0.5V to +20V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5V to V_{DD} +0.5V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10mA
POWER DISSIPATION PER PACKAGE (P_D):
  For T_A = -55°C to +100°C 500mW
  For T_A = +100°C to +125°C ..... Derate Linearity at 12mW/°C to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
  FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types)..... 100mW
OPERATING-TEMPERATURE RANGE (T_A) .....-55°C to +125°C
STORAGE TEMPERATURE RANGE (T_{stg}) .....-65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
  At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max ..... +265°C

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A= Full Package-Temperature Range)	3	18	V

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25^oC$, $C_L = 50$ pF, Input $t_r, t_f = 20$ ns

CHARACTERISTIC	TEST CONDITIONS	V_{DD} Volts	LIMITS Typ.	LIMITS Max.	UNITS
Propagation Delay: High-to-Low, t_{PHL}	R_L* = 120 Ω	5	100	200	ns
		10	45	90	
		15	30	60	
Low-to-High, t_{PLH}	R_L* = 120 Ω	5	100	200	ns
		10	60	120	
		15	50	100	
Transition Time: High-to-Low, t_{THL}	R_L* = 120 Ω	5	50	100	ns
		10	20	40	
		15	10	20	
Low-to-High, t_{TLH}	R_L* = 120 Ω	5	50	100	ns
		10	35	70	
		15	25	50	
Average Input Capacitance, C_{IN}	Any Input		5	7.5	pF
Average Output Capacitance, C_{OUT}	Any Output		30	–	pF

* R_L is external pull-up resistor to V_{DD}.

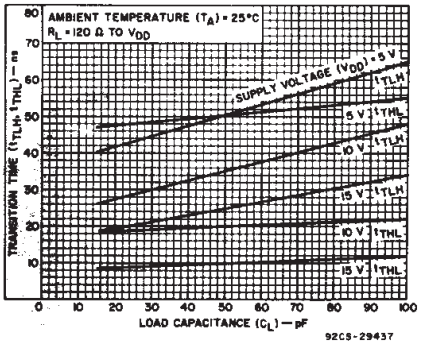


Fig.4 – Typical transition time as a function of load capacitance.

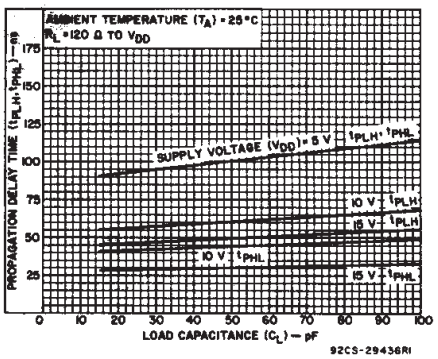


Fig.5 – Typical propagation delay time as a function of load capacitance.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS V_O (V)	V_{IN} (V)	V_{DD} (V)	LIMITS AT INDICATED TEMPERATURES (°C) –55	–40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	UNITS
Quiescent Device Current I_{DD} Max.	–	0,5	5	1	1	30	30	–	0.02	1	μA
	–	0,10	10	2	2	60	60	–	0.02	2	
	–	0,15	15	4	4	120	120	–	0.02	4	
	–	0,20	20	20	20	600	600	–	0.04	20	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	21	20	14	12	16	32	–	mA
	1	0,5	5	44	42	30	25	34	68	–	
	0.5	0,10	10	49	46	32	28	37	74	–	
	1	0,10	10	89	85	60	51	68	136	–	
	0.5	0,15	15	66	63	44	38	50	100	–	
Output High (Source) Current I_{OH} Min.	No Internal Pull-Up Device										
Input Low Voltage V_{IL} Max.*	4.5	–	5	1.5				–	–	1.5	V
	9	–	10	3				–	–	3	
	13.5	–	15	4				–	–	4	
Input High Voltage V_{IH} Min.*	0.5,4.5	–	5	3.5				3.5	–	–	
	1,9	–	10	7				7	–	–	
	1.5,13.5	–	15	11				11	–	–	
Input Current I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$±10^{-5}$	±0.1	μA
Output Leakage Current I_{OZ} Max.	18	0,18	18	2	2	20	20	–	10^{-4}	2	μA

* Measured with external pull-up resistor, R_L = 10 kΩ to V_{DD}.

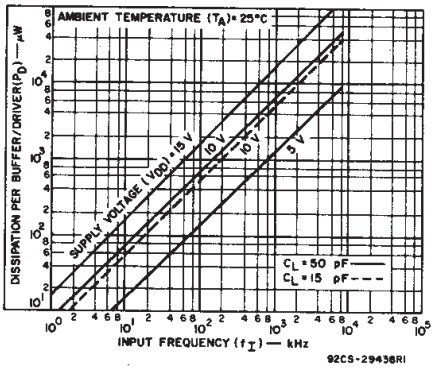


Fig.6 – Typical power dissipation as a function of input frequency.

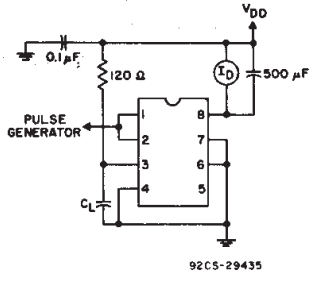
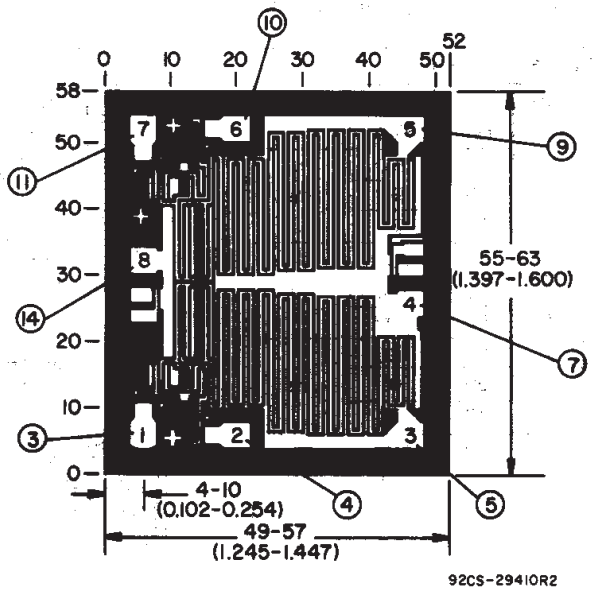


Fig. 7 – Power-dissipation test circuit for CD40107BE.



NOTE: NOS. IN PADS FOR CD40107BE
NOS. OUTSIDE CHIP FOR CD40107BF

Dimensions and Pad Layout for CD40107BH.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

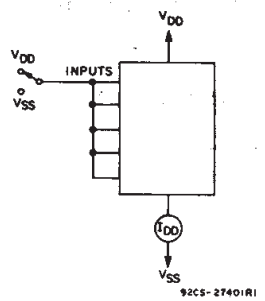


Fig.8 – Quiescent-device current test circuit.

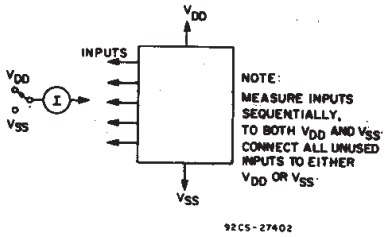


Fig. 9 – Input-current test circuit.

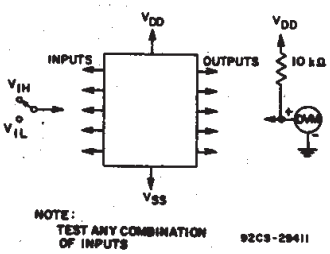
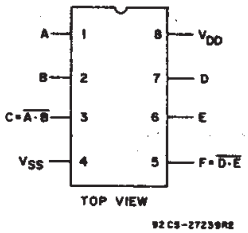
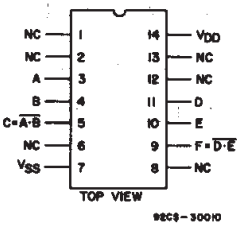


Fig.10 – Input-voltage test circuit.



CD40107BE



CD40107BF

TERMINAL ASSIGNMENTS

Special Considerations for CD40107B

1. **Limiting Capacitive Currents for CL > 500 pF, V_{DD} > 15 V.**
   For V_{DD} > 15 V, and load capacitance (C_L) from output to ground > 500 pF, an external 25 Ω series limiting resistor should be inserted between the output terminal and C_L. No external resistor is necessary if C_L < 500 pF or V_{DD} < 15 V.
2. **Driving Inductive Loads**
   When using the CD40107B to drive inductive loads, the load should be shunted with a diode to prevent high voltages from developing across the CD40107B output.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CD40107BE	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD40107BE
CD40107BE.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD40107BE
CD40107BF	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD40107BF
CD40107BF.A	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD40107BF
CD40107BF3A	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD40107BF3A
CD40107BF3A.A	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD40107BF3A
CD40107BM	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM0107
CD40107BM.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM0107
CD40107BM96	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM0107
CD40107BM96.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM0107
CD40107BPSR	Active	Production	SO (PS) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM0107B
CD40107BPSR.A	Active	Production	SO (PS) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM0107B
CD40107BPW	Obsolete	Production	TSSOP (PW) | 8	-	-	Call TI	Call TI	-55 to 125	CM0107B
CD40107BPWR	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM0107B
CD40107BPWR.A	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM0107B

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF CD40107B, CD40107B-MIL :

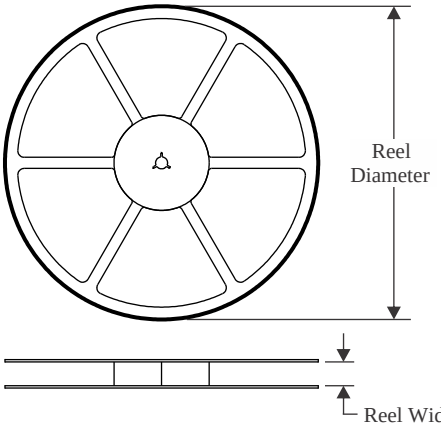
- Catalog : CD40107B
- Military : CD40107B-MIL

NOTE: Qualified Version Definitions:

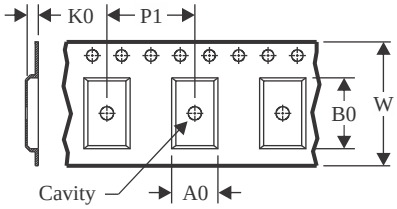
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

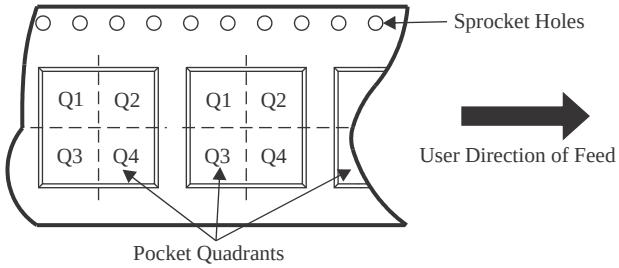


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

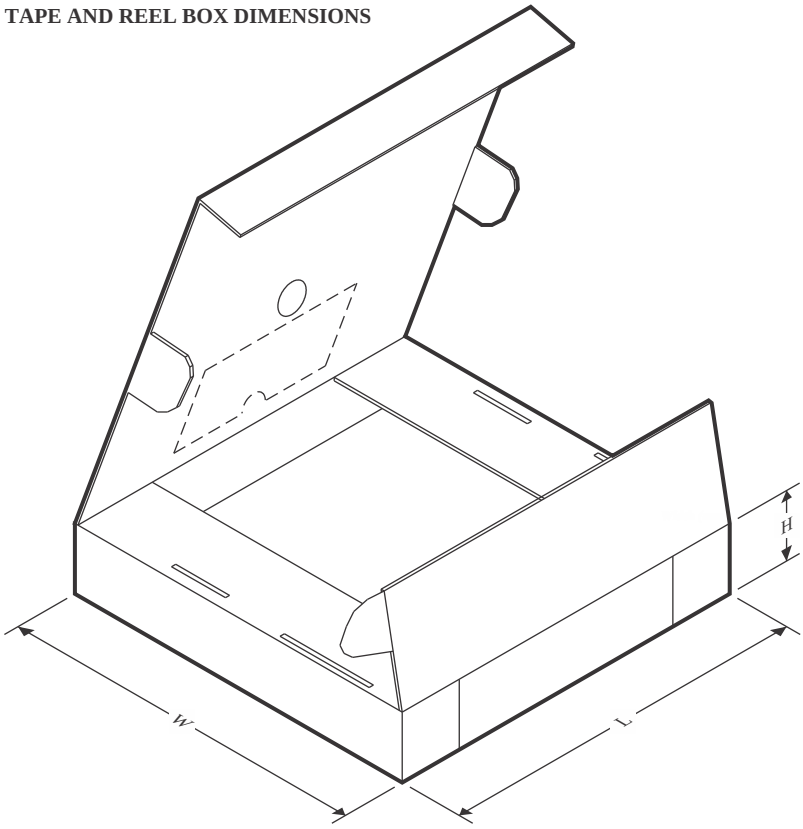
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD40107BM96	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
CD40107BPSR	SO	PS	8	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
CD40107BPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

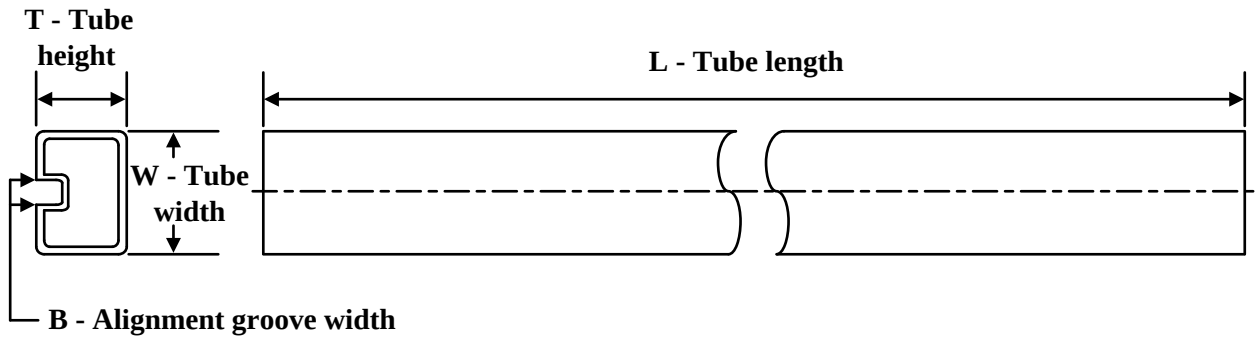
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD40107BM96	SOIC	D	8	2500	353.0	353.0	32.0
CD40107BPSR	SO	PS	8	2000	356.0	356.0	35.0
CD40107BPWR	TSSOP	PW	8	2000	356.0	356.0	35.0

TUBE



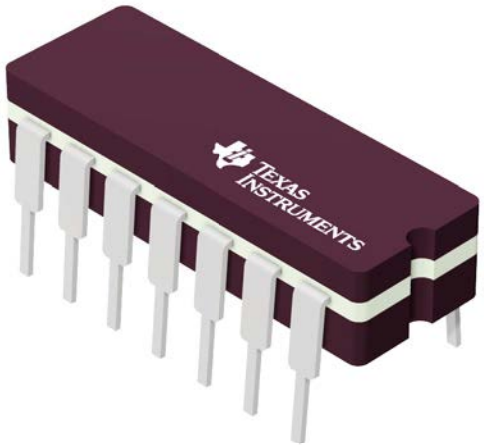
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
CD40107BE	P	PDIP	8	50	506	13.97	11230	4.32
CD40107BE.A	P	PDIP	8	50	506	13.97	11230	4.32
CD40107BM	D	SOIC	8	75	507	8	3940	4.32
CD40107BM	D	SOIC	8	75	506.6	8	3940	4.32
CD40107BM.A	D	SOIC	8	75	507	8	3940	4.32
CD40107BM.A	D	SOIC	8	75	506.6	8	3940	4.32

GENERIC PACKAGE VIEW

J 14 CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

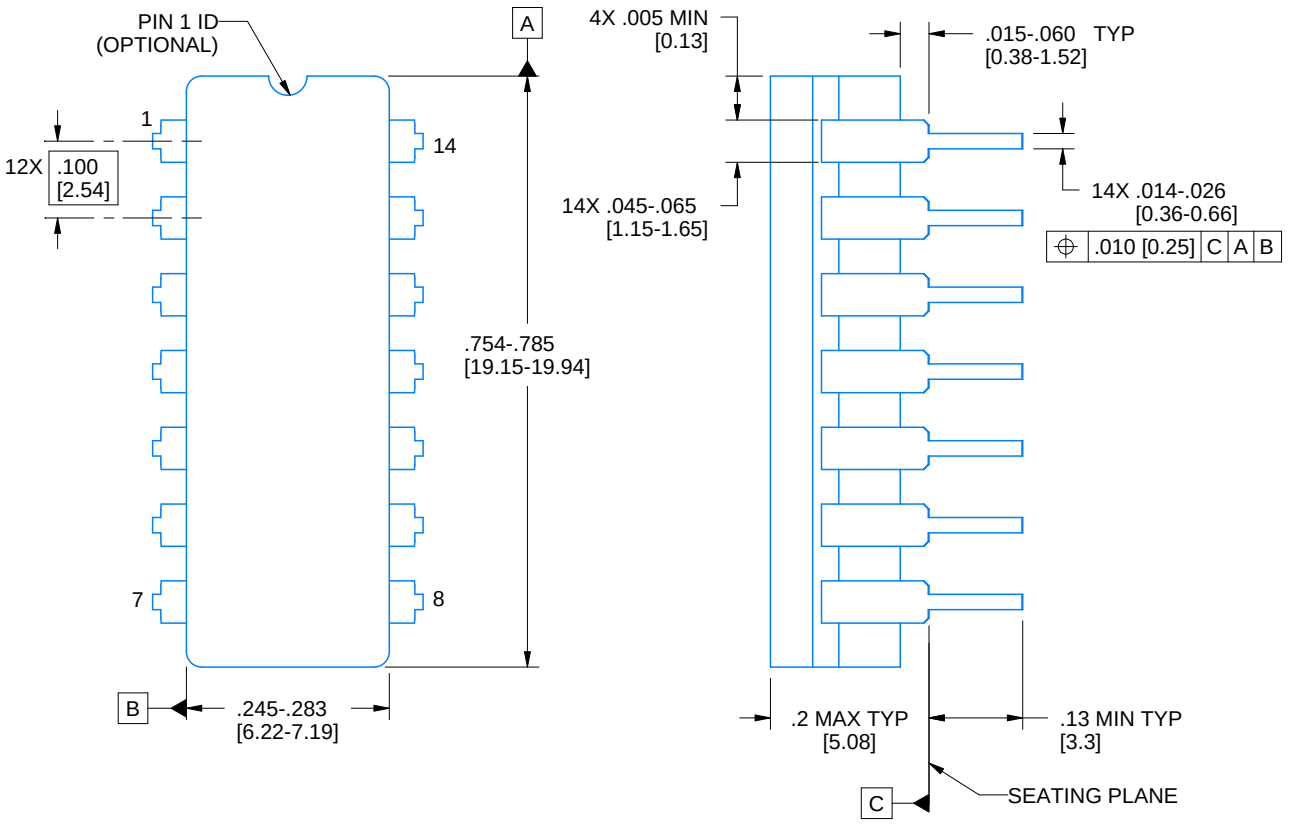
4040083-5/G

PACKAGE OUTLINE

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

NOTES:

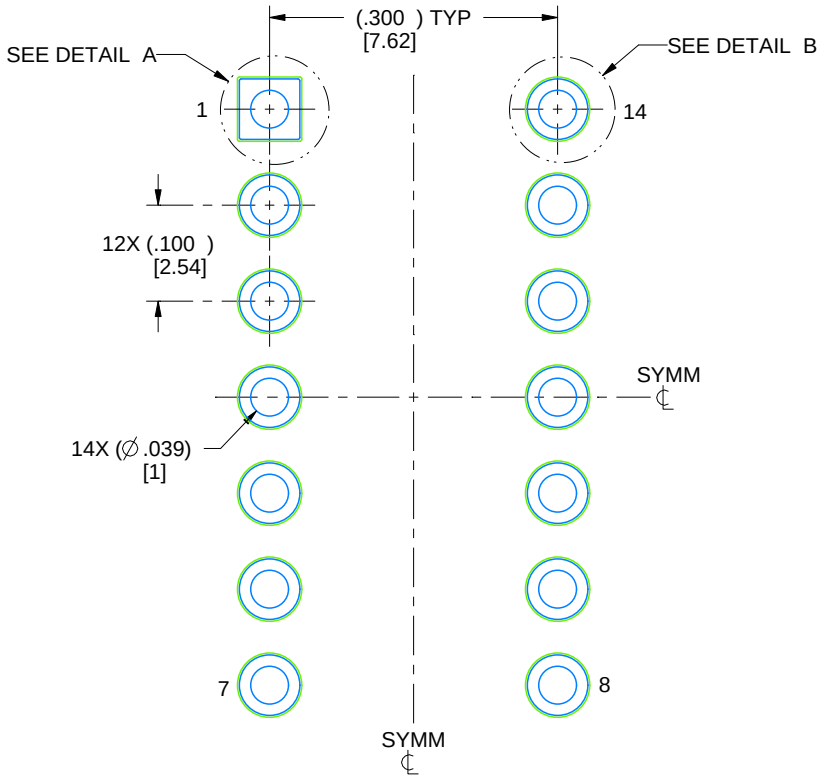
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermitically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

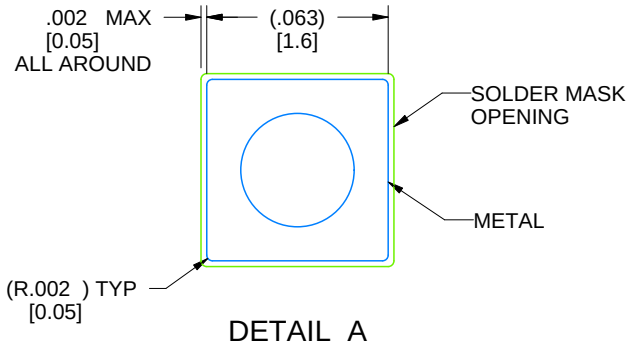
J0014A

CDIP - 5.08 mm max height

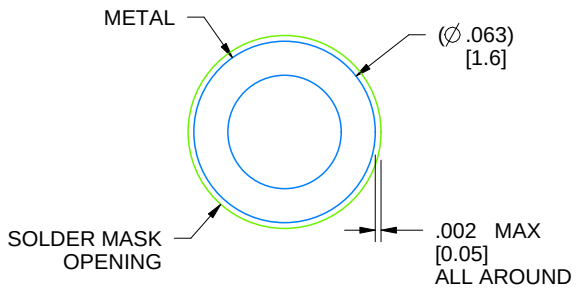
CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



DETAIL A
SCALE: 15X



DETAIL B
13X, SCALE: 15X

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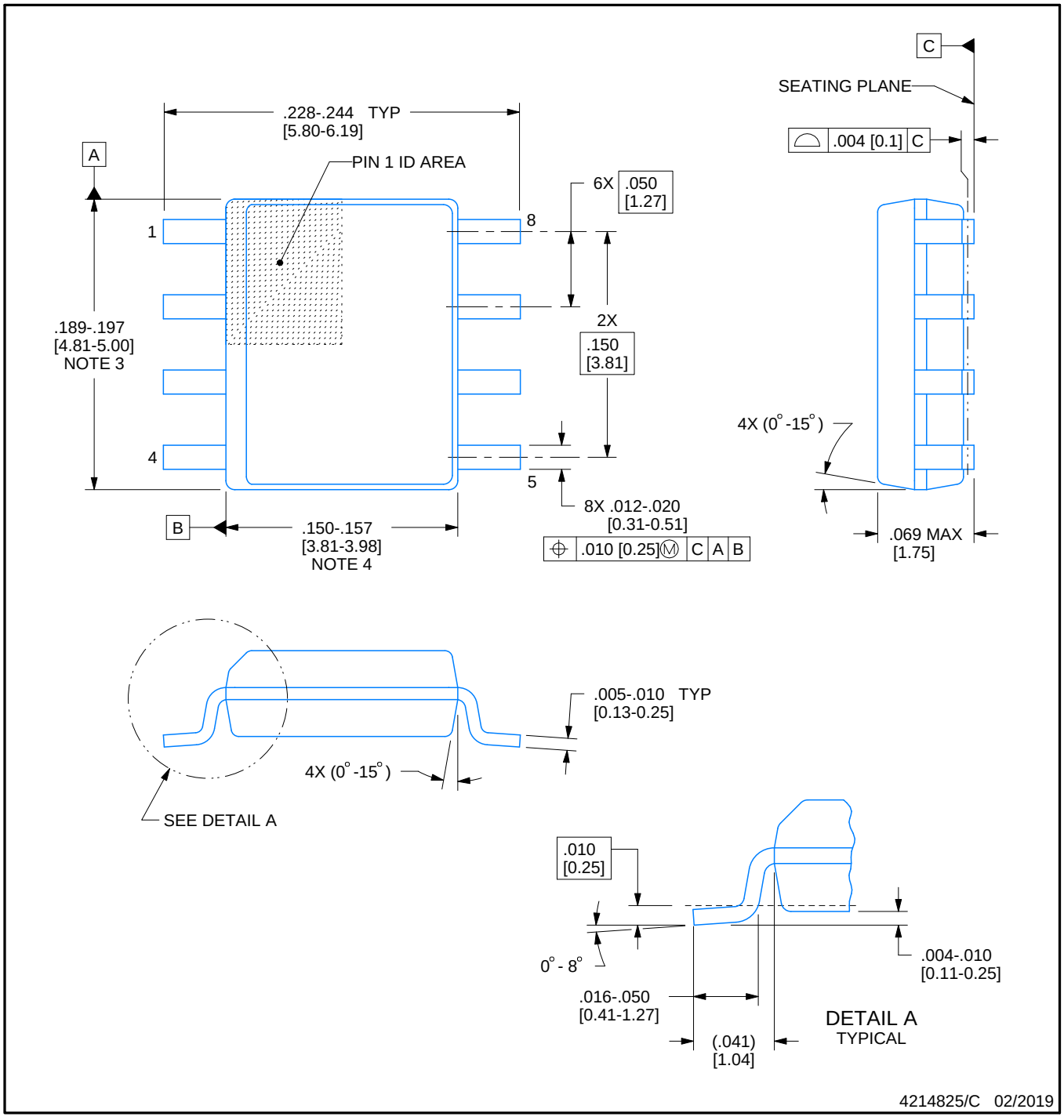
PACKAGE OUTLINE

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

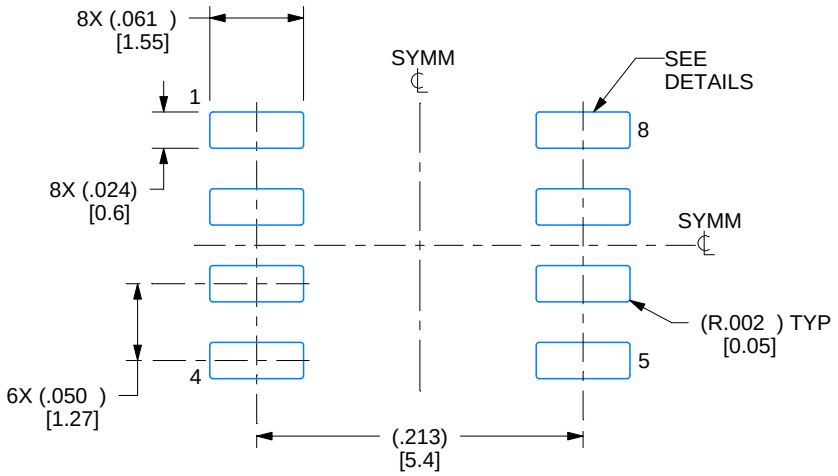
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

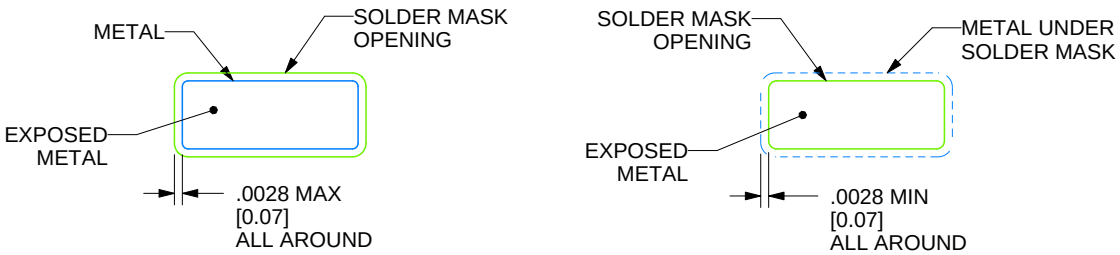
D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

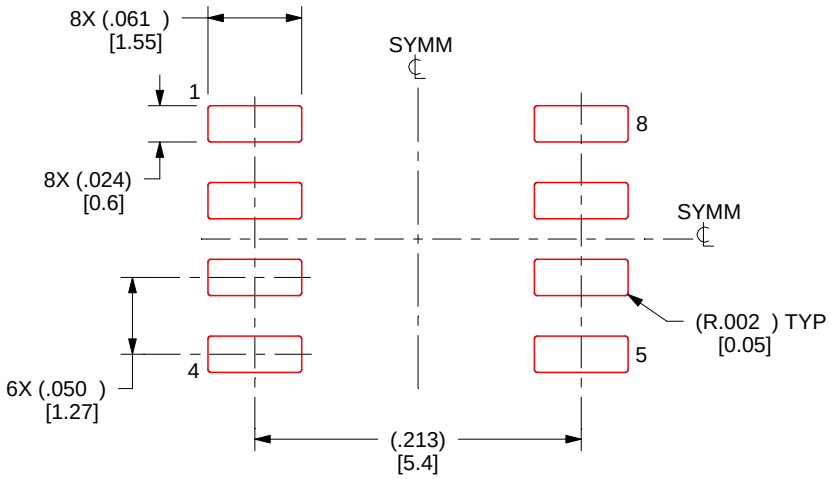
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

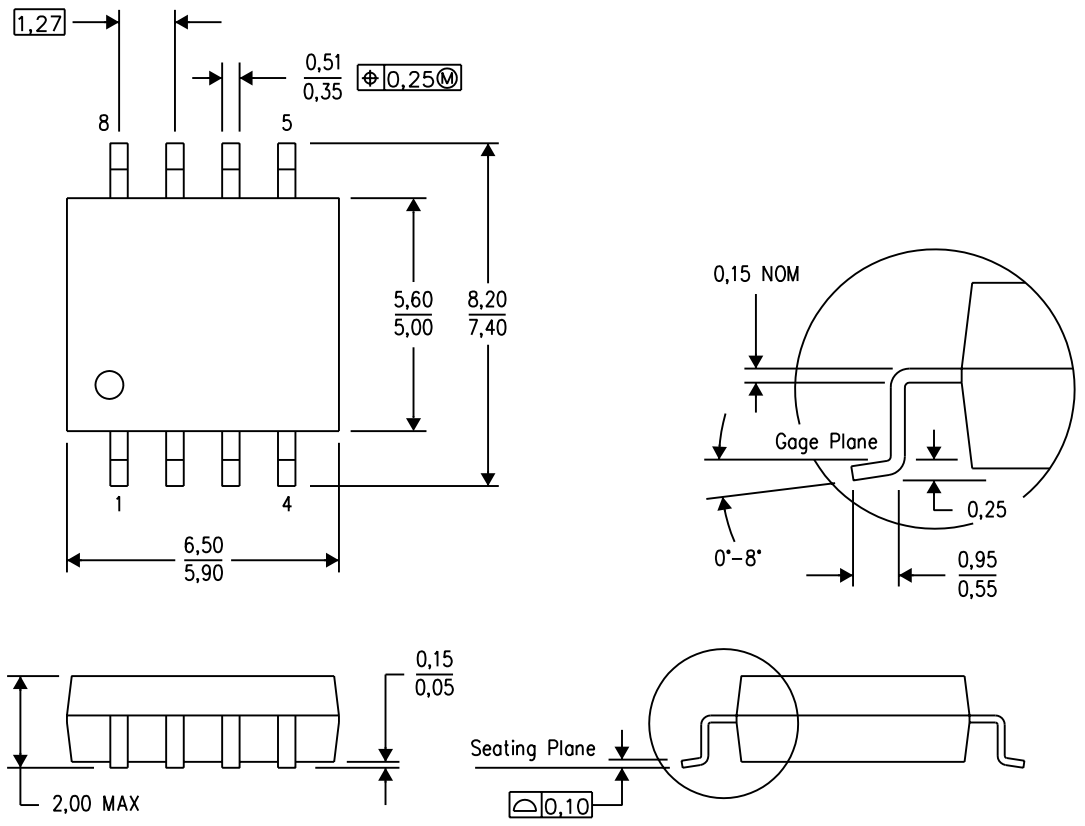
4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

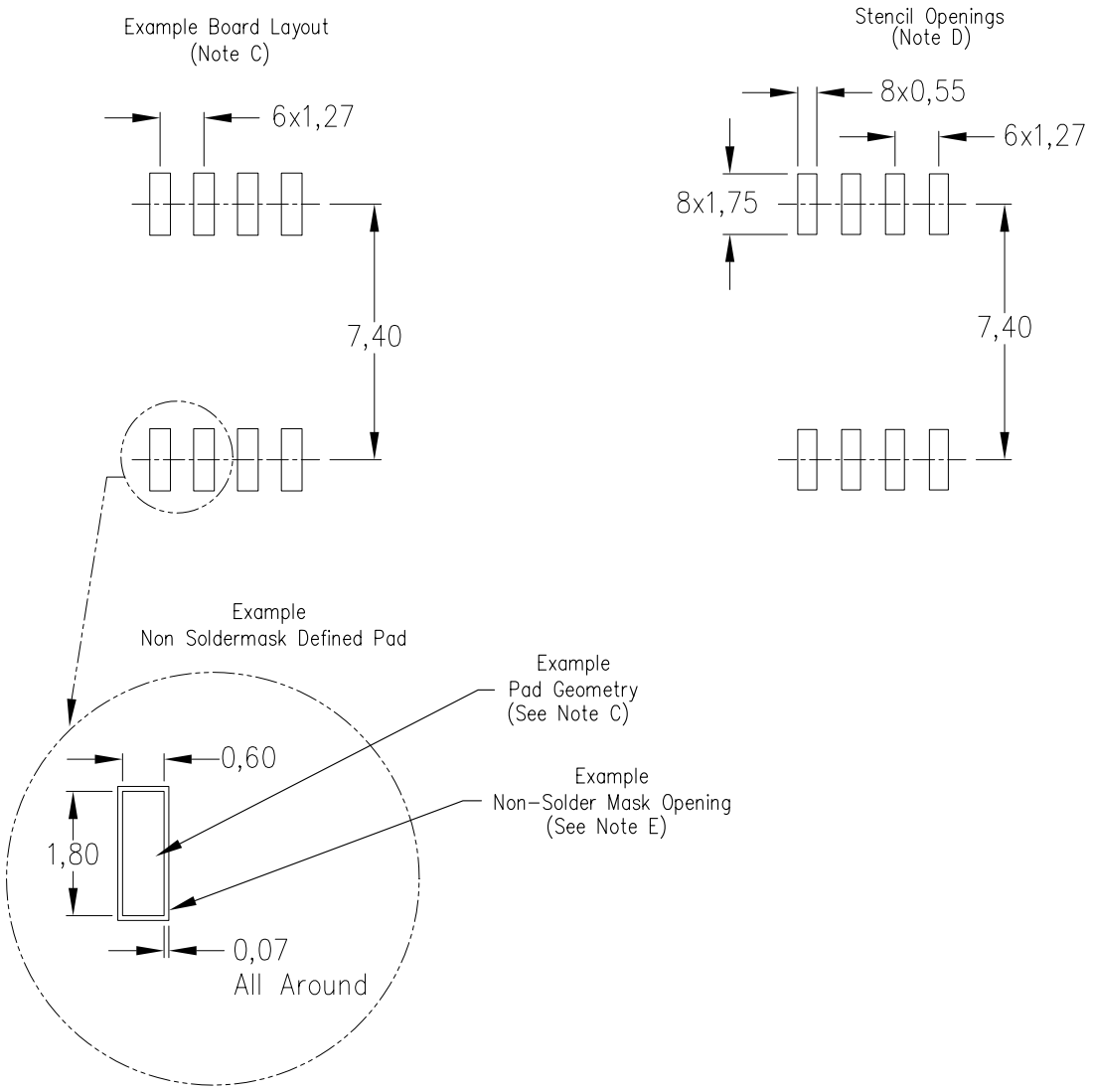
PS (R-PDSO-G8) **PLASTIC SMALL-OUTLINE PACKAGE**



4040063/C 03/03

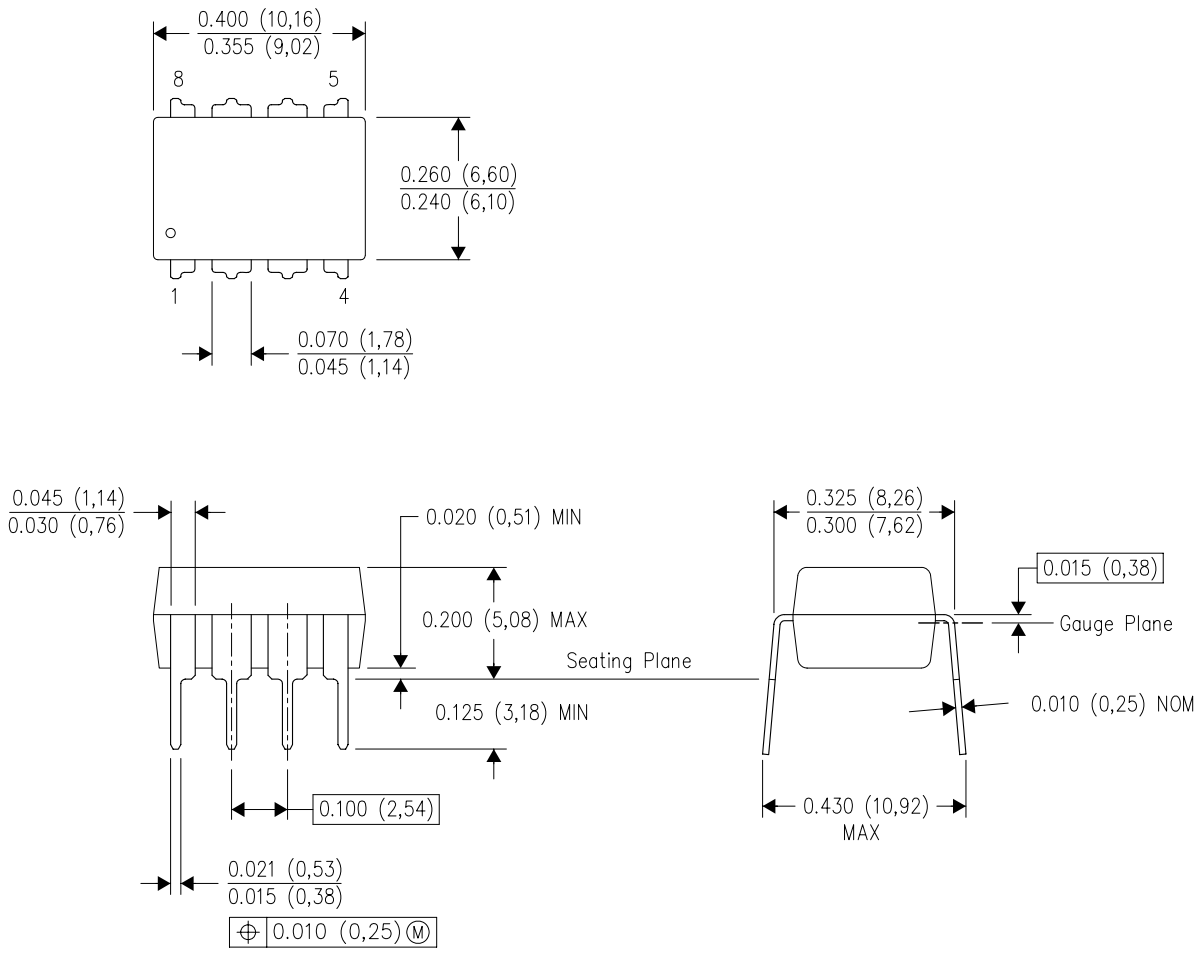
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PS (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



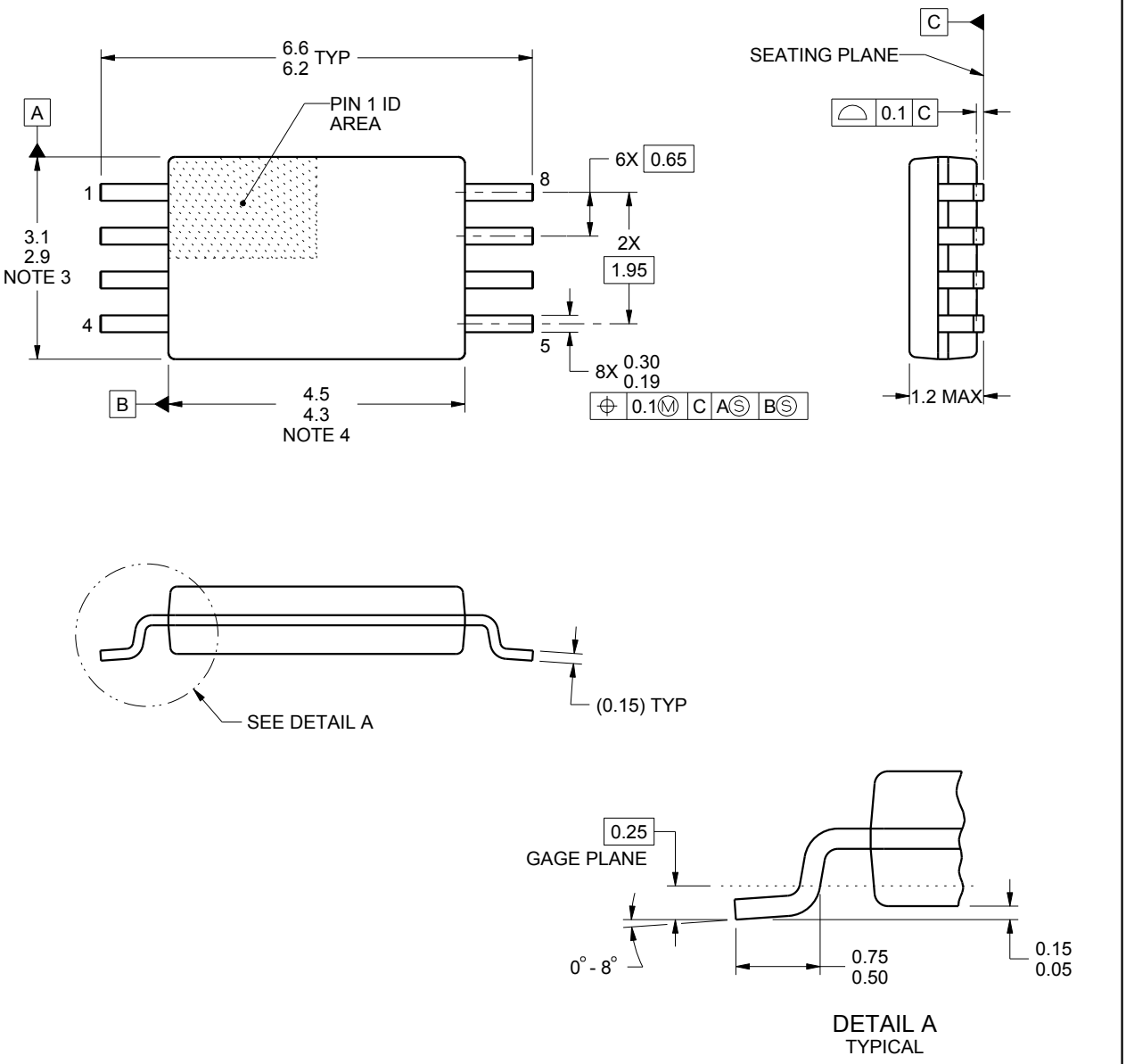
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

PACKAGE OUTLINE

PW0008A

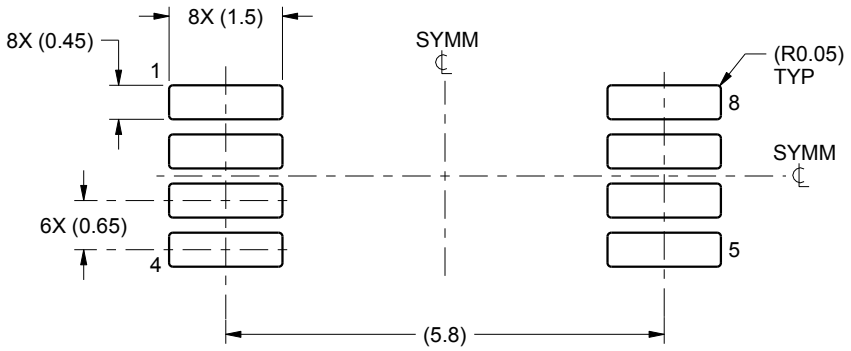
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

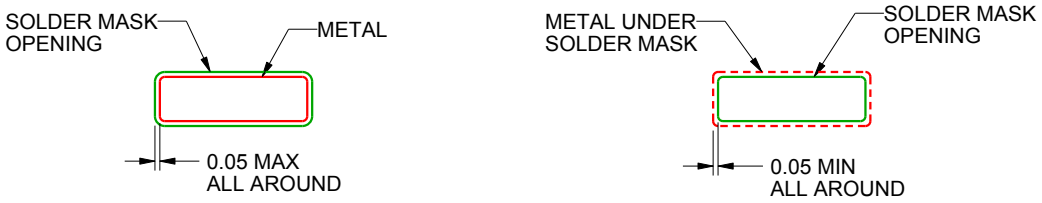


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

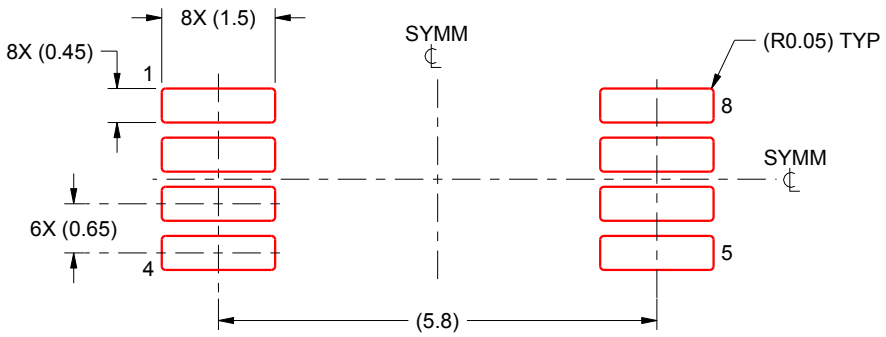
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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