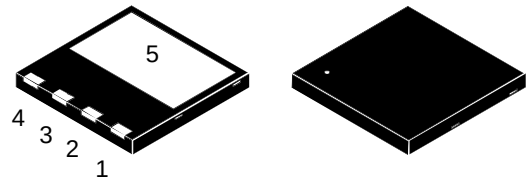
STL47N60M6

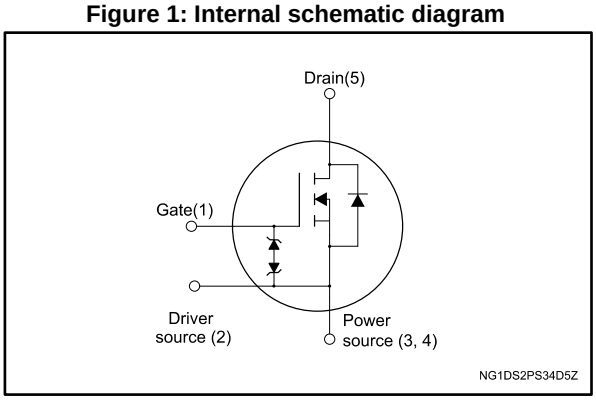
N-channel 600 V, 0.065 Ω typ., 31 A MDmesh™ M6 Power MOSFET in a PowerFLAT™ 8x8 HV package

Datasheet - target specification



PowerFLAT™ 8x8 HV

Figure 1: Internal schematic diagram



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STL47N60M6	600 V	0.080 Ω	31 A

- Reduced switching losses
- Lower $R_{DS(on)}$ x area vs previous generation
- Low gate input resistance
- 100% avalanche tested
- Zener-protected
- Excellent switching performance thanks to the extra driving source pin

Applications

- Switching applications

Description

The new MDmesh™ M6 technology incorporates the most recent advancements to the well-known and consolidated MDmesh family of SJ MOSFETs. STMicroelectronics builds on the previous generation of MDmesh devices through its new M6 technology, which combines excellent $R_{DS(on)}$ * area improvement with one of the most effective switching behaviors available, as well as a user-friendly experience for maximum end-application efficiency.

Table 1: Device summary

Order code	Marking	Package	Packing
STL47N60M6	47N60M6	PowerFLAT™ 8x8 HV	Tape and reel

Contents

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	±25	V
I_D(1)	Drain current (continuous) at T_C = 25 °C	31	A
I_D(1)	Drain current (continuous) at T_C= 100 °C	20	A
I_{DM}(2)	Drain current (pulsed)	TBD	A
P_{TOT}	Total dissipation at T_C = 25 °C	189	W
dv/dt(3)	Peak diode recovery voltage slope	15	V/ns
dv/dt(4)	MOSFET dv/dt ruggedness	50	V/ns
T_{stg}	Storage temperature range	-55 to 150	°C
T_j	Operating junction temperature range		

Notes:

(1)This value is limited by package.

(2)Pulse width is limited by safe operating area.

(3)I_{SD} ≤ 31 A, di/dt ≤ 400 A/µs, $V_{DS\ peak}$ < $V_{(BR)DSS}$, V_{DD} = 400 V

(4)V_{DS} ≤ 480 V

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case	0.66	°C/W
$R_{thj\text{-}pcb}$(1)	Thermal resistance junction-pcb	45	°C/W

Notes:

(1)When mounted on 1 inch^2 FR-4, 2 Oz copper board

Table 4: Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by T_{jmax})	TBD	A
E_{AS}	Single pulse avalanche energy (starting T_j = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	TBD	mJ

2 Electrical characteristics

(T_C= 25 °C unless otherwise specified)

Table 5: On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	600			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 600 V			1	µA
		V_{GS} = 0 V, V_{DS} = 600 V, T_C = 125 °C(1)			100	µA
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = ±25 V			±5	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	3.25	4	4.75	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 15.5 A		0.065	0.080	Ω

Notes:

(1)Defined by design, not subject to production test.

Table 6: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS}= 100 V, f = 1 MHz, V_{GS} = 0 V	-	TBD	-	pF
C_{oss}	Output capacitance		-	TBD	-	pF
C_{rss}	Reverse transfer capacitance		-	TBD	-	pF
$C_{oss\ eq.}$(1)	Equivalent output capacitance	V_{DS} = 0 to 480 V, V_{GS} = 0 V	-	TBD	-	pF
R_G	Intrinsic gate resistance	f = 1 MHz, I_D=0 A	-	1.5	-	Ω
Q_g	Total gate charge	V_{DD} = 480 V, I_D = 40 A, V_{GS} = 0 to 10 V (see *Figure 3: "Gate charge test circuit"*)	-	57	-	nC
Q_{gs}	Gate-source charge		-	TBD	-	nC
Q_{gd}	Gate-drain charge		-	TBD	-	nC

Notes:

(1)$C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.

Table 7: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 300 V, I_D = 20 A, R_G = 4.7 Ω, V_{GS} = 10 V (see *Figure 2: "Switching times test circuit for resistive load"* and *Figure 7: "Switching time waveform"*)	-	TBD	-	ns
t_r	Rise time		-	TBD	-	ns
$t_{d(off)}$	Turn-off-delay time		-	TBD	-	ns
t_f	Fall time		-	TBD	-	ns

Table 8: Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} (1)	Source-drain current		-		31	A
I_{SDM} (1),(2)	Source-drain current (pulsed)		-		TBD	A
V_{SD} (3)	Forward on voltage	V_{GS} = 0 V, I_{SD} = 31 A	-		1.6	V
t_{rr}	Reverse recovery time	I_{SD} = 40 A, di/dt = 100 A/µs, V_{DD} = 100 V (see *Figure 4: " Test circuit for inductive load switching and diode recovery times"*)	-	TBD		ns
Q_{rr}	Reverse recovery charge		-	TBD		µC
I_{RRM}	Reverse recovery current		-	TBD		A
t_{rr}	Reverse recovery time	I_{SD} = 40 A, di/dt = 100 A/µs, V_{DD} = 100 V, T_j = 150 °C (see *Figure 4: " Test circuit for inductive load switching and diode recovery times"*)	-	TBD		ns
Q_{rr}	Reverse recovery charge		-	TBD		µC
I_{RRM}	Reverse recovery current		-	TBD		A

Notes:

(1)This value is limited by package.

(2)Pulse width is limited by safe operating area.

(3)Pulsed: pulse duration = 300 µs, duty cycle 1.5%.

3 Test circuits

Figure 2: Switching times test circuit for resistive load

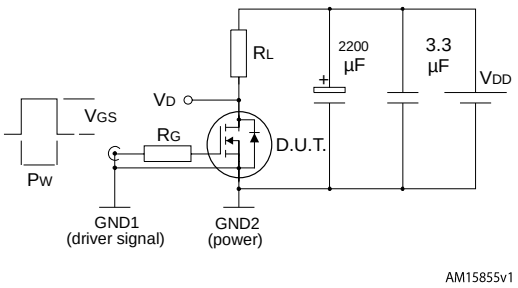


Figure 3: Gate charge test circuit

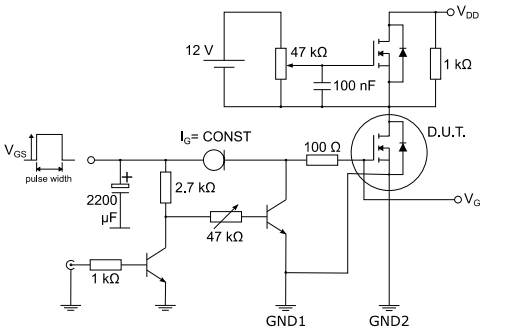


Figure 4: Test circuit for inductive load switching and diode recovery times

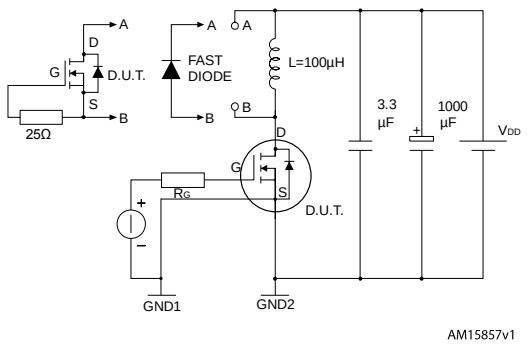


Figure 5: Unclamped inductive load test circuit

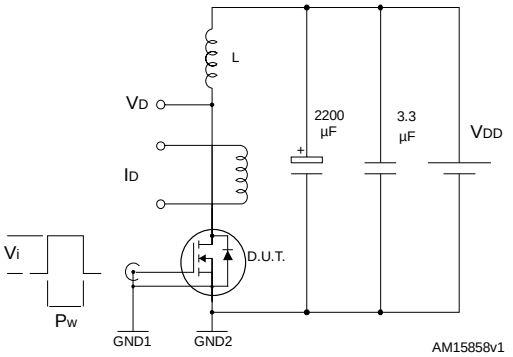


Figure 6: Unclamped inductive waveform

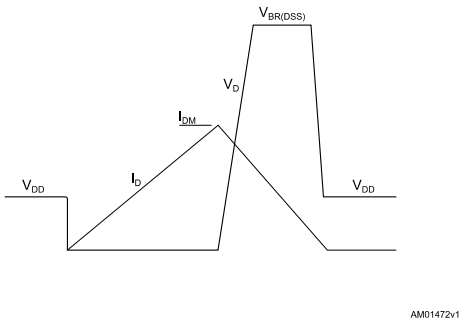
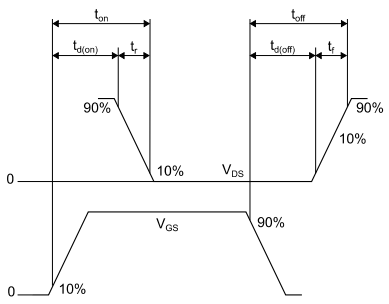


Figure 7: Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

4.1 PowerFLAT™ 8x8 HV package information

Figure 8: PowerFLAT™ 8x8 HV package outline

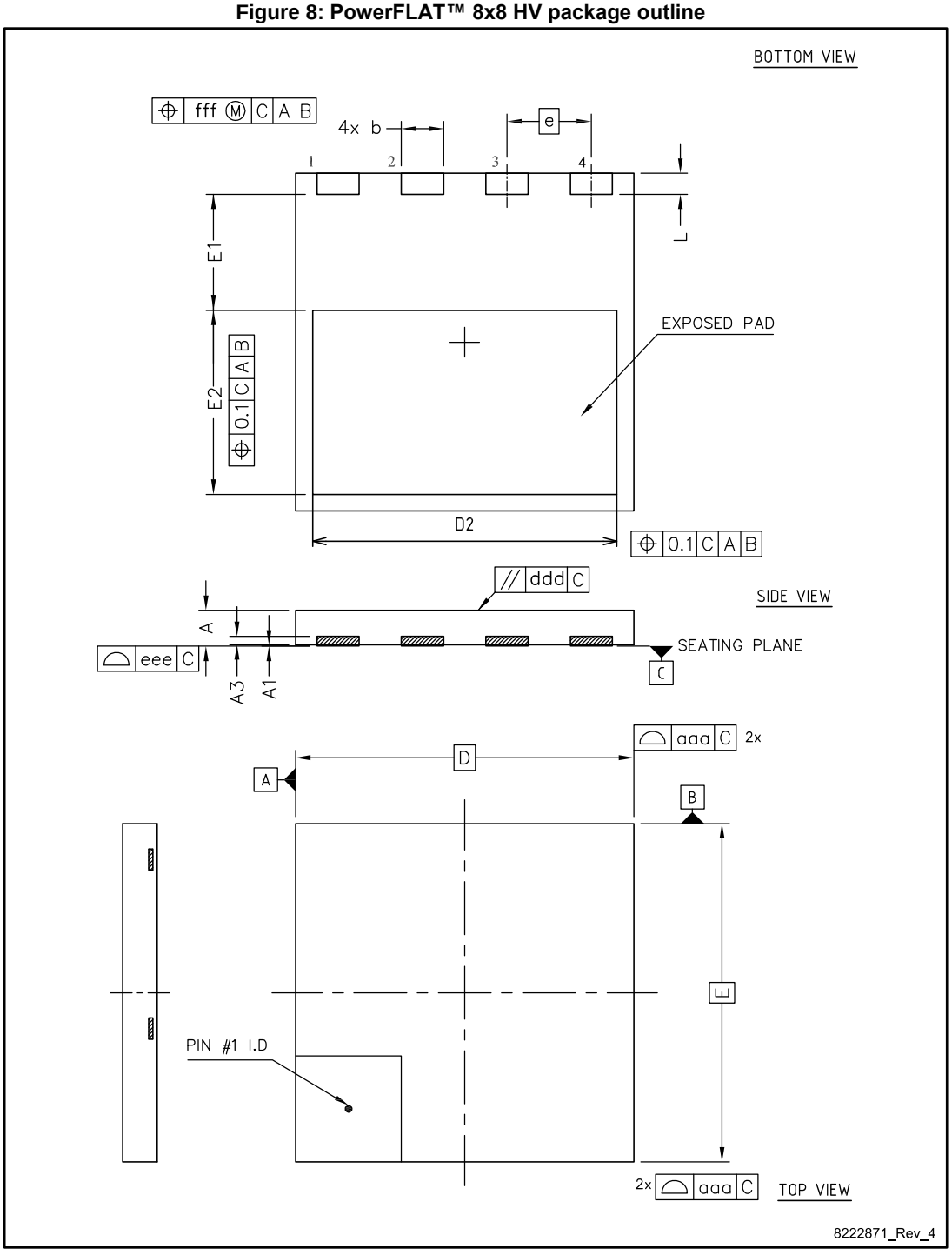
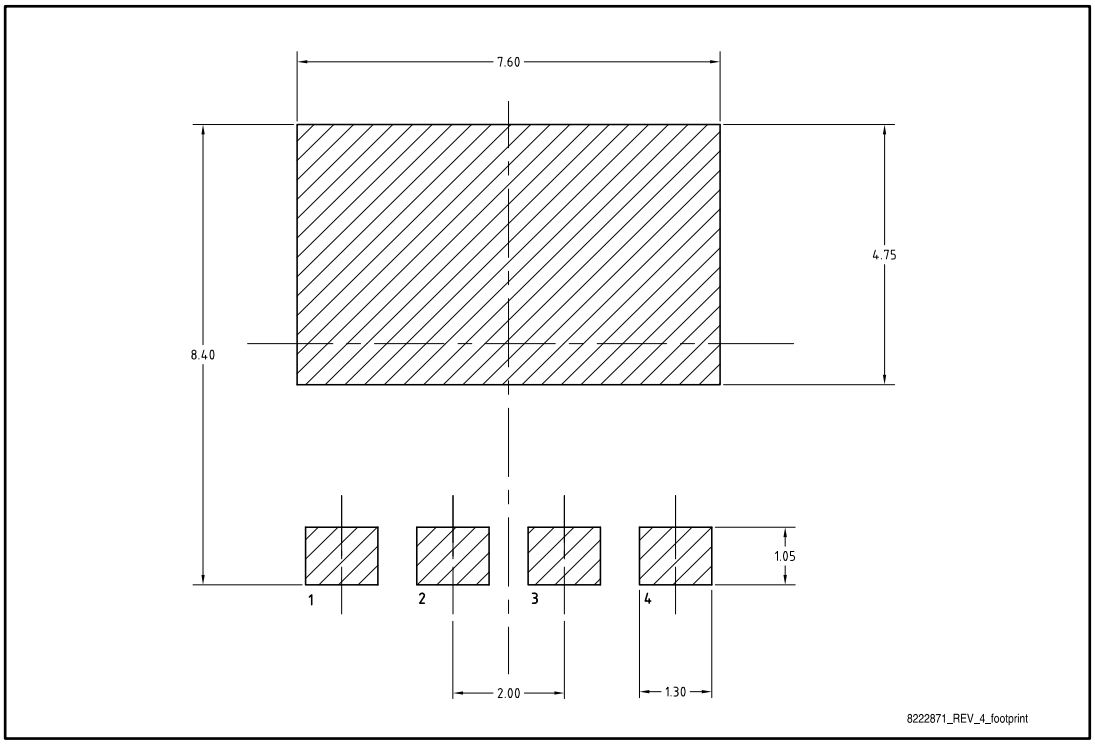


Table 9: PowerFLAT™ 8x8 HV mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.75	0.85	0.95
A1	0.00		0.05
A3	0.10	0.20	0.30
b	0.90	1.00	1.10
D	7.90	8.00	8.10
E	7.90	8.00	8.10
D2	7.10	7.20	7.30
E1	2.65	2.75	2.85
E2	4.25	4.35	4.45
e		2.00	
L	0.40	0.50	0.60
aaa		0.10	
ddd		0.05	
eee		0.05	
fff		0.05	

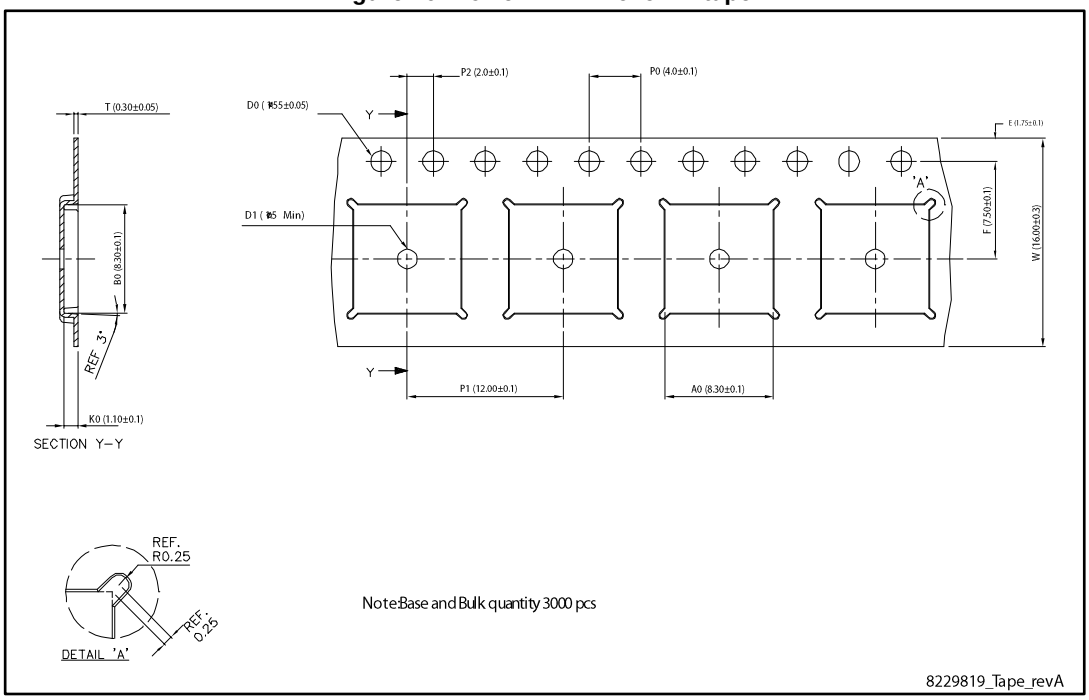
Figure 9: PowerFLAT™ 8x8 HV footprint



All dimensions are in millimeters.

4.2 PowerFLAT™ 8x8 HV packing information

Figure 10: PowerFLAT™ 8x8 HV tape



All dimensions are in millimeters.

Figure 11: PowerFLAT™ 8x8 HV package orientation in carrier tape

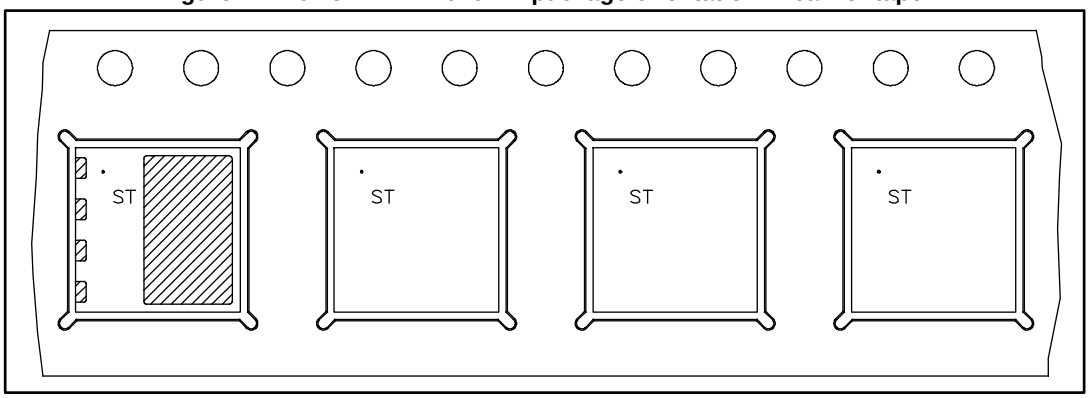
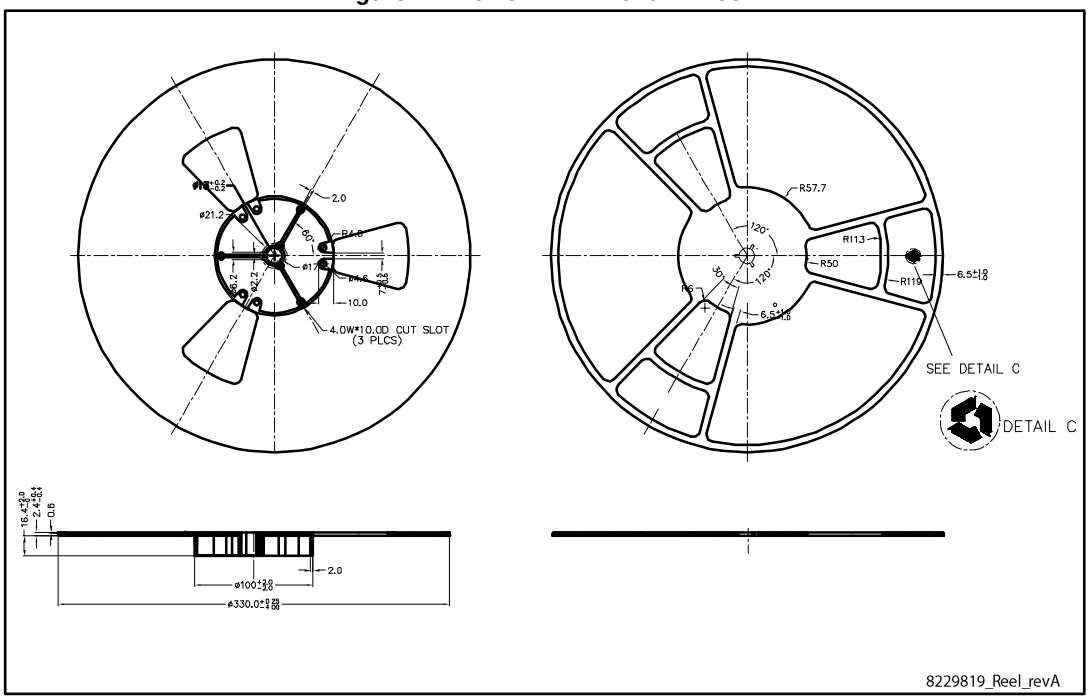


Figure 12: PowerFLAT™ 8x8 HV reel



All dimensions are in millimeters.

5 Revision history

Table 10: Document revision history

Date	Revision	Changes
15-Nov-2017	1	First release

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