



SY88024L

11.3Gbps VCSEL DRIVER

General Description

The SY88024L is a single 3.3V supply, small form factor VCSEL driver for datacom applications at data rates up to 11.3Gbps. The driver can deliver modulation current up to 20mA and a bias current up to 20mA.

All support documentation can be found on Micrel's web site at: www.micrel.com.

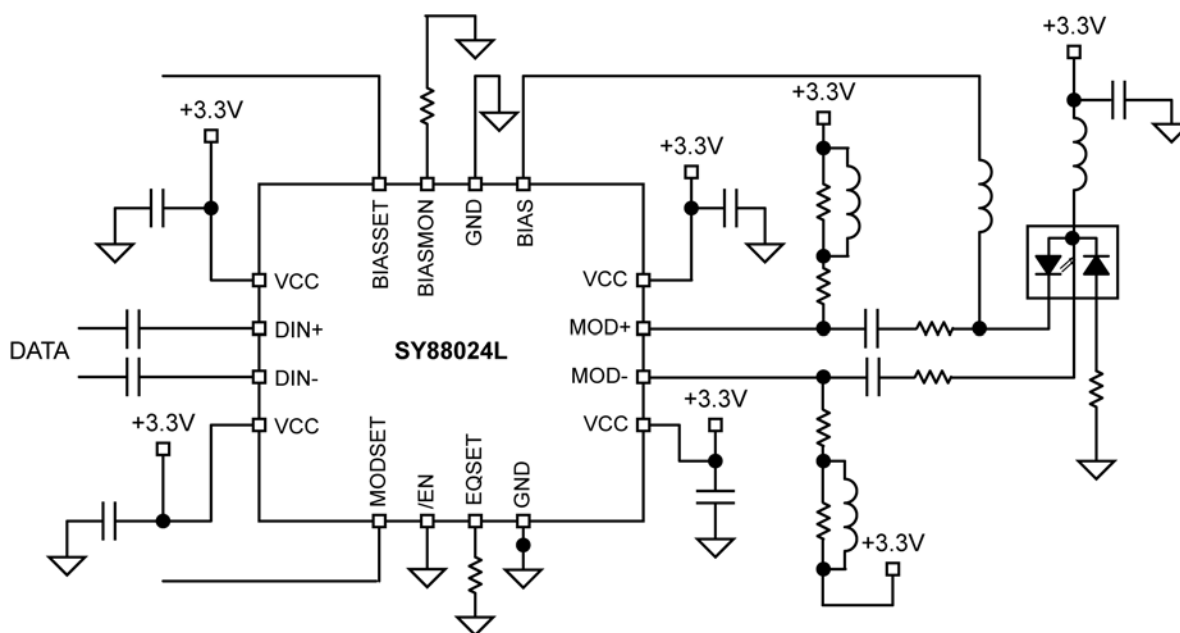
Features

- Operates from a single 3.3V supply
- Operation up to 11.3Gbps
- Modulation current up to 20mA
- Bias current up to 20mA
- Small form factor 3mm x 3mm QFN package

Applications

- Multi-rate LAN up to 11.3Gbps: 8xFC, 10G GbE.
- SFP+, XFP, XPAK, XENPAK, X2, MSA 300 optical modules

Typical Application



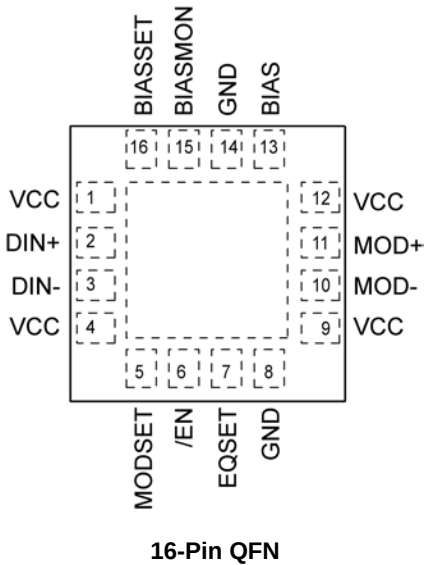
Ordering Information⁽¹⁾

Part Number	Voltage	Temperature Range	Package	Lead Finish
SY88024LMG	3.3V	−40° to +85°C	QFN-16	NiPdAu Pb-Free
SY88024LMGTR ⁽²⁾	3.3V	−40° to +85°C	QFN-16	NiPdAu Pb-Free

Notes:

- 1. Contact factory for die availability. Dice are guaranteed at T_A = +25°C, DC Electricals only.
- 2. Tape and Reel.

Pin Configuration



Pin Description

Pin Number	Pin Name	Pin Function
1, 4, 9, 12	VCC	Supply Voltage. Bypass with a 0.1μF//0.01μF low ESR capacitor as close to the VCC pins as possible.
8, 14	GND	Ground. Ground and exposed pad must be connected to the plane of the most negative potential.
2	DIN+	Non-inverting input data. Internally terminated with 50Ω to VCC.
3	DIN–	Inverting input data. Internally terminated with 50Ω to VCC.
5	MODSET	Modulation current setting and control. Apply a voltage within the range 0V to 1.2V to this pin to set the modulation current. Input impedance 25kΩ.
6	/EN	Active Low TTL. Internal 75kΩ pull down to GND. The driver is enabled when this pin is unconnected or /EN is asserted low and disabled when /EN asserted high.
7	EQSET	Install a resistor from this pin to GND to set the desired equalization level. 0Ω will provide maximum equalization and 2kΩ or higher will provide negligible equalization. Leave open if no equalization is needed.
10	MOD–	Inverted modulation current output. Provides modulation current when input data is negative.
11	MOD+	Non-inverted modulation current output. Provides modulation current when input data is positive.
13	BIAS	BIAS Current Output
15	BIASMON	Bias Current Monitor. Install an external resistor from this pin to GND to convert the output current to a voltage proportional to the bias current
16	BIASSET	Bias current setting and control. Apply a voltage within the range 0V to 1.2V to this pin to set the bias current. Input impedance 25kΩ.

Truth Table

DIN+	DIN-	/EN	MOD+ ⁽¹⁾	MOD-	Laser Output ⁽²⁾
L	H	L	H	L	L
H	L	L	L	H	H
X	X	H	H	H	L

Notes:

1. $I_{MOD} = 0$ when MOD+ = H.
2. Assuming that the laser cathode is tied to MOD+.

Absolute Maximum Ratings⁽¹⁾

Supply Voltage (V_{IN}) -0.5V to +4.0V
 CML Input Voltage (V_{IN}) $V_{CC}-1.2V$ to $V_{CC}+0.5V$
 TTL Control Input Voltage (V_{IN}) 0V to V_{CC}
 Lead Temperature (soldering, 20sec.) +260°C
 Storage Temperature (T_s) -65°C to +150°C

Operating Ratings⁽²⁾

Supply Voltage (V_{CC}) +3.0V to +3.6V
 Ambient Temperature (T_A) -40°C to +85°C
 Package Thermal Resistance⁽³⁾
 QFN
 (θ_{JA}) Still-air 60°C/W
 (ψ_{JB}) 33°C/W

DC Electrical Characteristics

$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ and $V_{CC} = +3.0V$ to $+3.6V$, unless otherwise noted. Typical values are $V_{CC} = +3.3V$, $T_A = 25^\circ\text{C}$, $I_{MOD} = 6mA$, $I_{BIAS} = 6mA$.

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{CC}	Power Supply Current	Modulation and bias currents excluded		50	65 ⁽⁴⁾	mA
V_{MOD_MIN}	Minimum Voltage Required at the Driver Output (headroom) for Proper Operation		1.2			V
V_{BIAS_MIN}	Minimum Voltage Required at the BIAS Output (headroom) for Proper Operation		1.2			V
R_{IN}	Input Resistance, Single Ended		45	50	55	Ω
V_{ID}	Differential Input Voltage Swing		100		1000	mV _{PP}
V_{IL}	/EN Input Low				0.8	V
V_{IH}	/EN Input High		2			V
I_{BIAS}	Bias Current		1		20	mA
I_{BIAS_OFF}	Bias OFF Current	Current at BIAS when the device is disabled			150	μA
R_{MODSET}	Input Resistance at MODSET Pin			25		k Ω
V_{MODSET}	Voltage Range at MODSET Pin	I_{MOD} range 2mA to 20mA			1.2	V
$R_{BIASSET}$	Input Resistance at BIASSET Pin			25		k Ω
$V_{BIASSET}$	Voltage Range at BIASSET Pin	I_{BIAS} range 1mA to 20mA			1.2	V

Notes:

- Exceeding the absolute maximum rating may damage the device.
- The device is not guaranteed to function outside its operating rating.
- Package Thermal Resistance assumes exposed pad is soldered (or equivalent) to the devices most negative potential on the PCB. θ_{JB} uses a 4-layer and θ_{JA} in still air unless otherwise stated.
- Maximum I_{CC} measured with $I_{MOD} = 20mA$ and $I_{BIAS} = 20mA$ and MOD+/MOD- tied to VCC.

AC Electrical Characteristics

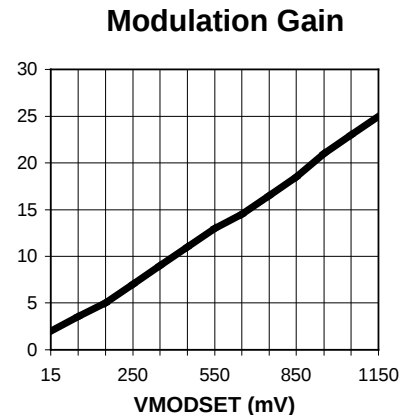
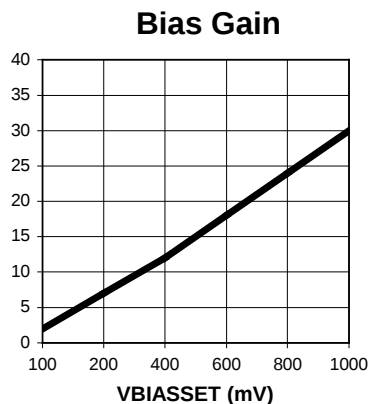
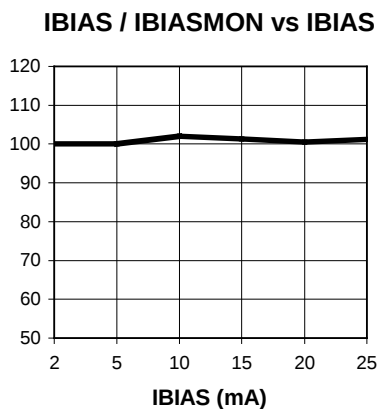
$T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ and $V_{CC} = +3.0\text{V}$ to $+3.6\text{V}$, unless otherwise noted. Typical values are $V_{CC} = +3.3\text{V}$, $T_A = 25^{\circ}\text{C}$, $I_{MOD} = 6\text{mA}$, $I_{BIAS} = 6\text{mA}$.

Symbol	Parameter	Condition	Min	Typ	Max	Units
	Data Rate	NRZ			11.3	Gbps
$I_{MOD}^{(5)}$	Modulation Current	AC-coupled	2		$20^{(6)}$	mA
I_{MOD_OFF}	Modulation OFF Current	Current at MOD+ and MOD- when the device is disabled			150	μA
t_r	Output Current Rise Time	20% to 80%, 25 Ω load		25	35	ps
t_f	Output Current Fall Time	20% to 80%, 25 Ω load		25	35	ps
DJ	Deterministic Jitter	K25.8 pattern at 11.3Gbps, $V_{IN} = 200\text{mV}_{PP}$		4		pS _{PP}
RJ	Random Jitter	K25.8 pattern at 11.3Gbps, $V_{IN} = 200\text{mV}_{PP}$		0.3		pS _{PP}

Notes:

5. I_{MOD} is defined as the current going into the external load, which is equal to the total current of the output device subtracted by the current going into the internal 50 Ω pull-up.
6. $I_{MOD(MAX)}$ is defined for a 50 Ω external load.

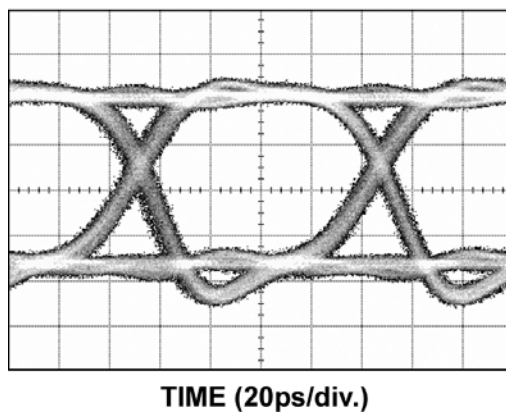
Typical Characteristics



Note:
 I_{MOD} is defined for a 50Ω external load.

Functional Characteristics

Electrical Eye Diagram
PRBS 2⁷-1 @10.3125Gbps,
 $R_L = 19\Omega$, $I_{MOD} = 10\text{mA}$



Input and Output Stages

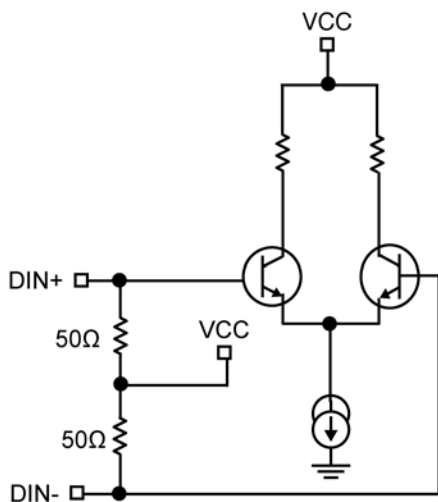


Figure 1a. Simplified Input Stage

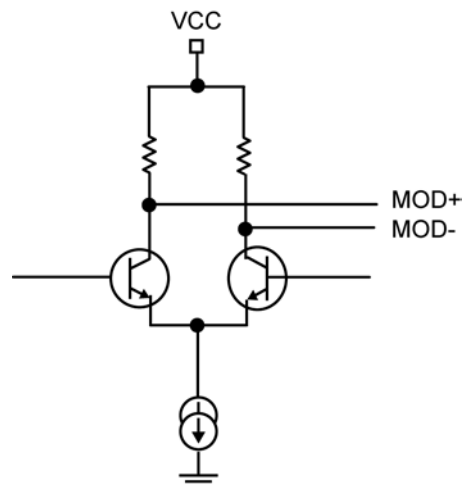


Figure 1b. Simplified Output Stage

Interfacing the Input to Differential Logic Drivers

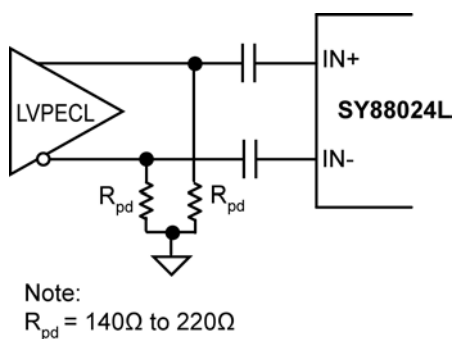


Figure 2a. AC-Coupling to LVPECL Driver

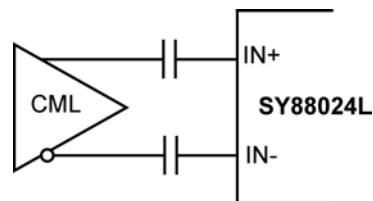
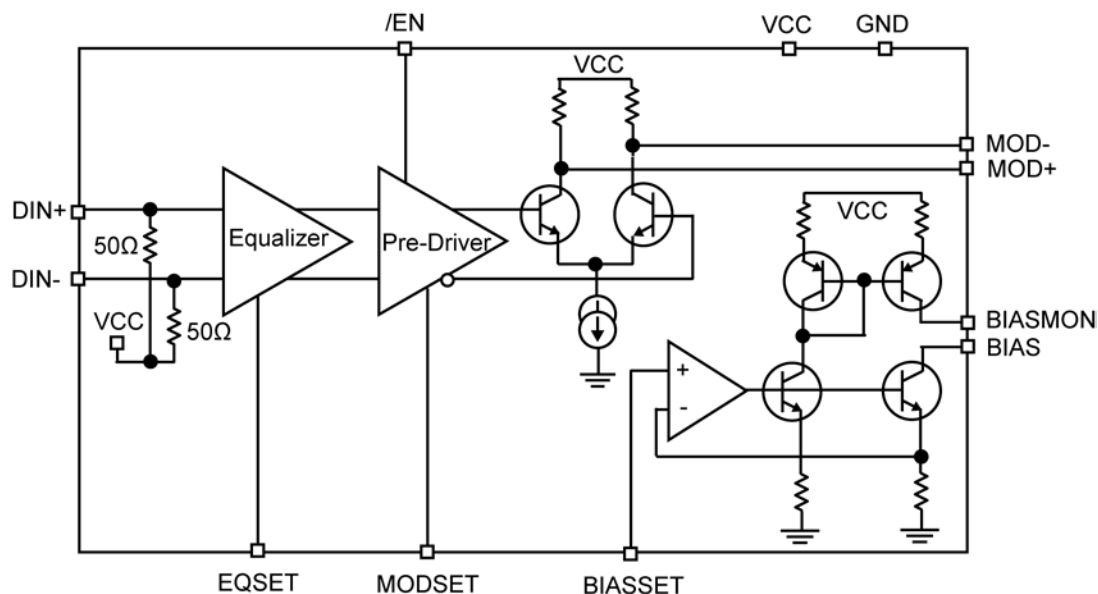


Figure 2b. AC-Coupling to CML Driver

Functional Diagram



Functional Description

As shown on the block diagram above, the driver is composed from an input equalizer, and a modulation block consisting of a pre-driver, and a current source.

Equalizer

The input equalizer allows for compensation of up to 9" of FR4 microstrip trace or equivalent. The equalization restores the losses in high frequency components of the signal caused by its travel on the line card traces and through the connectors between the line card and the module before it reaches the input stage. The amount of equalization is programmable with a resistor from pin 7 to ground.

Modulator

The modulator consists of a pre-driver and a current source. The modulation current is set in the pre-driver by applying a voltage within the range 0V to 1.2V to pin 5 (MODSET). The pre-driver provides the current to the output stage, which consists of a current source

composed from a differential pair which collectors are connected to MOD+/MOD- pins and have 50Ω internal termination to VCC. The Modulation gain curve on page 6 shows modulation current variation versus the applied voltage at MODSET pin.

Bias

The bias is set by applying a voltage within the range 0V to 1.2V to pin 16 (BIASSET). The bias gain curve on page 6 shows bias current variation versus the applied voltage at pin 16.

The SY88024L driver is designed to work with one of the Micrel's MIC300X series of controllers which have built in APC (Automatic Power Control) circuit and a serial interface for programming modulation and bias, temperature compensation tables, setting registers, and monitoring registers read back. Refer to the MIC3001/MIC3002/MIC3003 datasheets for more details. The applications section below shows how to set up the driver to work correctly with the MIC300X controller.

Application Information

management IC MIC300X.

Figure 3, below, illustrates a typical optical transceiver using the SY88024L and one of the Micrel's FOM

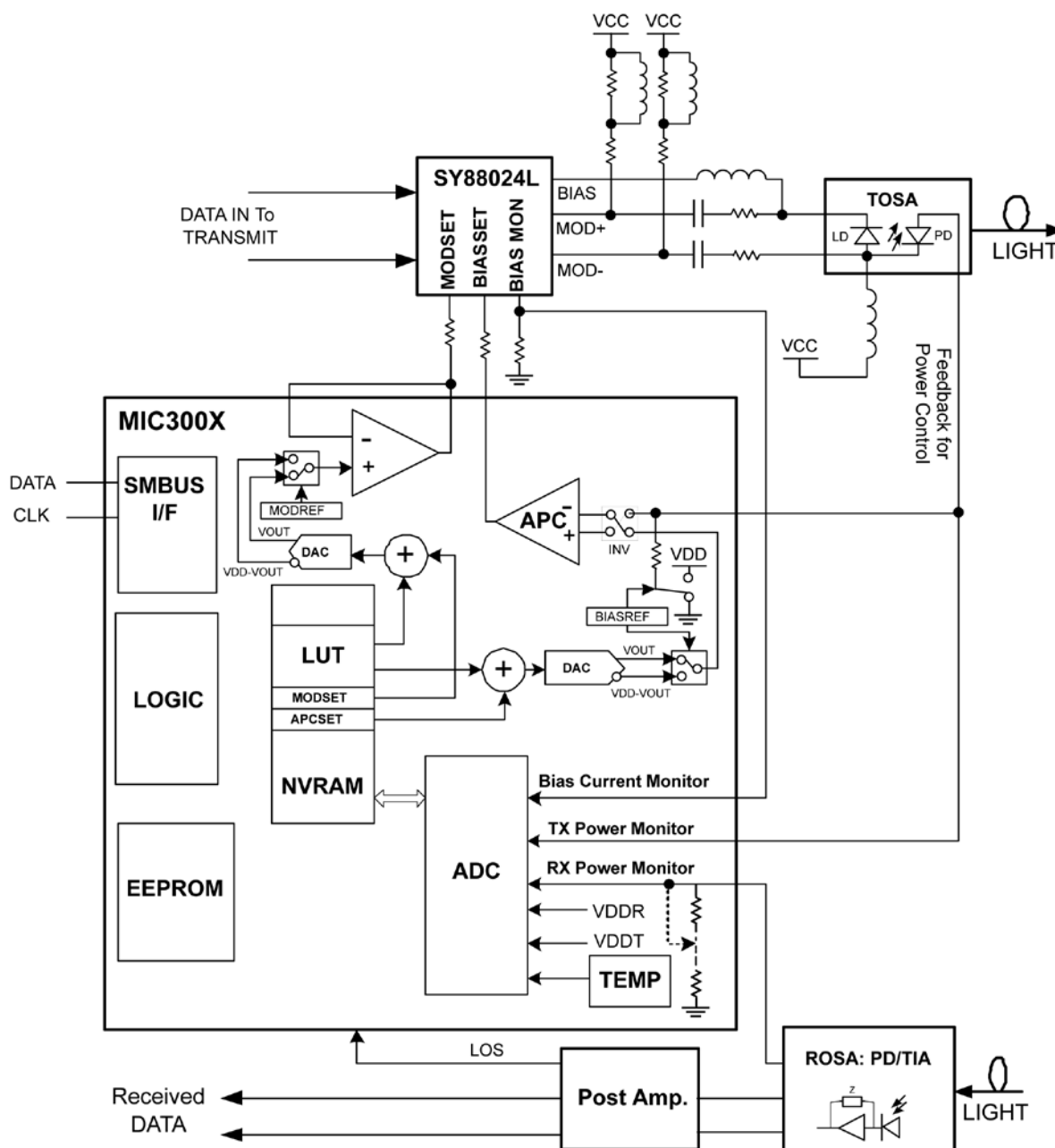
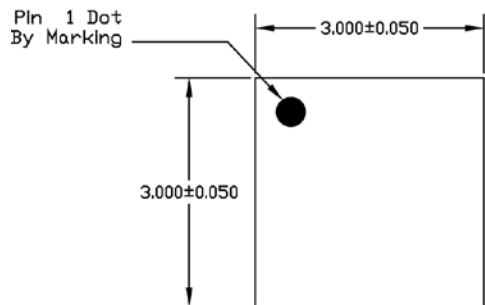
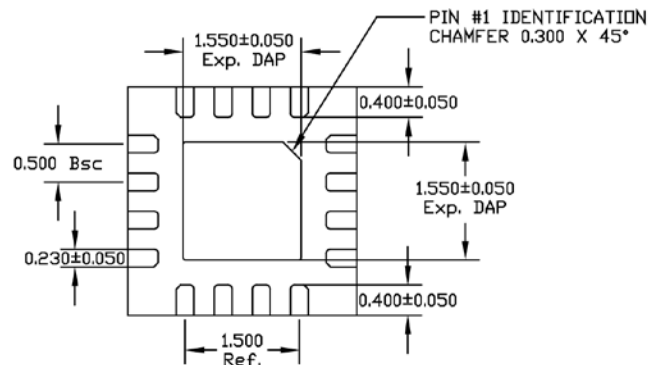


Figure 3. Typical Optical Transceiver

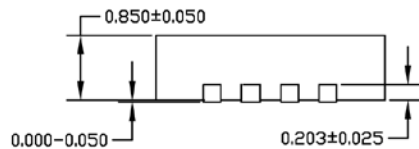
Package Information



TOP VIEW



BOTTOM VIEW



SIDE VIEW

NOTE:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. MAX. PACKAGE WARPAGE IS 0.05 mm.
3. MAXIMUM ALLOWABLE BURRS IS 0.076 mm IN ALL DIRECTIONS.
4. PIN #1 ID ON TOP WILL BE LASER/INK MARKED.

16-Pin (3mm x 3mm) QFN

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