

DTM64362E

2 GB - 240-Pin 1Rx8 Unbuffered Non-ECC DDR3 DIMM



Identification

DTM64362E 256Mx64
2GB 1Rx8 PC3-10600U-9-11-A1

Performance range

Clock / Module Speed / CL-t_{RCD} -t_{RP}

667 MHz / PC3-10600 / 9-9-9

533 MHz / PC3-8500 / 8-8-8

533 MHz / PC3-8500 / 7-7-7

400 MHz / PC3-6400 / 6-6-6

Features

240-pin JEDEC-compliant DIMM, 133.35 mm wide by 30 mm high

Operating Voltage: 1.5 V ±0.075

I/O Type: SSTL_15

Data Transfer Rate: 10.6 Gigabytes/sec

Data Bursts: 8 and burst chop 4 mode

ZQ Calibration for Output Driver and On-Die Termination (ODT)

Programmable ODT / Dynamic ODT during Writes

Programmable CAS Latency: 6, 7, 8 and 9

Differential Data Strobe signals

SDRAM Addressing (Row/Col/Bank): 15/10/3

Fully RoHS Compliant

Description

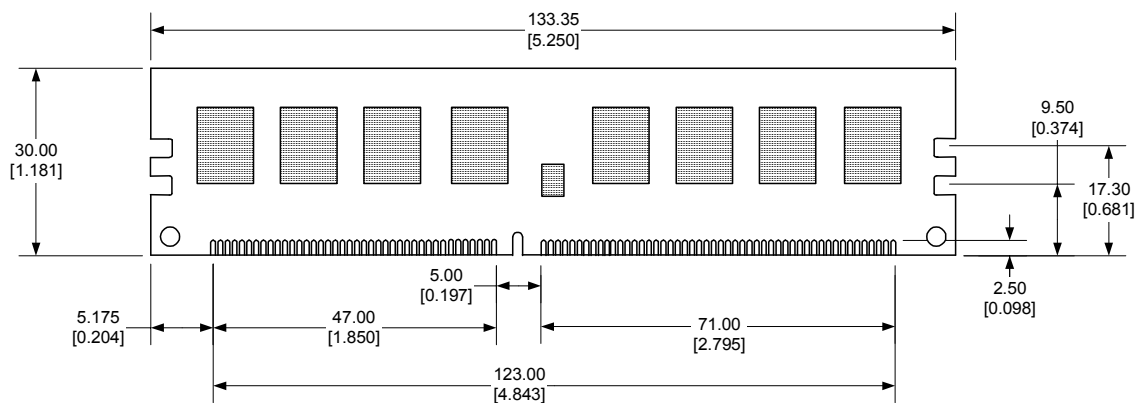
DTM64362E is an Unbuffered 256Mx64 memory module, which conforms to JEDEC's DDR3, PC3-10600 standard. The assembly is Single-Rank containing - eight 256Mx8 DDR3 Samsung SDRAMs. One 2K-bit EEPROM is used for Serial Presence Detect.

Both output driver strength and input termination impedance are programmable to maintain signal integrity on the I/O signals.

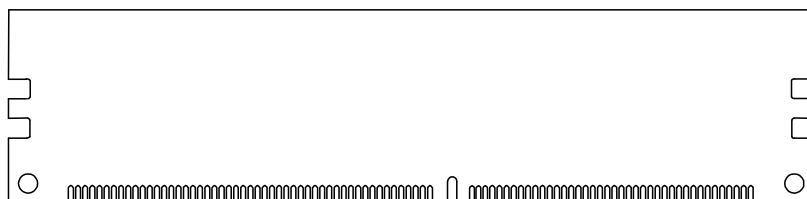
Pin Configuration						Pin Description	
Front Side			Back Side			Name	Function
1 V _{REFDQ}	31 DQ25	61 A2	91 DQ41	121 V _{SS}	151 V _{SS}	181 A1	211 V _{SS} CB[7:0] Data Check Bits
2 V _{SS}	32 V _{SS}	62 V _{DD}	92 V _{SS}	122 DQ4	152 DM3	182 V _{DD}	212 DM5 DQ[63:0] Data Bits
3 DQ0	33 /DQS3	63 CK1 **	93 /DQS5	123 DQ5	153 NC	183 V _{DD}	213 NC DQS[8:0], /DQS[8:0] Differential Data Strobes
4 DQ1	34 DQS3	64 /CK1 **	94 DQS5	124 V _{SS}	154 V _{SS}	184 CK0	214 V _{SS} DM[8:0] Data Mask
5 V _{SS}	35 V _{SS}	65 V _{DD}	95 V _{SS}	125 DM0	155 DQ30	185 /CK0	215 DQ46 CK[1:0], /CK[1:0] Differential Clock Inputs
6 /DQS0	36 DQ26	66 V _{DD}	96 DQ42	126 NC	156 DQ31	186 V _{DD}	216 DQ47 CKE[1:0] Clock Enables
7 DQS0	37 DQ27	67 V _{REFCA}	97 DQ43	127 V _{SS}	157 V _{SS}	187 /Event, NC**	217 V _{SS} /CAS Column Address Strobe
8 V _{SS}	38 V _{SS}	68 PAR _{IN} , NC**	98 V _{SS}	128 DQ6	158 CB4 **	188 A0	218 DQ52 /RAS Row Address Strobe
9 DQ2	39 CB0 **	69 VDD	99 DQ48	129 DQ7	159 CB5 **	189 V _{DD}	219 DQ53 /S[3:0] Chip Selects
10 DQ3	40 CB1 **	70 A10/AP	100 DQ49	130 V _{SS}	160 V _{SS}	190 BA1	220 V _{SS} /WE Write Enable
11 V _{SS}	41 V _{SS}	71 BA0	101 V _{SS}	131 DQ12	161 DM8 **	191 V _{DD}	221 DM6 A[15:0] Address Inputs
12 DQ8	42 /DQS8 **	72 V _{DD}	102 /DQS6	132 DQ13	162 NC	192 /RAS	222 NC BA[2:0] Bank Addresses
13 DQ9	43 DQS8 **	73 /WE	103 DQS6	133 V _{SS}	163 V _{SS}	193 /S0	223 V _{SS} ODT[1:0] On Die Termination Inputs
14 V _{SS}	44 V _{SS}	74 /CAS	104 V _{SS}	134 DM1	164 CB6 **	194 V _{DD}	224 DQ54 SA[2:0] SPD Address
15 /DQS1	45 CB2 **	75 V _{DD}	105 DQ50	135 NC	165 CB7 **	195 ODT0	225 DQ55 SCL SPD Clock Input
16 DQS1	46 CB3 **	76 /S1, NC**	106 DQ51	136 V _{SS}	166 V _{SS}	196 A13	226 V _{SS} SDA SPD Data Input/Output
17 V _{SS}	47 V _{SS}	77 ODT1, NC **	107 V _{SS}	137 DQ14	167 NC (TEST)	197 V _{DD}	227 DQ60 /EVENT Temperature Sensing
18 DQ10	48 V _{TT}	78 V _{DD}	108 DQ56	138 DQ15	168 /RESET	198 /S3, NC**	228 DQ61 /RESET Reset for register and DRAMs
19 DQ11	49 V _{TT}	79 /S2, NC **	109 DQ57	139 V _{SS}	169 CKE1, NC **	199 V _{SS}	229 V _{SS} PAR_IN Parity bit for Addr/Ctrl
20 V _{SS}	50 CKE0	80 V _{SS}	110 V _{SS}	140 DQ20	170 V _{DD}	200 DQ36	230 DM7 /ERR_OUT Error bit for Parity Error
21 DQ16	51 V _{DD}	81 DQ32	111 /DQS7	141 DQ21	171 A15 **	201 DQ37	231 NC A12/BC Combination input: Addr12/Burst Chop
22 DQ17	52 BA2	82 DQ33	112 DQS7	142 V _{SS}	172 A14 **	202 V _{SS}	232 V _{SS} A10/AP Combination input: Addr10/Auto-precharge
23 V _{SS}	53 /ERR _{OUT} , NC**	83 V _{SS}	113 V _{SS}	143 DM2	173 V _{DD}	203 DM4	233 DQ62 V _{SS} Ground
24 /DQS2	54 V _{DD}	84 /DQS4	114 DQ58	144 NC	174 A12/BC	204 NC	234 DQ63 V _{DD} Power
25 DQS2	55 A11	85 DQS4	115 DQ59	145 V _{SS}	175 A9	205 V _{SS}	235 V _{SS} V _{DDSPD} SPD EEPROM Power
26 V _{SS}	56 A7	86 V _{SS}	116 V _{SS}	146 DQ22	176 V _{DD}	206 DQ38	236 V _{DDSPD} V _{REFDQ} Reference Voltage for DQ's
27 DQ18	57 V _{DD}	87 DQ34	117 SA0	147 DQ23	177 A8	207 DQ39	237 SA1 V _{REFCA} Reference Voltage for CA
28 DQ19	58 A5	88 DQ35	118 SCL	148 V _{SS}	178 A6	208 V _{SS}	238 SDA V _{TT} Termination Voltage
29 V _{SS}	59 A4	89 V _{SS}	119 SA2	149 DQ28	179 V _{DD}	209 DQ44	239 V _{SS} NC No Connection
30 DQ24	60 V _{DD}	90 DQ40	120 V _{TT}	150 DQ29	180 A3	210 DQ45	240 V _{TT}

** Not used

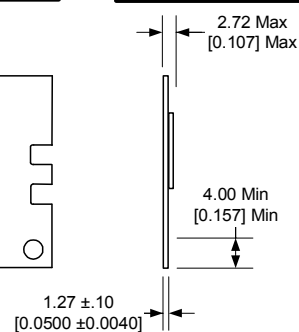
Front view



Back view



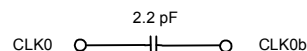
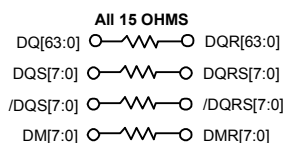
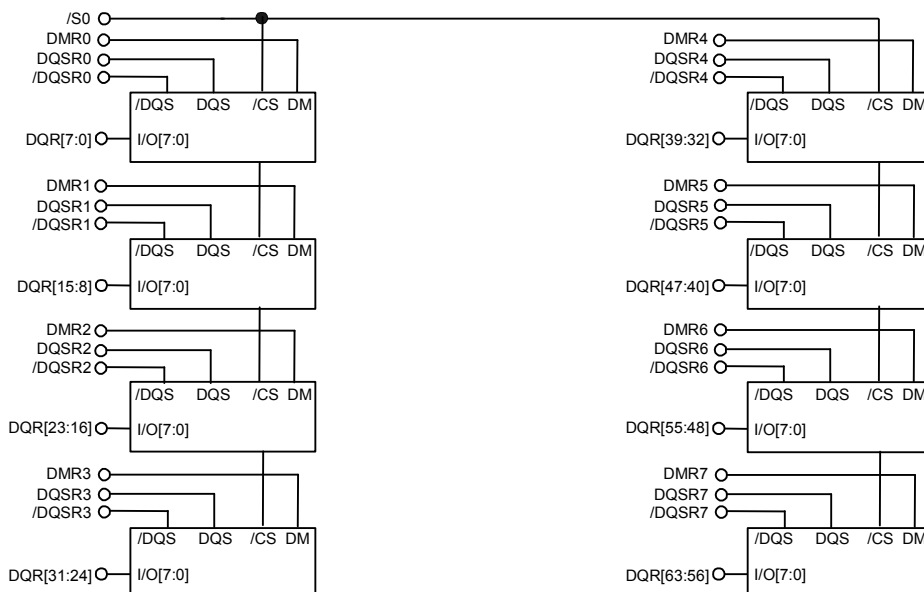
Side view



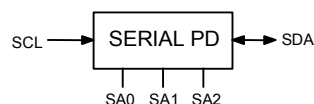
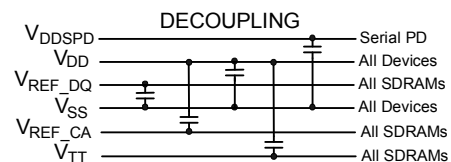
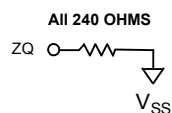
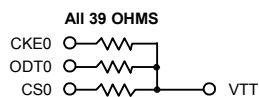
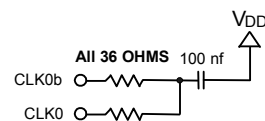
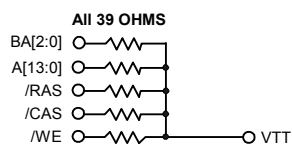
Notes

Tolerances on all dimensions except where otherwise indicated are ± 0.13 (.005).

All dimensions are expressed: millimeters [inches]



GLOBAL SDRAM CONNECTS



Absolute Maximum Ratings

(Note: Operation at or above Absolute Maximum Ratings can adversely affect module reliability.)

PARAMETER	Symbol	Minimum	Maximum	Unit
Temperature, non-Operating	$T_{STORAGE}$	-55	100	C
Ambient Temperature, Operating	T_A	0	70	C
DRAM Case Temperature, Operating	T_{CASE}	0	95	C
Voltage on V_{DD} relative to V_{SS}	V_{DD}	-0.4	1.975	V
Voltage on Any Pin relative to V_{SS}	V_{IN}, V_{OUT}	-0.4	1.975	V

Notes:

DRAM Operating Case Temperature above 85C requires 2X refresh.

Recommended DC Operating Conditions ($T_A = 0$ to 70 C, Voltage referenced to $V_{SS} = 0$ V)

PARAMETER	Symbol	Minimum	Typical	Maximum	Unit	Note
Power Supply Voltage	V_{DD}	1.425	1.5	1.575	V	
I/O Reference Voltage	V_{REFDQ}	0.49 V_{DD}	0.50 V_{DD}	0.51 V_{DD}	V	1
I/O Reference Voltage	V_{REFCA}	0.49 V_{DD}	0.50 V_{DD}	0.51 V_{DD}	V	1

Notes:

1. The value of V_{REF} is expected to equal one-half V_{DD} and to track variations in the V_{DD} DC level. Peak-to-peak noise on V_{REF} may not exceed $\pm 1\%$ of its DC value. For Reference $V_{DD}/2 \pm 15$ mV.

DC Input Logic Levels, Single-Ended ($T_A = 0$ to 70 C, Voltage referenced to $V_{SS} = 0$ V)

PARAMETER	Symbol	Minimum	Maximum	Unit
Logical High (Logic 1)	$V_{IH(DC)}$	$V_{REF} + 0.1$	V_{DD}	V
Logical Low (Logic 0)	$V_{IL(DC)}$	V_{SS}	$V_{REF} - 0.1$	V

AC Input Logic Levels, Single-Ended ($T_A = 0$ to 70 C, Voltage referenced to $V_{SS} = 0$ V)

PARAMETER	Symbol	Minimum	Maximum	Unit
Logical High (Logic 1)	$V_{IH(AC)}$	$V_{REF} + 0.175$	-	V
Logical Low (Logic 0)	$V_{IL(AC)}$	-	$V_{REF} - 0.175$	V

Differential Input Logic Levels ($T_A = 0$ to 70°C , Voltage referenced to $V_{SS} = 0\text{ V}$)

PARAMETER	Symbol	Minimum	Maximum	Unit
Differential Input Logic High	$V_{IH,DIFF}$	+0.200	DC: V_{DD} AC: $V_{DD}+0.4$	V
Differential Input Logic Low	$V_{IL,DIFF}$	DC: V_{SS} AC: $V_{SS}-0.4$	-0.200	V
Differential Input Cross Point Voltage relative to $V_{DD}/2$	V_{IX}	- 0.150	+ 0.150	V

Capacitance ($T_A = 25^\circ\text{C}$, $f = 100\text{ MHz}$)

PARAMETER	Pin	Symbol	Minimum	Maximum	Unit
Input Capacitance, Clock	CK0, /CK0,	C_{CK}	8.6	13.4	pF
Input Capacitance, Address	BA[2:0], A[14:0], /RAS, /CAS, /WE	C_I	6	10.4	pF
Input Capacitance Control	/S0, CKE0, ODT0	C_I	6	10.4	pF
Input/Output Capacitance	DQ[63:0], DQS[7:0], /DQS[7:0], DM[7:0]	C_{IO}	1.5	2.5	pF
ZQ Capacitance	ZQ	C_{ZQ}	-	6	pF

DC Characteristics ($T_A = 0$ to 70°C , Voltage referenced to $V_{SS} = 0\text{ V}$)

PARAMETER	Symbol	Minimum	Maximum	Unit	Note
Input Leakage Current (Any input $0\text{ V} < V_{IN} < V_{DD}$)	I_{IL}	-18	+18	μA	1,2
Output Leakage Current ($0\text{ V} < V_{OUT} < V_{DDQ}$)	I_{OL}	-10	+10	μA	2,3

Notes:

- 1) All other pins not under test = 0 V
- 2) Values are shown per pin
- 3) DQ's, DQS, DQS and ODT are disabled

I_{DD} Specifications and Conditions (T_A = 0 to 70 °C, Voltage referenced to V_{SS} = 0 V)

PARAMETER	Symbol	Test Condition	Max Value	Unit
Operating One Bank Active-Precharge Current	I _{DD0}	Operating current : One bank ACTIVATE-to-PRECHARGE	288	mA
Operating One Bank Active-Read-Precharge Current	I _{DD1}	Operating current : One bank ACTIVATE-to-READ-to-PRECHARGE	361	mA
Precharge Power-Down Current	I _{DD2P}	Precharge power down current: (Slow exit)	87	mA
Precharge Power-Down Current	I _{DD2P}	Precharge power down current: (Fast exit)	108	mA
Precharge Quiet Standby Current	I _{DD2Q}	Precharge quiet standby current	144	mA
Precharge Standby Current	I _{DD2N}	Precharge standby current	144	mA
Active Power-Down Current	I _{DD3P}	Active power-down current	123	mA
Active Standby Current	I _{DD3N}	Active standby current	215	mA
Operating Burst Write Current	I _{DD4W}	Burst write operating current	578	mA
Operating Burst Read Current	I _{DD4R}	Burst read operating current	542	mA
Burst Refresh Current	I _{DD5}	Refresh current	830	mA
Self Refresh Current	I _{DD6}	Self-refresh temperature current: MAX T _C = 85°C	86	mA
Operating Bank Interleave Read Current	I _{DD7}	All bank interleaved read current	975	mA

AC Operating Conditions

PARAMETER	Symbol	Min	Max	Unit
Internal read command to first data	t_{AA}	13.125	20	ns
CAS-to-CAS Command Delay	t_{CCD}	4	-	t_{CK}
Clock High Level Width	$t_{CH(avg)}$	0.47	0.53	t_{CK}
Clock Cycle Time	t_{CK}	1.5	1.875	ns
Clock Low Level Width	$t_{CL(avg)}$	0.47	0.53	t_{CK}
Data Input Hold Time after DQS Strobe	t_{DH}	65	-	ps
DQ Input Pulse Width	t_{DIPW}	400	-	ps
DQS Output Access Time from Clock	t_{DQSCK}	-255	+255	ps
Write DQS High Level Width	t_{DQSH}	0.4	0.6	$t_{CK(avg)}$
Write DQS Low Level Width	t_{DQSL}	0.4	0.6	$t_{CK(avg)}$
DQS-Out Edge to Data-Out Edge Skew	t_{DQSQ}	-	125	ps
Data Input Setup Time Before DQS Strobe	t_{DS}	30	-	ps
DQS Falling Edge from Clock, Hold Time	t_{DSH}	0.2	-	$t_{CK(avg)}$
DQS Falling Edge to Clock, Setup Time	t_{DSS}	0.2	-	$t_{CK(avg)}$
Clock Half Period	t_{HP}	minimum of t_{CH} or t_{CL}	-	ns
Address and Command Hold Time after Clock	t_{IH}	140	-	ps
Address and Command Setup Time before Clock	t_{IS}	65	-	ps
Load Mode Command Cycle Time	t_{MRD}	4	-	t_{CK}
DQ-to-DQS Hold	t_{QH}	0.38	-	$t_{CK(avg)}$
Active-to-Precharge Time	t_{RAS}	36	$9 \cdot t_{REFI}$	ns
Active-to-Active / Auto Refresh Time	t_{RC}	49.125	-	ns
RAS-to-CAS Delay	t_{RCD}	13.125	-	ns
Average Periodic Refresh Interval $0^{\circ}C \leq T_{CASE} < 85^{\circ}C$	t_{REFI}	-	7.8	μs
Average Periodic Refresh Interval $0^{\circ}C \leq T_{CASE} < 95^{\circ}C$	t_{REFI}	-	3.9	μs
Auto Refresh Row Cycle Time	t_{RFC}	160	-	ns
Row Precharge Time	t_{RP}	13.125	-	ns
Read DQS Preamble Time	t_{RPRE}	0.9	Note-1	$t_{CK(avg)}$
Read DQS Postamble Time	t_{RPST}	0.3	Note-2	$t_{CK(avg)}$
Row Active to Row Active Delay	t_{RRD}	Max(4nCK, 6ns)	-	ns
Internal Read to Precharge Command Delay	t_{RTP}	Max(4nCK, 7.5ns)	-	ns
Write DQS Preamble Setup Time	t_{WPRE}	0.9	-	$t_{CK(avg)}$
Write DQS Postamble Time	t_{WPST}	0.3	-	$t_{CK(avg)}$
Write Recovery Time	t_{WR}	15	-	ns
Internal Write to Read Command Delay	t_{WTR}	Max(4nCK, 7.5ns)	-	ns

Notes:

1. The maximum preamble is bound by $t_{LZDQS}(min)$
2. The maximum postamble is bound by $t_{HZDQS}(max)$



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