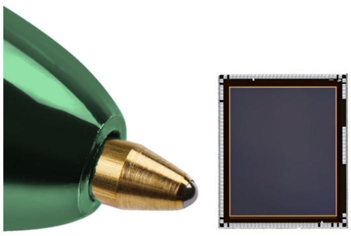
VD16GZ

Datasheet

Compact and high-sensitivity 1.5 megapixel RGB-NIR global shutter image sensor



Order code	Description
VD16GZCCA/RW	RGB-NIR, bare die as reconstructed wafer

Features

- Cutting-edge performance of ST proprietary pixel:
  - **BSI structure:** Provides superior QE, MTF, and angular response.
  - **Full DTI technology:** Further increases sensitivity and sharpness.
  - **Versatile imaging:** Benefits both color and NIR (850 nm, 940 nm) image capture.
  - **Reliable supply:** Proprietary technology from ST foundry in France, ensures a safe supply.
- Easy integration into your system:
  - **Ultracompact die:** Centered design to minimize your system size.
  - **Small optical format:** 4.6 mm (1/4") at full resolution and 3.7 mm (1/5") with 1 MP crop.
  - **Low-power consumption:** Ideal for battery-powered devices.
  - **Robust design:** Ensures high image quality at various temperatures.
- A complete toolbox of in-sensor features:
  - **Stunning images:** Achieved with in-sensor AE and various corrections.
  - **Data optimization:** Multiple features to optimize data size and frame rates such as crop, and programmable sequences.
  - **Enhanced controls:** 8 GPIOs enabling extra controls such as trigger or LED synchronization.
- Seamless connection to embedded processing platforms:
  - **MIPI CSI-2 interface:** 1 or 2 lanes enabling direct connection to entry-level cost-effective processing platforms.
  - **Turnkey solutions:** Start your development immediately with our sensor boards, modules, and drivers for the VD16GZ image sensor.
- The VD16GZ color and near infrared image sensor is also available in monochrome (VD56G3) and color RGB (VD66GY) versions.

Description

The VD16GZ is part of the new generation of image sensors developed by STMicroelectronics for professional and consumer vision applications. Leveraging state-of-the-art technologies developed by ST's own foundry, the sensor provides outstanding performance in color and near infrared. With its RGB-NIR pattern, the VD16GZ is perfectly suited for multispectral imaging and for the many applications requiring the simultaneous capture of both color and near infrared images.

Application

- Home and service robots
- Smart appliances
- Agriculture
- Drones and UAVs
- Industrial robots and AGVs
- Quality inspection
- 3D stereo imaging
- Security and biometrics

1 Acronyms and abbreviations

Table 1. Acronyms and abbreviations

Acronym/abbreviation	Definition
ADC	analog to digital converter
AE	autoexposure
AGV	automated guided vehicle
AR	augmented reality
CCI	camera control interface
CP	charge pump
CRA	chief ray angle
CSI	camera serial interface
DTI	deep trench isolation
EMC	electromagnetic compatibility
EMI	electromagnetic interference
FoV	field of view
fps	frames per second
GPIO	general-purpose input/output
I^2C	inter-integrated circuit (bus)
ISL	intelligent status line
ISP	image signal processor
LDO	low dropout regulator
LED	light-emitting diode
MCU	microcontroller unit
MIPI	mobile industry processor interface
MTF	modulation transfer function
NIR	near infrared
OIF	output interface
OTP	one-time programmable
PLL	phase-locked loop
PWM	pulse-width modulation
QE	quantum efficiency
RI	relative illumination
SW	software
UAV	unmanned aerial vehicle
UI	user interface for host to sensor communication
VR	virtual reality

2 Product overview

2.1 Functional description summary

The VD16GZ is designed to be mounted in a system equipped with a dual bandpass filter lens. The organization of the RGB-NIR 4x4 kernel is optimized for the generation of high contrast NIR images and high-quality RGB images. These images are obtained after external host processing applying NIR removal and debayerization.

The VD16GZ is a 1.5-megapixel global shutter image sensor featuring a matrix of 1124 x 1364 pixels. With its global shutter operation, all pixels are synchronized to capture light at the same time. This removes the motion blur that can affect rolling shutter image sensors, when capturing changing or moving scenes.

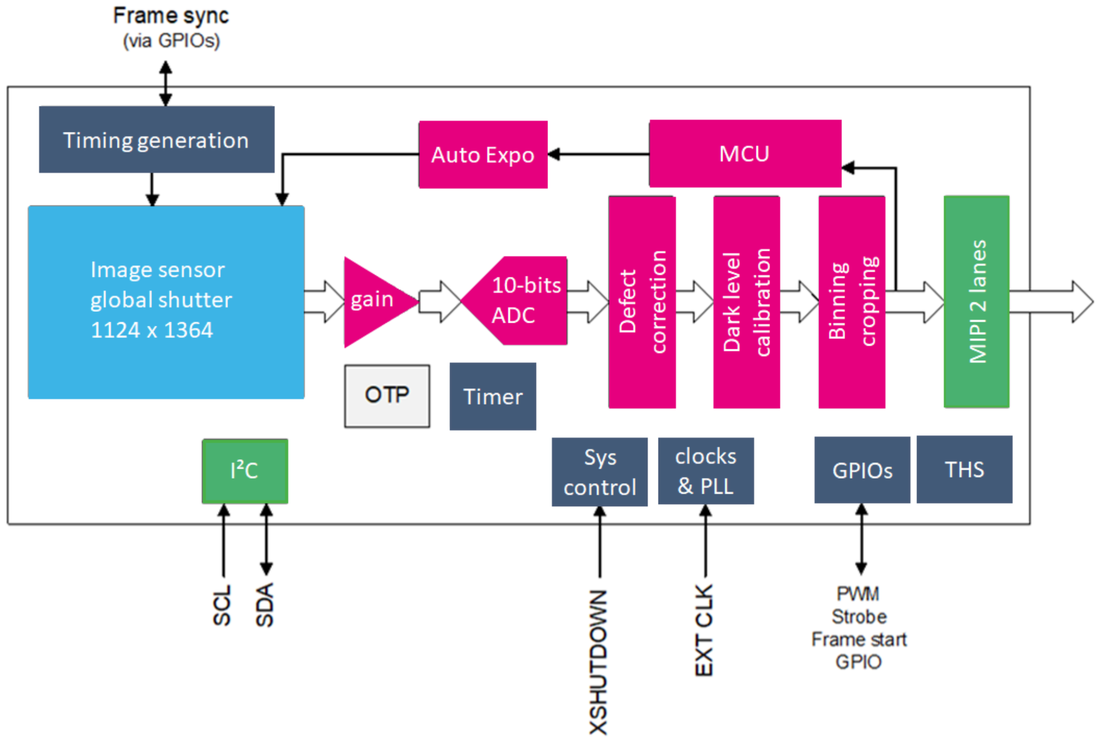
Once the exposure is finished, each pixel information is transferred in a storage node, before being read and digitized one pixel row after the other. The image data are digitized using internal 10-bit ADCs. Additional gains can be applied before ADC stage (for example, analog gain) or after ADC stage (for example, digital gain). Following the digital conversion, various image preprocessing and correction algorithms can be applied into the sensor before data output, such as autoexposure or binning.

The image data are output as frames of RAW8 or RAW10 data through a MIPI CSI-2 interface. The sensor can be configured to operate with either 1 or 2 MIPI CSI-2 lanes to best fit with host processing requirements.

The VD16GZ is synchronized to the rest of the system by means of an external clock, triggers, and general-purpose input/output (GPIO) signals that can be used to enable synchronization of several sensor readouts or to control strobe light sources during exposure time.

The device is fully configurable through the I²C serial interface and provides flexible frame-to-frame parameter configuration changes via the use of programmable contexts. It also embeds a one-time programmable (OTP) nonvolatile memory to be written by 32-bit words.

Figure 1. Functional block diagram



2.2 Technical specifications summary

Table 2. **Technical specifications**

Category	Parameter	VD16GZ specifications
Resolution	Resolution	1.53 MP
	Pixel array [H x V]	1124 x 1364
	Aspect ratio	5:6
Pixel	Shutter type	Global shutter
	Illumination type	Back side illuminated (BSI)
	Pixel size	2.61 µm
Color	Color option	RGB-NIR
Frame rates (maximum)	Full resolution	88 fps
	1 MP resolution	121 fps
	VGA resolution	237 fps
Optical characteristics	Pixel array size [H x V]	2.93 mm x 3.56 mm
	Optical format	1/4” (4.61 mm)
	CRA	30° linear
Mechanical characteristics	Die footprint [H x V]	3.65 mm x 4.34 mm
	Die centering (optical vs. mechanical)	Yes
	Die pinout	115 pins
	Operating temperature range	-30 to +85°C
Electronic characteristics	Sensor data interface	MIPI CSI-2 | 1 or 2 lanes
	Sensor control interface	I²C, up to 1 Mbits/s
	Output format	RAW8, RAW10
	Supply voltages	2.8 V – 1.8 V – 1.15 V
	External clock frequency	6 to 27 MHz
	Power consumption	145 mW (typical at 60 fps) / 4 mW (Standby)
Embedded features	Image quality optimization	• Autoexposure • Automatic dark calibration • Analog and digital gains
	Data and frame rate optimization	• Cropping • Context management with up to 4 contexts
	Others	• Mirror/Flip • Test pattern generation • Temperature sensor • 8 programmable GPIOs for LED control, PWM control, autonomous or controlled external frame start

3 Functional description

3.1 Interfaces

3.1.1 Inter-integrated circuit (I²C)

The VD16GZ is configured and controlled via an I²C interface operating in either fast mode (up to 400 kHz) or fast mode plus (up to 1 MHz) at 1.8 V. After the MCU boot sequence, the default I²C configuration is fast mode plus with a sink capability set to 20 mA. Drive capability can be decreased to 4 mA (fast mode) by writing a dedicated register once the system has booted. Device addressing uses a CCI protocol with 2 byte subaddresses. The default sensor address is 0x20 (including R/W bit), and can be overridden:

- Permanently by storing a non-null value in a dedicated OTP register.
- Dynamically with a firmware command when the MCU state is SW_STANDBY.

3.1.2 Camera serial interface (CSI)

The sensor is ready to connect via a dual lane mobile industry processor interface (MIPI) CSI-2 serial interface.

The dual lane MIPI CSI-2 serial interface supports up to 1.5 Gbps per lane. It is the industry standard for low electromagnetic interference (EMI) and excellent electromagnetic compatibility (EMC) high-speed interfacing. The CSI lane number can be lowered to a single lane. Resolution is scalable between RAW8 and RAW10.

3.2 Power supplies

The power supplies required by the sensor are:

- 2.8 V for the analog blocks
- 1.8 V for the digital I/Os
- 1.15 V for the core digital logic and MIPI CSI-2 output drivers

The pixel array requires different positive and negative voltages, all internally generated by charge pumps and regulators. Four voltage references, internally generated, need external decoupling capacitors. The internal MCU handles the entire power management of the sensor to guarantee the lowest power consumption at any given time.

3.3 Clock and PLL

An input clock is required from an external digital clock source in the range of 6 to 27 MHz. Firmware is preconfigured for a 12 MHz external source clock. Two built-in PLL (phase-locked loop) blocks generate all necessary internal clocks for the pixel array, processing pipe, and output interface.

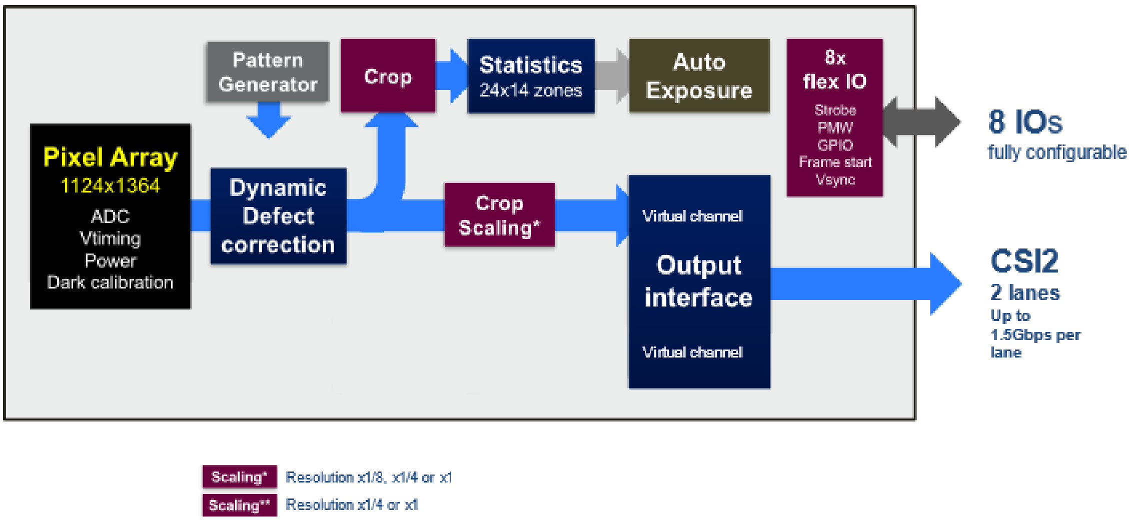
3.4 Video pipe

The video pipe performs several features designed to ensure a high quality image. These features include:

- Analog subsampling
- Pattern generation
- Dynamic defective pixel correction
- Dark calibration
- Autoexposure
- Digital binning
- Embedded status lines
- Output interface
- Context management
- Cropping

The diagram below presents the features implementation in the video pipe

Figure 2. Image signal processor schematic

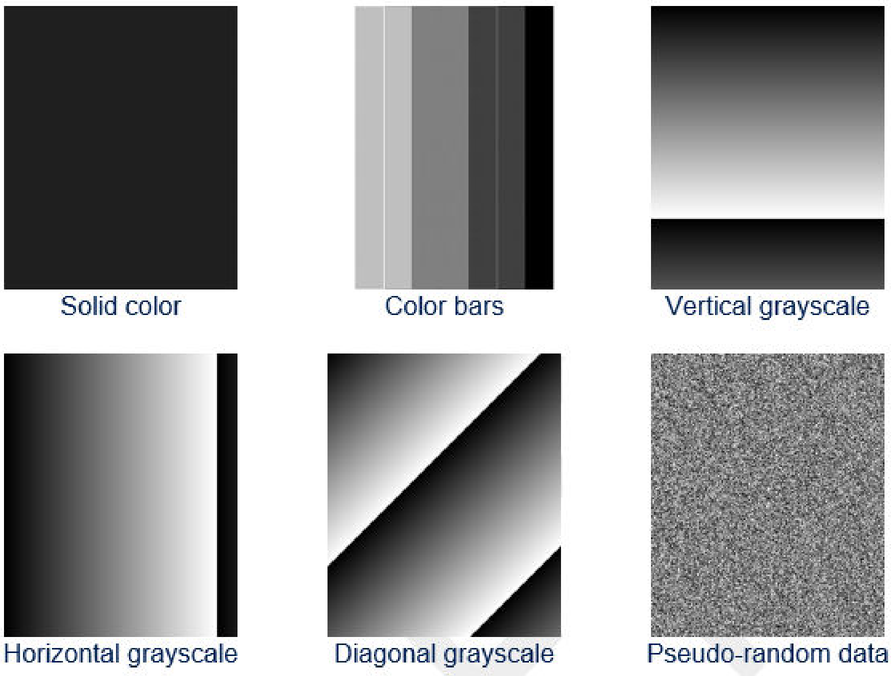


3.4.1 Pattern generation

The pattern generation allows the generation of digital patterns in the output frame for test and debug. It is also possible to insert a cross bar in the image with configurable position, size, and brightness. The available patterns are:

- Solid color
- Color bars
- Vertical gray scale
- Horizontal gray scale
- Diagonal gray scale
- Pseudorandom data

Figure 3. Available patterns



3.4.2 Defective pixel correction

Active pixels are automatically corrected by a dynamic algorithm embedded in the sensor ISP, enabling defect-free images straight out of the sensor without further algorithm development or processing resources.

The advanced correction algorithm can correct singlet and couplet of defects and take into account local spatial gradients.

The host can program the strength of the correction to find the perfect balance between systematic defect correction and preserving existing textures/patterns in the image. The correction strength evolves automatically with exposure time. This mechanism can be deactivated for debugging purposes and for specific use cases such as structured light.

Note: Because of the specific RGB-NIR 4x4 kernel pattern where blue and red pixel positions toggle along the matrix, defective pixel correction can slightly modify blue and red channel information at transitions. Green and NIR information are not affected.

3.4.3 Dark calibration

The pixel matrix has dedicated lines with shielded pixels that dynamically retrieve the dark level and subtract it from the active image. Temperature, exposure time, or gain changes are compensated. Temporal smoothing and fractional bit dithering are applied to avoid a sudden one-code step. This block also embeds a programmable digital gain control feature with a granularity of 1/256 followed by a configurable pedestal to offset the dark level along the ISP pipe.

3.4.4 Analog and digital gains

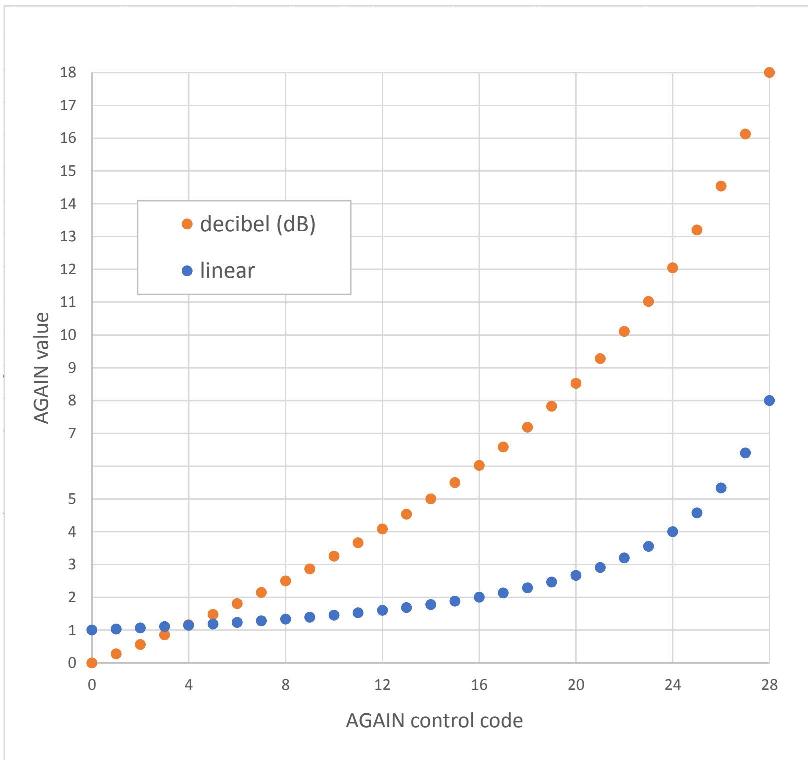
The VD16GZ enables to adjust analog and digital gains on the image to optimize image quality depending on the lighting conditions. Gains are adjusted automatically when autoexposure is enabled, or by manual control when autoexposure is disabled.

Analog gain ranges from x1 (+ 0 dB) up to x8 (+18 dB) with 29 steps following a 1/X behavior enabling to benefit from fine gain granularity at low gain and wider granularity at high gains to better adjust image quality. It follows the following formula:

$$Analog\ gain(x) = \frac{32}{32 - x}$$

Where x is an integer from 0 to 28.

Figure 4. Analog gain progression versus control code



Four digital gains (one per color channel) can be applied, each of them ranging from 1.0 up to 8.0 minus one-step control with a step control of 1/256th so approximately 0.0039.

3.4.5 Autoexposure

The autoexposure (AE) feature computes and automatically applies the ideal exposure time and gain factors to get the optimum average luminance in the image. The autoexposure algorithm is performed directly in the sensor, to benefit from automatic exposure without the need to develop any dedicated algorithm or to allocate processor resources to the computation.

The sensor can also operate in manual mode where exposure parameters are provided by the host.

The host can configure autoexposure module parameters that control brightness target, convergence speed, and stability. The region of interest (ROI) used for autoexposure can be set independently from the image capture region.

A specific antiflickering mode can be selected to mitigate artifacts introduced by ambient light frequency and frame rate differences.

A dedicated I^2C status register provides the image average brightness information when the sensor is set to autoexposure or manual exposure mode. This information is also available in the status lines (ISL) embedded at the beginning of each frame. Refer to Section 3.4.8: Embedded status lines for ISL description.

3.4.6 Analog subsampling

The devices support x2 and x4 subsampling which reduces overall image size and keeps the same field of view (FoV). Subsampling is applied vertically and horizontally during the ADC readout, where every two or every four pixels are read. When subsampling is used, the frame rate can be increased by decreasing the frame length.

Note: Because of the specific RGB-NIR 4x4 kernel pattern where blue and red pixel positions toggle along the matrix, using analog subsampling (by 2 or by 4) results in a loss of blue or red channel information. Green and NIR information are not affected.

3.4.7 Digital binning

The digital binning process reduces the image resolution by a factor of 2 or 4 in each direction. Central and neighboring pixels are weighted to produce the digital binned image, avoiding special phase shift and artifacts which may occur on the output image. Digital binning and subsampling are mutually exclusive.

Note: Because of the specific RGB-NIR 4x4 kernel pattern where blue and red pixel positions toggle along the matrix, using digital binning (by 2 or by 4) results in a loss of blue or red channel information. Green and NIR information are not affected.

3.4.8 Embedded status lines

The output interface (OIF) embeds the intelligent status line generator, which allows metadata to be sent through the MIPI image data interface. The ISL follows the SMIA CSI-2, simplified, 2-byte, tagged data format for RAW8 data packing. There are two ISL lines transmitted at the beginning of each frame. Each data packet is 256 bytes long. The length of the ISL can be stretched to equal the active line packet size.

The MCU has access to a bank of status registers, refreshed at each frame, and providing detailed information on the current state of the sensor. Most of the content of this bank is also available in ISLs. The ISL contains all information related to the current transmitted frame such as:

- Clock settings
- Cropping and orientation parameters
- Analog and digital gains
- Integration time
- Frame counter index
- Thermal sensor values
- Dark calibration parameters

Transmission of ISL data packets can be disabled by configuring a static register during SW_STANDBY state before streaming. ISL data packets have their own programmable "data types" and "virtual channels".

3.4.9 Output interface

The output interface (OIF) embeds two data lanes of the MIPI D-PHY interface. It supports up to 1.5 Gbps of data per lane. The OIF outputs active pixel data in RAW10 or RAW8.

The OIF can output a combination of the following:

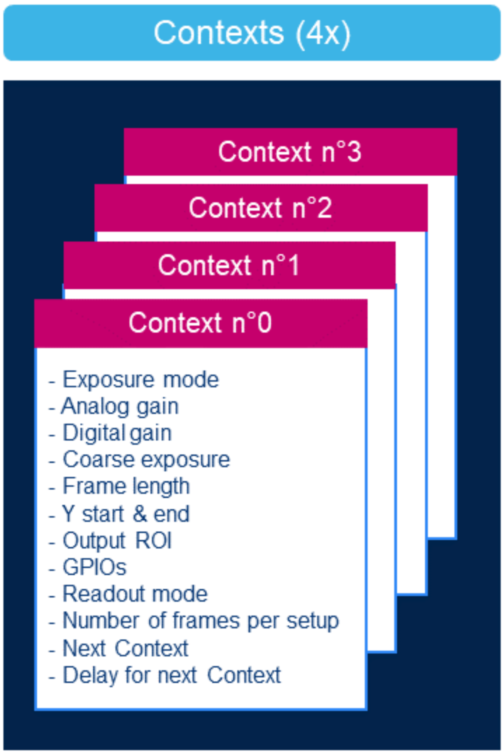
- Intelligent status lines
- Active pixel data

The OIF supports multiple virtual channels and different data types for active pixels and ISL data.

3.4.10 Context management

The sensor allows the configuration of up to four different rolling contexts (or frame setups). Parameters that can be specifically defined in a context are listed in the figure below.

Figure 5. Context parameters



Contexts can be chained one to another in an ending or non-ending sequence.

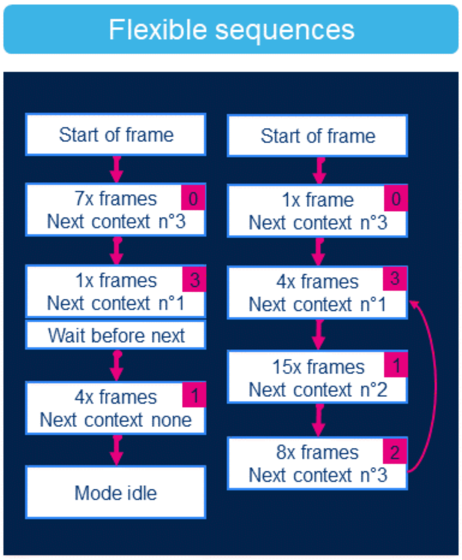


Figure 6. **Example of ending and non-ending multicontext sequence**

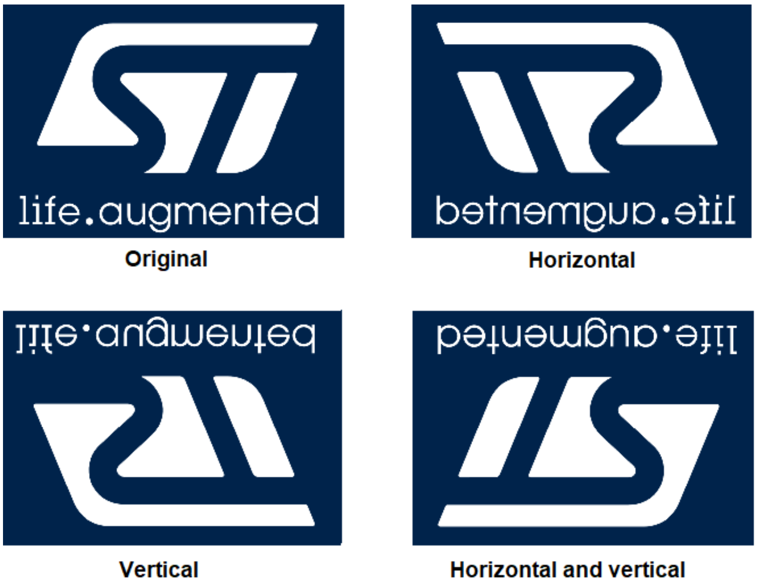
3.4.11 Cropping

The host can accurately choose which area of the whole pixel array it receives. This reduces traffic on the CSI interface and saves processing time.

3.4.12 Orientation

The sensor image can be horizontally (mirror) and/or vertically flipped, as illustrated in the following figure.

Figure 7. **Image orientation**



3.5 Synchronization modes

The sensor has multiple synchronization modes:

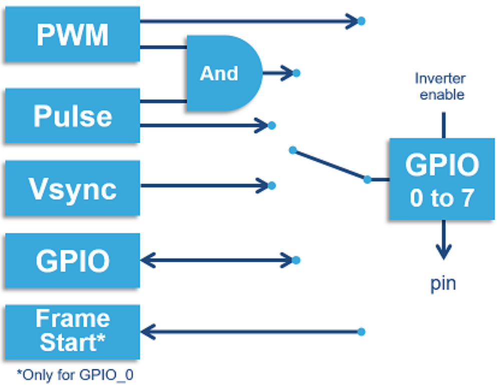
1. Leader mode
   – Image streaming starts right after the execution of a streaming initialization command sent over the I^2C bus
   – After the initialization sequence, wait for a rising edge event on GPIO0 to start streaming images
2. Follower mode
   – Using GPIO pulses
   – Using I^2C triggering commands

3.6 General purpose input/outputs (GPIOs)

The sensor provides eight GPIOs:

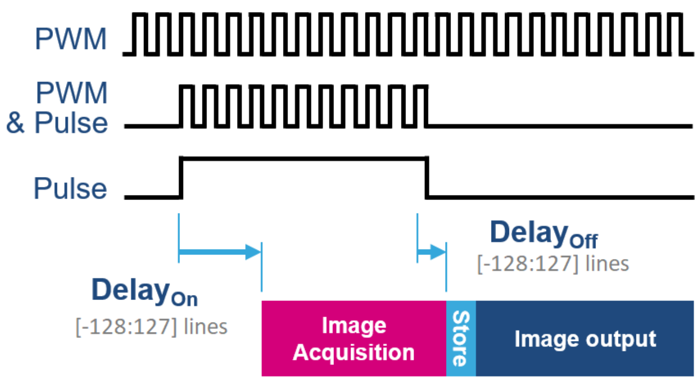
- GPIO0 is used as a frame start synchronization signal or as a generic GPIO if not used for this function
- GPIO[1-7] are used as PWM outputs, pulse (strobe) outputs, VSYNC, or as a generic GPIO, as per the configuration

Figure 8. GPIO modes



All GPIO settings are fully configurable for the four context setups. Each output signal can be mapped to one or several of the GPIOs. All GPIOs have configurable polarity.

Figure 9. PWM and pulse overview



During SW_STANDBY state the GPIOs can be controlled as output low/high or input.

3.7 Sensor firmware

The sensor is presenting to the host a user interface (bank of registers), accessible via the I²C bus.

The host writes high-level parameters in the user interface and an MCU inside the sensor applies the proper sensor configuration based on UI settings provided by the host.

3.8 Use case examples

Table 3. **Example of functional use cases**

Resolution	Maximum fps	Typical data rate
1124 x 1364	88	2 lanes, 800 Mbps per lane
1124 x 1364	88	1 lane, 1500 Mbps
720 x 1280	90	2 lanes, 800 Mbps per lane
640 x 480	210	1 lane at 1500 Mbps
320 x 240	360	1 lane at 1500 Mbps

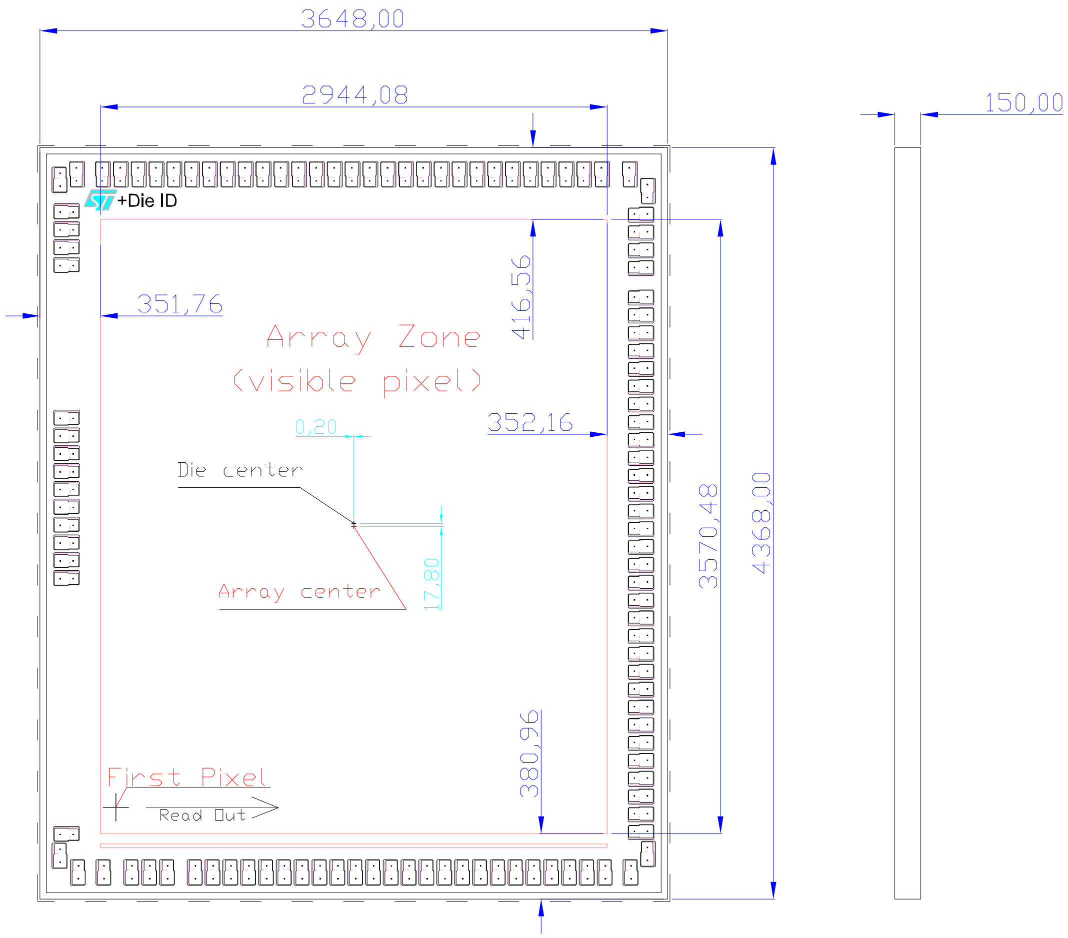
4 Die specification

In the table below, the die dimensions are after sawing.

Table 4. Die dimensions

Description	North, (+y) µm	East, (+x) µm	South, (-y) µm	West, (-x) µm
Chip center	0.0	0.0	0.0	0.0
Optical center	—	-0.2	-17.80	—
First active pixel	1767.44	1471.84	-1803.04	-1472.24
First µlens	—	—	—	—
Inner edge of pad	2025.9	1665.9	-2025.9	-1665.9
Center of pad	2065.9	1705.9	-2065.9	-1705.9
Edge of chip	2184 ±10	1824 ±10	-2184 ±10	-1824 ±10
1/2 scribe width	50.0	50.0	50.0	50.0

Figure 10. Die mechanical dimensions (µm)



5 Pin description and assignment

Table 5. Pin description

Pin name	Type	Description	Reset state	Reference supply
Power supply				
VCORE	PWR	1.15 V power supply for the digital core		1.15 V
VDDIO		1.8 V power supply for I/Os		1.8 V
VANA		2.8 V analog power supply		2.8 V
DGND		Digital ground		VDDIO
AGND		Analog ground		VANA
Reference				
LDO2V4	REF	Internal reference (must be connected together)		VANA
VCPNEG_IN		Must be connected to VCPNEG_OUT		
VCPNEG_OUT		Must be connected to VCPNEG_IN		
VCPPOS_IN		Must be connected to VCPPOS_OUT		
VCPPOS_OUT		Must be connected to VCPPOS_IN		
VDDAMP		All VDDAMP (internal reference) must be connected together		VDDIO
CSI-2 interface				
DATA1P, DATA1N	MIPI DPHY	CSI-2 data lane 1, positive and negative	Low	VCORE
DATA2P, DATA2N		CSI-2 data lane 2, positive and negative		
CLKP, CLKN		CSI-2 clock, positive and negative		
Host interface				
XSHUTDOWN	I	Reset active low		VDDIO
SDA	I/O	I²C data		
SCL	I	I²C clock		
GPIO0	I/O	General-purpose I/O and strobe light control	Low	
GPIO1				
GPIO2				
GPIO3				
GPIO4				
GPIO5				
GPIO6				
GPIO7				
CLKIN	I	Input clock		
Other pins				
PORTEST	I	Must be connected to digital ground		VDDIO
NC		Not connected		
RCALIB		Not connected		

Table 6. Pin coordinates

The pin coordinates (0, 0) are the die center

Pin number	Bonding point X coordinate	Bonding point Y coordinate	Net name
1	-1611.62	2065.9	VCPPOS_OUT
2	-1461.56	2065.9	VANA
3	-1357.52	2065.9	AGND
4	-1253.97	2065.9	DGND
5	-1150.42	2065.9	VCORE
6	-1046.87	2065.9	AGND
7	-943.32	2065.9	DGND
8	-839.77	2065.9	VCORE
9	-736.22	2065.9	VANA
10	-632.67	2065.9	VANA
11	-529.12	2065.9	AGND
12	-425.57	2065.9	VCORE
13	-322.02	2065.9	NC
14	-218.47	2065.9	VANA
15	-114.92	2065.9	NC
16	-11.37	2065.9	AGND
17	92.18	2065.9	VANA
18	195.73	2065.9	DGND
19	299.28	2065.9	VCORE
20	402.83	2065.9	DGND
21	506.38	2065.9	VANA
22	609.93	2065.9	AGND
23	713.48	2065.9	VANA
24	817.03	2065.9	AGND
25	920.62	2065.9	DGND
26	1024.17	2065.9	DGND
27	1127.77	2065.9	SDA
28	1231.32	2065.9	SCL
29	1334.87	2065.9	VCORE
30	1438.42	2065.9	XSHUTDOWN
31	1600.34	2065.9	VDDIO
32	1705.9	1969.53	NC
33	1705.9	1798.29	GPIO0
34	1705.9	1694.72	PORTST
35	1705.9	1591.15	DGND
36	1705.9	1487.58	GPIO1
37	1705.9	1316.29	GPIO2
38	1705.9	1212.71	DGND
39	1705.9	1109.14	VCORE
40	1705.9	1005.58	DGND

Pin number	Bonding point X coordinate	Bonding point Y coordinate	Net name
41	1705.9	902	VCORE
42	1705.9	798.44	DGND
43	1705.9	694.87	LDO2V4
44	1705.9	591.29	VCORE
45	1705.9	487.73	DGND
46	1705.9	384.16	VDDIO
47	1705.9	280.58	GPIO3
48	1705.9	177.02	VCORE
49	1705.9	73.44	DGND
50	1705.9	-30.13	GPIO4
51	1705.9	-133.69	NC
52	1705.9	-237.26	VCORE
53	1705.9	-340.83	DGND
54	1705.9	-444.41	DGND
55	1705.9	-547.98	DGND
56	1705.9	-651.54	VCORE
57	1705.9	-755.12	AGND
58	1705.9	-858.69	GPIO5
59	1705.9	-962.25	GPIO6
60	1705.9	-1065.83	GPIO7
61	1705.9	-1169.39	VDDIO
62	1705.9	-1272.96	VANA
63	1705.9	-1376.54	LDO2V4
64	1705.9	-1480.11	DGND
65	1705.9	-1583.67	VCORE
66	1705.9	-1687.25	DGND
67	1705.9	-1790.82	CLKIN
68	1705.9	-1959.03	VDDIO
69	1611.63	-2065.9	DGND
70	1461.52	-2065.9	DGND
71	1357.95	-2065.9	VDDAMP
72	1254.38	-2065.9	VCORE
73	1150.81	-2065.9	DGND
74	1047.24	-2065.9	DGND
75	943.67	-2065.9	DATA2N
76	840.1	-2065.9	DATA2P
77	736.53	-2065.9	VDDAMP
78	632.96	-2065.9	CLKN
79	529.39	-2065.9	DGND
80	425.82	-2065.9	CLKP
81	322.25	-2065.9	VCORE

Pin number	Bonding point X coordinate	Bonding point Y coordinate	Net name
82	218.68	-2065.9	VDDAMP
83	115.11	-2065.9	DATA1N
84	11.54	-2065.9	DATA1P
85	-92.03	-2065.9	DGND
86	-195.6	-2065.9	LDO2V4
87	-299.17	-2065.9	VDDAMP
88	-402.74	-2065.9	RCALIB
89	-506.31	-2065.9	DGND
90	-609.88	-2065.9	VCORE
91	-713.45	-2065.9	AGND
92	-817.02	-2065.9	AGND
93	-920.59	-2065.9	NC
94	-1081.63	-2065.9	NC
95	-1185.2	-2065.9	DGND
96	-1288.77	-2065.9	AGND
97	-1451.06	-2065.9	VCORE
98	-1601.12	-2065.9	VANA
99	-1705.9	-1969.53	AGND
100	-1705.9	-1808.5	VCPNEG_IN
101	-1705.9	-321.68	VCPNEG_OUT
102	-1705.9	-218.11	AGND
103	-1705.9	-114.54	DGND
104	-1705.9	-10.97	VANA
105	-1705.9	92.6	VANA
106	-1705.9	196.17	NC
107	-1705.9	299.74	NC
108	-1705.9	403.31	NC
109	-1705.9	506.88	VCORE
110	-1705.9	610.45	AGND
111	-1705.9	1498.25	VCPPOS_IN
112	-1705.9	1601.82	VCORE
113	-1705.9	1705.38	VANA
114	-1705.9	1808.95	AGND
115	-1705.9	1959.04	VANA

6 Application schematic

6.1 Additional components

Dedicated additional capacitors are required to complete the circuit. These are listed in Table 7. Capacitor needs below. The capacitors should be selected to maintain their capacitance value within the indicated tolerance over the full range of maximum voltages, operating temperatures, and aging.

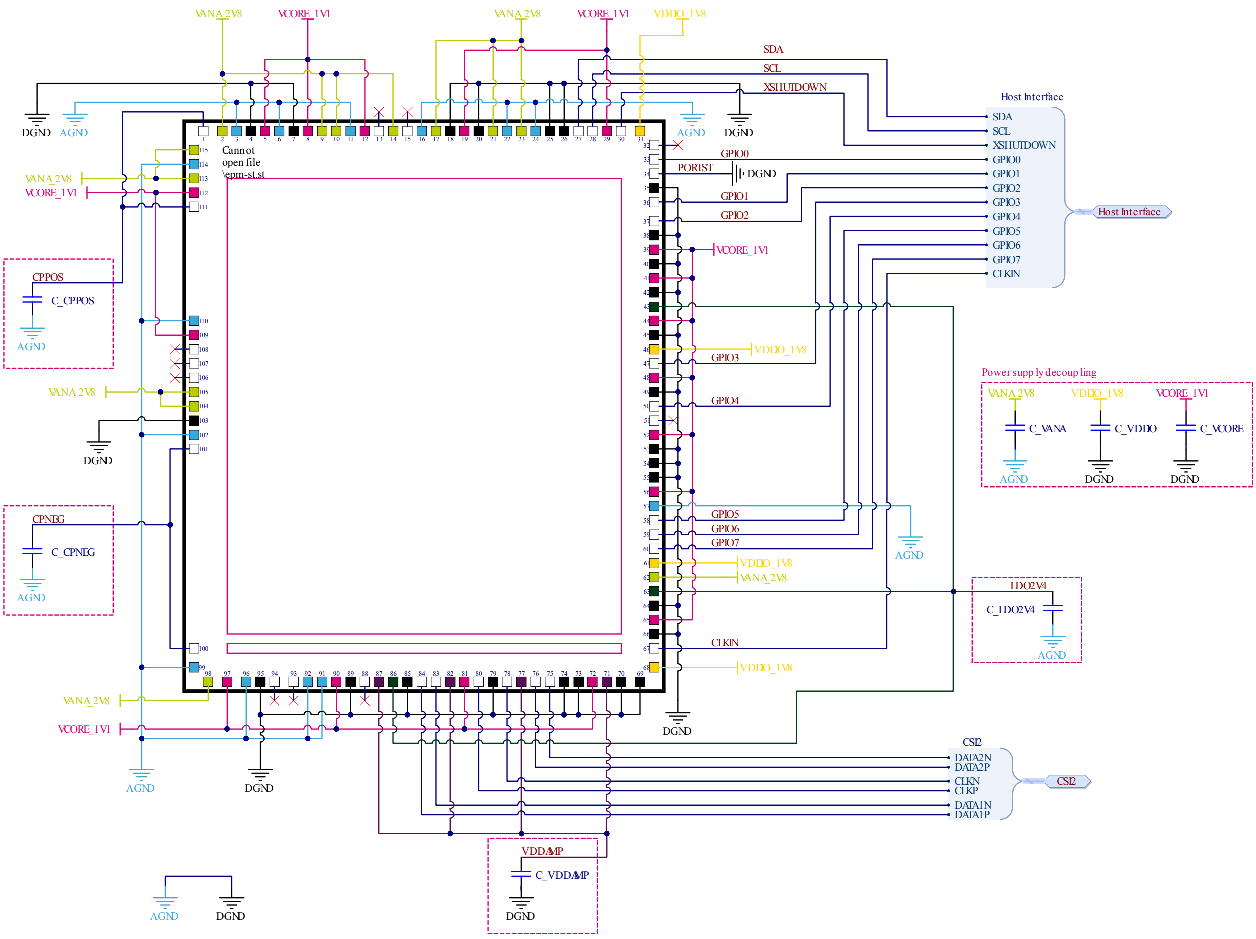
Capacitor values are based on capacitor positions (embedded in the camera module or external to the camera module).

External capacitors are required to properly filter out supply noise. Optimal reference in terms of value and size is subject to application board architecture and topology. The external capacitor values provided in the table below may be increased to compensate real supply noise.

Table 7. **Capacitor needs**

Associated pin name	Capacitor position	Typical voltage	Minimum capacitance	Typical capacitance	Maximum capacitance	Operating frequencies	Capacitor ground	Purpose
CPPOS_IN, CPPOS_OUT	Embedded	3.55 V	330 nF	470 nF	560 nF	160 MHz	AGND	CP tank capacitor
CPNEG_IN, CPNEG_OUT	Embedded	-2.0 V	650 nF	0.88 µF	1.04 µF	160 MHz	AGND	CP tank capacitor
VDDIO	Embedded	1.8 V				1 MHz	DGND	Supply decoupling
	External		1 µF					
VCORE	Embedded	1.15 V	470 nF			800 MHz 1 GHz - 1.5 GHz 160 MHz - 200 MHz	DGND	Supply decoupling
	External		10 µF				DGND	Supply decoupling
VANA	Embedded	2.8 V	100 nF			160 MHz	AGND	Supply decoupling
	External		10 µF					
LDO2V4	Embedded	2.4 V	100 nF		1 µF	DC	AGND	LDO capacitor
VDDAMP	Embedded	1.15 V	100 nF		1 µF	1.5 GHz	DGND	Supply decoupling

Figure 11. Application schematic



6.2 Layout guidelines

For good PCB design practice, observe the following image sensor layout:

- Use power and ground planes to supply power to the sensor.
- Join grounds i.e. join AGND and DGND into one single, solid GND plane underneath the sensor.
- Connect this GND plane to the sensor pins with one via per GND pin.
- To minimize risk of emissions, shield all vias and tracks attached to supplies by their respective GND nets.
- Maximize copper fill on the power planes near the sensor and use vias to improve heat transfer from the sensor. Consider including additional heatsinks close to the sensor if it is to be used at high temperatures.
- Route the high-speed signal pairs of the MIPI CSI-2 interface with balanced and controlled impedance differential traces (50 Ω single-ended impedance, 100 Ω differential impedance). This is a requirement for high-speed signaling. Route each pair together and match them in length to target a maximum 10 ps skew.

VCPNEG_IN and VCPNEG_OUT must be connected together with a short track. The required decoupling capacitor shall be placed on this path and not on an isolated track.

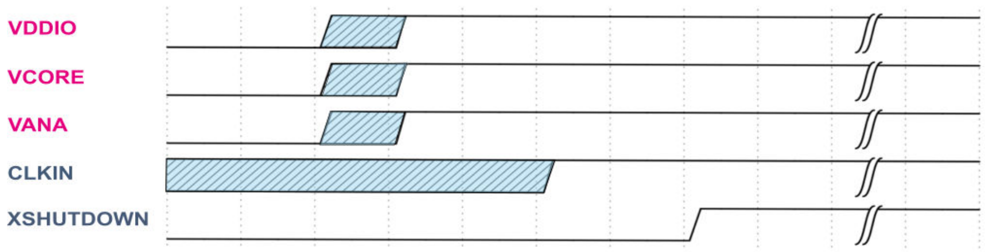
VCPPOS_IN and VCPPOS_OUT must be connected together with a short track. The required decoupling capacitor shall be placed on this path and not on an isolated track.

6.3 Device power up sequence

To power on the device:

- Provide all the external supplies (VCORE, VDDIO, VANA) according to the device characteristics described in Section 8: Electrical characteristics. As long as XSHUTDOWN is low, the device is in HW_STANDBY state.
- You can switch on the external supplies and CLKIN in any order.
- Set XSHUTDOWN to high.

Figure 12. Power up sequence



The device has power-on-reset (POR) detection cells with hysteresis on VCORE and VDDIO power supplies. POR is released after a typical delay of 20 µs on the rising edge.

Bursts with a duration of less than 2 µs (typical) are ignored.

Table 8. POR typical threshold

Supply	POR typical threshold rising edge (V)	POR typical threshold falling edge (V)
VCORE	0.65	0.55
VDDIO	1.1	0.95

6.4 Device power down sequence

The power down sequence must be done as follows:

1. If the sensor is in STREAMING state, then set it to SW_STANDBY state and wait for the command to complete.
2. Set XSHUTDOWN to low.
3. External supplies can be switched off in any order, as well as CLKIN.

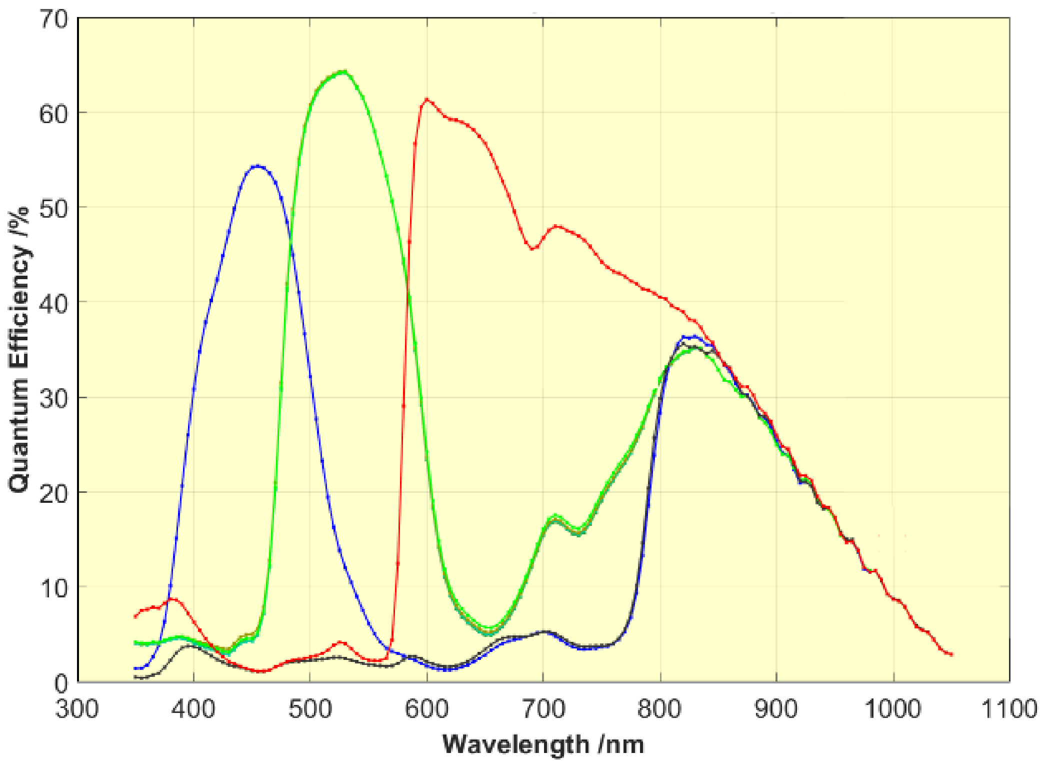
7 Pixel performance

The information listed in this section is for typical parts at ambient temperature (Tj = 40°C).

7.1 Quantum efficiency

Quantum efficiency (QE) is the percentage of incident photons converted into electrons.

Figure 13. VD16GZ QE



7.2 MTF

The modulation transfer function (MTF) measures the ability of the device to differentiate spatial frequencies. The MTF value represents the contrast restitution for the corresponding spatial frequency. In other words, it describes the contrast attenuation. It is a sharpness indicator that quantifies to what extent the image sensor can capture and discriminate tiny detailed contrast of an object in the field of view.

The figure below presents the on-axis MTF, measured in a 100x100 pixel ROI using the slanted-edge method, following ISO12233 sfrmat5. Note that in the following figure, Ny is the spatial Nyquist frequency.

Figure 14. On-axis vertical and horizontal pixel MTF @ 532 nm

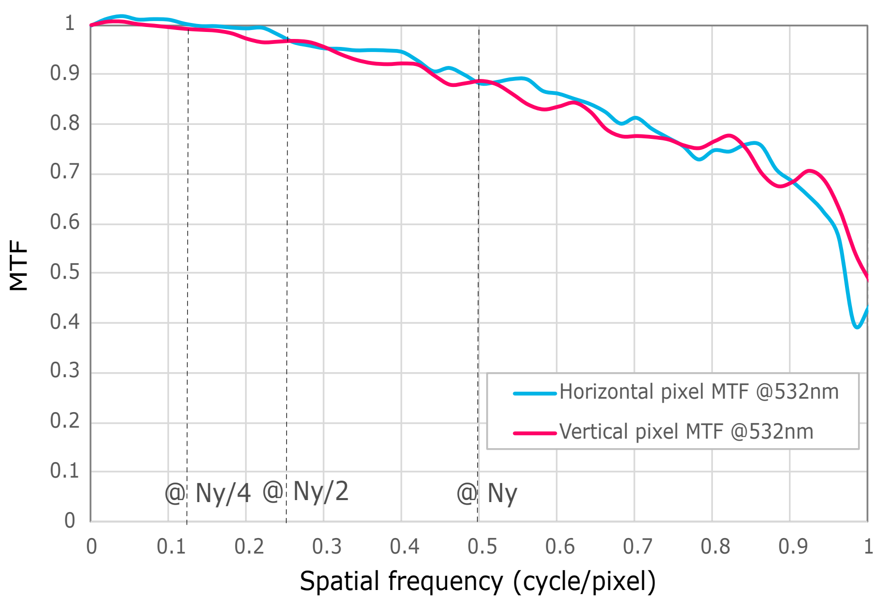
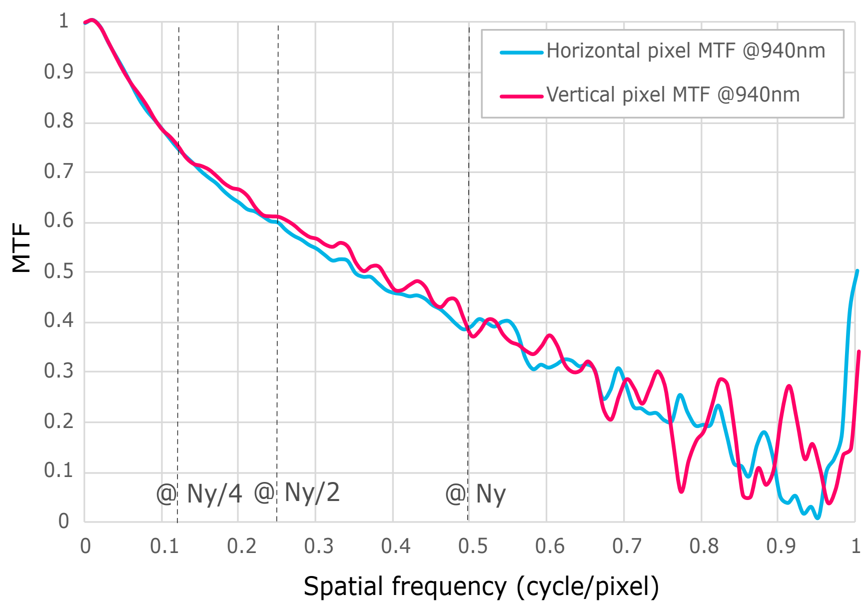


Figure 15. On-axis vertical and horizontal pixel MTF @ 940 nm



7.3 Color pattern

The VD16GZ is a color and NIR image sensor featuring a 4x4 pattern that is sensitive to red, green, blue and NIR (see figure below).

Figure 16. **VD16GZ 4x4 pattern**

7.4 Microlenses and CRA matching

Each pixel of the matrix has its own microlens covering it.

The purpose of the microlens is to concentrate and optimize photon capture by passing through the module lens down to the photo diode to increase sensor light sensitivity and to maximize the amount of light received by each pixel.

The light beam has an incidence angle change when passing through the module lens, increasing from center to periphery. This is the chief ray angle (CRA).

To compensate for the change of CRA over the matrix, the microlens position over the pixels progressively shifts from matrix center to matrix borders.

The design of the sensor microlens shift is optimized for matching a lens with CRA of 30° at corners and follows a linear shift shape.

It is recommended to match the CRA of the lens with the CRA of the image sensor to maximize image quality. Featuring advanced BSI pixel technology, the VD16GZ provides high relative illumination (RI) uniformity up to the image corners, which enables users to select lenses with different CRA with limited impact.

The following figure presents the CRA tolerance range in lens selection for maintaining a RI uniformity over 90% across the image.

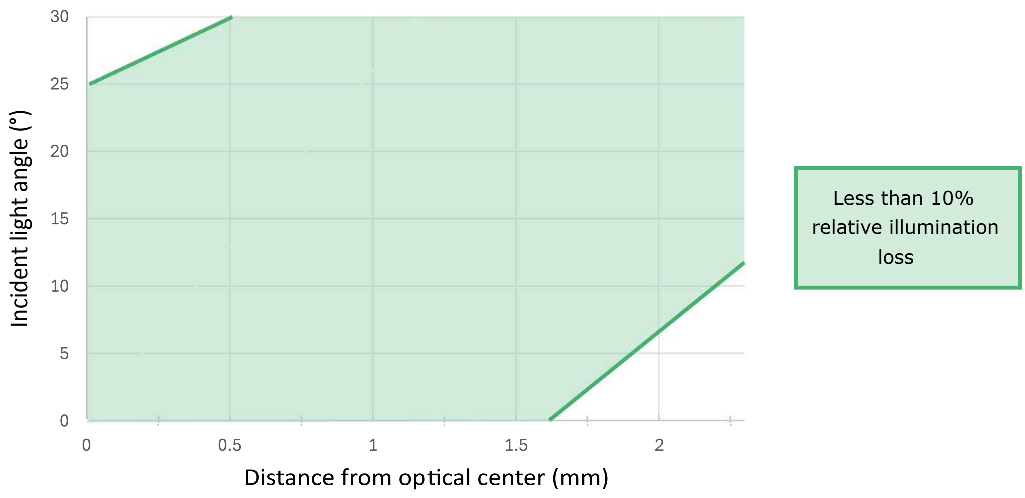


Figure 17. Guideline for lens CRA matching

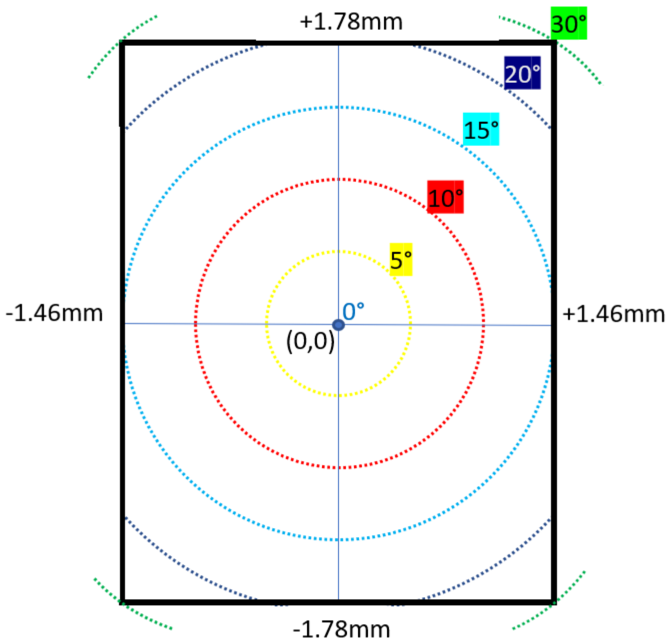


Figure 18. Co-centric pixel microlens CRA shift

8 Electrical characteristics

The electrical characteristics have been measured under the following typical conditions:

- Full resolution (1124 x 1364)
- 60 fps
- Nominal power supply levels
- External clock at 12 MHz
- Junction temperature at 60°C
- Nominal voltage

8.1 Absolute maximum ratings

Caution: Stresses above those listed under "Absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 9. Absolute maximum ratings

Symbol	Parameter	Max	Unit
VDDIO	Digital I/O power supply	2.5	V
VANA	Analog power supply	3.5	V
VCORE	Digital core power supply	1.4	V
VESD, electrostatic discharge model	Human body model (HBM)	±2	kV
	Charge device model (CDM)	±500	V

8.2 Operating conditions

Table 10. Operating conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
VDDIO	Digital IO power supply	1.7	1.8	1.9	V
VANA	Analog power supply	2.65	2.8	2.95	
VCORE	Digital core power supply	1.08	1.15	1.26	
Temperature					
T JF	Junction temperature (functional operation)	-30	—	85	°C

8.3 Power consumption

Table 11. Typical power consumption

Values below are measured for the conditions listed in Section 8: Electrical characteristics, but they also include process variability.

State	VDDIO (nominal)			VCORE (nominal)			VANA (nominal)			Unit	Total power		
	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		Typ.	Max.	Unit
Reset	0.0075	0.013	0.017	0.2	2.1	6.5	0.028	0.038	0.05		2.5	—	
SW_STANDBY	0.0075	0.013	0.017	1	3.3	7.5	0.028	0.043	0.05		4	—	
Streaming image 60 fps	7.5	8.5	11.0	50	57	65	18	22.8	25	mA	145	—	mW
Leader mode 30 fps	—	6.8	—	—	49.5	—	—	17.4	—		120	—	
Follower mode 0 fps	—	5.5	—	—	43	—	—	13.5	—		97	—	

Table 12. Maximum supply consumption

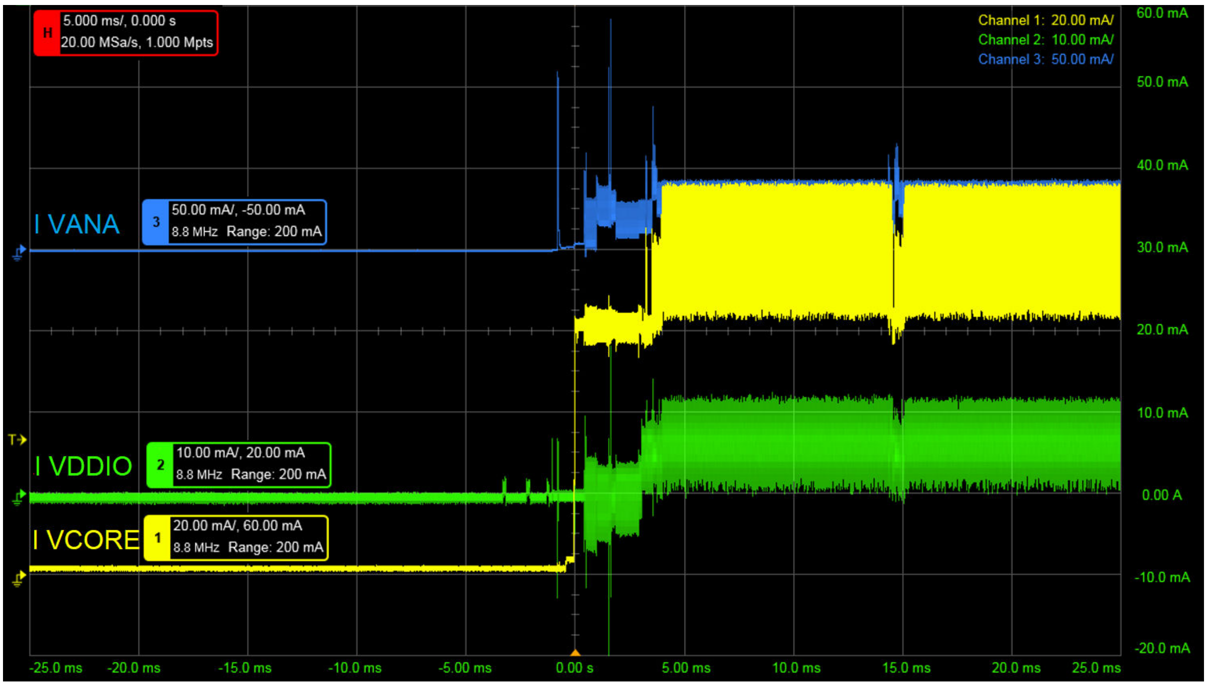
Values below are measured for the worst conditions of process, voltage, and temperature.

State	VDDIO (mA)	VCORE (mA)	VANA (mA)
SW_STANDBY	0.02	23	0.1
Streaming image 60 fps	11	86	25

8.3.1 Current profile

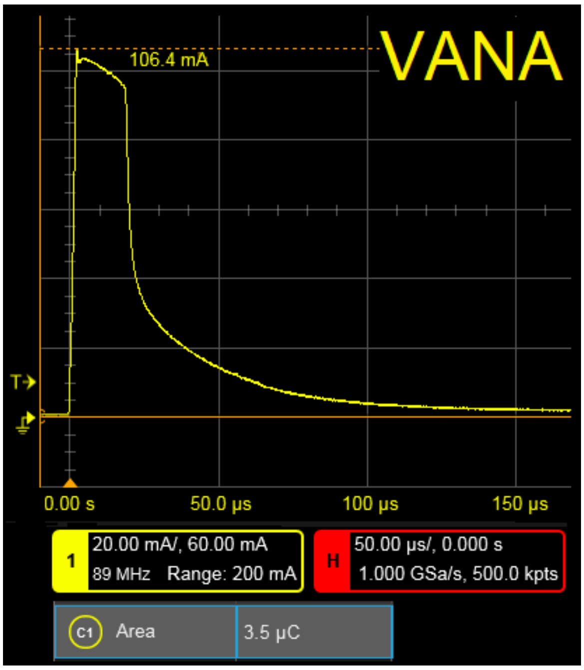
Figure 19 and Figure 20 are evaluated on one device.

Figure 19. Start streaming and the first frame of typical current profile (mA) over time (ms)



Note: Figure 19. Start streaming and the first frame of typical current profile (mA) over time (ms) is captured at maximum temperature and voltage.

Figure 20. Detail of VANA first transient pulse energy



8.4 CLKIN input

V_{CLKINL}, V_{CLKINH}, f_{CLKIN}, CtoCjitter, and Duty cycle are evaluated on a limited number of devices.

Table 13. Typical CLKIN input

The CLKIN input is for all voltage and temperature conditions.

Symbol	Parameter	Min.	Max.	Unit
V_{CLKINL}	DC-coupled square wave low-level input	-0.3	0.3 x VDDIO	V
V_{CLKINH}	DC-coupled square wave high-level input	0.7 x VDDIO	VDDIO + 0.3	
f_{CLKIN}	Clock input frequency	6	27	MHz
CtoCjitter	Clock maximum cycle-to-cycle jitter	—	200	ps
Duty cycle	Clock duty cycle	40	60	%
I_{CLKIN}	Input leakage current	—	10	µA

8.5 Digital inputs

Table 14. Digital inputs over process variations at 60°C

Symbol	Parameter	Min.	Max.	Unit
V_{IL}	Low-level input voltage	-0.3	0.3 x VDDIO	V
V_{IH}	High-level input voltage	0.7 x VDDIO	VDDIO + 0.3	
I_{Leak}	Input leakage current [1]	—	10	µA

1. *For 0 ≤ VI ≤ VDDIO*

8.6 Digital outputs

Table 15. Digital outputs

The digital outputs are over process variations at 60°C.

Symbol	Parameter	Conditions	Min.	Max.	Unit
V_{OL}	Low-level output voltage	IOL = -4 mA	—	0.4	V
V_{OH}	High-level output voltage	IOH = 4 mA	VDDIO - 0.4V	—	
I_{max}	Maximum current	—	—	4	mA

8.7 I²C interface - SDA, SCL

The I²C timing and voltage conform with the norm: UM10204-I2C-bus specification and user manual, Rev. 6, 4 April 2014.

8.8 CSI-2 interface

The CSI-2 interface conforms with the MIPI DPHY specification v1.1.

9 Package information

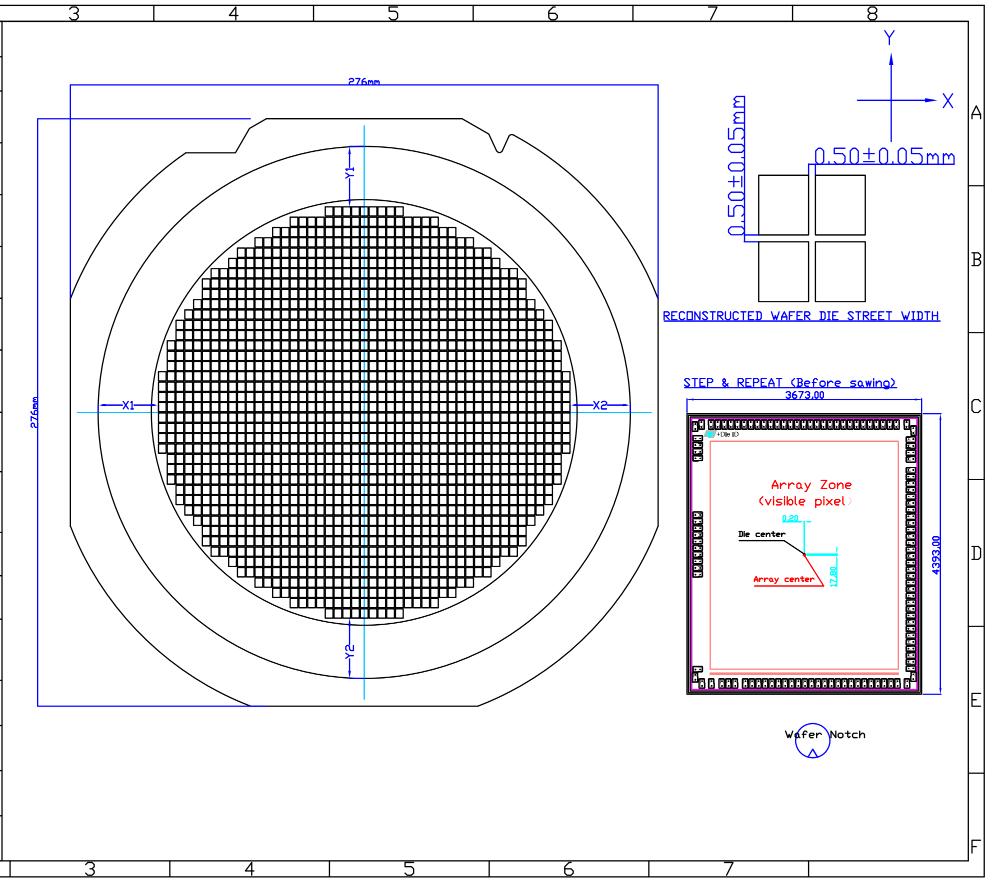
To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

9.1 Packing

Tested dice are delivered as sawn dice which are reconstructed into a wafer format on UV-tape, and delivered on a metallic ring (see figure below). The frames are packed in plastic containers, each including a maximum of 13 double-spaced reconstructed wafer rings. A mapping information file is also provided for localizing dice that may have been damaged during wafer reconstruction on sticking foil.

Figure 21. Reconstructed wafer information

FEATURE	DESCRIPTION
GRINDING THICKNESS	150um±7m
SINGULATED DIE SIZE	X=3648um±20um Y=4368um±20um
SCRIBE WIDTH	X=100um Y=100um
BOND PAD SIZE	141 x 75 um
BOND PAD OPENING	75x75um wire bond area
MINIMUM BOND PAD PITCH	103um
OPTICAL ARRAY (OPTICAL CENTER FROM DIE CENTER)	X=-0.2um Y=-17.8um
RECONSTRUCTED WAFER STREET WIDTH	500±50um
RW SIZE	≤200mm
RW OFFSET	(X1-X2)/2=0 ±5mm
	(Y1-Y2)/2=0 ±5mm
PLACEMENT ACCURACY X,Y,THETA	X,Y(±50um) Theta<1°
SHIPPING TAPE	UV TAPE (ADWILL D-175)
FILM FRAME	COMPACT DISCO STAINLESS SUS420
MAXIMUM TOTAL DIE COUNT	1460 EA
RW LAYOUT	X=47 Y=40



9.2 Storage information

Store all packing material in an appropriate indoor area. This is to prevent any dust and/or damage from the sun, external light, and physical shocks.

Keep the temperature between 15ºC and 35ºC.

Keep the relative humidity range between 10% and 70% maximum.

Store the reconstructed wafers under vacuum, in their original supplied sealed packing until they are used.

After the packing seal is broken, store the reconstructed wafers under nitrogen (N2) within dedicated closed shelves until they are processed.

Use the trace code to count the storage time. It is written on the package label.

The maximum storage time of the reconstructed wafer is:

- Six months from the trace code date. This is when the wafer is kept in the original sealed packing.
- One week from the trace code date. This is when the original packing seal is open.

The maximum storage time defines the maximum time that can be waited for reconstructed wafer processing. Processing may be for picking and placing, and module integration. If the maximm storage time is not respected, safe processing is not guaranteed.

Note: For further information on reconstructed wafer specifications for visual inspection and packing, refer to the technical note TN1497.

Revision history

Table 16. Document revision history

Date	Version	Changes
08-Dec-2022	1	Initial release
07-Oct-2024	2	First public release

Contents