400-mA Subminiature High-Efficiency Programmable DC-DC Converter With Linear Mode

Check for Samples: LM2608

FEATURES

- **Subminiature 10-Pin Thin DSBGA Package**
- **Only Four Tiny Surface-Mount External Components Required**
- **Uses Small Ceramic Capacitors**
- **Internal Soft Start**
- **Current and Thermal Shutdown Protection**
- **No External Compensation Required**

KEY SPECIFICATIONS

- **Operates from a Single Li-Ion Cell (2.8V to 5.5V)**
- **Pin Selectable Output Voltage (1.5V/1.8V or 1.3V/1.5V Versions), Without External Feedback Resistors**
- **400mA Maximum Load Capability**
- **±1% PWM Mode DC Output Voltage Precision (Excluding External Reference Tolerance)**
- **5mV typ PWM Mode Output Voltage Ripple**
- **20 µA typ Quiescent Current (Linear Mode)**
- **0.02µA typ Shutdown Mode Current**
- **Internal Synchronous Rectification for High Efficiency (91% at $2.8V_{IN}$, $1.8V_{OUT}$)**
- **600kHz PWM Mode Switching Frequency**
- **SYNC Input for PWM Mode Frequency Synchronization from 500kHz to 1MHz**
- **15% Accuracy for F_{OSC} and I_{lim}**

APPLICATIONS

- **Mobile Phones**
- **Hand-Held Radios**
- **Battery Powered Devices**

DESCRIPTION

The LM2608 step-down DC-DC converter is optimized for powering ultra-low voltage circuits from a single Lithium-Ion cell. It provides up to 400mA over an input voltage range of 2.8V to 5.5V. Operating from a 1.35V reference, this device provides pin-selectable output voltages of 1.3V/1.5V (300mA) for low voltage version or 1.5V/1.8V (400mA) for high voltage version. This allows adjustment for DSP or CPU voltage options, as well as dynamic output voltage switching for reduced power consumption. Internal synchronous rectification provides high efficiency.

Typical Application Circuit

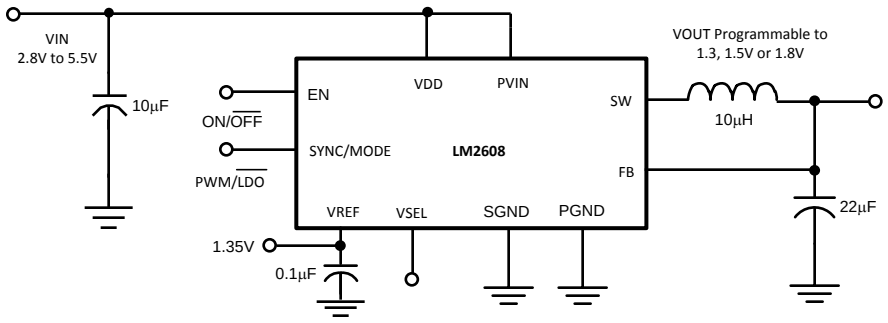

Figure 1. Application Circuit

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DESCRIPTION (CONTINUED)

The LM2608 offers superior features and performance for mobile phones and similar portable applications with complex power management systems. Pin-selectable PWM low-noise and linear micropower modes offer improved system control for maximizing battery life. During full power operation, fixed-frequency PWM mode reduces interference in RF and data acquisition applications by minimizing noise harmonics at sensitive IF and sampling frequencies. A SYNC input allows synchronizing the switching frequency in a range of 500kHz to 1MHz to avoid noise from intermodulation with system frequencies. Linear operation reduces quiescent current to 20µA (typ) during system standby for extended battery life. It provides up to 3 mA in the linear mode. Shutdown reduces battery consumption to 0.02µA (typ.).

The LM2608 is available in a 10 pin DSBGA package. This package uses wafer level chip-scale DSBGA technology and offers the smallest possible size. A high switching frequency (600KHz) allows use of tiny surface-mount components. Only four small external surface-mount components, an inductor and three ceramic capacitors are required. Pin selectable output voltage eliminates the need for bulky external feedback resistors.

Connection Diagrams

DSBGA Package

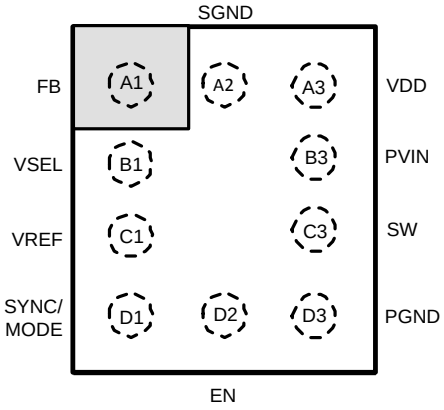


Figure 2. TOP VIEW

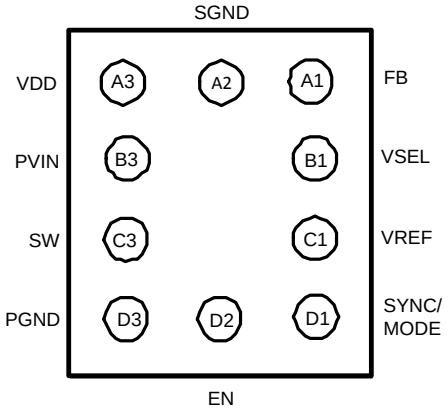


Figure 3. BOTTOM VIEW

ORDERING INFORMATION(1)(2)(3)

Part Number	Vout
LM2608ATL-1.3/NOPB	1.3V
LM2608ATL-1.8/NOPB	1.8V
LM2608ATLX-1.3/NOPB	1.3V
LM2608ATLX-1.8/NOPB	1.8V

(1) All devices have pin selection for 1.5V option.
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(3) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Pin Description

Pin Number(1)	Pin Name	Function
A1	FB	Feedback Analog Input. Connect to the output at the output filter capacitor (see Figure 4)
B1	VSEL	Output Voltage Selection Input. Set this digital input to: VDD for 1.8V output voltage (1.5V for LM2608ATL-1.3) SGND for 1.5V output voltage (1.3V for LM2608ATL-1.3)
C1	VREF	External Reference Input. Drive this analog input with a 1.35V reference to set the output voltage. The LM2608 uses an internal reference while in LDO mode.(2)
D1	SYNC/MODE	Synchronization Input. Use this digital input for frequency synchronization or mode control. Set: SYNC/MODE = high for low-noise 600kHz PWM mode SYNC/MODE = low for low-current LDO mode SYNC/MODE = 500kHz - 1MHz external clock for synchronization to an external clock in PWM mode. See *Synchronization and Operating Modes* in the *Device Information* section.
D2	EN	Enable Input. Set this Schmitt trigger digital input high for normal operation.
D3	PGND	Power Ground
C3	SW	Switching Node connection to the internal PFET switch and NFET synchronous rectifier. Connect to an inductor with a saturation current rating that exceeds the max. Switch Peak Current Limit specification of the LM2608 (see Figure 4)
B3	PVIN	Power Supply Input to the internal PFET switch. Connect to the input filter capacitor (see Figure 4).
A3	VDD	Analog Supply Input. If board layout is not optimum, an optional 0.1µF ceramic capacitor is suggested (see Figure 4)
A2	SGND	Analog and Control Ground

(1) Note that the pin numbering scheme for the DSBGA package was revised in April,2002 to conform to JEDEC standard. Only the pin numbers were revised. No changes to the physical location of the inputs/outputs were made. For reference purpose, the obsolete numbering had FB as pin 1, VSEL as pin 2, VREF as pin 3, SYNC as pin 4, EN as pin 5, PGND as pin 6, SW as pin 7, PVIN as pin 8, VDD as pin 9 and SGND as pin 10.
(2) The LM2608 PWM mode output voltage precision is ±1% when operating from an external 1.35V reference voltage.

Absolute Maximum Ratings(1)(2)

PVIN, VDD, to SGND	−0.2V to +6V
PGND to SGND	−0.2V to +0.2V
EN, SYNC/MODE, VSEL to SGND	−0.2V to +6V
FB, SW	(GND −0.2V) to (VDD +0.2V)
Storage Temperature Range	−45°C to +150°C
Lead temperature (Soldering, 10 sec.)	260°C
Junction Temperature(3)	−25°C to 125°C
Minimum ESD Rating, Human body model, C = 100pF, R = 1.5 kΩ	±2.0kV
Thermal Resistance (θ_{JA})(4)	140°C/W

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings are conditions for which the device is intended to be functional, but parameter specifications may not be ensured. For ensured specifications and associated test conditions, see the Min and Max limits and Conditions in the Electrical Characteristics table. Electrical Characteristics table limits are ensured by production testing, design or correlation using standard Statistical Quality Control methods. Typical (Typ) specifications are mean or average values from characterization at 25°C and are not specified.
(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.
(3) Thermal shutdown will occur if the junction temperature exceeds the 150°C maximum junction temperature of the device.
(4) Thermal resistance specified with 2 layer PCB(0.5/0.5 oz. cu).

Electrical Characteristics

Specifications with standard typeface are for $T_A = T_J = 25°C$, and those in **bold face type** apply over the full Operating Temperature Range ($T_A = T_J = -25°C$ to $+85°C$). Unless otherwise specified, PVIN = VDD = EN = SYNC = 3.6V, VSEL = 0V, VREF = 1.35V.

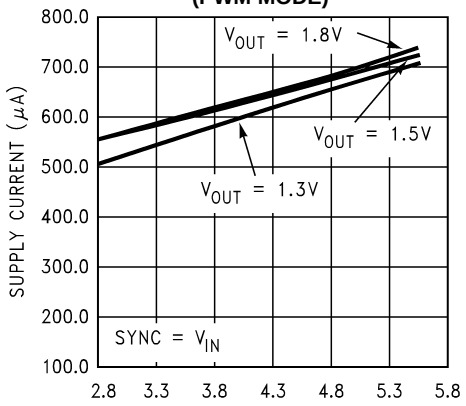
Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{IN}	Input voltage range (1)	PVIN = VDD, VSEL = V_{IN}	2.8		5.5	V
V_{FB}	Feedback voltage PWM mode SYNC/MODE = V_{IN} (2)	LM2608ATL-1.3, VSEL = 0V	**1.287**	1.30	**1.313**	V
		LM2608ATL-1.3, VSEL = V_{IN}	**1.485**	1.50	**1.515**	
		LM2608ATL-1.8, VSEL = 0V	**1.485**	1.50	**1.515**	
		LM2608ATL-1.8, VSEL = V_{IN}	**1.782**	1.80	**1.818**	
$V_{FB, LIN}$	Feedback voltage LIN mode (SYNC/MODE =0V) V_{IN}= 3.6V I_{OUT} = 100µA	LM2608ATL-1.3, VSEL = 0V	**1.261**	1.30	**1.339**	V
		LM2608ATL-1.3, VSEL = V_{IN}	**1.455**	1.50	**1.545**	
		LM2608ATL-1.8, VSEL = 0	**1.455**	1.50	**1.545**	
		LM2608ATL-1.8, VSEL = V_{IN}	**1.746**	1.80	**1.854**	
ΔV_{OUT_LDO}	Line regulation	I_{OUT} = 100µA		0.1		%/V
	Load regulation	V_{IN}= 3.6V, I_{OUT} = 10µA to 1.5mA		1.0		%/mA
V_{HYST}	OVP comparator hysteresis voltage (3)	PWM Mode		45	**75**	mV
I_{SHDN}	Shutdown supply current	EN = 0V		0.02	**3**	µA
$I_{Q, PWM}$	DC bias current into VDD (PWM mode)	FB = 2V SYNC/MODE =V_{IN}		590	**725**	µA
$I_{Q, LIN}$	DC bias current into VDD (LDO mode)	SYNC/MODE = 0V, I_{OUT} = 0 mA		20	**30**	
$R_{DSON (P)}$	Pin-pin resistance for PFET			370	500	mΩ
$R_{DSON (N)}$	Pin-pin resistance for NFET			330	500	mΩ
$R_{DSON , TC}$	FET resistance temperature coefficient			0.5		%/C
$I_{SC, LDO}$	Short circuit (LDO)	V_{OUT} = GND SYNC/MODE = 0V	**3**	6	**8**	mA
I_{lim}	Switch peak current limit (4)	LM2608ATL-1.3	**383**	460	**518**	mA
		LM2608ATL-1.8	**510**	620	**690**	
V_{EN_H}	EN positive going threshold voltage (5)			0.80	**1.3**	V
V_{EN_L}	EN negative going threshold voltage (5)		**0.4**	0.75		V
V_{SYNC_H}	SYNC/MODE positive going threshold voltage			0.85	**1.3**	V
V_{SYNC_L}	SYNC/MODE negative going threshold voltage		**0.4**	0.80		V
V_{SEL_H}	V_{SEL} positive going threshold voltage			0.80	**1.3**	V
V_{SEL_L}	V_{SEL} negative going threshold voltage		**0.4**	0.75		V
I_{SEL}	VSEL pulldown current	VSEL = 1.2V		0.70	**2**	µA
I_{REF}	Input current into VREF pin			15	**150**	nA
f_{sync}	SYNC/MODE clock frequency range (6)		**500**		**1000**	kHz
F_{OSC}	Internal oscillator frequency	LM2608ATL-1.3/1.8, PWM Mode	**510**	610	**690**	kHz
T_{min}	Minimum ON-Time of PFET switch in PWM mode			200		ns

(1) The LM2608 is designed for cell phone applications where turn-on after system power-up is controlled by the system processor and internal UVLO (Under Voltage LockOut) circuitry is unnecessary. The LM2608 has no UVLO circuitry and should be kept in shutdown by holding the EN pin low until the input voltage exceeds 2.8V. Although the LM2608 exhibits safe behavior while enabled at low input voltages, this is not specified.
(2) The LM2608 PWM mode output voltage precision is ±1% when operating from an external 1.35V reference voltage.
(3) The hysteresis voltage is the minimum voltage swing on FB that causes the internal feedback and control circuitry to turn the internal PFET switch on and then off, during test mode.
(4) Current limit is built-in, fixed, and not adjustable. If the current limit is reached while the output is pulled below about 0.7V, the internal PFET switch turns off for 2.5 µs to allow the inductor current to diminish.
(5) EN is a Schmitt trigger digital input with logic thresholds that are independent of supply voltage at the VDD pin.
(6) SYNC driven with an external clock switching between VDD and GND. When an external clock is present at SYNC, the IC is forced into PWM mode at the external clock frequency. The LM2608 synchronizes to the rising edge of the external clock.

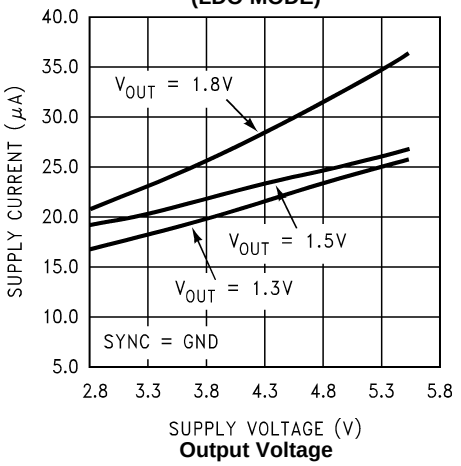
Typical Operating Characteristics

LM2608ATL, Circuit of Figure 4, V_{IN} = 3.6V, T_A = 25°C, L_1 = 10 µH, unless otherwise noted.

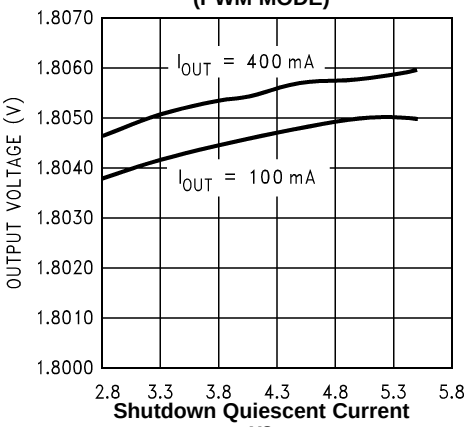
Quiescent Supply Current vs Supply Voltage (PWM MODE)



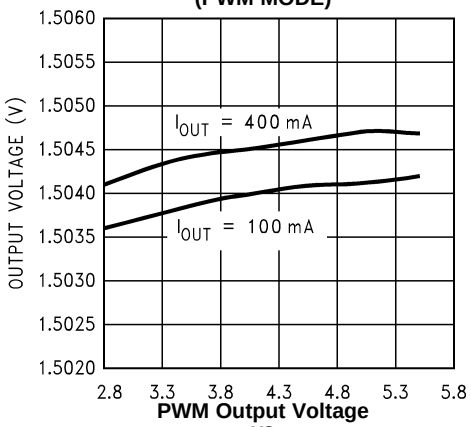
Quiescent Supply Current vs Supply Voltage (LDO MODE)



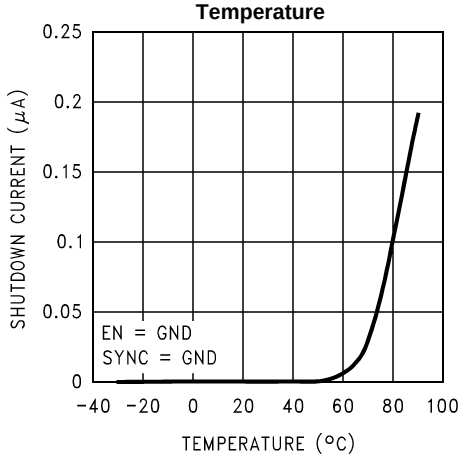
Output Voltage vs Supply Voltage (PWM MODE)



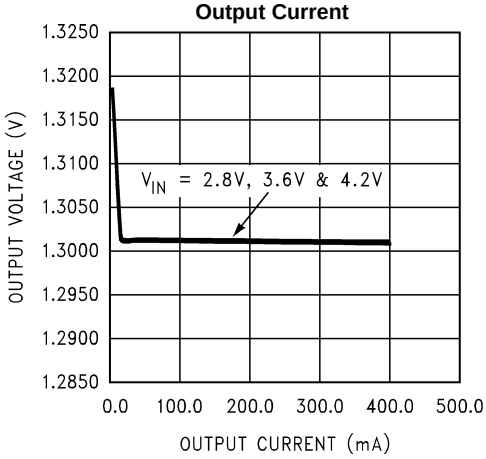
Output Voltage vs Supply Voltage (PWM MODE)



Shutdown Quiescent Current vs Temperature



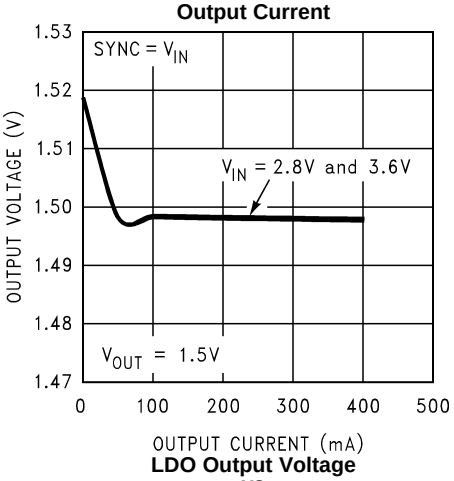
PWM Output Voltage vs Output Current



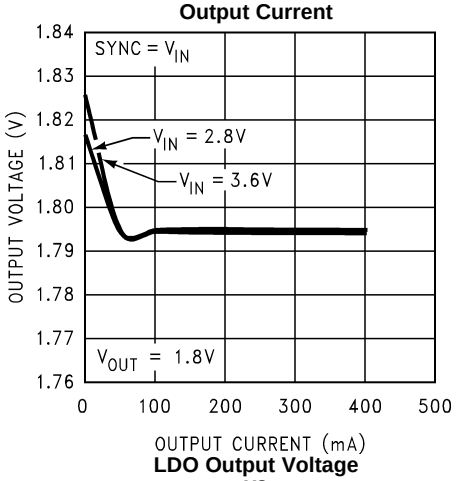
Typical Operating Characteristics (continued)

LM2608ATL, Circuit of Figure 4, V_{IN} = 3.6V, T_A = 25°C, L_1 = 10 µH, unless otherwise noted.

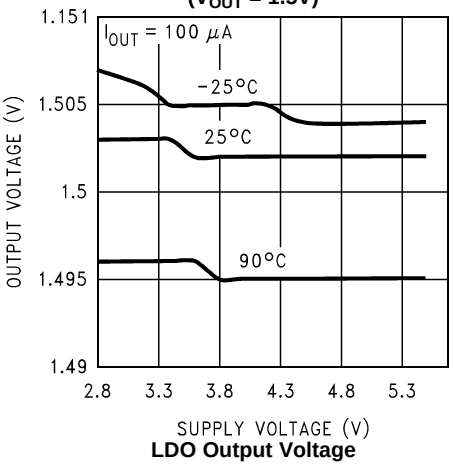
PWM Output Voltage vs Output Current



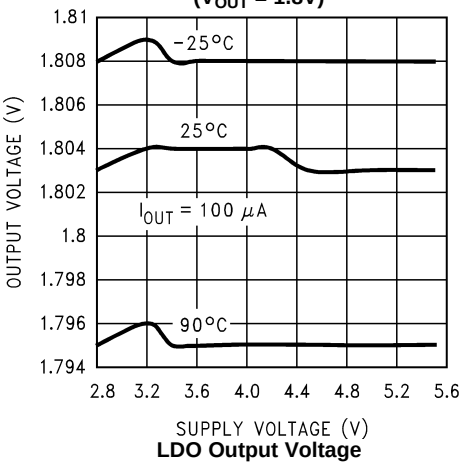
PWM Output Voltage vs Output Current



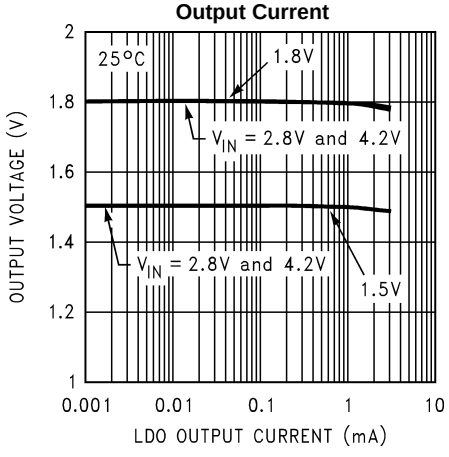
LDO Output Voltage vs Supply Voltage (V_{OUT} = 1.5V)



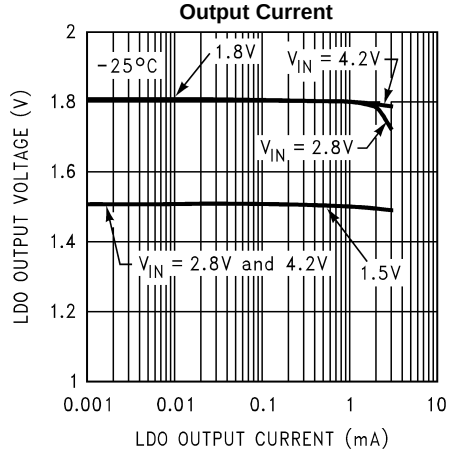
LDO Output Voltage vs Supply Voltage (V_{OUT} = 1.8V)



LDO Output Voltage vs Output Current



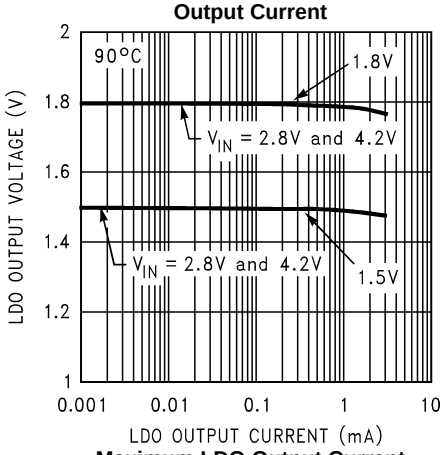
LDO Output Voltage vs Output Current



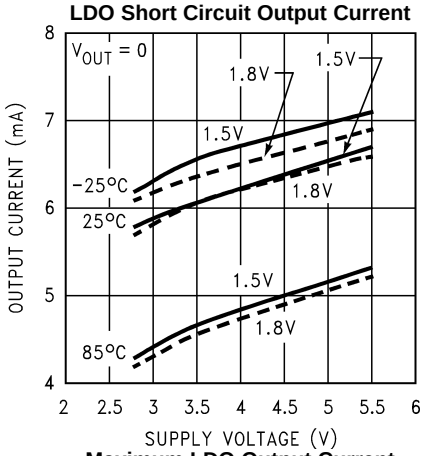
Typical Operating Characteristics (continued)

LM2608ATL, Circuit of Figure 4, V_{IN} = 3.6V, T_A = 25°C, L_1 = 10 µH, unless otherwise noted.

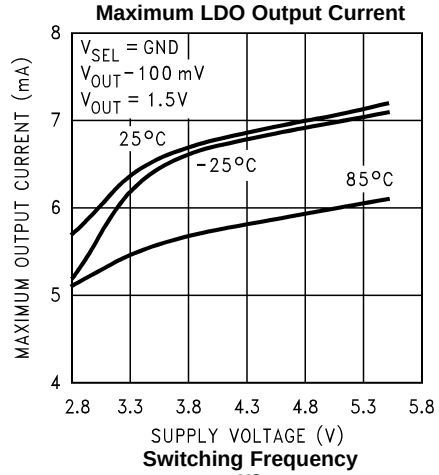
LDO Output Voltage vs Output Current



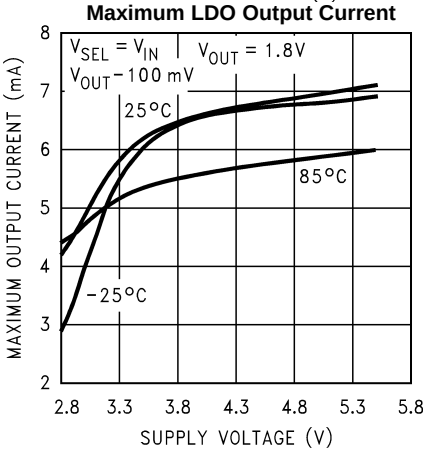
LDO Short Circuit Output Current



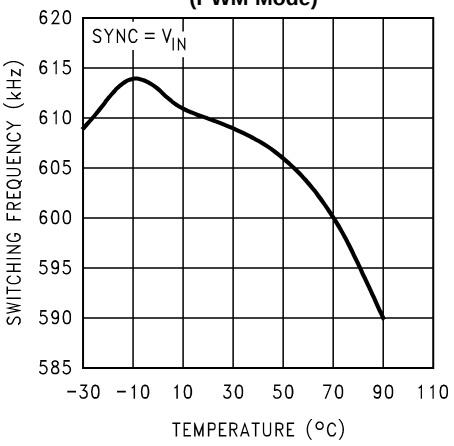
Maximum LDO Output Current



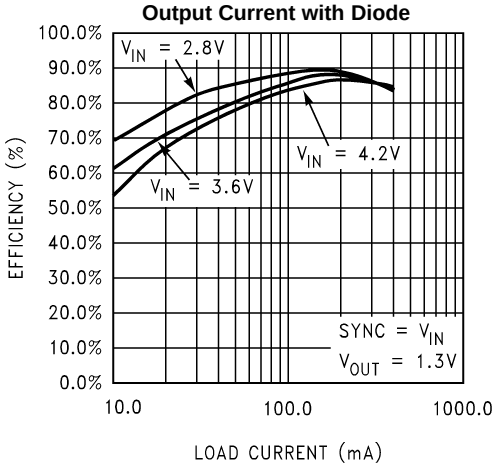
Maximum LDO Output Current



Switching Frequency vs Temperature (PWM Mode)



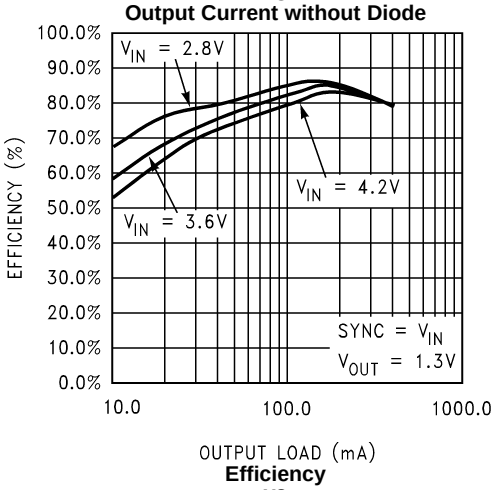
Efficiency vs Output Current with Diode



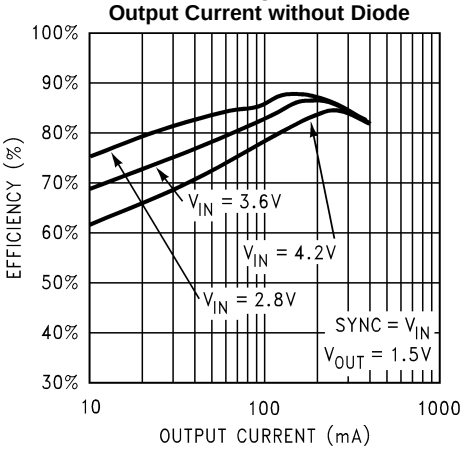
Typical Operating Characteristics (continued)

LM2608ATL, Circuit of Figure 4, V_{IN} = 3.6V, T_A = 25°C, L_1 = 10 µH, unless otherwise noted.

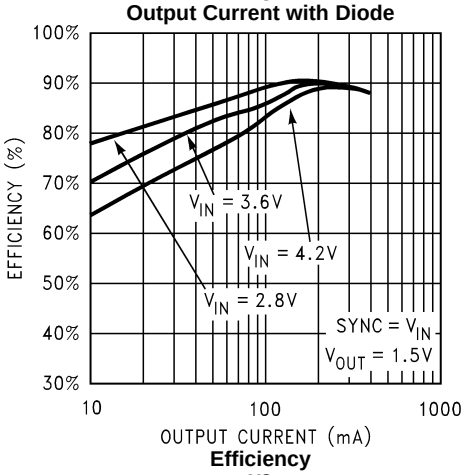
Efficiency vs Output Current without Diode



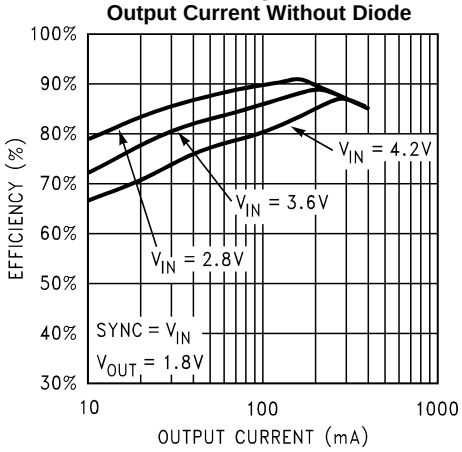
Efficiency vs Output Current without Diode



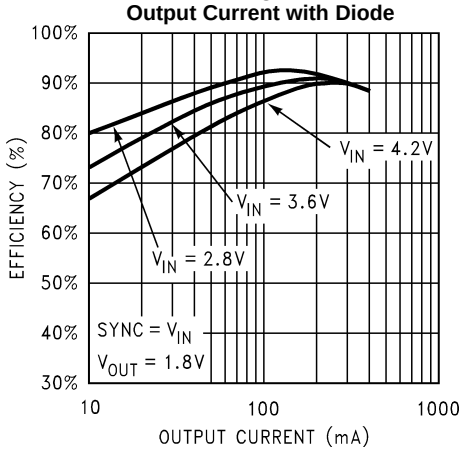
Efficiency vs Output Current with Diode



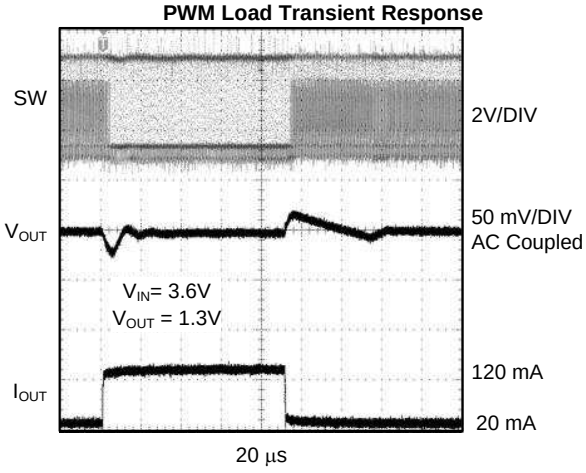
Efficiency vs Output Current Without Diode



Efficiency vs Output Current with Diode



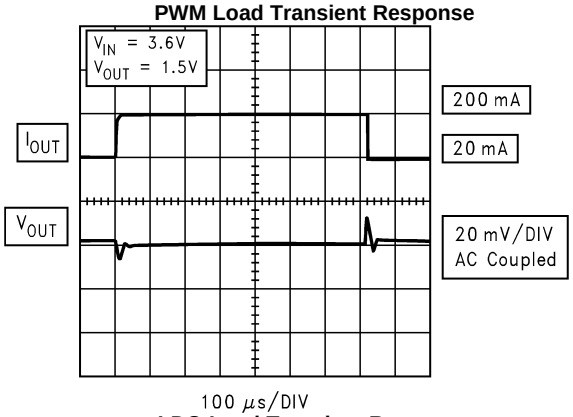
PWM Load Transient Response



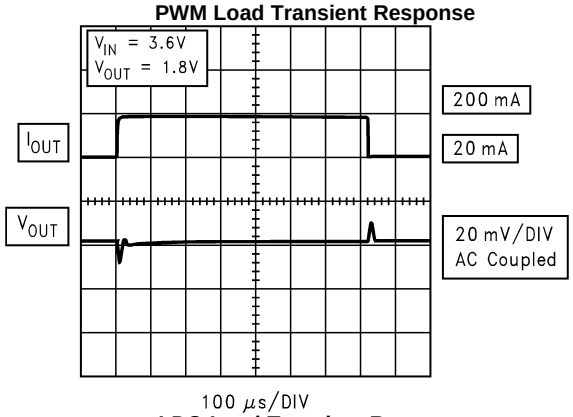
Typical Operating Characteristics (continued)

LM2608ATL, Circuit of Figure 4, V_{IN} = 3.6V, T_A = 25°C, L_1 = 10 µH, unless otherwise noted.

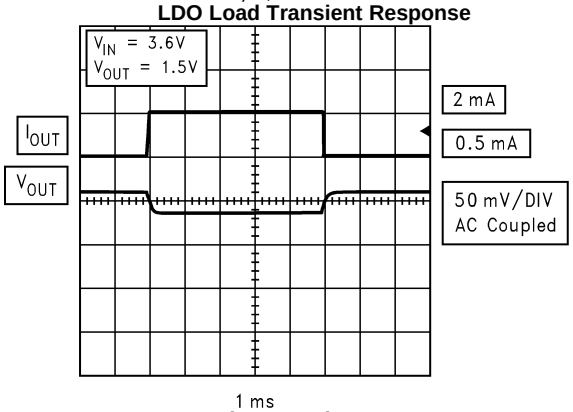
PWM Load Transient Response



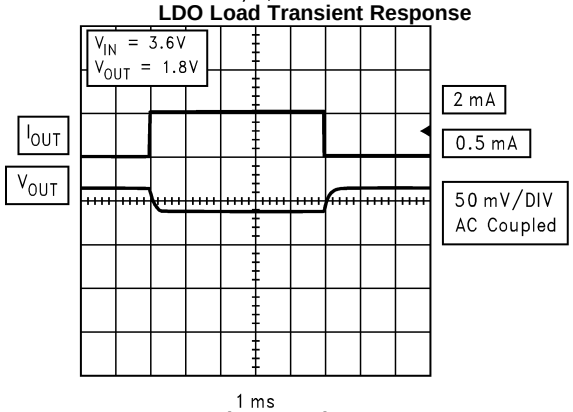
PWM Load Transient Response



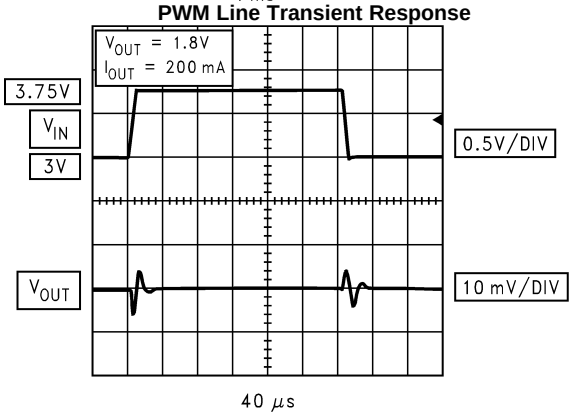
LDO Load Transient Response



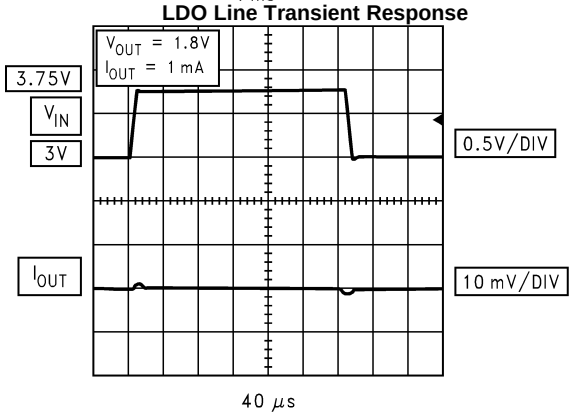
LDO Load Transient Response



PWM Line Transient Response



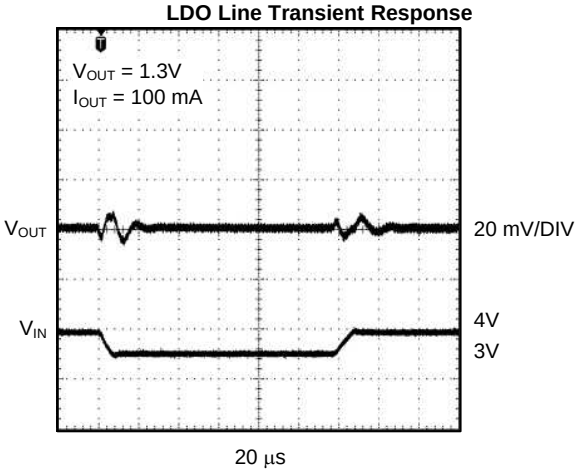
LDO Line Transient Response



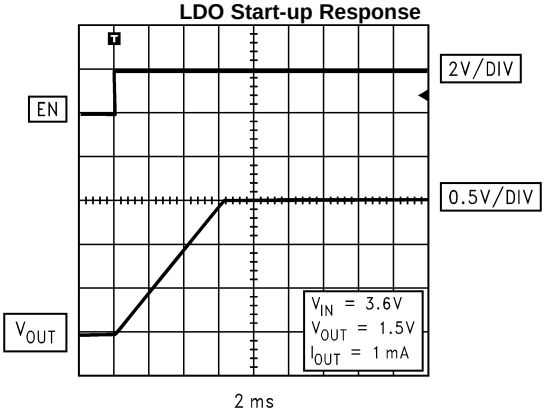
Typical Operating Characteristics (continued)

LM2608ATL, Circuit of Figure 4, V_{IN} = 3.6V, T_A = 25°C, L_1 = 10 µH, unless otherwise noted.

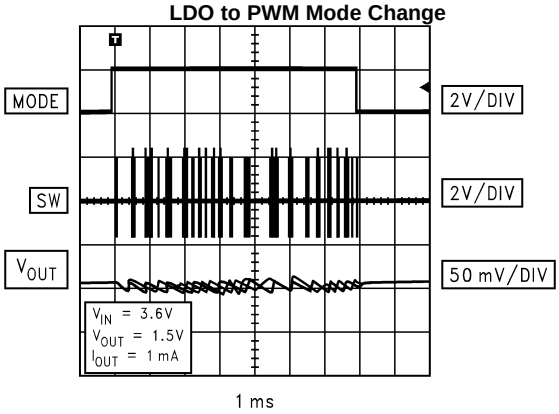
LDO Line Transient Response



LDO Start-up Response



LDO to PWM Mode Change



DEVICE INFORMATION

The LM2608 is an easy to use, step-down DC-DC converter optimized for powering low-voltage CPUs or DSPs in cell phones and other miniature battery powered devices. It provides pin-selectable output voltages of 1.3V, 1.5V or 1.8V from a single 2.8V to 5.5V Li-ion battery cell. It is designed for a maximum load capability of 400mA. It uses synchronous rectification in PWM mode for high efficiency, typically 91% for a 100mA load with 1.8V output, 2.8V input.

The device has all three of the pin-selectable operating modes required for cell phones and other complex portable devices. Such applications typically spend a small portion of their time operating at full power. During full power operation, synchronized or fixed-frequency PWM mode offers full output current capability while minimizing interference to sensitive IF and data acquisition circuits. These applications spend the remainder of their time in low-current standby operation or shutdown to conserve battery power. During standby operation, LDO mode reduces quiescent current to 20µA (typ.) to maximize battery life. Shutdown mode reduces battery consumption to 0.02µA (typ.).

The LM2608 offers good performance and a full set of features. It is based on a current-mode buck architecture with cycle-by-cycle current limiting. DC PWM mode output voltage precision is ±1%. The SYNC/MODE input accepts an external clock between 500kHz and 1MHz. The output voltage selection pin eliminates external feedback resistors. Additional features include soft-start, current overload protection, output over-voltage protection and thermal shutdown protection.

The LM2608 is constructed using a chip-scale 10-pin DSBGA package. The DSBGA package offers the smallest possible size for space critical applications, such as cell phones. Required external components are only a small 10µH inductor, and tiny 10µF, 22µF and 0.1µF ceramic capacitors for reduced board area.

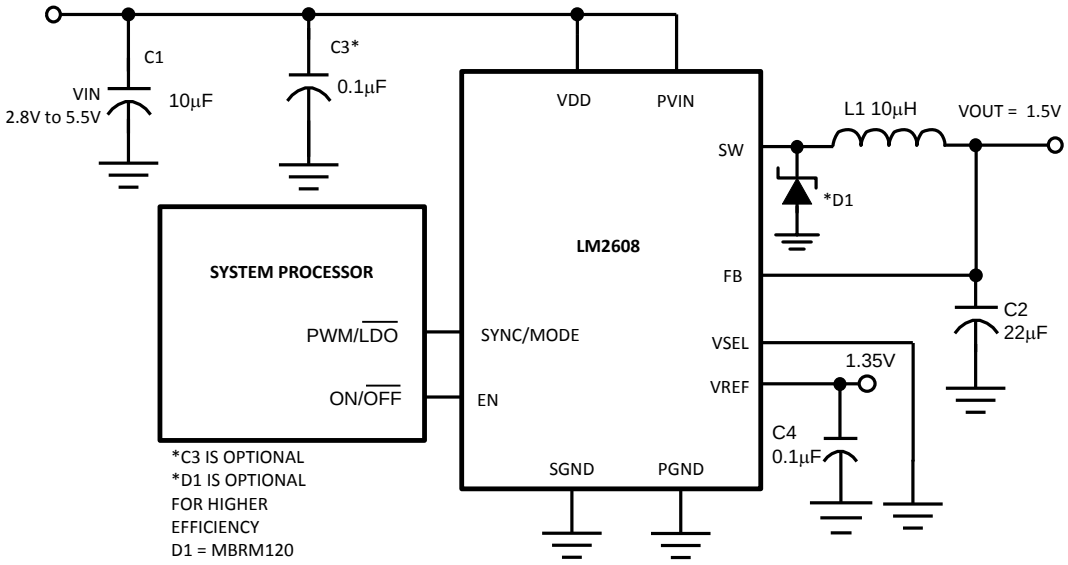


Figure 4. Typical Operating Circuit

Circuit Operation

Referring to Figure 4, Figure 5, and Figure 6 the LM2608 operates as follows: During the first part of each switching cycle, the control block in the LM2608 turns on the internal PFET switch. This allows current to flow from the input through the inductor to the output filter capacitor and load. The inductor limits the current to a ramp with a slope of $(V_{IN} - V_{OUT})/L$, by storing energy in a magnetic field. During the second part of each cycle, the controller turns the PFET switch off, blocking current flow from the input, and then turns the NFET synchronous rectifier on. In response, the inductor's magnetic field collapses, generating a voltage that forces current from ground through the synchronous rectifier to the output filter capacitor and load. As the stored energy is transferred back into the circuit and depleted, the inductor current ramps down with a slope of V_{OUT}/L. If the inductor current reaches zero before the next cycle, the synchronous rectifier is turned off to prevent current reversal. The output filter capacitor stores charge when the inductor current is high, and releases it when low, smoothing the voltage across the load.

The output voltage is regulated by modulating the PFET switch on-time to control the average current sent to the load. The effect is identical to sending a duty-cycle modulated rectangular wave formed by the switch and synchronous rectifier to a low-pass filter created by the inductor and output filter capacitor. The output voltage is equal to the average voltage at the SW pin.

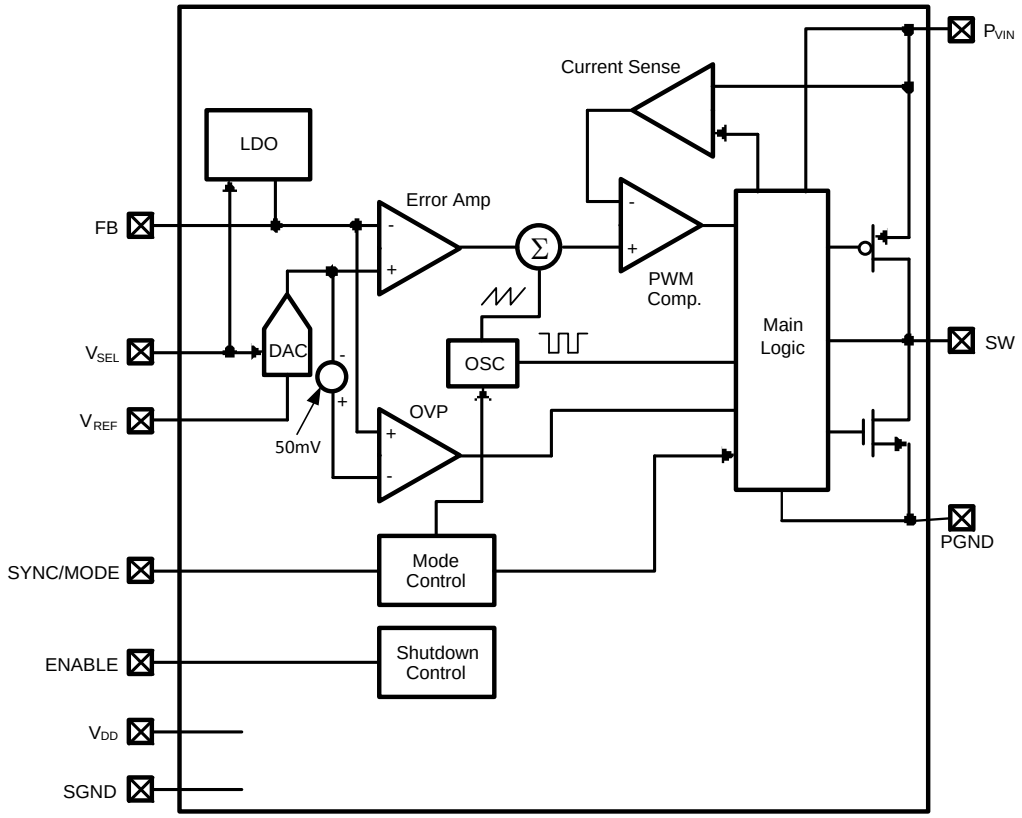


Figure 5. Simplified Functional Diagram

PWM Operation

The LM2608 can be set to current-mode PWM operation by connecting the SYNC/MODE pin to VDD. While in PWM (Pulse Width Modulation) mode, the output voltage is regulated by switching at a constant frequency and then modulating the energy per cycle to control power to the load. Energy per cycle is set by modulating the PFET switch on-time pulse-width to control the peak inductor current. This is done by controlling the PFET switch using a flip-flop driven by an oscillator and a comparator that compares a ramp from the current-sense amplifier with an error signal from a voltage-feedback error amplifier. At the beginning of each cycle, the oscillator sets the flip-flop and turns on the PFET switch, causing the inductor current to ramp up. When the current sense signal ramps past the error amplifier signal, the PWM comparator resets the flip-flop and turns off the PFET switch, ending the first part of the cycle. The NFET synchronous rectifier turns on until the next clock pulse or the inductor current ramps to zero. If an increase in load pulls the output voltage down, the error amplifier output increases, which allows the inductor current to ramp higher before the comparator turns off the PFET switch. This increases the average current sent to the output and adjusts for the increase in the load.

Before going to the PWM comparator, the current sense signal is summed with a slope compensation ramp from the oscillator for stability of the current feedback loop. During the second part of the cycle, a zero crossing detector turns off the NFET synchronous rectifier if the inductor current ramps to zero.

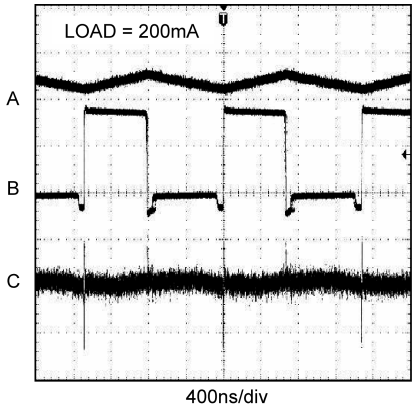


Figure 6. PWM Mode Switching Waveform

LDO Operation

Connecting the SYNC/MODE pin to SGND sets the LM2608 to Linear mode operation. While in LDO (Low Dropout regulator) mode, the output voltage is regulated by the internal LDO to supply up to 3mA. This is done by using an internal pass transistor and an error amplifier to sense the output voltage and maintain the desired output voltage. During LDO mode, the PFET and NFET network switch off to reduce quiescent current.

Operating Mode Selection (SYNC/MODE Pin)

The SYNC/MODE digital input pin is used to select between PWM and LDO operating modes. Set SYNC/MODE high (above 1.3V) for 600kHz PWM operation. Set SYNC/MODE low (below 0.4V) to select LDO mode to reduced current consumption when the system is in standby. The LM2608 has an over-voltage protection feature that may activate if the device is left in PWM mode under low-load conditions to prevent the output voltage from rising too high. See *Overvoltage Protection*, for more information.

Select modes with the SYNC/MODE pin using a signal with a slew rate faster than 5V/100µs. Use a comparator Schmitt trigger or logic gate to drive the SYNC/MODE pin. Do not leave the pin floating or allow it to linger between logic levels. These measures will prevent output voltage errors that could otherwise occur in response to an indeterminate logic state.

Frequency Synchronization (SYNC/MODE Pin)

The SYNC/MODE input can also be used for frequency synchronization. To synchronize the LM2608 to an external clock, supply a digital signal to the SYNC/MODE pin with a voltage swing exceeding 0.4V to 1.3V. During synchronization, the LM2608 initiates cycles on the rising edge of the clock. When synchronized to an external clock, it operates in PWM mode. The device can synchronize to an external clock over frequencies from 500kHz to 1MHz.

Use the following waveform and duty-cycle guidelines when applying an external clock to the SYNC/MODE pin. The duty cycle can be between 30% and 70%. Clock under/overshoot should be less than 100mV below GND or above VDD. When applying noisy clock signals, especially sharp edged signals from a long cable during evaluation, terminate the cable at its characteristic impedance; add an RC filter to the SYNC pin, if necessary, to soften the slew rate and over/undershoot. Note that sharp edged signals from a pulse or function generator can develop under/overshoot as high as 10V at the end of an improperly terminated cable.

Overvoltage Protection

The LM2608 has an over-voltage comparator that prevents the output voltage from rising too high when the device is left in PWM mode under low-load conditions. Otherwise, the output voltage could rise out of regulation from the minimum energy transferred per cycle due to the 200nS minimum on-time of the PFET switch while in PWM mode. When the output voltage rises by 45mV over its regulation threshold, the OVP comparator inhibits PWM operation to skip pulses until the output voltage returns to the regulation threshold. In over voltage protection, output voltage and ripple increase slightly.

Shutdown Mode

Setting the EN input low, to SGND, places the LM2608 in a 0.02µA (typ) shutdown mode. During shutdown, the PFET switch, NFET synchronous rectifier, reference, control and bias of the LM2608 are turned off. Setting EN high to VDD enables normal operation. While turning on, soft start is activated. EN is a Schmitt trigger digital input with thresholds that are independent of the input voltage at VDD.

EN must be set low to turn off the LM2608 during undervoltage conditions when the supply is less than the 2.8V minimum operating voltage. The LM2608 is designed for mobile phones and similar applications where power sequencing is determined by the system controller and internal UVLO (Under Voltage LockOut) circuitry is unnecessary. The LM2608 has no UVLO circuitry. Although the LM2608 exhibits good behavior while enabled at low input voltages, this is not specified.

Internal Synchronous Rectification

The LM2608 uses an internal NFET as a synchronous rectifier to improve efficiency by reducing rectifier forward voltage drop and associated power loss. In general, synchronous rectification provides a significant improvement in efficiency whenever the output voltage is relatively low compared to the voltage drop across an ordinary rectifier diode.

Under moderate and heavy loads, the internal NFET synchronous rectifier is turned on during the inductor current down-slope in the second part of each cycle. The synchronous rectifier is turned off prior to the next cycle, or when the inductor current ramps near zero at light loads. The NFET is designed to conduct through its intrinsic body diode during transient intervals before it turns on, eliminating the need for an external diode.

Current Limiting

A current limit feature allows the LM2608 to protect itself and external components during overload conditions. Current limiting is implemented using an independent internal comparator. In PWM mode, cycle-by-cycle current limiting is normally used. If an excessive load pulls the output voltage down to approximately 0.7V, then the device switches to a timed current limit mode. In timed current limit mode the internal P-FET switch is turned off after the current comparator trips and the beginning of the next cycle is inhibited for 2.5µs to force the instantaneous inductor current to ramp down to a safe value. Timed current limit prevents the loss of current control seen in some products when the output voltage is pulled low in serious overload conditions.

Current Limiting and PWM Mode Transient Response Considerations

The LM2608 was designed for fast response to moderate load steps. Harsh transient conditions during loads above 300mA can cause the inductor current to swing up to the maximum current limit, resulting in PWM mode jitter or instability from activation of the current limit comparator. To avoid this jitter or instability, do not power-up or start the LM2608 into a full load (loads near or above 400mA). Do not change operating modes or output voltages when operating at a full load. Avoid extremely sharp and wide-ranging load steps to full load, such as from <30mA to >350mA.

Pin Selectable Output Voltage

The LM2608 features pin-selectable output voltage to eliminate the need for external feedback resistors. The output can be set to 1.3V, 1.5V or 1.8V by configuring the VSEL pin. See *Setting the Output Voltage* in the *Application Information* section for further details.

Soft-Start

The LM2608 is designed to be started in LDO mode. Under these conditions, the output voltage will increase at a rate determined by the LDO current limit and the output capacitor and load. This ramp time is typically in the millisecond range. The LM2608 may be started in PWM mode as well. Under these conditions, the reference voltage for the error amp is ramped up in about 100µs and the output voltage will follow. In this way, the input inrush current and output voltage overshoot can be minimized.

Thermal Shutdown Protection

The LM2608 has thermal shutdown protection in PWM mode to protect from short-term misuse and overload conditions. When the junction temperature exceeds 150°C, the device shuts down and re-starts in soft start after the temperature drops below 130°C. Prolonged operation in thermal overload conditions may damage the device and is considered bad practice.

APPLICATION INFORMATION

SETTING THE OUTPUT VOLTAGE

The LM2608 features pin-selectable output voltage to eliminate the need for external feedback resistors. Select an output voltage of 1.3V, 1.5V or 1.8V by configuring the VSEL pin, as directed in Table 1.

Table 1. VSEL Output Voltage Selection Settings

Output Voltage Options	V_{OUT}	VSEL
LM2608 - 1.3 (300mA)	1.3V	GND
	1.5V	VDD
LM2608 - 1.8 (400mA)	1.5V	GND
	1.8V	VDD

VSEL may be set high by connecting to VDD or low by connecting to SGND. Optionally, VSEL may be driven by digital gates that provide over 1.2V for a high state and less than 0.4V for a low state to ensure valid logic levels. The VSEL input has an internal 0.7 µA (typ) pull-down that pulls the input low, when left unconnected. Leaving this pin open is acceptable, but setting the pin high or low is recommended.

INDUCTOR SELECTION

A 10µH inductor with a saturation current rating over the current limit (I_{LIM}) of the LM2608 is recommended for most applications. The inductor's resistance should be less than 0.3Ω for good efficiency. Table 2 lists suggested inductors and suppliers.

Table 2. Suggested Inductors and Their Suppliers

Model	Vendor	Phone	FAX
DO1608C-103	Coilcraft	847-639-6400	847-639-1469
DO1606T-103	Coilcraft		
UP1B-100	Coiltronics	561-241-7876	561-241-9339
UP0.4CB-100	Coiltronics		
ELL6GM100M	Panasonic	714-373-7366	714-373-7323
ELL6PM100M	Panasonic		
P1174.103T	Pulse Engineering	858-674-8100	858-674-8262
P0770.103T	Pulse Engineering	858-674-8100	858-674-8262
CDRH5D18-100	Sumida	847-956-0666	847-956-0702
CDRH4D28-100	Sumida		
CDC5D23-100	Sumida		
NP05D B100M	Taiyo Yuden	847-925-0888	847-925-0899
NP04S B100N	Taiyo Yuden		
SLF6025T-100M1R0	TDK	847-803-6100	847-803-6296
SLF6020T-100MR90	TDK		
A918CY-100M	Toko	847-297-0070	847-699-7864
A915AY-100M	Toko		

For low-cost applications, an unshielded bobbin inductor is suggested. For noise critical applications, a toroidal or shielded-bobbin inductor should be used. A good practice is to lay out the board with overlapping footprints of both types for design flexibility. This allows substitution of a low-noise toroidal inductor, in the event that noise from low-cost bobbin models is unacceptable.

The saturation current rating is the current level beyond which an inductor loses its inductance. Beyond this rating, the inductor loses its ability to limit current through the PFET switch to a ramp and allows the switch current to increase rapidly. This can cause poor efficiency, regulation errors or stress to DC-DC converters like the LM2608. Saturation occurs when the magnetic flux density from current through the windings of the inductor exceeds what the inductor's core material can support with energy storage in a corresponding magnetic field.

Table 3. Suggested Capacitors and Their Suppliers

Model	Size	Vendor	Phone	FAX
22µF, X7R or X5R Ceramic Capacitor for C2 (Output Filter Capacitor)				
C3225X5RIA226M	1210	TDK	847-803-6100	847-803-6296
JMK325BJ226MM	1210	Taiyo-Yuden	847-925-0888	847-925-0899
ECJ4YB0J226M	1210	Panasonic	714-373-7366	714-373-7323
GRM42-2X5R226K6.3	1210	muRata	404-436-1300	404-436-3030
10µF, 6.3V, X7R or X5R Ceramic Capacitor for C1 (Input Filter Capacitor)				
C2012X5R0J106M	0805	TDK	847-803-6100	847-803-6296
JMK212BJ106MG	0805	Taiyo Yuden	847-925-0888	847-925-0899
ECJ3YB0J106K	1206	Panasonic	714-373-7366	714-373-7323
GRM40X5R106K6.3	0805	muRata	404-436-1400	404-436-3030

CAPACITOR SELECTION

Use a 10µF, 6.3V, X7R or X5R ceramic input filter capacitor and a 22µF, X7R or X5R ceramic output filter capacitor. These provide an optimal balance between small size, cost, reliability and performance. Do not use Y5V ceramic capacitors. Table 3 lists suggested capacitors and suppliers.

A 10µF ceramic capacitor can be used for the output filter capacitor for smaller size in applications where the worst-case transient load step is less than 200mA. Use of a 10µF output capacitor trades off smaller size for an increase in output voltage ripple, and undershoot during line and load transient response.

The input filter capacitor supplies current to the PFET switch of the LM2608 in the first part of each cycle and reduces voltage ripple imposed on the input power source. The output filter capacitor smooths out current flow from the inductor to the load, helps maintain a steady output voltage during transient load changes and reduces output voltage ripple. These capacitors must be selected with sufficient capacitance and sufficiently low ESR to perform these functions.

The ESR, or equivalent series resistance, of the filter capacitors is a major factor in voltage ripple.

DSBGA PACKAGE ASSEMBLY AND USE

Use of the DSBGA package requires specialized board layout, precision mounting and careful reflow techniques, as detailed in Application Note AN-1112 (Literature Number SNVA009). Refer to the section *Surface Mount Technology (SMT) Assembly Considerations*. For best results in assembly, alignment ordinals on the PC board should be used to facilitate placement of the device. Since DSBGA packaging is a new technology, all layouts and assembly means must be thoroughly tested prior to production. In particular, proper placement, solder reflow and resistance to thermal cycling must be verified.

The 10-Bump package used for the LM2608 has 300micron solder balls and requires 10.82mil (0.275mm) pads for mounting on the circuit board. The trace to each pad should enter the pad with a 90° entry angle to prevent debris from being caught in deep corners. Initially, the trace to each pad should be 6 mil wide, for a section 6 mil long or longer, as a thermal relief. Then each trace should neck up to its optimal width over a span of 11 mils or more, so that the taper extends beyond the edge of the package. The important criterion is symmetry. This ensures the solder bumps on the LM2608 re-flow evenly and that the device solders level to the board. In particular, special attention must be paid to the pads for bumps D3, C3, B3, A3 and A2. Because PVIN and PGND are typically connected to large copper planes, inadequate thermal reliefs can result in late or inadequate reflow of these bumps.

The pad style used with DSBGA package must be the NSMD (non-solder mask defined) type. This means that the solder-mask opening is larger than the pad size or 14.7mils for the LM2608. This prevents a lip that otherwise forms if the solder-mask and pad overlap. This lip can hold the device off the surface of the board and interfere with mounting. See Application Note AN-1112 (Literature Number SNVA009) for specific instructions.

BOARD LAYOUT CONSIDERATIONS

PC board layout is an important part of DC-DC converter design. Poor board layout can disrupt the performance of a DC-DC converter and surrounding circuitry by contributing to EMI, ground bounce, and resistive voltage loss in the traces. These can send erroneous signals to the DC-DC converter IC, resulting in poor regulation or instability. Poor layout can also result in reflow problems leading to poor solder joints between the DSBGA package and board pads. Poor solder joints can result in erratic or degraded performance.

Good layout for the LM2608 can be implemented by following a few simple design rules:

1. Place the LM2608 on 10.82mil pads for DSBGA package. As a thermal relief, connect to each pad with a 6mil wide trace (DSBGA), 6mils long or longer, then incrementally increase each trace to its optimal width over a span so that the taper extends beyond the edge of the package. The important criterion is symmetry to ensure re-flow occurs evenly (see *DSBGA Package Assembly and Use*).
2. Place the LM2608, inductor and filter capacitors close together and make the traces short. The traces between these components carry relatively high switching currents and act as antennas. Following this rule reduces radiated noise. Place the capacitors and inductor within 0.2in (5mm) of the LM2608.
3. Arrange the components so that the switching current loops curl in the same direction. During the first part of each cycle, current flows from the input filter capacitor, through the LM2608 and inductor to the output filter capacitor and back through ground, forming a current loop. In the second part of each cycle, current is pulled up from ground, through the LM2608 by the inductor, to the output filter capacitor and then back through ground, forming a second current loop. Routing these loops so the current curls in the same direction prevents magnetic field reversal between the two part-cycles and reduces radiated noise.
4. Connect the ground pins of the LM2608 and filter capacitors together using generous component-side copper fill as a pseudo-ground plane. Then, connect this to the ground-plane (if one is used) with several vias. This reduces ground-plane noise by preventing the switching currents from circulating through the ground plane. It also reduces ground bounce at the LM2608 by giving it a low-impedance ground connection.
5. Use wide traces between the power components and for power connections to the DC-DC converter circuit. This reduces voltage errors caused by resistive losses across the traces.
6. Route noise sensitive traces, such as the voltage feedback path, away from noisy traces between the power components. The voltage feedback trace must remain close to the LM2608 circuit and should be routed away from noisy components. This reduces EMI radiated onto the DC-DC converter's own voltage feedback trace.
7. Place noise sensitive circuitry, such as radio IF blocks, away from the DC-DC converter, CMOS digital blocks and other noisy circuitry. Interference with noise-sensitive circuitry in the system can be reduced through distance.

In mobile phones, for example, a common practice is to place the DC-DC converter on one corner of the board, arrange the CMOS digital circuitry around it (since this also generates noise), and then place sensitive preamplifiers and IF stages on the diagonally opposing corner. Often, the sensitive circuitry is shielded with a metal pan and power to it is post-regulated to reduce conducted noise, using low-dropout linear regulators, such as the LP2966.

REVISION HISTORY

Changes from Revision D (May 2013) to Revision D	Page

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM2608ATLX-1.8/NOPB	ACTIVE	DSBGA	YPA	10		TBD	Call TI	Call TI	-30 to 85	S44A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

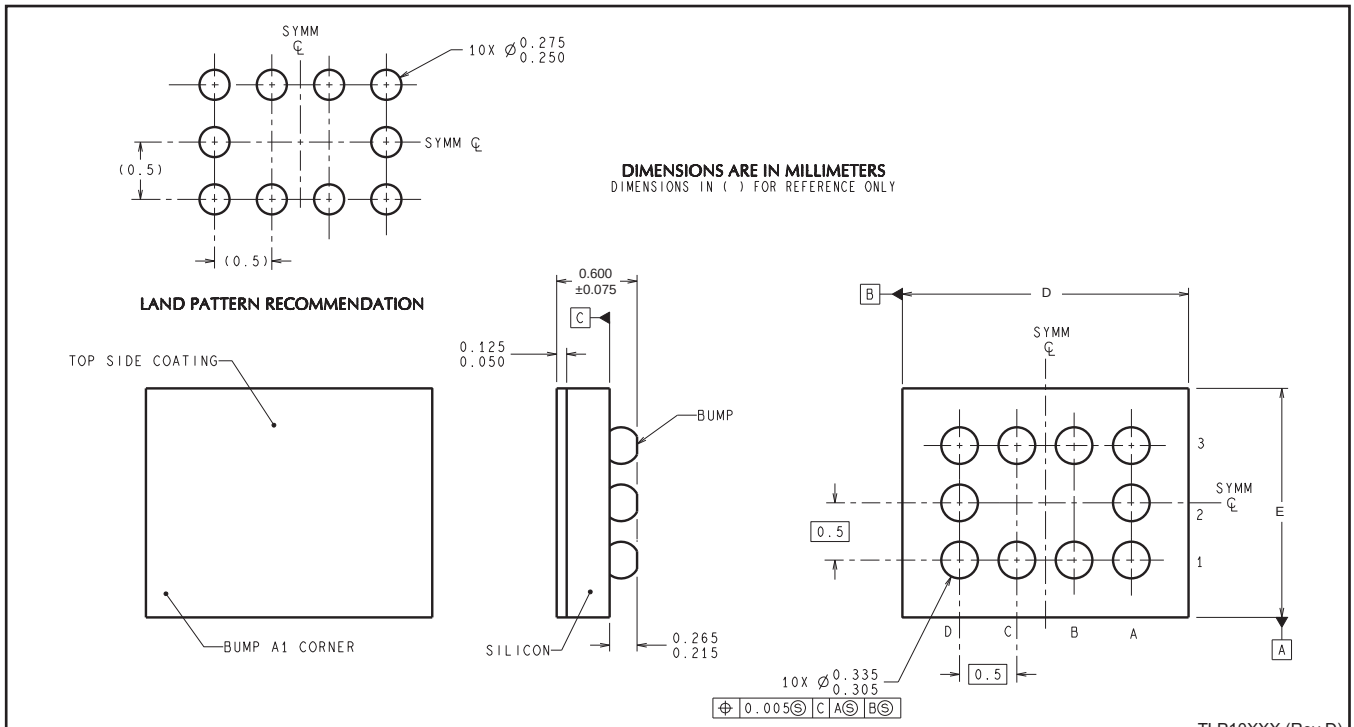
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

YPA0010



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NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

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