HA-5002

110MHz, High Slew Rate, High Output Current Buffer

FN2921
Rev 12.00
October 18, 2013

The HA-5002 is a monolithic, wideband, high slew rate, high output current, buffer amplifier.

Utilizing the advantages of the Intersil D.I. technologies, the HA-5002 current buffer offers 1300V/µs slew rate with 110MHz of bandwidth. The ±200mA output current capability is enhanced by a 3Ω output impedance.

The monolithic HA-5002 will replace the hybrid LH0002 with corresponding performance increases. These characteristics range from the 3000kΩ input impedance to the increased output voltage swing. Monolithic design technologies have allowed a more precise buffer to be developed with more than an order of magnitude smaller gain error.

The HA-5002 will provide many present hybrid users with a higher degree of reliability and at the same time increase overall circuit performance.

For the military grade product, refer to the HA-5002/883 datasheet.

Features

- Voltage gain 0.995
- High input impedance 3000kΩ
- Low output impedance 3Ω
- Very high slew rate. 1300V/µs
- Very wide bandwidth 110MHz
- High output current . . . . . ±200mA
- Pulsed output current 400mA
- Monolithic construction
- Pb-Free available (RoHS Compliant)

Applications

- Line driver
- Data acquisition
- 110MHz buffer
- Radar cable driver
- High power current booster
- High power current source
- Sample and holds
- Video products

Ordering Information

PART NUMBER	PART MARKING	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
HA2-5002-2	HA2- 5002-2	-55 to +125	8 Pin Metal Can	T8.C
HA4P5002-5Z (Note 1)	HA4P 5002-5Z	0 to +75	20 Ld PLCC (Pb-free)	N20.35
HA9P5002-5Z (Note 1)	5002 5Z	0 to +75	8 Ld SOIC (Pb-free)	M8.15
HA9P5002-9Z (Note 1)	5002 9Z	-40 to +85	8 Ld SOIC (Pb-free)	M8.15

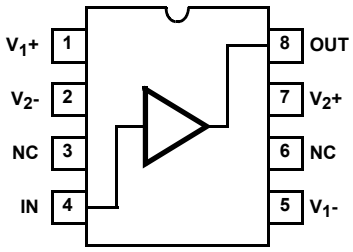
NOTE:

1. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

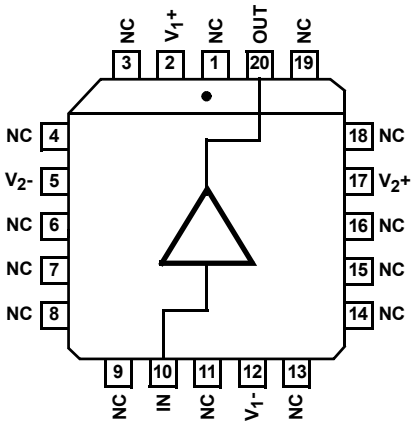
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Pinouts

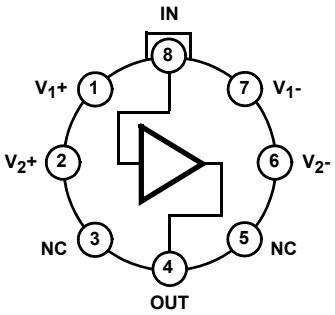
HA-5002
(8 LD SOIC)
TOP VIEW



HA-5002
(20 LD PLCC)
TOP VIEW



HA-5002
(8 PIN METAL CAN)
TOP VIEW



NOTE: Case Voltage = Floating

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Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 44V
Input Voltage . . . . . V_1+ to V_1-
Output Current (Continuous) . . . . . ±200mA
Output Current (50ms On, 1s Off) . . . . . ±400mA

Operating Conditions

Temperature Range
HA-5002-2 . . . . . -55°C to +125°C
HA-5002-5 . . . . . 0°C to +75°C
HA-5002-9 . . . . . -40°C to +85°C

Thermal Information

Thermal Resistance	θ_{JA} (°C/W)	θ_{JC} (°C/W)
Metal Can Package (Notes 3, 4)	155	67
PLCC Package (Note 3).	74	N/A
SOIC Package (Note 3)	157	N/A

Max Junction Temperature (Hermetic Packages, Note 2). . . . . +175°C
Max Junction Temperature (Plastic Packages, Note 2). . . . . +150°C
Max Storage Temperature Range . . . . . -65°C to +150°C
Max Lead Temperature (Soldering 10s) . . . . . +300°C
(PLCC and SOIC - Lead Tips Only)

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

2. Maximum power dissipation, including load conditions, must be designed to maintain the maximum junction temperature below +175°C for the can packages, and below +150°C for the plastic packages.
3. For θ_{JA} is measured with the component mounted on an evaluation PC board in free air.
4. For θJC, the “case temp” location is the center of the exposed metal pad on the package underside.

Electrical Specifications

V_{SUPPLY} = ±12V to ±15V, R_S = 50Ω, R_L = 1kΩ, C_L = 10pF, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP (°C)	HA-5002-2			HA-5002-5, -9			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS									
Offset Voltage		25	-	5	20	-	5	20	mV
		Full	-	10	30	-	10	30	mV
Average Offset Voltage Drift		Full	-	30	-	-	30	-	µV/°C
Bias Current		25	-	2	7	-	2	7	µA
		Full	-	3.4	10	-	2.4	10	µA
Input Resistance		Full	1.5	3	-	1.5	3	-	MΩ
Input Noise Voltage	10Hz-1MHz	25	-	18	-	-	18	-	μV_{P-P}
TRANSFER CHARACTERISTICS									
Voltage Gain (V_{OUT} = ±10V)	R_L = 50Ω	25	-	0.900	-	-	0.900	-	V/V
	R_L = 100Ω	25	-	0.971	-	-	0.971	-	V/V
	R_L = 1kΩ	25	-	0.995	-	-	0.995	-	V/V
	R_L = 1kΩ	Full	0.980	-	-	0.980	-	-	V/V
-3dB Bandwidth	V_{IN} = $1V_{P-P}$	25	-	110	-	-	110	-	MHz
AC Current Gain		25	-	40	-	-	40	-	A/mA
OUTPUT CHARACTERISTICS									
Output Voltage Swing	R_L = 100Ω	25	±10	±10.7	-	±10	±11.2	-	V
	R_L = 1kΩ, V_S = ±15V	Full	±10	±13.5	-	±10	±13.9	-	V
	R_L = 1kΩ, V_S = ±12V	Full	±10	±10.5	-	±10	±10.5	-	V
Output Current	V_{IN} = ±10V, R_L = 40Ω	25	-	220	-	-	220	-	mA
Output Resistance		Full	-	3	10	-	3	10	Ω
Harmonic Distortion	V_{IN} = $1V_{RMS}$, f = 10kHz	25	-	<0.005	-	-	<0.005	-	%
TRANSIENT RESPONSE									
Full Power Bandwidth (Note 5)		25	-	20.7	-	-	20.7	-	MHz
Rise Time		25	-	3.6	-	-	3.6	-	ns
Propagation Delay		25	-	2	-	-	2	-	ns
Overshoot		25	-	30	-	-	30	-	%
Slew Rate		25	1.0	1.3	-	1.0	1.3	-	V/ns
Settling Time	To 0.1%	25	-	50	-	-	50	-	ns
Differential Gain	R_L = 500Ω	25	-	0.06	-	-	0.06	-	%
Differential Phase	R_L = 500Ω	25	-	0.22	-	-	0.22	-	°

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Electrical Specifications V_{SUPPLY} = ±12V to ±15V, R_S = 50Ω, R_L = 1kΩ, C_L = 10pF, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP (°C)	HA-5002-2			HA-5002-5, -9			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
POWER REQUIREMENTS									
Supply Current		25	-	8.3	-	-	8.3	-	mA
		Full	-	-	10	-	-	10	mA
Power Supply Rejection Ratio	A_V = 10V	Full	54	64	-	54	64	-	dB

NOTE:

5. $FPBW = \frac{\text{Slew Rate}}{2\pi V_{PEAK}}$; V_P = 10V.

Test Circuit and Waveforms

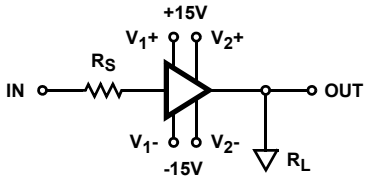
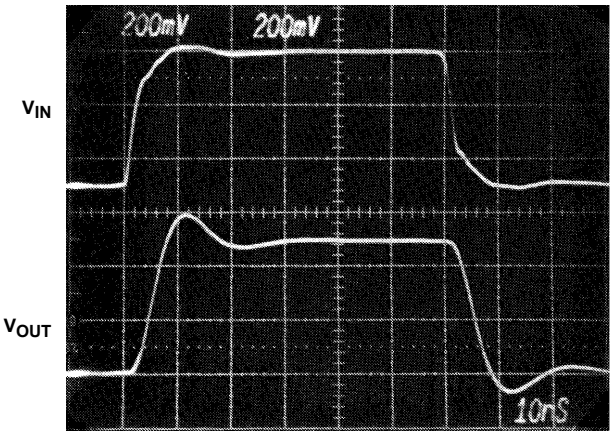
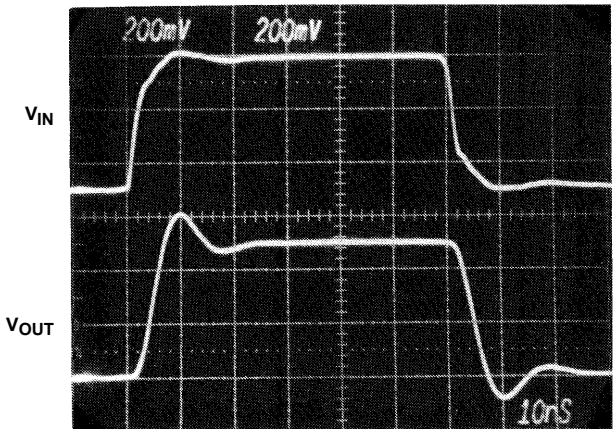


FIGURE 1. LARGE AND SMALL SIGNAL RESPONSE



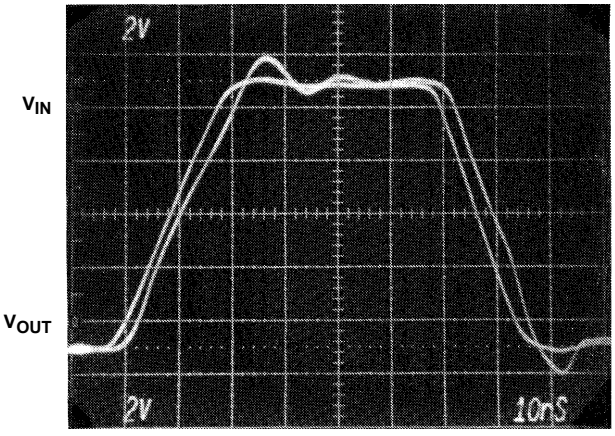
R_S = 50Ω, R_L = 100Ω

SMALL SIGNAL WAVEFORMS



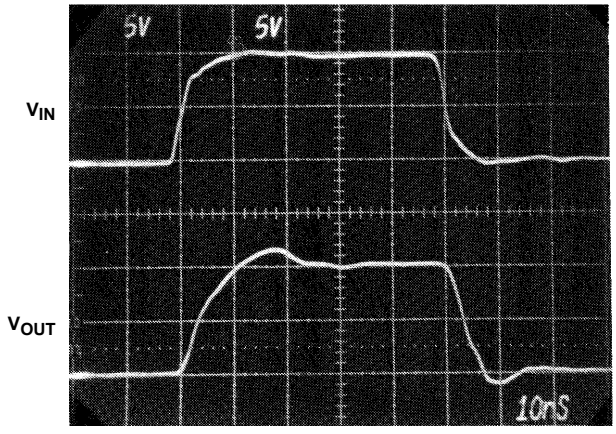
R_S = 50Ω, R_L = 1kΩ

SMALL SIGNAL WAVEFORMS



R_S = 50Ω, R_L = 100Ω

LARGE SIGNAL WAVEFORMS

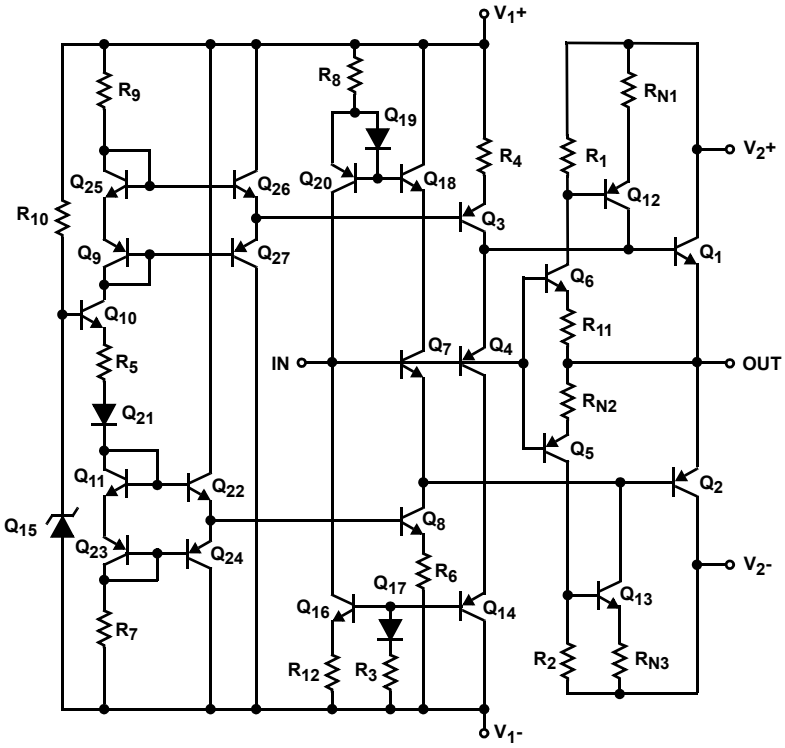


R_S = 50Ω, R_L = 1kΩ

LARGE SIGNAL WAVEFORMS

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Schematic Diagram



Application Information

Layout Considerations

The wide bandwidth of the HA-5002 necessitates that high frequency circuit layout procedures be followed. Failure to follow these guidelines can result in marginal performance.

Probably the most crucial of the RF/video layout rules is the use of a ground plane. A ground plane provides isolation and minimizes distributed circuit capacitance and inductance which will degrade high frequency performance.

Other considerations are proper power supply bypassing and keeping the input and output connections as short as possible which minimizes distributed capacitance and reduces board space.

Power Supply Decoupling

For optimal device performance, it is recommended that the positive and negative power supplies be bypassed with capacitors to ground. Ceramic capacitors ranging in value from 0.01 to 0.1µF will minimize high frequency variations in supply voltage, while low frequency bypassing requires larger valued capacitors since the impedance of the capacitor is dependent on frequency.

It is also recommended that the bypass capacitors be connected close to the HA-5002 (preferably directly to the supply pins).

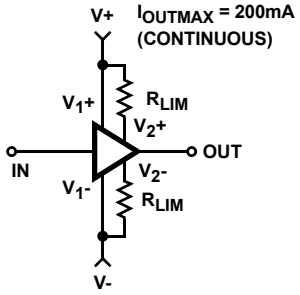
Operation at Reduced Supply Levels

The HA-5002 can operate at supply voltage levels as low as ±5V and lower. Output swing is directly affected as well as slight reductions in slew rate and bandwidth.

Short Circuit Protection

The output current can be limited by using the following circuit:

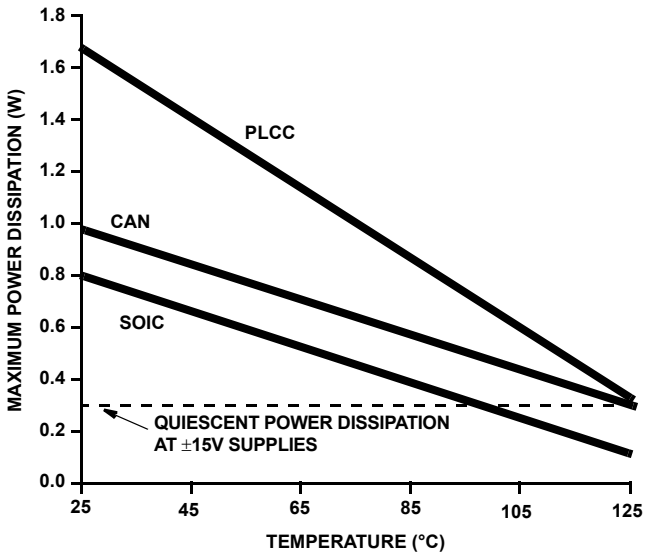
$$R_{LIM} = \frac{V+}{I_{OUTMAX}} = \frac{V-}{I_{OUTMAX}}$$



Capacitive Loading

The HA-5002 will drive large capacitive loads without oscillation but peak current limits should not be exceeded. Following the formula I = Cdv/dt implies that the slew rate or the capacitive load must be controlled to keep peak current below the maximum or use the current limiting approach as shown. The HA-5002 can become unstable with small capacitive loads (50pF) if certain precautions are not taken. Stability is enhanced by any one of the following: a source resistance in series with the input of 50Ω to 1kΩ; increasing capacitive load to 150pF or greater; decreasing C_{LOAD} to 20pF or less; adding an output resistor of 10Ω to 50Ω; or adding feedback capacitance of 50pF or greater. Adding source resistance generally yields the best results.

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$$P_{DMAX} = \frac{T_{JMAX} - T_A}{\theta_{JC} + \theta_{CS} + \theta_{SA}}$$

Where: T_{JMAX} = Maximum Junction Temperature of the Device

T_A = Ambient

θ_{JC} = Junction to Case Thermal Resistance

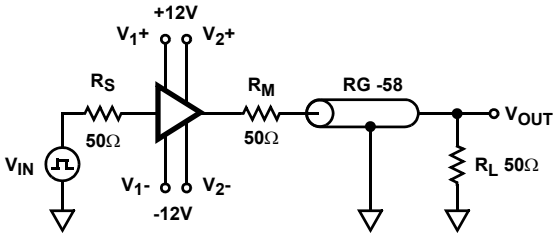
θ_{CS} = Case to Heat Sink Thermal Resistance

θ_{SA} = Heat Sink to Ambient Thermal Resistance

Graph is based on: $P_{DMAX} = \frac{T_{JMAX} - T_A}{\theta_{JA}}$

FIGURE 2. MAXIMUM POWER DISSIPATION vs TEMPERATURE

Typical Application



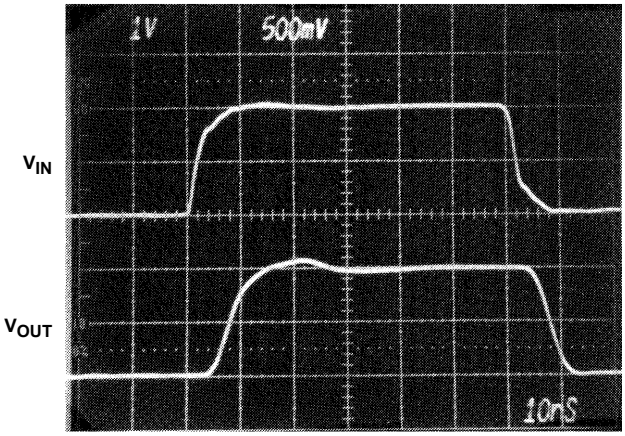


FIGURE 3. COAXIAL CABLE DRIVER - 50Ω SYSTEM

Typical Performance Curves

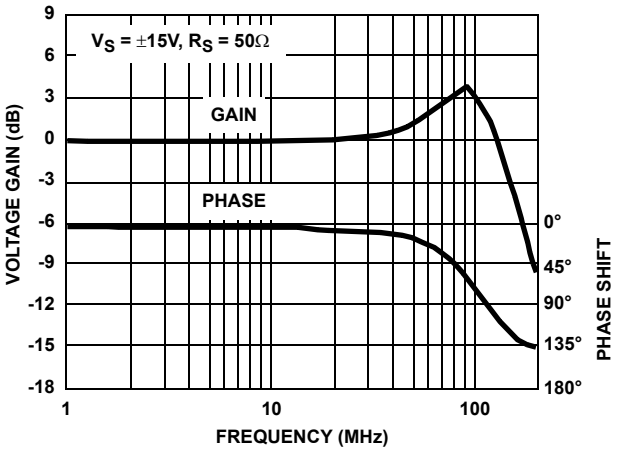


FIGURE 4. GAIN/PHASE vs FREQUENCY (R_L = 1kΩ)

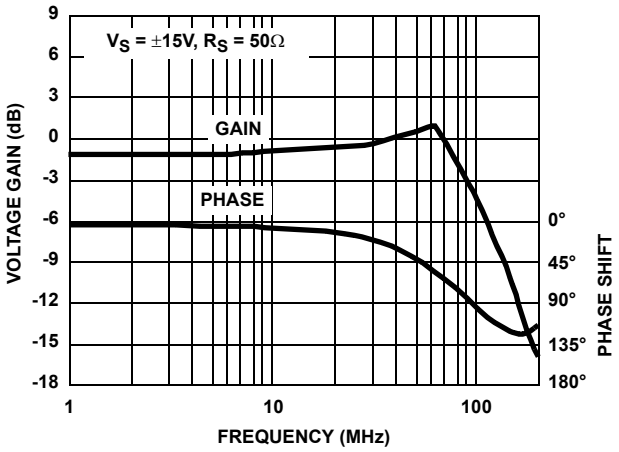


FIGURE 5. GAIN/PHASE vs FREQUENCY (R_L = 50Ω)

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Typical Performance Curves (Continued)

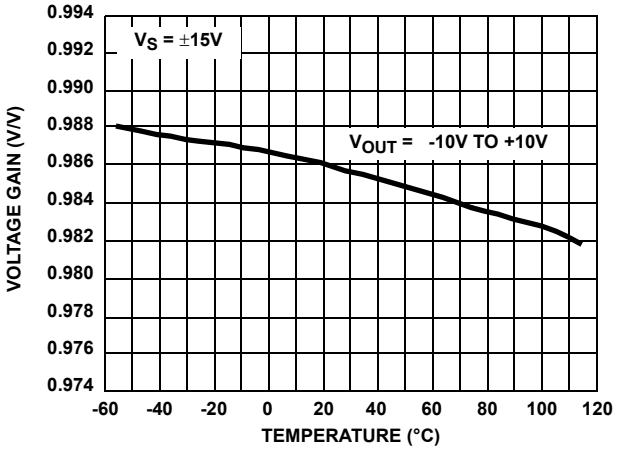


FIGURE 6. VOLTAGE GAIN vs TEMPERATURE (R_L = 100Ω)

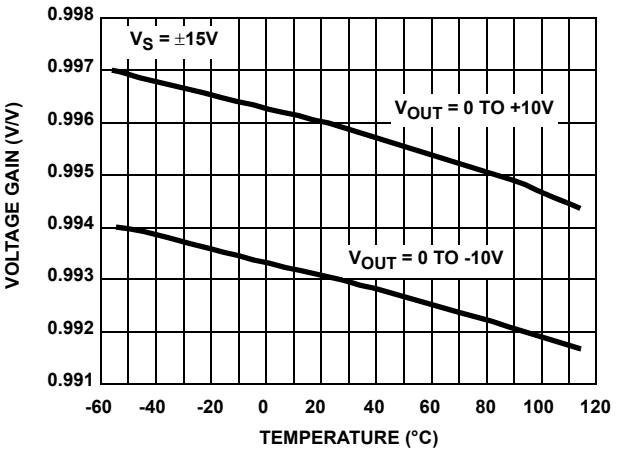


FIGURE 7. VOLTAGE GAIN vs TEMPERATURE (R_L = 1kΩ)

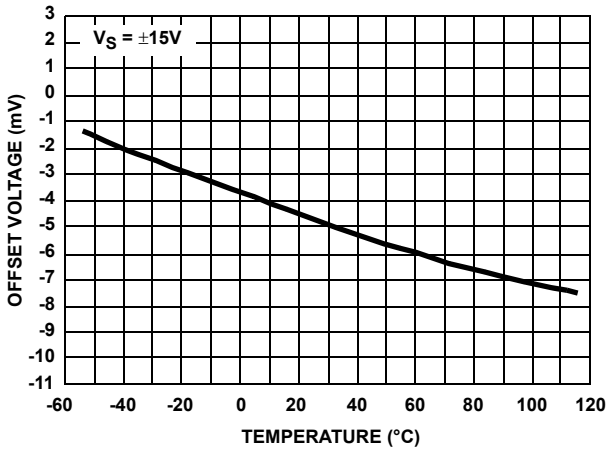


FIGURE 8. OFFSET VOLTAGE vs TEMPERATURE

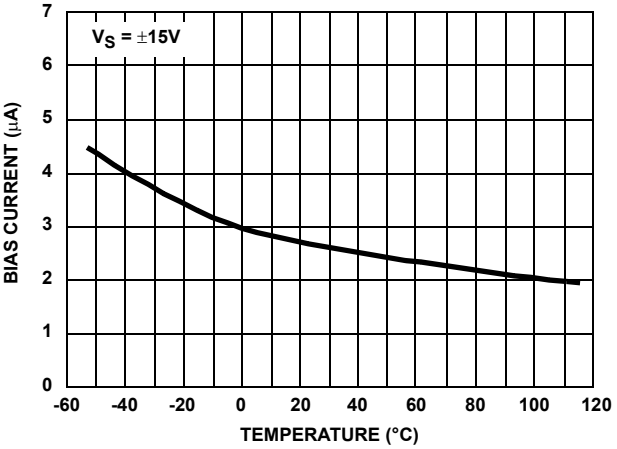


FIGURE 9. BIAS CURRENT vs TEMPERATURE

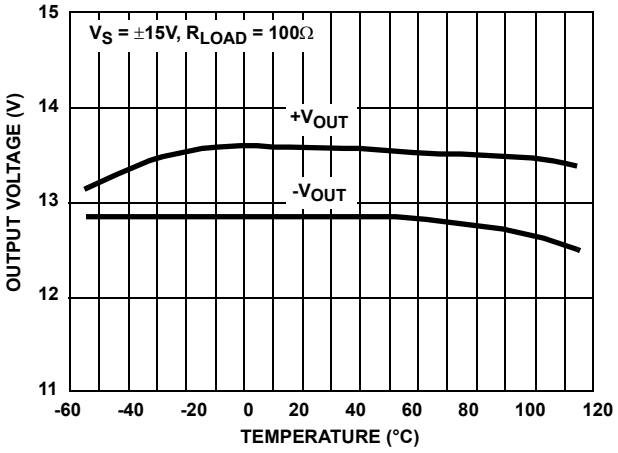


FIGURE 10. MAXIMUM OUTPUT VOLTAGE vs TEMPERATURE

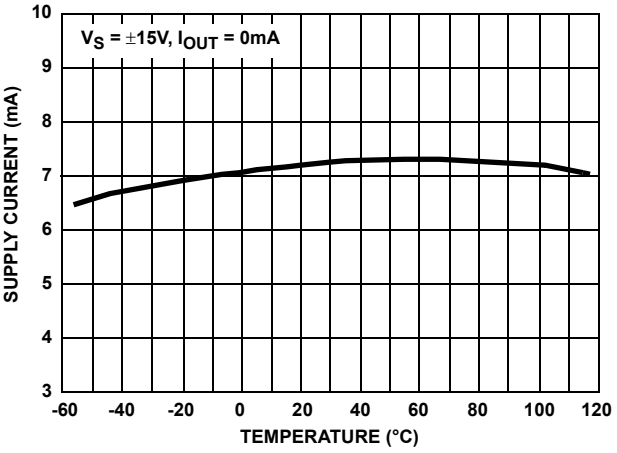


FIGURE 11. SUPPLY CURRENT vs TEMPERATURE

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Typical Performance Curves (Continued)

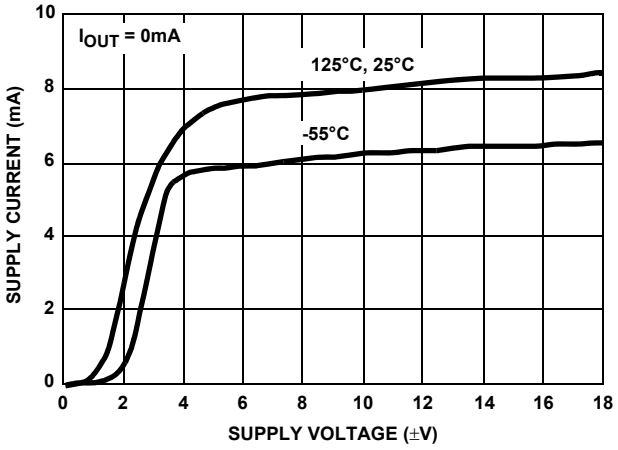


FIGURE 12. SUPPLY CURRENT vs SUPPLY VOLTAGE

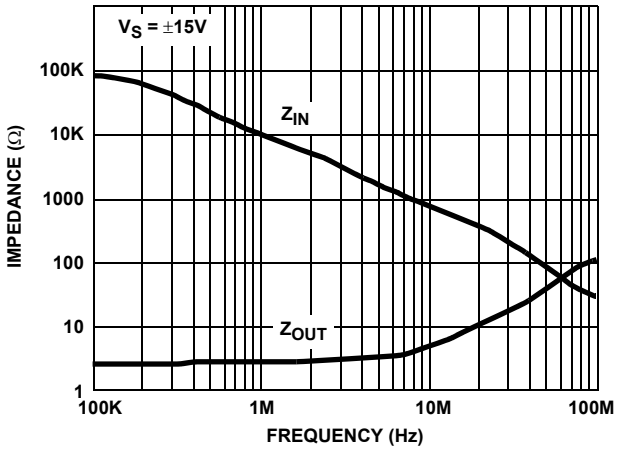


FIGURE 13. INPUT/OUTPUT IMPEDANCE vs FREQUENCY

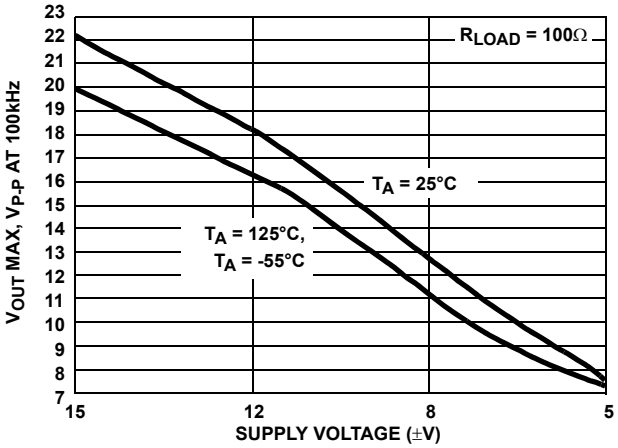


FIGURE 14. V_{OUT} MAXIMUM vs V_{SUPPLY}

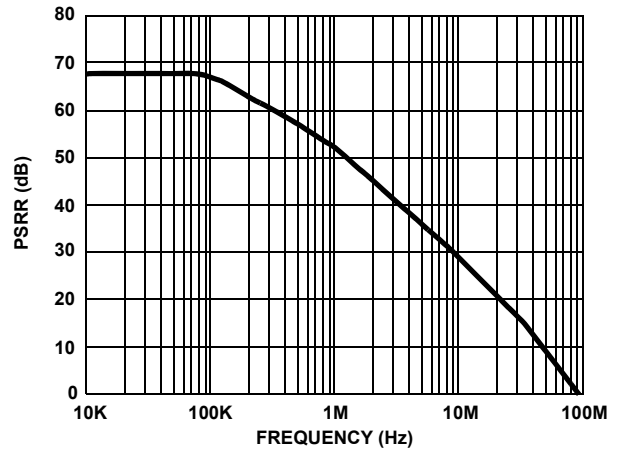


FIGURE 15. PSRR vs FREQUENCY

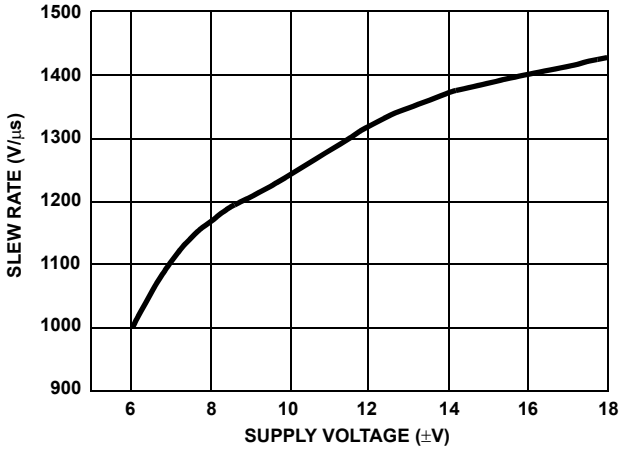


FIGURE 16. SLEW RATE vs SUPPLY VOLTAGE

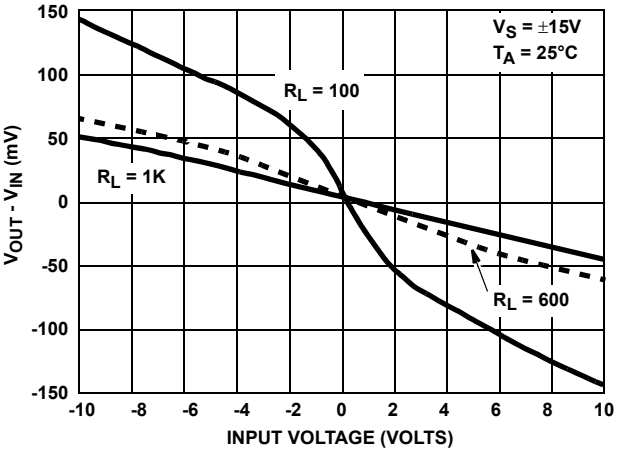


FIGURE 17. GAIN ERROR vs INPUT VOLTAGE

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Die Characteristics

SUBSTRATE POTENTIAL (POWERED UP):

V_1-

TRANSISTOR COUNT:

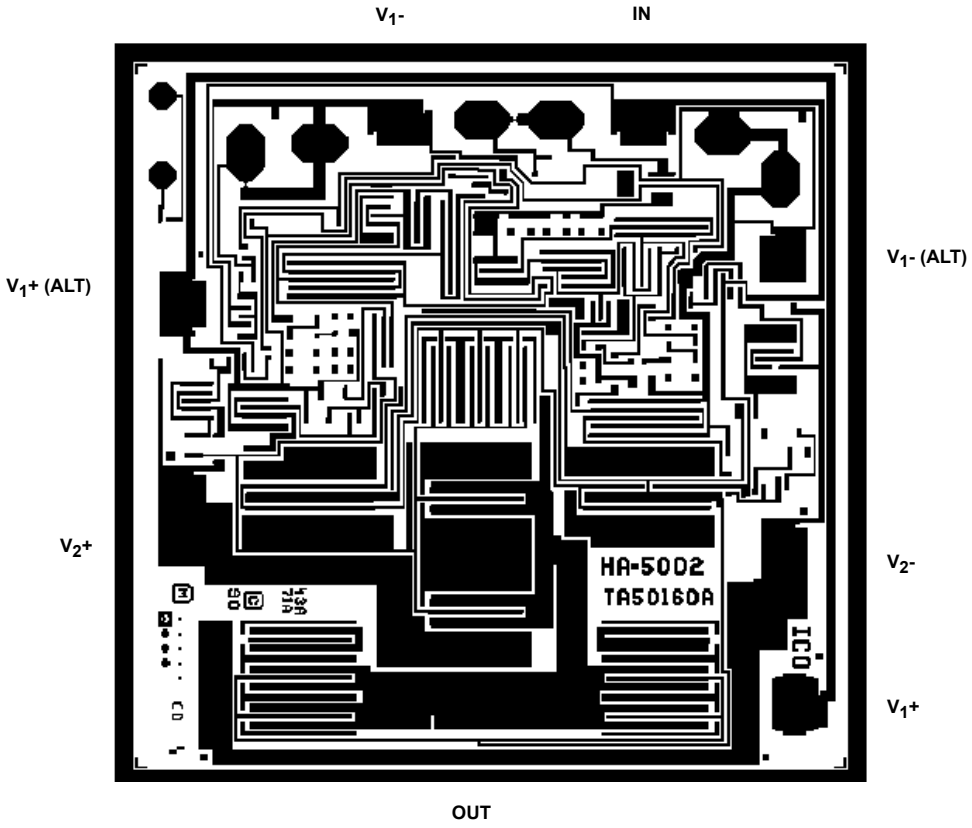
27

PROCESS:

Bipolar Dielectric Isolation

Metallization Mask Layout

HA-5002



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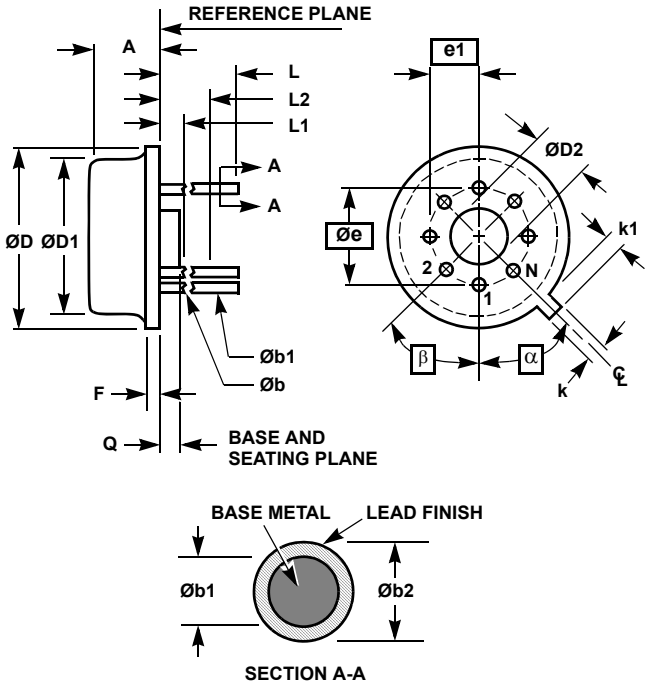
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Metal Can Packages (Can)



NOTES:

1. (All leads) Øb applies between L1 and L2. Øb1 applies between L2 and 0.500 from the reference plane. Diameter is uncontrolled in L1 and beyond 0.500 from the reference plane.
2. Measured from maximum diameter of the product.
3. α is the basic spacing from the centerline of the tab to terminal 1 and β is the basic spacing of each lead or lead position (N -1 places) from α, looking at the bottom of the package.
4. N is the maximum number of terminal positions.
5. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
6. Controlling dimension: INCH.

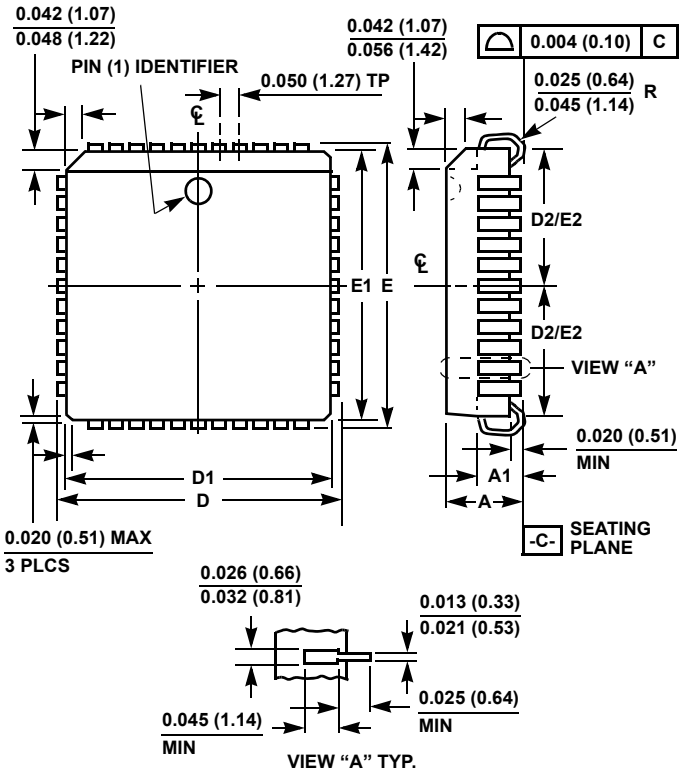
T8.C MIL-STD-1835 MACY1-X8 (A1)
8 LEAD METAL CAN PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.165	0.185	4.19	4.70	-
Øb	0.016	0.019	0.41	0.48	1
Øb1	0.016	0.021	0.41	0.53	1
Øb2	0.016	0.024	0.41	0.61	-
ØD	0.335	0.375	8.51	9.40	-
ØD1	0.305	0.335	7.75	8.51	-
ØD2	0.110	0.160	2.79	4.06	-
e	0.200 BSC		5.08 BSC		-
e1	0.100 BSC		2.54 BSC		-
F	-	0.040	-	1.02	-
k	0.027	0.034	0.69	0.86	-
k1	0.027	0.045	0.69	1.14	2
L	0.500	0.750	12.70	19.05	1
L1	-	0.050	-	1.27	1
L2	0.250	-	6.35	-	1
Q	0.010	0.045	0.25	1.14	-
α	45^o BSC		45^o BSC		3
β	45^o BSC		45^o BSC		3
N	8		8		4

Rev. 0 5/18/94

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Plastic Leaded Chip Carrier Packages (PLCC)



N20.35 (JEDEC MS-018AA ISSUE A)
20 LEAD PLASTIC LEADED CHIP CARRIER PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.165	0.180	4.20	4.57	-
A1	0.090	0.120	2.29	3.04	-
D	0.385	0.395	9.78	10.03	-
D1	0.350	0.356	8.89	9.04	3
D2	0.141	0.169	3.59	4.29	4, 5
E	0.385	0.395	9.78	10.03	-
E1	0.350	0.356	8.89	9.04	3
E2	0.141	0.169	3.59	4.29	4, 5
N	20		20		6

Rev. 2 11/97

NOTES:

1. Controlling dimension: INCH. Converted millimeter dimensions are not necessarily exact.
2. Dimensions and tolerancing per ANSI Y14.5M-1982.
3. Dimensions D1 and E1 do not include mold protrusions. Allowable mold protrusion is 0.010 inch (0.25mm) per side. Dimensions D1 and E1 include mold mismatch and are measured at the extreme material condition at the body parting line.
4. To be measured at seating plane -C- contact point.
5. Centerline to be determined where center leads exit plastic body.
6. "N" is the number of terminal positions.

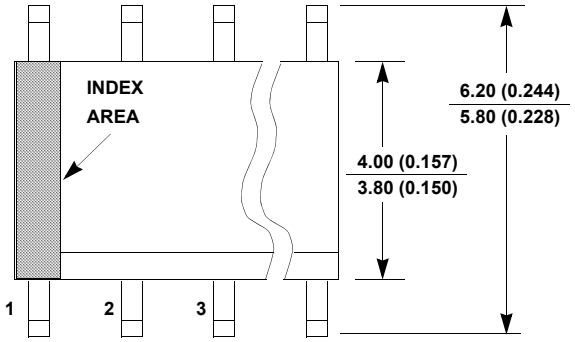
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Package Outline Drawing

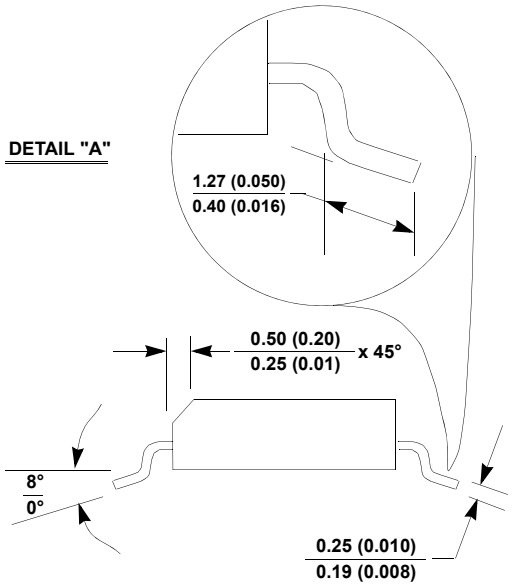
M8.15

8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

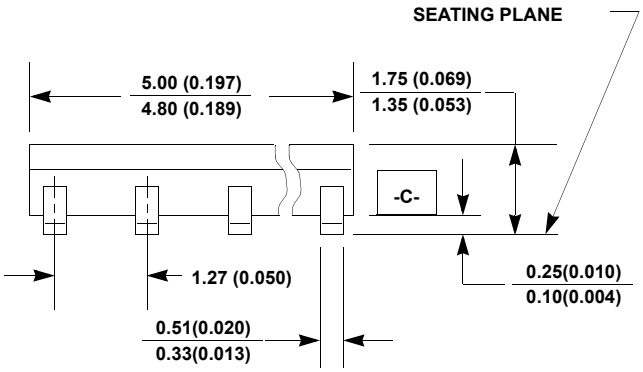
Rev 4, 1/12



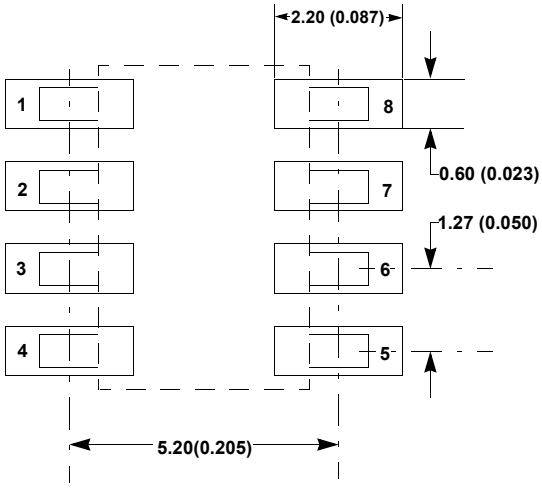
TOP VIEW



SIDE VIEW "B"



SIDE VIEW "A"



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimensioning and tolerancing per ANSI Y14.5M-1994.
2. Package length does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
3. Package width does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
4. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
5. Terminal numbers are shown for reference only.
6. The lead width as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
7. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.
8. This outline conforms to JEDEC publication MS-012-AA ISSUE C.

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