Stepping Motor Driver Series

Microstep 36V Series Stepping Motor Driver

BD63860EFV

No.12009EAT09

●Description

BD63860EFV is a high-grade stepping motor driver with an internal 3-bit DAC, designed to drive bipolar stepping motors in eighth-step modes. The IC features several integrated protection circuits and achieves excellent thermal dissipation performance due to its low ON-resistance DMOS output transistors and high-dissipation power package.
This IC is rated for 36 V maximum input voltage / 2.5 A maximum output current and employs a constant-current, PWM allowing for full-, half-, quarter- and eighth-step excitation modes. Additionally, the current decay mode can be freely set to a ratio of fast and slow decay, allowing the IC to adapt to the optimum control conditions for every motor.
The single-power supply configuration allows for easy design and layout in the application.

●Features

1) Single power supply input (Vin max. 36 V)
2) Rated output current: 2.5 A (peak)
3) Low ON-resistance DMOS output (0.8 Ω total across upper + lower FETs)
4) Serial/CLK-IN drive mode (integrated translator circuit)
5) PWM constant-current control (fixed chopping frequency)
6) Built-in spike noise cancel function (external noise filter is unnecessary)
7) Full-, half-, quarter- and eighth-step functionality
8) AUTO decay mode
9) Current decay mode switching function (linearly variable fast/slow decay ratio)
10) Normal rotation & reverse rotation switching function
11) Power-save function
12) Built-in logic input pull-down resistor
13) Power-on reset function
14) Thermal shutdown circuit (TSD)
15) Over-current protection circuit (OCP)
16) Under-voltage lockout circuit (UVLO)
17) Over-voltage lockout circuit (OVLO)
18) Ghost Supply Prevention (protects against malfunction when power supply is disconnected)
19) Micro-miniature, ultra-thin and high heat-radiation (exposed metal type) HTSSOP package

●Applications

Laser printers, multi-function printers, inkjet printers, scanners, mini printers, PPCs, photo printers, etc.

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●**Absolute maximum ratings** (Ta = 25°C)

Parameter	Symbol	Limit	Unit
Supply voltage	$V_{CC1,2}$	-0.2 – 36.0	V
Power dissipation	Pd	1.45 *1	W
		4.7 *2	
Control pin input voltage	V_{IN}	-0.2 – 7.0	V
RNF maximum voltage	V_{RNF}	1.0	V
Maximum output current	I_{OUT}	2.5 *3	A / phase
Operating temperature range	T_{opr}	-25 – 85	°C
Storage temperature range	T_{stg}	-55 – 150	°C
Junction temperature	T_{jmax}	150	°C

*1 IC mounted on 70mm x 70mm x 1.6mm glass-epoxy board. Derated at 11.6 mW/°C above Ta = 25°C.
*2 IC mounted on 4-layer recommended board. Derated at 37.6 mW/°C above Ta = 25°C.
*3 Not to exceed Pd, ASO and Tjmax = 150°C.

●**Operating conditions** (Ta = -25 – 85 °C)

Parameter	Symbol	Limit			Unit
		Min	Typ	Max	
Supply voltage	$V_{CC1,2}$	16	24	28	V
Output current(DC)	I_{OUT}		1.5	1.7 *4	A/phase

*4 Not to exceed Pd, ASO.

●**Electrical characteristics** (unless otherwise specified, Ta = 25°C, Vcc1,2 = 24 V)

Item	Symbol	Limit			Unit	Condition
		Min	Typ	Max		
Overall Device						
Circuit current at standby	I_{CCST}	-	0.4	2.0	mA	PS = L
Circuit current	I_{CC}	-	4.0	7.0	mA	PS = H, VREF = 2 V
Control inputs (PS, RESET, ENABLE, CLK, CW/CCW, MODE1, MODE2, SR)						
H level input voltage	V_{INH}	2.0	-	5.5	V	
L level input voltage	V_{INL}	0	-	0.8	V	
H level input current	I_{INH}	38	55	94	µA	V_{IN} = 5.5 V
L level input current	I_{INL}	-10	0	-	µA	V_{IN} = 0 V
Outputs (OUT1A, OUT1B, OUT2A, OUT2B)						
Output ON-resistance	R_{ON}	-	0.8	1.0	Ω	I_{OUT} = 1.5 A, total across top and bottom FET
Output leak current	I_{LEAK}	-	-	10	µA	
Current control						
RNF input current	I_{RNF}	-40	-20	-	µA	RNF = 0 V
VREF input current	I_{VREF}	-2.0	-0.1	-	µA	VREF = 0 V
VREF input voltage range	V_{REF}	0	-	3.2	V	
VCR input current	I_{VCR}	60	100	140	µA	V_{VCR} = 3.3 V
VCR input voltage range	V_{VCR}	3.0	-	5.5	V	
MTH input current	I_{MTH}	-2.0	-0.1	-	µA	MTH = 0 V
MTH input voltage range	V_{MTH}	0	-	3.5	V	
Comparator threshold 1	V_{CTH1}	0.212	0.250	0.288	V	VREF = 2 V, 100%
Comparator threshold 2	V_{CTH2}	0.142	0.177	0.212	V	VREF = 2 V, 70.71%
Comparator threshold 3	V_{CTH3}	0.076	0.096	0.116	V	VREF = 2 V, 38.27%
Minimum on time	t_{ONMIN}	0.21	0.54	0.92	µs	R=39kΩ,C=1000pF

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●Pin function table

No.	Name	Function	No.	Name	Function
1	RNF1	Output current-sense resistor connection	15	VCC2	Power supply terminal
2	N.C.	No connection	16	SR	
3	CW/CCW	Motor rotation direction setting terminal	17	RESET	Reset terminal
4	OUT1A	H-bridge output terminal	18	OUT2B	H-bridge output terminal
5	MTH	Current decay ratio setting terminal	19	CLK	Clock input terminal (for advancing electrical angle)
6	CR1	PWM frequency setting RC connection	20	TEST	Test terminal (connect to GND during normal use)
7	GND	Ground terminal	21	GND	Ground terminal
8	VREF	Output current value setting terminal	22	N.C.	No connection
9	CR2	PWM frequency setting RC connection	23	N.C.	No connection
10	VCR	Decay mode setting terminal	24	N.C.	No connection
11	OUT2A	H-bridge output terminal	25	OUT1B	H-bridge output terminal
12	MODE2	Motor excitation mode setting terminal	26	ENABLE	Output enable terminal
13	MODE1	Motor excitation mode setting terminal	27	PS	Power save terminal
14	RNF2	Output current-sense resistor connection	28	VCC1	Power supply terminal

●Block diagram, application circuit, input/output equivalent circuits

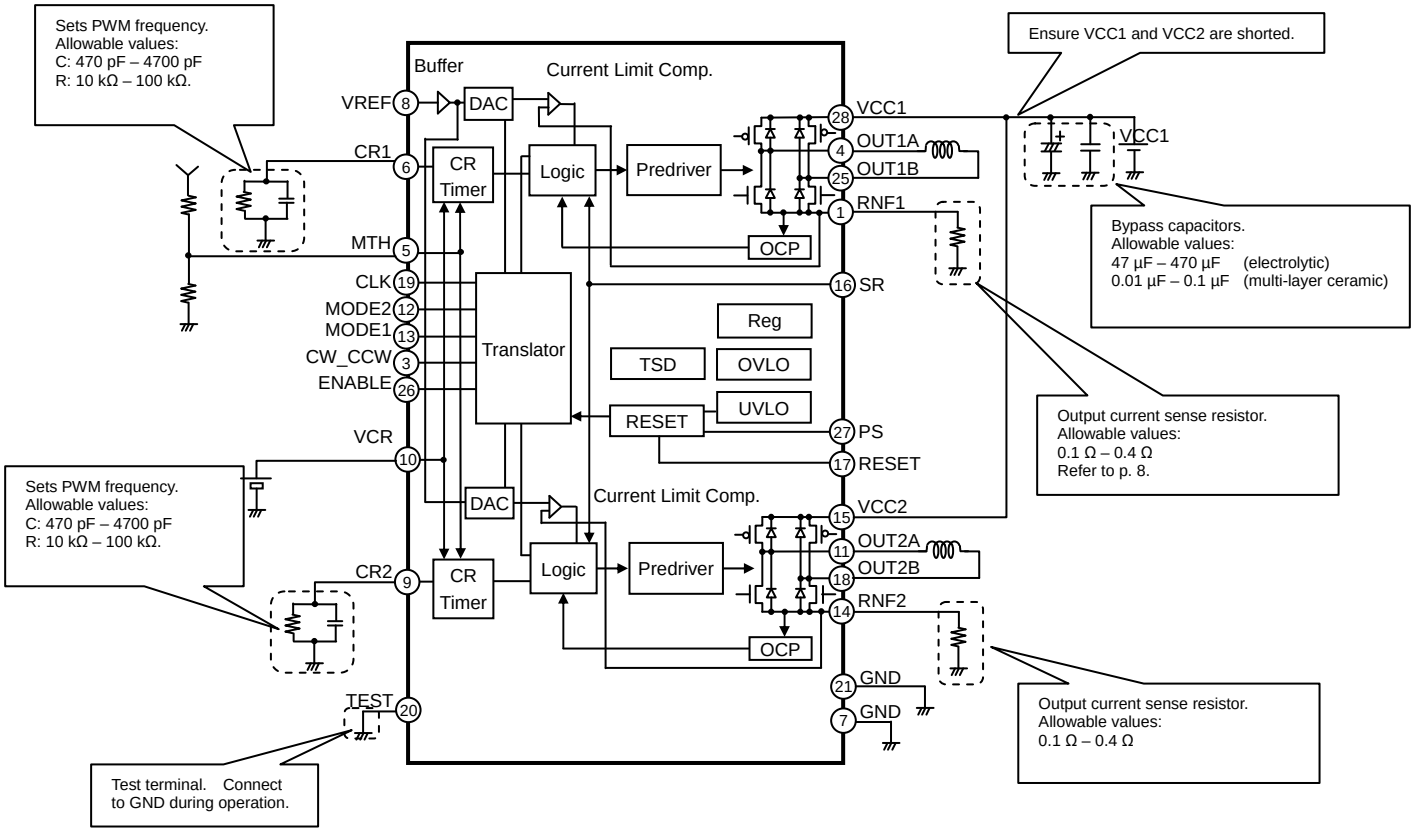


Fig.1 Block Diagram / Application Circuit

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●Pin descriptions

○ CLK – Clock input terminal for advancing output electrical angle

CLK is triggered at the rising edge of the input clock signal. The electrical angle output advances by one step for each CLK pulse input. As the motor may misstep if excessive noise is present on the CLK terminal, the traces leading to this pin should be designed such that noise is kept to a minimum.

○ MODE1, MODE2 – Motor excitation mode terminal

Sets the motor excitation mode. Refer to the following table:

MODE1	MODE2	Excitation mode
L	L	Full Step
H	L	Half Step A
L	H	Quarter Step
H	H	Eighth Step

Refer to pp. 12-13 for the timing chart and motor torque vectors for each excitation mode.
Changes to this pin are not synchronized with the CLK input and will reflect immediately in the operation of the IC (refer to p. 16).

○ CW/CCW – Motor rotation direction setting terminal

Set the motor's rotation direction. Changes to this pin are reflected at the rising edge of the next immediate CLK input pulse after the setting is changed (refer to p. 14).

CW/CCW	Rotation direction
L	Clockwise (Channel 2 current is output with a 90° phase-lag relative to channel 1)
H	Counterclockwise (Channel 2 current is output with a 90° phase-lead relative to channel 1)

○ ENABLE – Output enable terminal

Forcibly turns off all output transistors (leaving the motor output open). When ENABLE is set to a logic HI, the output electrical angle and operating mode is maintained even if a pulse is input to the CLK pin. However, bear in mind that when the ENABLE signal is switched from HI to LO, the output angle may change depending on whether the CLK input is HI or LO (refer to p. 15).

ENABLE	Motor output
L	ACTIVE
H	OPEN (electrical angle maintained)

○ PS – Power save terminal

Switches the IC to standby mode and holds all motor outputs open. Setting the IC to standby mode reinitializes the translator and resets the output angle to the default position (see below). Additionally, when switching from standby to normal mode, a delay of approximately 40μs (max.) occurs before motor output becomes active (refer to p. 11).

PS	State
L	Standby mode (reset)
H	Active mode

The default electrical angle for each excitation mode immediately following a reset is as follows (refer to pp. 12-13):

Excitation mode	Initial electrical angle
Full Step	45°
Half Step A	45°
Quarter Step	45°
Eighth Step	45°

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●Protection Circuits

○ Thermal shutdown (TSD)

This IC features an integrated thermal shutdown for protection against thermal destruction. When the IC's chip temperature rises above 175°C (typ.), the motor output is forced open. When the temperature returns to 150°C or less (typ.), the IC automatically resumes normal operation. However, even if TSD has engaged, the IC may become damaged if heat continues to be absorbed from an external source.

○ Over-current protection (OCP)

This IC features an integrated over-current protection circuit to protect against destruction if the motor outputs are shorted to one another, if VCC is shorted to the motor output, or if the motor output is shorted to GND. The circuit latches the motor output open if current flows above the maximum threshold for 4 µS (typ.), and is disengaged when the IC is power-cycled or if the PS terminal is reset. The OCP circuitry is designed only to protect the IC from irregular conditions (such as motor output shorts) and is not designed to be used as an active security device for the application. Therefore, applications should not be designed under the assumption that this circuitry will engage. After OCP has engaged, if irregular conditions continue after a power cycle or PS pin reset, OCP may engage repeatedly, causing the IC to generate heat or otherwise suffer damage. If the inductance of the IC's input/output wiring is large (e.g., due to long trace length), overload current may flow into the wiring before OCP engages, causing a jump in voltage on the input/output pin that may exceed the IC's absolute maximum rating and damage the IC. Additionally, if the IC conducts a current through the output that is larger than the specified output current rating but lower than the OCP threshold, the IC may heat up beyond its maximum rating (Tjmax = 150°C) and destroy itself. Therefore, ensure that the set output current does not exceeds the IC's maximum output rating.

○ Under-voltage lockout (UVLO)

This IC features an integrated under-voltage lockout function to prevent against output when powered by an insufficient supply voltage. If the supply voltage connected to the VCC terminal drops below 12 V (typ.), the motor output is forced open. This switching voltage threshold has a hysteresis of 1 V (typ.) to prevent malfunction due to noise on the input. This circuit does not function in power-save mode. Also, when driving the IC in serial (CLK-in) mode, the output angle is reinitialized to the default angle upon release of the UVLO circuitry.

○ Over-voltage lockout (OVLO)

This IC features an integrated over-voltage lockout function to prevent against output when powered by a supply voltage exceeding the rated input voltage range. If the supply voltage connected to the VCC terminal reaches 32 V (typ.), the motor output is forced open. This switching voltage threshold has a hysteresis of 1 V (typ.) and a noise-masking period of 4 µs (typ.) to prevent malfunction due to noise on the input. Although the IC features this integrated protection device, it may still be destroyed if the input voltage exceeds the IC's absolute maximum ratings. This circuit does not operate in power-save mode.

○ Ghost supply prevention

This IC features integrated ghost supply protection circuitry, which prevents the IC from being powered by a logic input when the power supply is disconnected or grounded. This circuitry prevents current from flowing through the integrated ESD protection diodes (located between logic input pins and the VCC pin), ensuring that the IC itself or any other peripherals connected to the VCC pin cannot be powered by an input signal on any logic terminals. Therefore, the circuit will not malfunction if a logic signal is input to the IC while the power supply is disconnected or grounded.

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●Power dissipation

○ HTSSOP-B28 package

The HTSSOP-B28 package features a heat-radiating metal slag mounted on the backside of the IC. Ensure that the PCB design incorporates large areas of copper to facilitate heat dissipation as much as possible. As the heat slag is shorted with the substrate of the IC die, ensure that the slag is connected to GND. Connecting the slag to a potential other than GND will cause the chip to malfunction. Also ensure that the backside of the chip is completely and firmly soldered onto the PCB. The ratings specified in this sheet assume the IC has been properly mounted and soldered, and that the PCB has been adequately designed to facilitate heat dissipation.

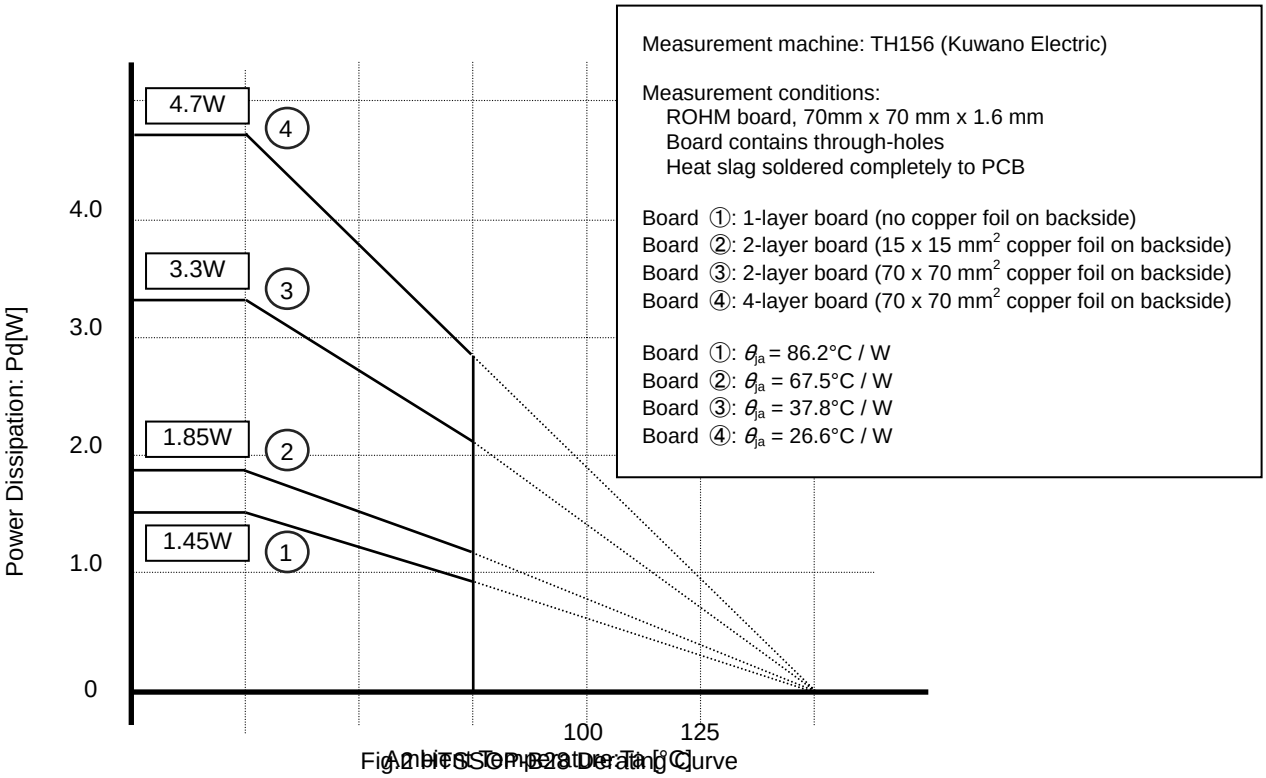


Fig.2 HTSOP-B28 Derating Curve

●Operation Notes

(1) Absolute maximum ratings

Use of the IC in excess of absolute maximum ratings (such as the input voltage or operating temperature range) may result in damage to the IC. Assumptions should not be made regarding the state of the IC (e.g., short mode or open mode) when such damage is suffered. If operational values are expected to exceed the maximum ratings for the device, consider adding protective circuitry (such as fuses) to eliminate the risk of damaging the IC.

(2) Power supply polarity

Connecting the power supply with a reverse polarity can damage IC. Take precautions when connecting the power supply lines. An external diode can be connected to the input for extra protection.

(3) Power supply lines

PCB design should allow for low-impedance GND and supply lines. To minimize noise on these lines, the GND section and supply lines of the digital and analog blocks should be routed separately on the PCB. Furthermore, for all power IC supply terminals, a capacitor should be connected between the power supply and GND terminal. If using electrolytic capacitors, note that their capacitance values may be reduced at lower temperatures.

(4) GND potential

The potential of the GND pin must be the minimum potential in the system in all operating conditions. Ensure that no pins are at a voltage below the GND at any time, regardless of transient characteristics.

(5) Backside heat slag

The metal heat slag integrated on the backside of the IC is connected internally with the backside of the IC die. Therefore, it should always be connected to GND. Connecting to any other potential may cause malfunction or destruction of the IC.

(6) Thermal design

Use a thermal design that allows for a sufficient margin for the package's rated power dissipation (Pd) under actual operating conditions. Keep in mind that the packaging of this IC series has been designed with an exposed heat slag on the backside of the package, and that this heat slag should be soldered completely to as broad a GND pattern as possible (on both the base fin of the slag as well as the entire backside) to improve heat dissipation.

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(7) Inter-pin shorts and mounting errors

Use caution when orienting and positioning the IC for mounting on printed circuit boards. Improper mounting may result in damage to the IC. Shorts between output pins or between output pins and the power supply or GND pins (caused by poor soldering or foreign objects) may result in damage to the IC.

(8) Actions in strong electromagnetic field

The IC is not designed for using in the presence of strong electromagnetic field. Be sure to confirm that no malfunction is found when using the IC in a strong electromagnetic field.

(9) ASO – Area of safe operation

When using the IC, ensure that operating conditions do not exceed absolute maximum ratings or ASO of the output transistors.

(10) Thermal shutdown circuit

The IC incorporates a built-in thermal shutdown circuit, which is designed to force the motor output open if the IC's internal temperature exceeds Tjmax = 150°C. It is not designed to protect the IC from damage or guarantee its operation. ICs should not be used after this function has activated, or in applications where the operation of this circuit is assumed.

TSD on temperature [°C] (Typ.)	Hysteresis Temperature [°C] (Typ.)
175	25

(11) Testing on application boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from a jig or fixture during the evaluation process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

(12) Input terminal of IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. PN junctions are formed at the intersection of these P layers with the N layers of other elements, creating parasitic diodes and/or transistors. For example (refer to the figure below):

When GND > Pin A and GND > Pin B, the PN junction operates as a parasitic diode

When GND > Pin B, the PN junction operates as a parasitic transistor

Parasitic diodes occur inevitably in the structure of the IC, and the operation of these parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Accordingly, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

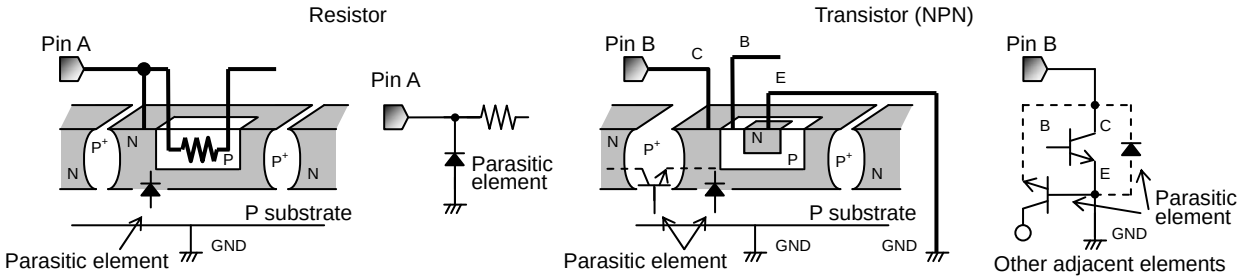


Fig.3 Example of Monolithic IC Structure

(13) Ground wiring patterns

When using both small-signal and large-current GND traces, the two ground traces should be routed separately but connected to a single ground potential within the application in order to avoid variations in the small-signal ground caused by large currents. Also ensure that the GND traces of external components do not cause variations on GND voltage. The power supply and ground lines must be as short and thick as possible to reduce line impedance.

(14) TEST Terminal

Connect the TEST pin to GND during operation.

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●Ordering part number

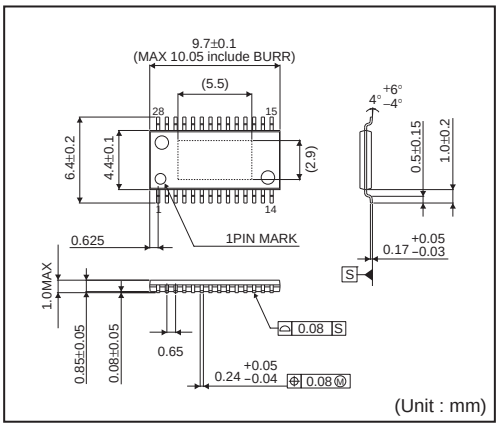
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形名

パッケージ
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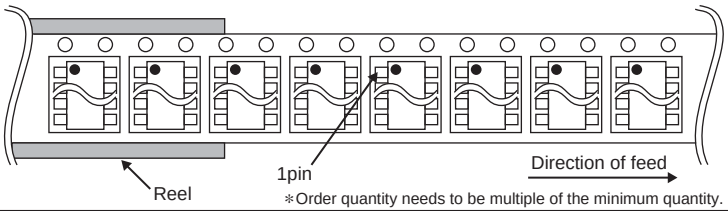
包装、フォーミング仕様
E2: リール状エンボステーピング

HTSSOP-B28



<Tape and Reel information>

Tape	Embossed carrier tape (with dry pack)
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

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CLASSⅣ		CLASSⅢ	

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   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
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   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation (Pd) depending on Ambient temperature (Ta). When used in sealed area, confirm the actual ambient temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

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2. In principle, the reflow soldering method must be used; if flow soldering method is preferred, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
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   - [b] the temperature or humidity exceeds those recommended by ROHM
   - [c] the Products are exposed to direct sunshine or condensation
   - [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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