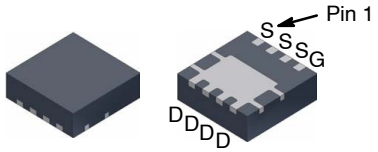
MOSFET – N-Channel, POWERTRENCH®

80 V, 20 A, 23 mΩ

FDMC86324

V_{DS}	$R_{DS(ON)}$ MAX	I_D MAX
80 V	23 mΩ @ 10 V	20 A
	37 mΩ @ 6 V	



Top Bottom

PQFN8 3.3 × 3.3, 0.65P
CASE 483AK

General Description

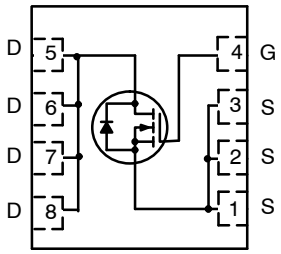
This N−Channel MOSFET is produced using **onsemi**'s advanced POWERTRENCH process that has been especially tailored to minimize the on−state resistance and yet maintain superior switching performance.

Features

- Max $R_{DS(on)}$ = 23 mΩ at V_{GS} = 10 V, I_D = 7 A
- Max $R_{DS(on)}$ = 37 mΩ at V_{GS} = 6 V, I_D = 4 A
- Low Profile − 1 mm Max in Power 33
- 100% UIL Tested
- Pb−Free, Halide Free and RoHS Compliant

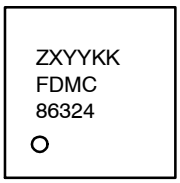
Applications

- DC−DC Conversion



N-CHANNEL MOSFET

MARKING DIAGRAM



Z = Assembly Plant Code
XYY = 3−Digit Date Code Format
KK = 2−Alphanumeric Lot Run Traceability Code
FDMC86324 = Specific Device Code

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted.)

Symbol	Parameter	Value	Unit
V_{DS}	Drain−Source Voltage	80	V
V_{GS}	Gate−Source Voltage	±20	V
I_D	Drain Current − Continuous (Package Limited) T_C = 25°C − Continuous (Silicon Limited) T_C = 25°C − Continuous (Note 1a) T_A = 25°C − Pulsed	 20 30 7 30	A
E_{AS}	Single Pulse Avalanche Energy (Note 3)	72	mJ
P_D	Power Dissipation T_C = 25°C Power Dissipation (Note 1a) T_A = 25°C	41 2.3	W
T_J, T_{STG}	Operating and Storage Junction Temperature Range	−55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case	3	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	53	°C/W

ORDERING INFORMATION

Device	Package	Shipping†
FDMC86324	PQFN8 (Pb−Free, Halide Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

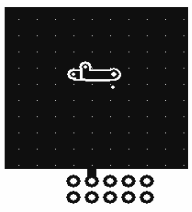
ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V	80	–	–	V
ΔBV_{DSS} /ΔT_J	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25°C	–	69	–	mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 64 V, V_{GS} = 0 V	–	–	1	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20 V, V_{DS} = 0 V	–	–	±100	nA
ON CHARACTERISTICS						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA	2.0	3.1	4.0	V
$\Delta V_{GS(th)}$ /ΔT_J	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25°C	–	–9	–	mV/°C
$R_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 7 A	–	19.1	23	mΩ
		V_{GS} = 6 V, I_D = 4 A	–	25.5	37	
		V_{GS} = 10 V, I_D = 7 A, T_J = 125°C	–	32.5	40	
g_{FS}	Forward Transconductance	V_{DD} = 10 V, I_D = 7 A	–	19	–	S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 50 V, V_{GS} = 0 V, f = 1 MHz	–	725	965	pF
C_{oss}	Output Capacitance		–	175	235	pF
C_{rss}	Reverse Transfer Capacitance		–	15	25	pF
R_g	Gate Resistance		–	0.5	–	Ω
SWITCHING CHARACTERISTICS						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 50 V, I_D = 7 A, V_{GS} = 10 V, R_{GEN} = 6 Ω	–	8	17	ns
t_r	Rise Time		–	4	10	ns
$t_{d(off)}$	Turn-Off Delay Time		–	14	25	ns
t_f	Fall Time		–	4	10	ns
$Q_{g(TOT)}$	Total Gate Charge	V_{GS} = 0 V to 10 V, V_{DD} = 50 V, I_D = 7 A	–	13	18	nC
		V_{GS} = 0 V to 5 V, V_{DD} = 50 V, I_D = 7 A	–	8	11	nC
Q_{gs}	Gate to Source Charge	V_{DD} = 50 V, I_D = 7 A	–	3.7	–	nC
Q_{gd}	Gate to Drain “Miller” Charge	V_{DD} = 50 V, I_D = 7 A	–	3.6	–	nC
DRAIN-SOURCE DIODE CHARACTERISTICS						
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = 7 A (Note 2)	–	0.81	1.3	V
		V_{GS} = 0 V, I_S = 2 A (Note 2)	–	0.75	1.2	
t_{rr}	Reverse Recovery Time	I_F = 7 A, di/dt = 100 A/μs	–	44	70	ns
Q_{rr}	Reverse Recovery Charge		–	40	65	nC

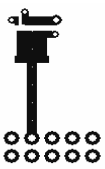
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTES:

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a 1.5 × 1.5 in. board of FR−4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user’s board design.



a) 53°C/W when mounted on a 1 in^2 pad of 2 oz. copper.



b) 125°C/W when mounted on a minimum pad of 2 oz. copper.

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.
3. Starting T_J = 25°C; N-ch: L = 1 mH, I_{AS} = 12 A, V_{DD} = 72 V, V_{GS} = 10 V.

TYPICAL CHARACTERISTICS

(T_J = 25°C unless otherwise noted)

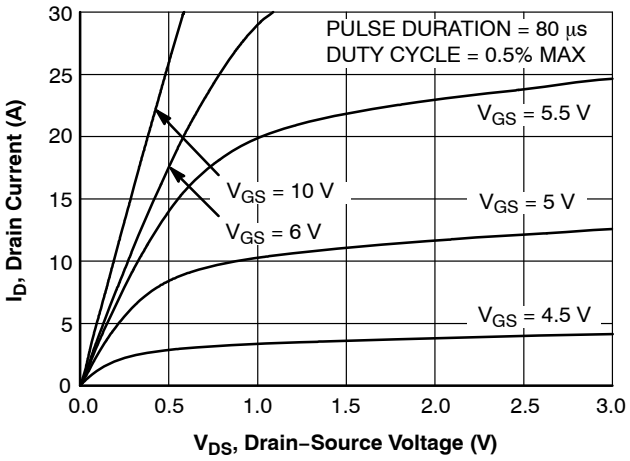


Figure 1. On−Region Characteristics

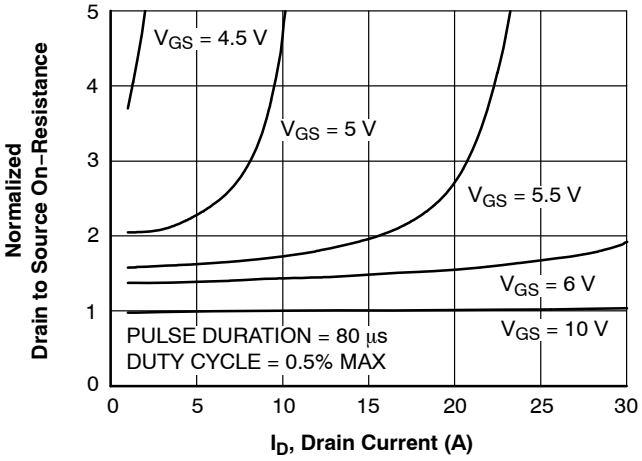


Figure 2. Normalized On−Resistance vs. Drain Current and Gate Voltage

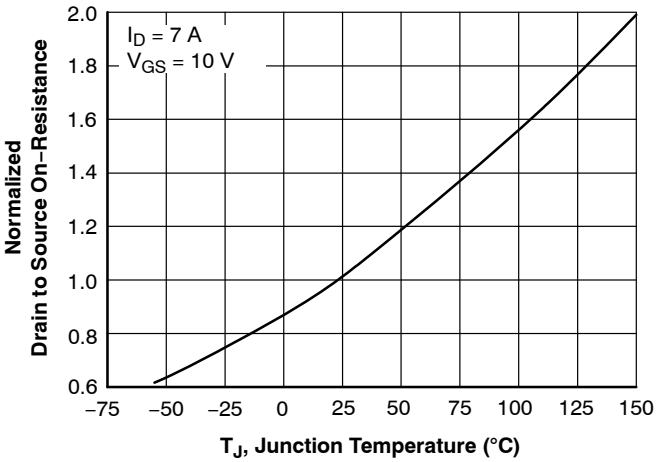


Figure 3. Normalized On−Resistance vs. Junction Temperature

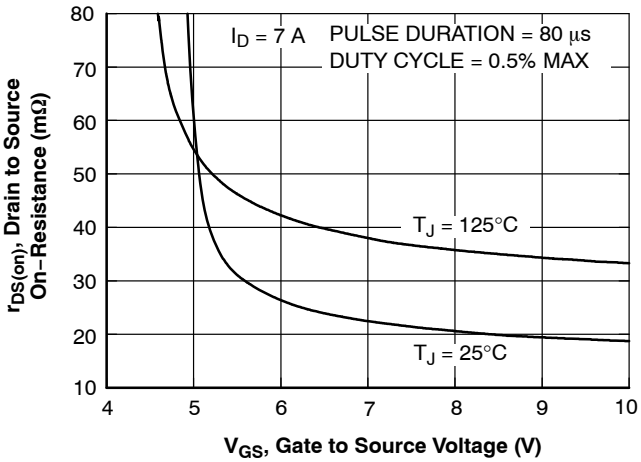


Figure 4. On−Resistance vs. Gate to Source Voltage

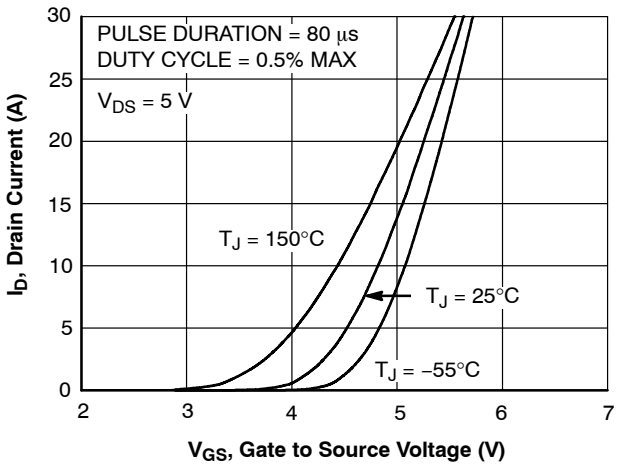


Figure 5. Transfer Characteristics

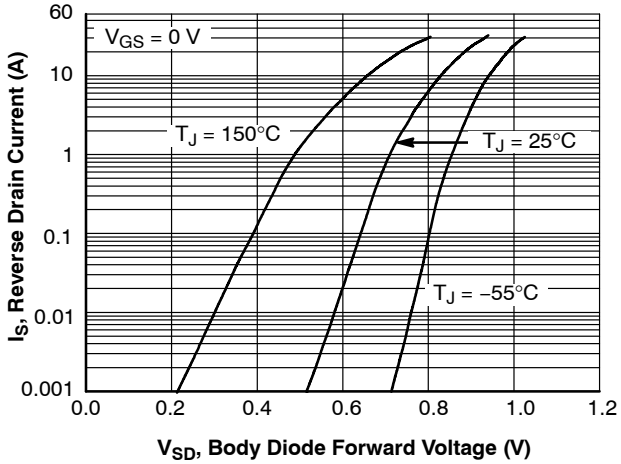


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS (CONTINUED)

(T_J = 25°C unless otherwise noted)

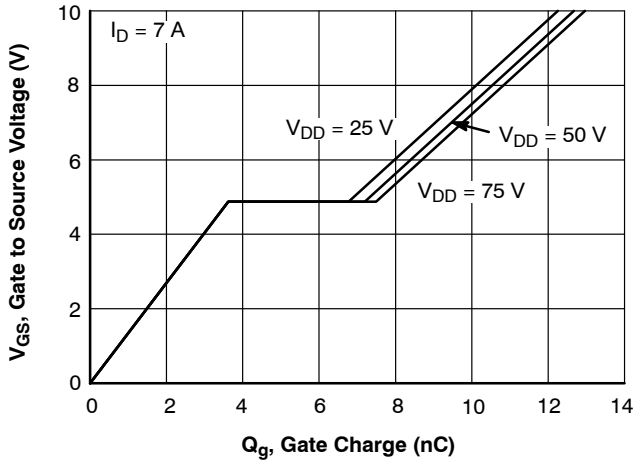


Figure 7. Gate Charge Characteristics

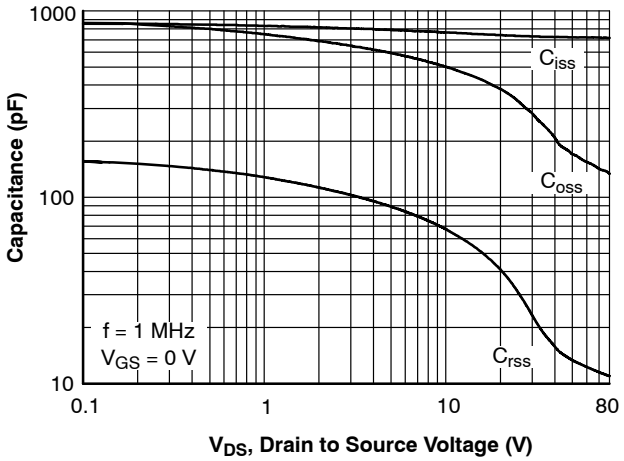


Figure 8. Capacitance vs. Drain to Source Voltage

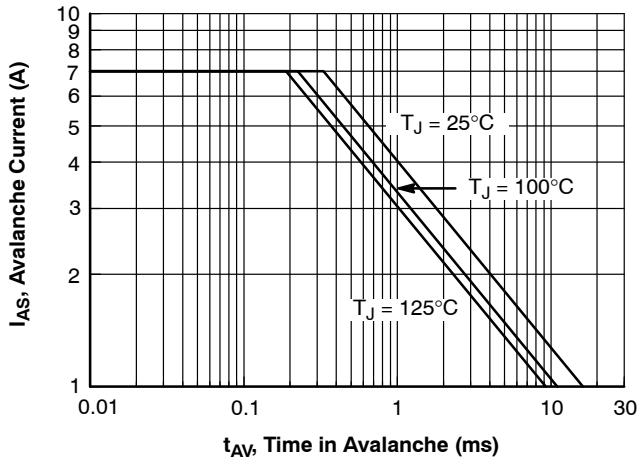


Figure 9. Unclamped Inductive Switching Capability

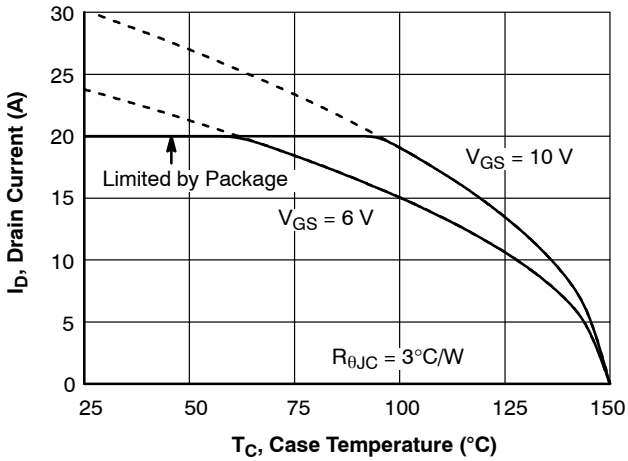


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

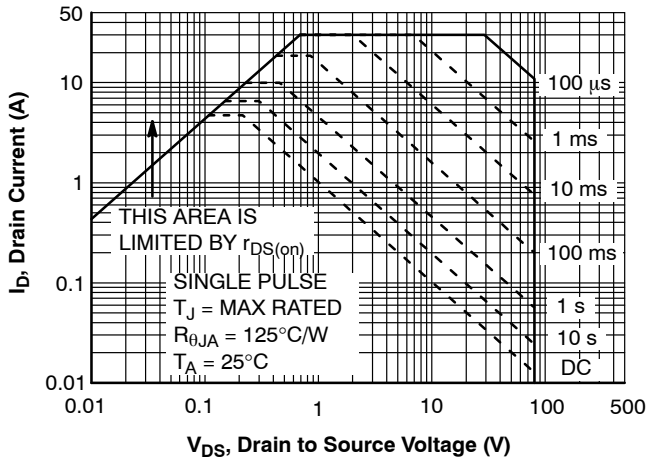


Figure 11. Forward Bias Safe Operating Area

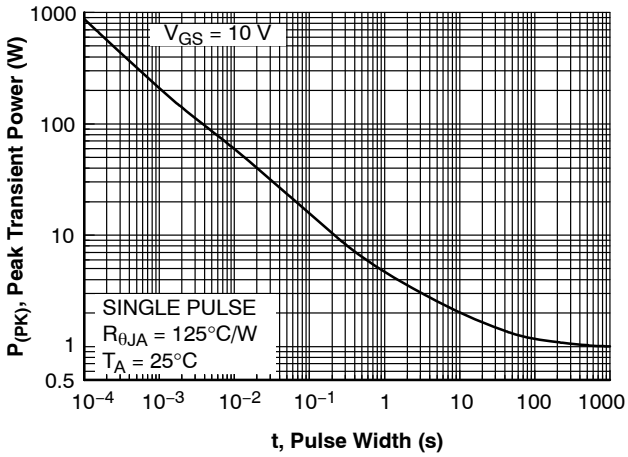


Figure 12. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS (CONTINUED)

(T_J = 25°C unless otherwise noted)

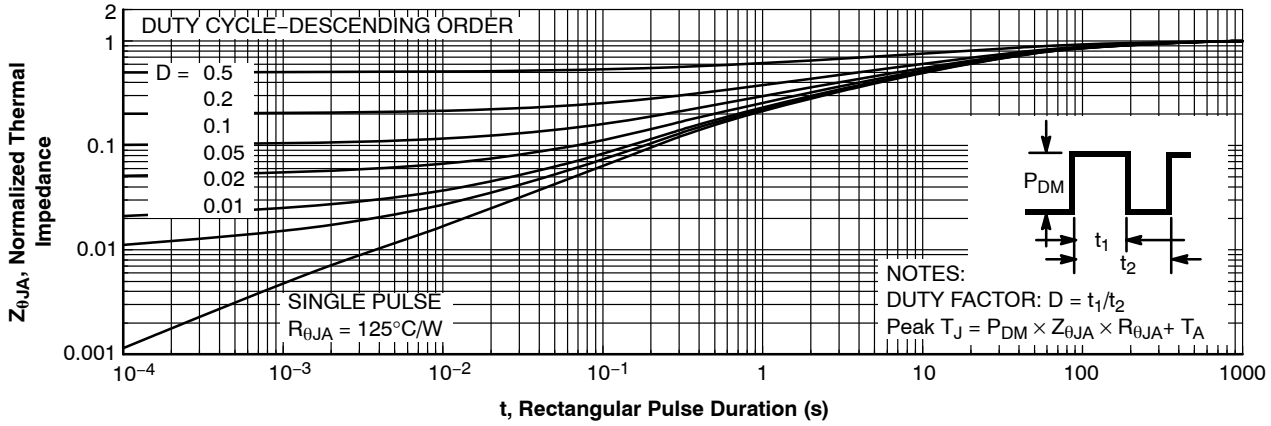
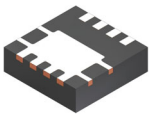
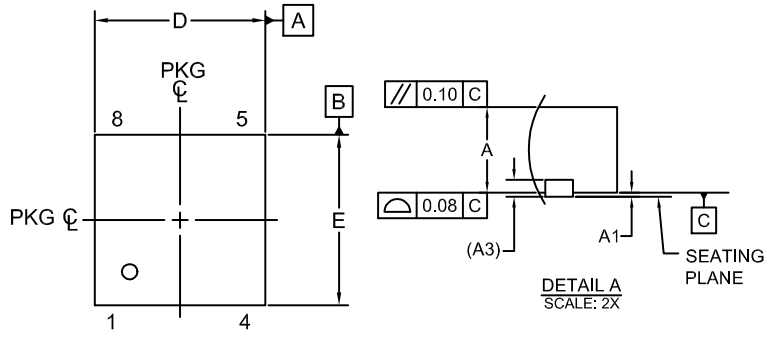


Figure 13. Junction−to−Ambient Transient Thermal Response Curve

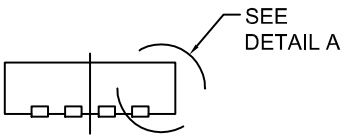


PQFN8 3.3X3.3, 0.65P
CASE 483AK
ISSUE B

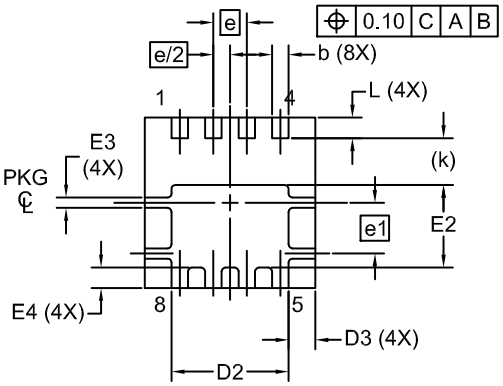
DATE 12 OCT 2021



TOP VIEW



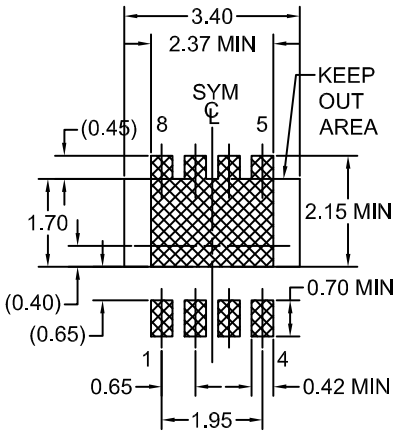
FRONT VIEW



BOTTOM VIEW

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
5. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
6. IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.



LAND PATTERN RECOMMENDATION

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0.00	-	0.05
A3	0.20 REF		
b	0.27	0.32	0.37
D	3.20	3.30	3.40
D2	2.17	2.27	2.37
D3	0.42	0.52	0.62
E	3.20	3.30	3.40
E2	1.50	1.60	1.70
E3	0.10	0.20	0.30
E4	0.29	0.39	0.49
e	0.65 BSC		
e/2	0.325 BSC		
e1	0.98 BSC		
k	0.91 REF		
L	0.30	0.40	0.50

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DESCRIPTION:	**PQFN8 3.3X3.3, 0.65P**		**PAGE 1 OF 1**

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