

# MCXA175/176/185/186/255/256/265/266

Enhanced Arm Cortex-M33 MCU with 180/240 MHz, up to 1024 KB Flash, and Security

Rev. 3 — 14 November 2025

Product data sheet

## Features

- Arm® Cortex®-M33 180MHz with 738 CoreMark® (4.10 CoreMark®/MHz) for MCXA175/176/255/256
- Arm Cortex-M33 240MHz with 984 CoreMark (4.10 CoreMark/MHz) for MCXA185/186/265/266
- Up to 1 MB Flash, 256 KB SRAM, up to 8 KB RAM with ECC
- All RAM can be retained down to Deep Power Down mode
- Internal free running oscillator (FRO180M) with  $\pm 1\%$  precision across the full temperature range
- Temperature range: -40 °C to 125 °C
- Down to 78  $\mu\text{A}/\text{MHz}$  Active current, 96  $\mu\text{A}$  Deep Sleep current, 32  $\mu\text{A}$  Power Down current, 473 nA Deep Power Down current

## Cores

- Arm 32-bit Cortex-M33 CPU, with FPU and DSP extension instruction set and MPU, no Trust Zone

## Processing Accelerators

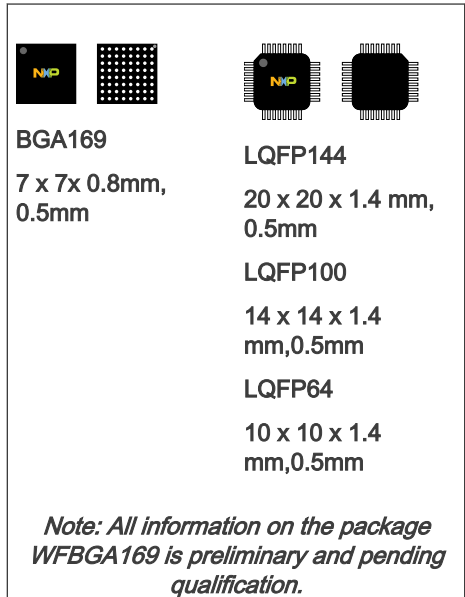
- SmartDMA, co-processor for applications such as parallel camera interface and keypad scanning

## Memories

- Single-bank Flash: Up to 1024 KB Flash with ECC (support one bit correction and two bits detection)
- Cache Engine with 8 KB RAM
- Up to 256 KB RAM of which 8 KB is shared with cache, configurable as up to 8 KB RAM with ECC (support one bit correction and two bits detection)
- All RAM can be retained down to Deep Power Down mode
- ROM

## Security

- EdgeLock Accelerator
  - TRNG
  - PKC (Public Key Cryptography), supports ECC and RSA encryption and decryption
  - SGI (Secure Generic Interface), provides AES256, SHA-2 and key generation/derivation
  - Secure key store with key usage policies (protection of platform integrity, manufacturing and applications keys)
- 128-bit Universal Unique Identifier (UUID) per device in accordance with IETF's RFC4122 version5 specification
- Device lifecycle management
- Flash read/write/execute permission protect by MBC and lockable



- Implicit-protected Flash Region (IFR)
- Security Monitoring:
  - Code Watchdog for code flow integrity checking
  - 6x Passive anti tamper pin detect
  - GLIKEY enforces security checks before allowing a write to security-sensitive register
- Secure Installer for secure manufacturing and IP theft protection in untrusted factory

#### Low-Power Performance

- **Active**
  - 78  $\mu$ A/MHz, in Active Mode (executing while(1) from flash, 3.3 V@25 °C)
- **Deep Sleep**
  - 96  $\mu$ A, 9.01  $\mu$ s wake-up (3.3 V@25 °C)
- **Power Down**
  - 32  $\mu$ A, 18.84  $\mu$ s wake-up (full SRAM retention, 3.3 V@25 °C)
- **Deep Power Down**
  - 473 nA, 1.57 ms wake-up (wake-up timer disabled, reset pin enabled, all SRAM off, 3.3 V@25 °C)

#### System and Clocks

- 180 MHz free-running oscillator (FRO180M)
  - Can be configured to 240MHz via software, applicable only to MCXA18x and MCXA26x devices
- 12 MHz free-running oscillator (FRO12M)
- 16 KHz free-running oscillator (FRO16K)
- Up to 50 MHz crystal oscillator
- One PLL
- Hardware and Software Watchdogs
- Asynchronous DMA modules (8-channels)

#### Communication Interfaces for Connectivity

- 2x LPSPI, 4x LPI2C, 6x LPUART
  - MCXA175/176/255/256 support 5x LPUART
- 1x I3C
- USB Full-speed (Device/Host) with on-chip FS PHY
- Up to 2x FlexCAN with FD
- FlexIO

#### Human Machine Interface

- 4 x 44 segment LCD interface

#### Advanced Motor Control

- Up to 2x FlexPWM, each FlexPWM has 4 sub-modules, providing 8 complementary outputs of PWM (no Nanoedge module)
- Up to 2x Quadrature Encoder/Decoder (eQDC)
- 2x AOI (AND/OR/Invert) module support up to 4 output triggers

**Analog**

- 2x 16-bit ADC
  - Up to 3.2 Msps in 16-bit mode, and 4 Msps in 12-bit mode
  - Up to 43 ADC Input channels total (depending on the package)
  - Integrated temperature sensor
- 1 x 12-bit DAC
  - Up to 1 Msps
- 2 x High-speed Comparators with 8 input pins and 8-bit DAC as internal reference
  - 1x LPCMP is functional down to Deep Power Down mode
- 1x OPAMP without PGA

**Timers**

- 5x 32-bit standard general-purpose asynchronous timers/counters (CTimer), each CTimer supports up to 4x capture inputs and 4x compare outputs, 3x PWM outputs. Specific timer events can be selected to generate DMA requests.
- Low power timer
- Frequency measurement timer
- Windowed watchdog timer
- Wake timer
- Micro-tick timer (UTICK)
- OS event timer
- RTC timer without external 32KHz input

**General-purpose input/outputs**

- Up to 114 GPIOs
- Up to eight 20 mA IO
- 50 MHz IO on P1, P3 and P4
- Up to 29-pin wake-up sources function down to deep power-down mode
- Support 1.71 V~3.6 V IO supply range

**Power Management**

- Integrated voltage regulator
  - Core LDO, other LDOs
- Operating voltage: 1.71 V to 3.6 V
- IOs: 1.71 V - 3.6 V full-performance

**Target Applications****Industrial**

- Energy Storage and Management System
- Smart Metering
- Factory Automation
- Industrial HMI
- Mobile Robotics Ecosystem

- Motion Control and Robotics
- Motor Drives
- Brushless DC Motor (BLDC) Control
- Permanent Magnet Synchronous Motor (PMSM) Control

## Smart Home

- Home Control Panel
- Major Home Appliances
- Robotic Appliance
- Smart Speaker
- Soundbar
- Gaming Accessories
- Smart Lighting
- Smart Power Socket and Light Switch

Table 1. Ordering Information

| Part Number <sup>[1][2]</sup> | Marking    | Core Speed (MHz) | Flash (KB) | SRAM (KB) | GPIO | Pin Count | Package |
|-------------------------------|------------|------------------|------------|-----------|------|-----------|---------|
| MCXA175VPN                    | MCXA175VPN | 180              | 512        | 128       | 114  | 169       | WFBGA   |
| MCXA175VLQ                    | MCXA175VLQ | 180              | 512        | 128       | 114  | 144       | LQFP    |
| MCXA175VLL                    | MCXA175VLL | 180              | 512        | 128       | 83   | 100       | LQFP    |
| MCXA175VLH                    | MCXA175VLH | 180              | 512        | 128       | 52   | 64        | LQFP    |
| MCXA176VPN                    | MCXA176VPN | 180              | 1024       | 256       | 114  | 169       | WFBGA   |
| MCXA176VLQ                    | MCXA176VLQ | 180              | 1024       | 256       | 114  | 144       | LQFP    |
| MCXA176VLL                    | MCXA176VLL | 180              | 1024       | 256       | 83   | 100       | LQFP    |
| MCXA176VLH                    | MCXA176VLH | 180              | 1024       | 256       | 52   | 64        | LQFP    |
| MCXA185VPN                    | MCXA185VPN | 240              | 512        | 128       | 114  | 169       | WFBGA   |
| MCXA185VLQ                    | MCXA185VLQ | 240              | 512        | 128       | 114  | 144       | LQFP    |
| MCXA185VLL                    | MCXA185VLL | 240              | 512        | 128       | 83   | 100       | LQFP    |
| MCXA185VLH                    | MCXA185VLH | 240              | 512        | 128       | 52   | 64        | LQFP    |
| MCXA186VPN                    | MCXA186VPN | 240              | 1024       | 256       | 114  | 169       | WFBGA   |
| MCXA186VLQ                    | MCXA186VLQ | 240              | 1024       | 256       | 114  | 144       | LQFP    |
| MCXA186VLL                    | MCXA186VLL | 240              | 1024       | 256       | 83   | 100       | LQFP    |
| MCXA186VLH                    | MCXA186VLH | 240              | 1024       | 256       | 52   | 64        | LQFP    |
| MCXA255VPN                    | MCXA255VPN | 180              | 512        | 128       | 114  | 169       | WFBGA   |
| MCXA255VLQ                    | MCXA255VLQ | 180              | 512        | 128       | 114  | 144       | LQFP    |
| MCXA255VLL                    | MCXA255VLL | 180              | 512        | 128       | 83   | 100       | LQFP    |
| MCXA255VLH                    | MCXA255VLH | 180              | 512        | 128       | 52   | 64        | LQFP    |

Table continues on the next page...

Table 1. Ordering Information ...continued

| Part Number [1][2] | Marking    | Core Speed (MHz) | Flash (KB) | SRAM (KB) | GPIO | Pin Count | Package |
|--------------------|------------|------------------|------------|-----------|------|-----------|---------|
| MCXA256VPN         | MCXA256VPN | 180              | 1024       | 256       | 114  | 169       | WFBGA   |
| MCXA256VLQ         | MCXA256VLQ | 180              | 1024       | 256       | 114  | 144       | LQFP    |
| MCXA256VLL         | MCXA256VLL | 180              | 1024       | 256       | 83   | 100       | LQFP    |
| MCXA256VLH         | MCXA256VLH | 180              | 1024       | 256       | 52   | 64        | LQFP    |
| MCXA265VPN         | MCXA265VPN | 240              | 512        | 128       | 114  | 169       | WFBGA   |
| MCXA265VLQ         | MCXA265VLQ | 240              | 512        | 128       | 114  | 144       | LQFP    |
| MCXA265VLL         | MCXA265VLL | 240              | 512        | 128       | 83   | 100       | LQFP    |
| MCXA265VLH         | MCXA265VLH | 240              | 512        | 128       | 52   | 64        | LQFP    |
| MCXA266VPN         | MCXA266VPN | 240              | 1024       | 256       | 114  | 169       | WFBGA   |
| MCXA266VLQ         | MCXA266VLQ | 240              | 1024       | 256       | 114  | 144       | LQFP    |
| MCXA266VLL         | MCXA266VLL | 240              | 1024       | 256       | 83   | 100       | LQFP    |
| MCXA266VLH         | MCXA266VLH | 240              | 1024       | 256       | 52   | 64        | LQFP    |

[1] As marked on package

[2] To confirm current availability of orderable part numbers, go to <http://www.nxp.com> and perform a part number search.

Table 2. Device Revision Number

| Device Mask Set Number | JTAG ID Register[PRN] |
|------------------------|-----------------------|
| 0P89K                  | 0x0726802B            |

Table 3. Related Resources

| Type                     | Description                                                                                                                          | Resource                                                                                                                                                                                                         |
|--------------------------|--------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Fact Sheet               | The Fact Sheet gives overview of the product key features and its uses.                                                              | MCXA1xx_FS and MCXA2xx_FS                                                                                                                                                                                        |
| Reference Manual         | The Reference Manual contains a comprehensive description of the structure and function (operation) of a device.                     | MCXAP144M240F61RM                                                                                                                                                                                                |
| Data Sheet               | The Data Sheet includes electrical characteristics and signal connections.                                                           | This document                                                                                                                                                                                                    |
| Chip Errata              | The chip mask set Errata provides additional or corrective information for a particular device mask set.                             | MCXA266VLQ_0P89K                                                                                                                                                                                                 |
| Package drawing          | Package dimensions are provided in package drawings.                                                                                 | <ul style="list-style-type: none"> <li>WFBGA169: 98ASA02230D</li> <li>LQFP144: <a href="#">98ASS23177W</a></li> <li>LQFP100: <a href="#">98ASS23308W</a></li> <li>LQFP64: <a href="#">98ASS23234W</a></li> </ul> |
| Software development kit | MCUXpresso SDK. An open source software development kit (SDK) built specifically for your processor and evaluation board selections. | <a href="http://www.nxp.com/mcuxpresso">http://www.nxp.com/mcuxpresso</a>                                                                                                                                        |

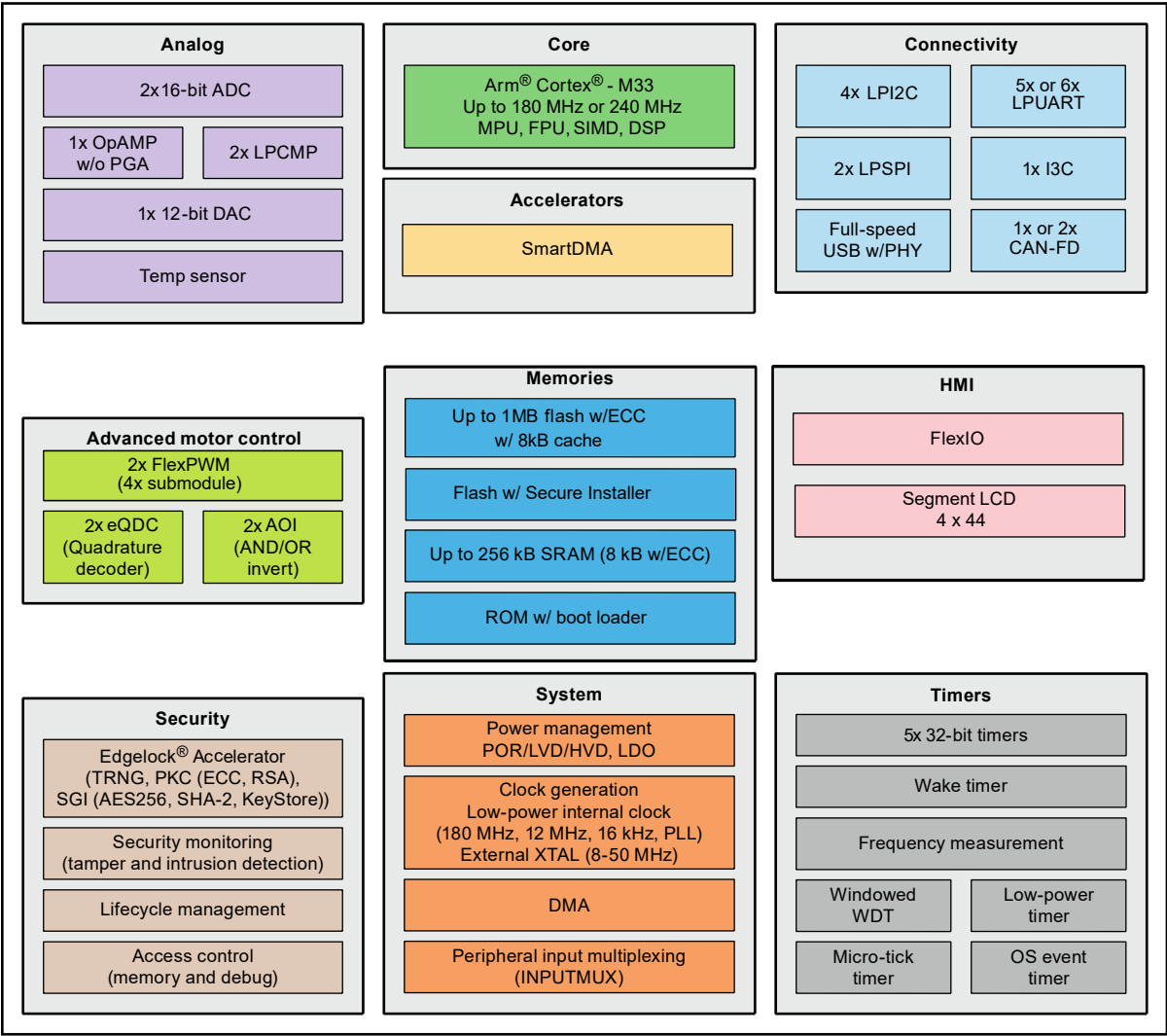
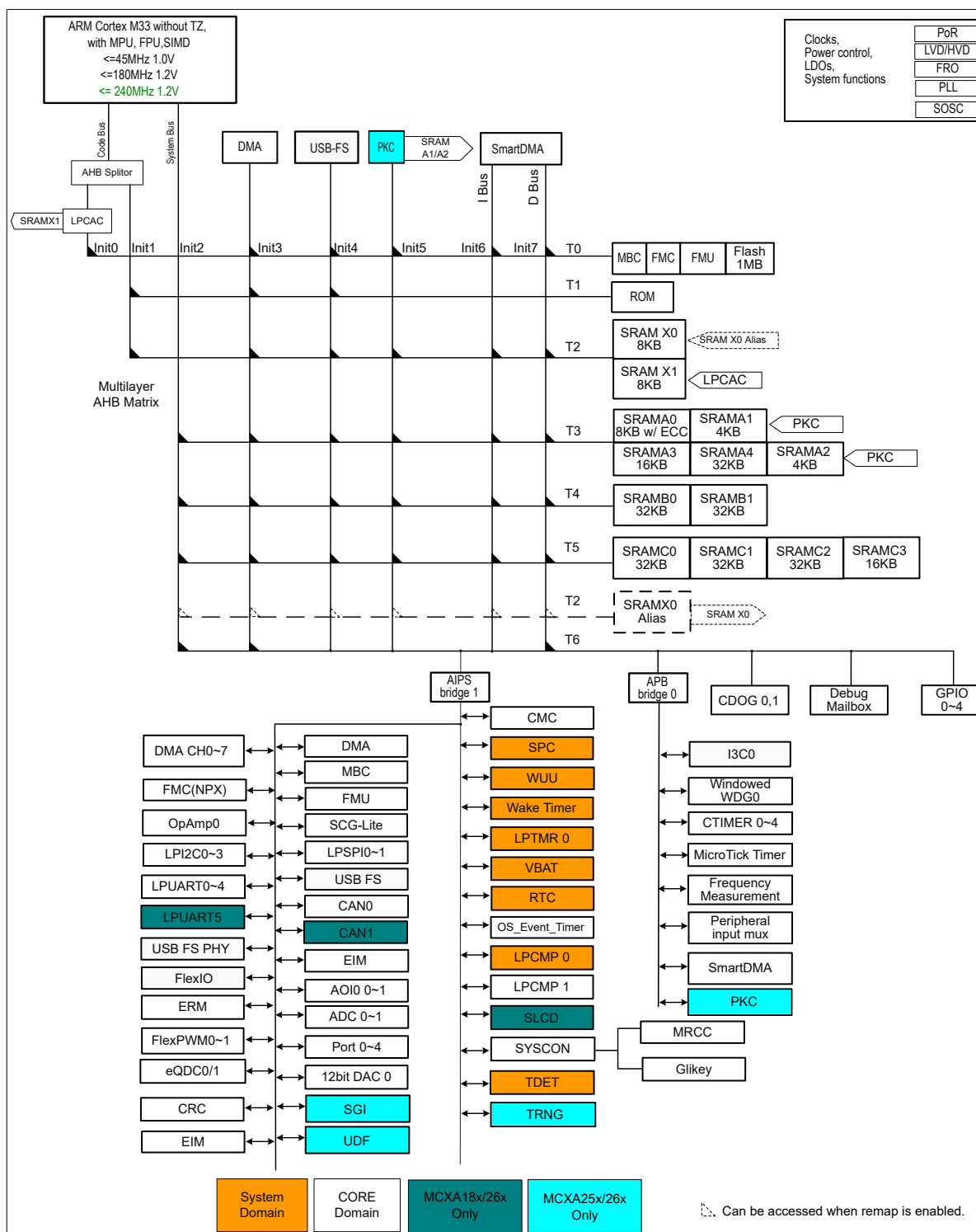


Figure 1. Block Diagram



### Figure 2. Bus Architecture

## 1 Feature Comparison

Table 4. Feature Comparison

|                           |                                                                                                                                         | MCX<br>A175               | MCX<br>A176 | MCX<br>A255 | MCX<br>A256 | MCX<br>A185                       | MCX<br>A186 | MCX<br>A265 | MCX<br>A266 |
|---------------------------|-----------------------------------------------------------------------------------------------------------------------------------------|---------------------------|-------------|-------------|-------------|-----------------------------------|-------------|-------------|-------------|
| Core Platform             | Core Cortex-M33                                                                                                                         | 180 MHz                   |             |             |             | 240 MHz                           |             |             |             |
|                           | Cache                                                                                                                                   | 8KB                       |             |             |             |                                   |             |             |             |
|                           | DMA                                                                                                                                     | 8 Channels                |             |             |             |                                   |             |             |             |
|                           | Wakeup unit(WUU)                                                                                                                        | Yes                       |             |             |             |                                   |             |             |             |
|                           | Pheripheral input multiplexing(INPUTMUX)                                                                                                | Yes                       |             |             |             |                                   |             |             |             |
| Processing Accelerators   | MAU                                                                                                                                     | No                        |             |             |             |                                   |             |             |             |
|                           | SmartDMA                                                                                                                                | Yes                       |             |             |             |                                   |             |             |             |
| Clock                     | Fast internal reference clock FRO180M                                                                                                   | 180 MHz                   |             |             |             | 180 MHz (or configure to 240 MHz) |             |             |             |
|                           | Slow internal reference clock FRO12M                                                                                                    | 12 MHz                    |             |             |             |                                   |             |             |             |
|                           | Low power internal reference clock FRO16K                                                                                               | 16.384 KHz                |             |             |             |                                   |             |             |             |
|                           | System oscillator with external crystal(SOSC)                                                                                           | 8 - 50 MHz                |             |             |             |                                   |             |             |             |
|                           | PLL                                                                                                                                     | Yes                       |             |             |             |                                   |             |             |             |
| Memory                    | Flash<br><br>512KB version include 8KB CMPA<br><br>1024KB version include 8KB CMPA<br><br>MCXA25x/26x include 56KB for Secure Installer | 512 KB                    | 1024 KB     | 512 KB      | 1024 KB     | 512 KB                            | 1024 KB     | 512 KB      | 1024 KB     |
|                           | SRAM<br><br>128KB version include 8KB with ECC<br><br>256KB version include 8KB with ECC and include 8KB SRAM shared with Cache         | 128 KB                    | 256 KB      | 128 KB      | 256 KB      | 128 KB                            | 256 KB      | 128 KB      | 256 KB      |
|                           | Error injection module (EIM)                                                                                                            | Yes                       |             |             |             |                                   |             |             |             |
|                           | Error recording module (ERM)                                                                                                            | Yes                       |             |             |             |                                   |             |             |             |
|                           | Security                                                                                                                                | Lifecycle management (LC) | Yes         |             |             |                                   |             |             |             |
| Read out protection (ROP) |                                                                                                                                         | Yes                       |             |             |             |                                   |             |             |             |

Table continues on the next page...

Table 4. Feature Comparison...continued

|                             |                                       |              | MCX<br>A175 | MCX<br>A176 | MCX<br>A255 | MCX<br>A256 | MCX<br>A185 | MCX<br>A186 | MCX<br>A265 | MCX<br>A266 |
|-----------------------------|---------------------------------------|--------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|
|                             | Memory block checker (MBC)            |              | Yes         |             |             |             |             |             |             |             |
|                             | GLIKEY                                |              | Yes         |             |             |             |             |             |             |             |
|                             | UUID                                  |              | 128-bit     |             |             |             |             |             |             |             |
|                             | Code watchdog (CDOG)                  |              | 1           | 2           |             | 1           |             | 2           |             |             |
|                             | Cyclic redundancy check (CRC)         |              | 1           |             |             |             |             |             |             |             |
|                             | Secure key management                 |              | No          | Yes         |             | No          |             | Yes         |             |             |
|                             | AES-256 <sup>[1]</sup>                |              | No          | Yes         |             | No          |             | Yes         |             |             |
|                             | SHA2 <sup>[1]</sup>                   |              | No          | Yes         |             | No          |             | Yes         |             |             |
|                             | PKC <sup>[1]</sup>                    |              | No          | Yes         |             | No          |             | Yes         |             |             |
|                             | TRNG <sup>[1]</sup>                   |              | No          | Yes         |             | No          |             | Yes         |             |             |
|                             | AGDET <sup>[1]</sup>                  |              | No          | Yes         |             | No          |             | Yes         |             |             |
|                             | Debug control <sup>[1]</sup>          |              | No          | Yes         |             | No          |             | Yes         |             |             |
|                             | Secure installer <sup>[1]</sup>       |              | No          | Yes         |             | No          |             | Yes         |             |             |
|                             | Passive anti<br>tamper pin            | WFBGA169(PN) | 6           |             |             |             |             |             |             |             |
|                             |                                       | LQFP144(LQ)  | 6           |             |             |             |             |             |             |             |
| LQFP100(LL)                 |                                       | 4            |             |             |             |             |             |             |             |             |
| LQFP64(LH)                  |                                       | 2            |             |             |             |             |             |             |             |             |
| Communication<br>Interfaces | LPUART                                |              | 5           |             |             |             | 6           |             |             |             |
|                             | LPSPi                                 |              | 2           |             |             |             |             |             |             |             |
|                             | LPI2C                                 |              | 4           |             |             |             |             |             |             |             |
|                             | I3C                                   |              | 1           |             |             |             |             |             |             |             |
|                             | USB Full Speed Port (Host/<br>Device) |              | Device Only |             | Device/Host |             |             |             |             |             |
|                             | FlexCAN                               |              | 1x CAN FD   |             |             |             | 2x CAN FD   |             |             |             |
|                             | FlexIO                                |              | 1           |             |             |             |             |             |             |             |
| HMI                         | segmend LCD                           |              | No          | 4 x 44      |             | No          |             | 4 x 44      |             |             |
| Analog                      | ADC                                   |              | 2           |             |             |             |             |             |             |             |
|                             | ADC Input<br>Pins                     | WFBGA169(PN) | 43          |             |             |             |             |             |             |             |
|                             |                                       | LQFP144(LQ)  | 43          |             |             |             |             |             |             |             |
|                             |                                       | LQFP100(LL)  | 39          |             |             |             |             |             |             |             |
|                             |                                       | LQFP64(LH)   | 28          |             |             |             |             |             |             |             |

Table continues on the next page...

Table 4. Feature Comparison...continued

|                         |                                      |              | MCX<br>A175      | MCX<br>A176 | MCX<br>A255 | MCX<br>A256 | MCX<br>A185 | MCX<br>A186 | MCX<br>A265 | MCX<br>A266 |
|-------------------------|--------------------------------------|--------------|------------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|
|                         | Low power comparator(LPCMP)          |              | 2                |             |             |             |             |             |             |             |
|                         | DAC                                  |              | 1                |             |             |             |             |             |             |             |
|                         | OpAmp(w/o<br>PGA)                    | WFBGA169(PN) | 1                |             |             |             |             |             |             |             |
|                         |                                      | LQFP144(LQ)  | 1                |             |             |             |             |             |             |             |
|                         |                                      | LQFP100(LL)  | 1                |             |             |             |             |             |             |             |
|                         |                                      | LQFP64(LH)   | 1                |             |             |             |             |             |             |             |
| Motor<br>Control        | FlexPWM <sup>[2]</sup>               |              | 2                |             |             |             |             |             |             |             |
|                         | AND/OR INVERT (AOI)                  |              | 2                |             |             |             |             |             |             |             |
|                         | Quadrature decoder (eQDC)            |              | 2                |             |             |             |             |             |             |             |
| Timer                   | 32-bit timer(Ctimer)                 |              | 5                |             |             |             |             |             |             |             |
|                         | Low power timer(LPTMR)               |              | 1                |             |             |             |             |             |             |             |
|                         | Micro-tick timer(UTICK)              |              | 1                |             |             |             |             |             |             |             |
|                         | OS event timer                       |              | 1                |             |             |             |             |             |             |             |
|                         | Windowed watchdog timer (WWDT)       |              | 1                |             |             |             |             |             |             |             |
|                         | Frequency measurement (FREQME)       |              | 1                |             |             |             |             |             |             |             |
|                         | Wake timer                           |              | 1                |             |             |             |             |             |             |             |
|                         | RTC <sup>[3]</sup>                   |              | 1                |             |             |             |             |             |             |             |
| IO                      | Independent IO supply <sup>[4]</sup> |              | No               |             |             |             |             |             |             |             |
|                         | 5 V tolerant IO <sup>[5]</sup>       |              | 2                |             |             |             |             |             |             |             |
|                         | High drive IO (20 mA) <sup>[6]</sup> |              | Up to 8          |             |             |             |             |             |             |             |
|                         | 50 MHz IO <sup>[7]</sup>             |              | Up to 22         |             |             |             |             |             |             |             |
| Packages <sup>[8]</sup> | GPIO/<br>Wakeup Pin                  | WFBGA169(PN) | 114/29           |             |             |             |             |             |             |             |
|                         |                                      | LQFP144(LQ)  | 114/29           |             |             |             |             |             |             |             |
|                         |                                      | LQFP100(LL)  | 83/25            |             |             |             |             |             |             |             |
|                         |                                      | LQFP64(LH)   | 52/19            |             |             |             |             |             |             |             |
| Temperature range       |                                      |              | -40 °C to 125 °C |             |             |             |             |             |             |             |

[1] This feature described in Security Reference Manual (SRM), user can request SRM document from nxp.com under NDA.

[2] There are 4 sub-modules for each FlexPWM module.

[3] RTC only support counter mode, no dedicate VBAT and not support external 32.768KHz crystal.

[4] MCX A345/A346 does not support 1.2 V IO power supply.

[5] P3\_27, P3\_28 are 5 V tolerant IOs

[6] P1\_8,P1\_9,P1\_30,P1\_31,P3\_1,P3\_0,P0\_16,P0\_17 are High Drive IOs

[7] 50 MHz IOs are located on P1, P3, P4 ports

[8] Show the package types and GPIO numbers and Wakeup pin numbers

## 2 Ratings

### 2.1 Thermal handling ratings

Table 5. Thermal handling ratings

| Symbol | Description                                  | Min | Typ | Max | Unit | Condition |
|--------|----------------------------------------------|-----|-----|-----|------|-----------|
| TSTG   | Storage temperature <sup>[1]</sup>           | –55 | —   | 150 | °C   | —         |
| TSDR   | Solder temperature, lead-free <sup>[2]</sup> | —   | —   | 260 | °C   | —         |

[1] Determined according to JEDEC Standard JESD22-A103, High Temperature Storage Life.

[2] Determined according to IPC/JEDEC Standard J-STD-020, Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices.

### 2.2 Moisture handling ratings

Table 6. Moisture handling ratings

| Symbol | Description                               | Min | Typ | Max | Unit | Condition |
|--------|-------------------------------------------|-----|-----|-----|------|-----------|
| MSL    | Moisture sensitivity level <sup>[1]</sup> | —   | —   | 3   | —    | —         |

[1] Determined according to IPC/JEDEC Standard J-STD-020, Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices.

### 2.3 ESD handling ratings

Table 7. ESD handling ratings

| Description                                                         | Rating           | Unit | Notes |
|---------------------------------------------------------------------|------------------|------|-------|
| Electrostatic discharge voltage, human body model                   | +/-2000          | V    | [1]   |
| Electrostatic discharge voltage, charged-device model               | +/-500           | V    | [2]   |
| Electrostatic discharge voltage, charged device model (corner pins) | +/-750           | V    | [2]   |
| Latch-up immunity level (Class II at 110 °C junction temperature)   | Immunity Level A | —    | [3]   |

[1] Determined according to ANSI/ESDA/JEDEC Standard JS-001-2023, For Electrostatic Discharge Sensitivity Testing, Human Body Model (HBM) - Device Level.

[2] Determined according to ANSI/ESDA/JEDEC Standard JS-002-2022, For Electrostatic Discharge Sensitivity Testing, Charged Device Model (CDM) - Device Level.

[3] Determined according to JEDEC Standard JESD78, IC Latch-Up Test.

### 2.4 Voltage and current maximum ratings

The table below shows the absolute minimum and maximum rating for the device. If the values are violated, device could be damaged. See Voltage and current for operating requirements, and Terminology and guidelines for definitions of terms.

Table 8. Voltage and current maximum ratings

| Symbol | Description                                                  | Min  | Typ | Max  | Unit | Condition |
|--------|--------------------------------------------------------------|------|-----|------|------|-----------|
| VDD    | Supply voltage for Port 0, Port 1, Port 2, Port 3 and Port 4 | -0.3 | —   | 3.63 | V    | —         |

*Table continues on the next page...*

Table 8. Voltage and current maximum ratings...continued

| Symbol     | Description                                            | Min  | Typ | Max                   | Unit | Condition |
|------------|--------------------------------------------------------|------|-----|-----------------------|------|-----------|
| VDD_ANA    | Supply voltage for ADC                                 | -0.3 | —   | 3.63                  | V    | —         |
| VDD_USB    | Supply voltage for USB analog                          | -0.3 | —   | 3.63                  | V    | —         |
| VUSB0_Dx   | USB0_DP and USB0_DM input voltage                      | -0.3 | —   | 3.63                  | V    | —         |
| VDIO       | Digital input voltage                                  | -0.3 | —   | VDD + 0.3             | V    | —         |
| VDIO_5VTOL | Digital input voltage for 5V tolerant I/O pins         | -0.3 | —   | min(VDD + 3.6V, 5.5V) | V    | —         |
| VAIO       | Analog input voltage <sup>[1]</sup>                    | -0.3 | —   | VDD_ANA + 0.3         | V    | —         |
| IDD        | Digital supply current <sup>[2]</sup>                  | —    | —   | 100                   | mA   | —         |
| ID         | Maximum current single pin limit (digital output pins) | -25  | —   | 25                    | mA   | —         |

[1] Analog pins are defined as pins that do not have an associated general-purpose I/O port function.  
[2] This limit is per supply pin. It includes all power pins, including VDD, VDD\_ANA, VDD\_USB.

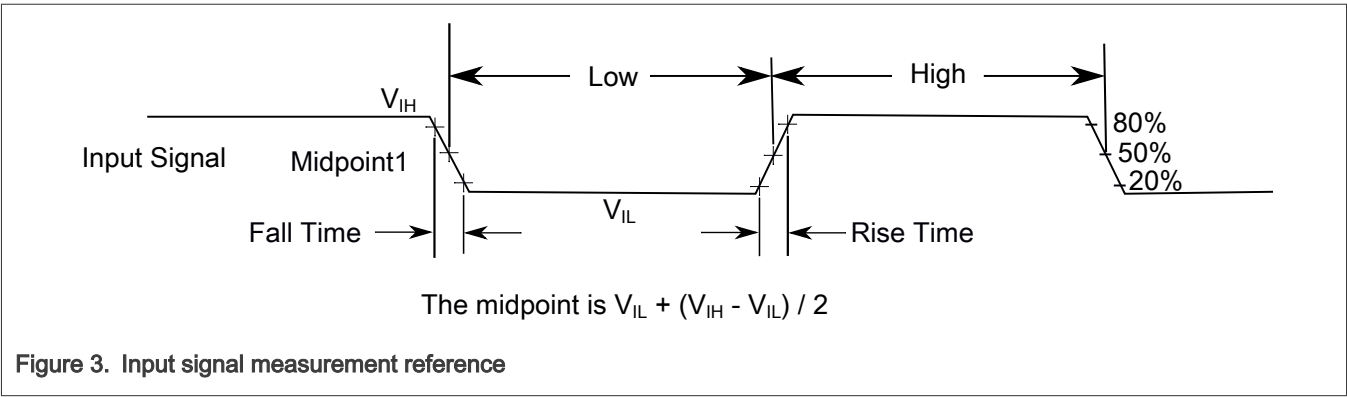
2.5 Required Power-On-Reset (POR) Sequencing

- VDD and VDD\_ANA must be same voltage

3 General

3.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.



3.2 Nonswitching electrical specifications

### 3.2.1 Voltage and current operating requirement

Table 9. Voltage and current operating requirement

| Symbol        | Description                                                                                                            | Min              | Typ | Max              | Unit | Condition                                    |
|---------------|------------------------------------------------------------------------------------------------------------------------|------------------|-----|------------------|------|----------------------------------------------|
| VDD           | Supply Voltage for IO, LDO, Flash, and LPCMP                                                                           | 1.71             | —   | 3.6              | V    | —                                            |
| VDD_ANA       | Supply voltage for ADC                                                                                                 | VDD - 0.1        | —   | VDD + 0.1        | V    | —                                            |
| VSS - VSS_ANA | VSS-to-VSS_ANA differential voltage                                                                                    | -0.1             | —   | 0.1              | V    | —                                            |
| VDD_USB       | Supply voltage for USB analog                                                                                          | 3.0              | —   | 3.6              | V    | —                                            |
| VIH           | Input high voltage                                                                                                     | $0.7 \times VDD$ | —   | —                | V    | $1.71 \text{ V} \leq VDD \leq 3.6 \text{ V}$ |
| VIH_5VTOL     | Input high voltage of 5V tolerant IO                                                                                   | $0.7 \times VDD$ | —   | —                | V    | $1.71 \text{ V} \leq VDD \leq 3.6 \text{ V}$ |
| VIL           | Input low voltage                                                                                                      | —                | —   | $0.3 \times VDD$ | V    | $1.71 \text{ V} \leq VDD \leq 3.6 \text{ V}$ |
| VIL_5VTOL     | Input low voltage of 5 V tolerant IO                                                                                   | —                | —   | $0.3 \times VDD$ | V    | $1.71 \text{ V} \leq VDD \leq 3.6 \text{ V}$ |
| VHYS          | Input hysteresis                                                                                                       | $0.1 \times VDD$ | —   | —                | V    | —                                            |
| VHYS_5VTOL    | Input hysteresis of 5 V tolerant IO                                                                                    | $0.1 \times VDD$ | —   | —                | V    | —                                            |
| IICIO         | IO pin DC injection current — per pin <sup>[1]</sup>                                                                   | -3               | —   | —                | mA   | VIN < VSS-0.3 V (negative current injection) |
| IICIO         | IO pin DC injection current — per pin <sup>[1]</sup>                                                                   | —                | —   | 3                | mA   | VIN > VDD+0.3 V (positive current injection) |
| IICcont       | Contiguous pin DC injection current —regional limit, includes sum of negative injection currents of 16 contiguous pins | -25              | —   | —                | mA   | Negative current injection                   |
| IICcont       | Contiguous pin DC injection current —regional limit, includes sum of negative injection currents of 16 contiguous pins | —                | —   | 25               | mA   | Positive current injection                   |
| VODPU         | Open drain pullup voltage level <sup>[2]</sup>                                                                         | VDD              | —   | VDD              | V    | —                                            |

[1] All I/O pins are internally clamped to VSS and VDD through an ESD protection diode. If VIN is greater than VDD\_MIN(=VSS-0.3 V) or is less than VDD\_MAX(=VDD+ 0.3 V), then there is no need to provide current limiting resistors at the pads. If this limit cannot be observed, then a current limiting resistor is required. The negative DC injection current limiting resistor is calculated as  $R = (-0.3 - VIN)/(-IICIO_{min})$ . The positive injection current limiting resistor is calculated as  $R = (VIN - VDD\_MAX)/IICIO_{max}$ . The actual resistor should be an order of magnitude higher to tolerate transient voltages

[2] Open drain outputs must be pulled to whichever supply voltage corresponds to that IO, VDD as appropriate.

### 3.2.2 HVD, LVD, and POR operating requirements

The device includes low-voltage detection (LVD) and high-voltage detection (HVD) power supervisor circuits for following power supplies:

- VDD

#### 3.2.2.1 VDD supply HVD, LVD, and POR Operating Requirements

Table 10. VDD supply HVD, LVD, and POR Operating Requirements

| Symbol        | Description                                                           | Min   | Typ   | Max   | Unit | Condition |
|---------------|-----------------------------------------------------------------------|-------|-------|-------|------|-----------|
| VHVDH_VDD     | VDD Rising high-voltage detect threshold (HVD assertion)              | 3.730 | 3.810 | 3.890 | V    | —         |
| VHVDH_HYS_VDD | VDD High-voltage inhibit reset/recover hysteresis                     | —     | 38    | —     | mV   | —         |
| VLVDH_VDD     | VDD Falling low-voltage detect threshold (LVD assertion) - high range | 2.567 | 2.619 | 2.673 | V    | —         |
| VLVDH_HYS_VDD | VDD Low-voltage inhibit reset/recover hysteresis - high range         | —     | 27    | —     | mV   | —         |
| VLVDL_VDD     | VDD Falling low-voltage detect threshold (LVD assertion) - low range  | 1.618 | 1.651 | 1.684 | V    | —         |
| VLVDL_HYS_VDD | VDD Low-voltage inhibit reset/recover hysteresis - low range          | —     | 16    | —     | mV   | —         |

### 3.2.3 Voltage and current operating behaviors

Table 11. Voltage and current operating behaviors

| Symbol | Description                                                   | Min       | Typ | Max | Unit | Condition                           |
|--------|---------------------------------------------------------------|-----------|-----|-----|------|-------------------------------------|
| VOH    | Output high voltage — Normal drive strength <sup>[1]</sup>    | VDD – 0.5 | —   | —   | V    | 2.7 V ≤ VDD ≤ 3.6 V, IOH = 4 mA     |
| VOH    | Output high voltage — Normal drive strength <sup>[1]</sup>    | VDD – 0.5 | —   | —   | V    | 1.71 V ≤ VDD < 2.7 V, IOH = 2.5 mA  |
| VOH    | Output high voltage — High drive strength <sup>[1][2]</sup>   | VDD – 0.5 | —   | —   | V    | 2.7 V ≤ VDD ≤ 3.6 V, IOH = 6 mA     |
| VOH    | Output high voltage — High drive strength <sup>[1][2]</sup>   | VDD – 0.5 | —   | —   | V    | 1.71 V ≤ VDD < 2.7 V, IOH = 3.75 mA |
| IOHT   | Output high current total for all ports                       | —         | —   | 100 | mA   | —                                   |
| VOL    | Output low voltage — Normal drive strength <sup>[1][3]</sup>  | —         | —   | 0.5 | V    | 2.7 V ≤ VDD ≤ 3.6 V, IOL = 4 mA     |
| VOL    | Output low voltage — Normal drive strength <sup>[1][3]</sup>  | —         | —   | 0.5 | V    | 1.71 V ≤ VDD < 2.7 V, IOL = 2.5 mA  |
| VOL    | Output low voltage — High drive strength <sup>[1][2][3]</sup> | —         | —   | 0.5 | V    | 2.7 V ≤ VDD ≤ 3.6 V, IOL = 6 mA     |

Table continues on the next page...

Table 11. Voltage and current operating behaviors...continued

| Symbol    | Description                                                                | Min                 | Typ   | Max   | Unit | Condition                           |
|-----------|----------------------------------------------------------------------------|---------------------|-------|-------|------|-------------------------------------|
| VOL       | Output low voltage — High drive strength <sup>[1][2][3]</sup>              | —                   | —     | 0.5   | V    | 1.71 V ≤ VDD < 2.7 V, IOL = 3.75 mA |
| IOLT      | Output low current total for all ports                                     | —                   | —     | 100   | mA   | —                                   |
| IIN       | Input leakage current (per pin) for full temperature range <sup>[4]</sup>  | —                   | 0.02  | 1     | μA   | —                                   |
| IIN       | Input leakage current (per pin) at 25 °C <sup>[4]</sup>                    | —                   | 0.001 | 0.025 | μA   | —                                   |
| IOZ       | Hi-Z (off-state) leakage current (per pin)                                 | —                   | 0.02  | 1     | μA   | —                                   |
| RPU       | Internal pullup resistors                                                  | 33                  | 50    | 75    | kΩ   | —                                   |
| RPU (I3C) | Internal pullup resistors <sup>[5]</sup>                                   | (VDD - 0.27 V)/3 mA | 1.75  | —     | kΩ   | —                                   |
| RPD       | Internal pulldown resistors                                                | 33                  | 50    | 75    | kΩ   | —                                   |
| RHPU      | High-resistance pullup option (PCR <sub>x</sub> [PV] = 1) <sup>[6]</sup>   | 0.67                | —     | 1.5   | MΩ   | —                                   |
| RHPD      | High-resistance pulldown option (PCR <sub>x</sub> [PV] = 1) <sup>[6]</sup> | 0.67                | —     | 1.5   | MΩ   | —                                   |
| VBG       | Bandgap voltage reference voltage                                          | 0.98                | 1.0   | 1.02  | V    | —                                   |

[1] For the HD pads, when setting DSE1=1, the IOH/IOL are four times higher at the same VOH/VOL.

[2] RESET\_B pins are always configured in high drive mode

[3] Open drain outputs must be pulled to VDD

[4] Measured at VDD = 3.6 V.

[5] Only I3C pins support this option

[6] Only RESET\_B pins support this option.

## 3.2.4 On-chip regulator electrical specifications

### 3.2.4.1 LDO\_CORE electrical specifications

Table 12. LDO\_CORE electrical specifications

| Symbol  | Description                   | Min  | Typ | Max | Unit | Condition           |
|---------|-------------------------------|------|-----|-----|------|---------------------|
| VDD     | LDO_CORE input supply voltage | 1.71 | —   | 3.6 | V    | —                   |
| ILOAD   | LDO_CORE max load current     | —    | —   | 96  | mA   | Over drive strength |
| ILOAD   | LDO_CORE max load current     | —    | —   | 2   | mA   | Low drive strength  |
| IDD     | LDO_CORE current consumption  | —    | —   | 250 | μA   | Over drive strength |
| IDD     | LDO_CORE current consumption  | —    | —   | 500 | nA   | Low drive strength  |
| IINRUSH | LDO_CORE inrush current       | —    | —   | 10  | mA   | —                   |

### 3.2.5 Power mode transition operating behaviours

All specifications in the following table assume this clock configuration:

- CPU clock = 180 MHz
- AHB clock = 180 MHz
- Clock source = FRO180M

#### 3.2.5.1 Power mode transition operating behaviors

Table 13. Power mode transition operating behaviors

| Symbol  | Description                                                                                                                                                                                  | Min | Typ   | Max   | Unit | Condition |
|---------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|-------|-------|------|-----------|
| tPOR    | After a POR event, amount of time to execution of the first instruction (measured from the point where VDD reach 1.8V) across the operating temperature range of the chip. <sup>[1][2]</sup> | —   | 2.94  | 2.98  | ms   | —         |
| tSLEEP  | Sleep → Active <sup>[1][2][3][4]</sup>                                                                                                                                                       | —   | 0.42  | 0.46  | μs   | —         |
| tDSLEEP | Deep Sleep → Active <sup>[1][2][3][4]</sup>                                                                                                                                                  | —   | 9.01  | 10.31 | μs   | —         |
| tPWDN   | Power Down → Active <sup>[1][2][3][5]</sup>                                                                                                                                                  | —   | 18.84 | 22.15 | μs   | —         |
| tDPWDN  | Deep Power Down → Active <sup>[1][2][3][4]</sup>                                                                                                                                             | —   | 1.57  | 1.59  | ms   | —         |

[1] Max value is mean+3 × sigma of tested values at the worst case of ambient temperature range and VDD 1.71 V to 3.6 V. Max values are based on characterization but not covered by test limits in production.

[2] Typical value is the average of values tested at Temperature=25 °C and VDD=3.3 V

[3] WFE used for low-power mode entry

[4] SPC->LPWKUP\_DELAY[LPWKUP\_DELAY] = 0x00 and the Core voltage level is configured as same level for Active and Low Power mode (SPC->ACTIVE\_CFG[CORELDO\_VDD\_LVL]=SPC->LP\_CFG[CORELDO\_VDD\_LVL] = 01b).

[5] SPC->LPWKUP\_DELAY[LPWKUP\_DELAY] = 0x5B and the Core voltage level is configured as different level for Active and Low Power mode (SPC->ACTIVE\_CFG[CORELDO\_VDD\_LVL] = 01b for Active mode, SPC->LP\_CFG[CORELDO\_VDD\_LVL] = 00b for Low Power mode)

### 3.2.6 Power consumption operating behaviors

The maximum values stated in the following sections represent characterized results equivalent to the mean plus three times the standard deviation (mean + 3 sigma).

#### 3.2.6.1 Power consumption operating behaviors

When calculating the total MCU current consumption the following considerations should be made:

- Specifications below only include power for the MCU itself including VDD, VDD\_ANA.
- VDD\_USB current draw are not included
- On top of the device's IDD current consumption, external loads applied to pins of the device need to be considered

Table 14. Power consumption operating behaviors

| Symbol                      | Description                                                                                                                                                                                                        | Condition <sup>[1]</sup> | Typ  | Unit |
|-----------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------|------|------|
| IDD_ACT_MD_1 <sup>[2]</sup> | 1. CPU_CLK = 45 MHz from FRO180M.<br>VDD_CORE = 1.0V from LDO_CORE Normal Drive. 2. All peripheral clocks disabled; Flash is configured to LP mode; Cache enabled. 3. While(1) loop executing from internal flash. | 25 °C                    | 3.32 | mA   |
|                             |                                                                                                                                                                                                                    | 105 °C                   | 5.78 | mA   |
|                             |                                                                                                                                                                                                                    | 125 °C                   | 7.98 | mA   |

Table continues on the next page...

Table 14. Power consumption operating behaviors...continued

| Symbol          | Description                                                                                                                                                                                                          | Condition <sup>[1]</sup> | Typ   | Unit |
|-----------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------|-------|------|
| IDD_ACT_MD_2    | 1. CPU_CLK = 45 MHz from FRO180M.<br>VDD_CORE = 1.0V from LDO_CORE Normal Drive. 2. All peripheral clocks enabled; Cache enabled. 3. While(1) loop executing from internal flash.                                    | 25 °C                    | 3.68  | mA   |
|                 |                                                                                                                                                                                                                      | 105 °C                   | 6.14  | mA   |
|                 |                                                                                                                                                                                                                      | 125 °C                   | 8.38  | mA   |
| IDD_ACT_MD_CM_1 | 1. CPU_CLK = 45 MHz from FRO180M.<br>VDD_CORE = 1.0V from LDO_CORE Normal Drive. 2. All peripheral clocks disabled; Flash is configured to LP mode; Cache enabled. 3. Coremark executing from internal flash.        | 25 °C                    | 4.09  | mA   |
|                 |                                                                                                                                                                                                                      | 105 °C                   | 6.55  | mA   |
|                 |                                                                                                                                                                                                                      | 125 °C                   | 8.74  | mA   |
| IDD_ACT_MD_CM_2 | 1. CPU_CLK = 45 MHz from FRO180M.<br>VDD_CORE = 1.0V from LDO_CORE Normal Drive. 2. All peripheral clocks enabled; Cache enabled. 3. Coremark executing from internal flash.                                         | 25 °C                    | 4.45  | mA   |
|                 |                                                                                                                                                                                                                      | 105 °C                   | 6.93  | mA   |
|                 |                                                                                                                                                                                                                      | 125 °C                   | 9.15  | mA   |
| IDD_ACT_OD_1    | 1. CPU_CLK = 180 MHz from FRO180M.<br>VDD_CORE = 1.2 V from LDO_CORE Normal Drive. 2. All peripheral clocks disabled; Flash is configured to LP mode; Cache enabled. 3. While(1) loop executing from internal flash. | 25 °C                    | 13.76 | mA   |
|                 |                                                                                                                                                                                                                      | 105 °C                   | 17.32 | mA   |
|                 |                                                                                                                                                                                                                      | 125 °C                   | 20.43 | mA   |
| IDD_ACT_OD_2    | 1. CPU_CLK = 180 MHz from FRO180M.<br>VDD_CORE = 1.2 V from LDO_CORE Normal Drive. 2. All peripheral clocks enabled; Cache enabled. 3. While(1) loop executing from internal flash.                                  | 25 °C                    | 15.13 | mA   |
|                 |                                                                                                                                                                                                                      | 105 °C                   | 18.89 | mA   |
|                 |                                                                                                                                                                                                                      | 125 °C                   | 21.99 | mA   |
| IDD_ACT_OD_CM_1 | 1. CPU_CLK = 180 MHz from FRO180M.<br>VDD_CORE = 1.2 V from LDO_CORE Normal Drive. 2. All peripheral clocks disabled; Flash is configured to LP mode; Cache enabled. 3. Coremark executing from internal flash.      | 25 °C                    | 17.79 | mA   |
|                 |                                                                                                                                                                                                                      | 105 °C                   | 21.45 | mA   |
|                 |                                                                                                                                                                                                                      | 125 °C                   | 24.61 | mA   |
| IDD_ACT_OD_CM_2 | 1. CPU_CLK = 180 MHz from FRO180M.<br>VDD_CORE = 1.2 V from LDO_CORE Normal Drive. 2. All peripheral clocks enabled; Cache enabled. 3. Coremark executing from internal flash.                                       | 25 °C                    | 18.88 | mA   |
|                 |                                                                                                                                                                                                                      | 105 °C                   | 22.79 | mA   |
|                 |                                                                                                                                                                                                                      | 125 °C                   | 25.94 | mA   |
| IDD_ACT_OD_3    | 1. CPU_CLK = 240 MHz from System PLL.<br>VDD_CORE = 1.2 V from LDO_CORE Normal Drive. 2. All peripheral clocks disabled; Cache enabled. 3. While(1) loop executing from internal flash.                              | 25 °C                    | 18.82 | mA   |
|                 |                                                                                                                                                                                                                      | 105 °C                   | 22.66 | mA   |
|                 |                                                                                                                                                                                                                      | 125 °C                   | 26.06 | mA   |
| IDD_ACT_OD_4    | 1. CPU_CLK = 240 MHz from System PLL.<br>VDD_CORE = 1.2 V from LDO_CORE Normal Drive. 2. All peripheral clocks enabled; Cache enabled. 3. While(1) loop executing from internal flash.                               | 25 °C                    | 20.1  | mA   |
|                 |                                                                                                                                                                                                                      | 105 °C                   | 24.02 | mA   |
|                 |                                                                                                                                                                                                                      | 125 °C                   | 27.46 | mA   |

Table continues on the next page...

Table 14. Power consumption operating behaviors...continued

| Symbol          | Description                                                                                                                                                                                       | Condition <sup>[1]</sup> | Typ   | Unit |
|-----------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------|-------|------|
| IDD_ACT_OD_CM_3 | 1. CPU_CLK = 240 MHz from System PLL. VDD_CORE = 1.2 V from LDO_CORE Normal Drive. 2. All peripheral clocks disabled; Cache enabled. 3. Coremark executing from internal flash.                   | 25 °C                    | 24.08 | mA   |
|                 |                                                                                                                                                                                                   | 105 °C                   | 28.11 | mA   |
|                 |                                                                                                                                                                                                   | 125 °C                   | 31.58 | mA   |
| IDD_ACT_OD_CM_4 | 1. CPU_CLK = 240 MHz from System PLL. VDD_CORE = 1.2 V from LDO_CORE Normal Drive. 2. All peripheral clocks enabled; Cache enabled. 3. Coremark executing from internal flash.                    | 25 °C                    | 25.37 | mA   |
|                 |                                                                                                                                                                                                   | 105 °C                   | 29.45 | mA   |
|                 |                                                                                                                                                                                                   | 125 °C                   | 32.97 | mA   |
| IDD_ACT_OD_5    | 1. CPU_CLK = 240 MHz from FRO180M in 240 MHz mode. VDD_CORE = 1.2 V from LDO_CORE Normal Drive. 2. All peripheral clocks disabled; Cache enabled. 3. While(1) loop executing from internal flash. | 25 °C                    | 17.58 | mA   |
|                 |                                                                                                                                                                                                   | 105 °C                   | 21.87 | mA   |
|                 |                                                                                                                                                                                                   | 125 °C                   | 25.55 | mA   |
| IDD_ACT_OD_6    | 1. CPU_CLK = 240 MHz from FRO180M in 240 MHz mode. VDD_CORE = 1.2 V from LDO_CORE Normal Drive. 2. All peripheral clocks disabled; Cache enabled. 3. While(1) loop executing from internal flash. | 25 °C                    | 23.31 | mA   |
|                 |                                                                                                                                                                                                   | 105 °C                   | 27.79 | mA   |
|                 |                                                                                                                                                                                                   | 125 °C                   | 31.61 | mA   |
| IDD_ACT_OD_CM_5 | 1. CPU_CLK = 240 MHz from FRO180M in 240 MHz mode. VDD_CORE = 1.2 V from LDO_CORE Normal Drive. 2. All peripheral clocks disabled; Cache enabled. 3. While(1) loop executing from internal flash. | 25 °C                    | 18.94 | mA   |
|                 |                                                                                                                                                                                                   | 105 °C                   | 23.31 | mA   |
|                 |                                                                                                                                                                                                   | 125 °C                   | 27.03 | mA   |
| IDD_ACT_OD_CM_6 | 1. CPU_CLK = 240 MHz from FRO180M in 240 MHz mode. VDD_CORE = 1.2 V from LDO_CORE Normal Drive. 2. All peripheral clocks disabled; Cache enabled. 3. While(1) loop executing from internal flash. | 25 °C                    | 24.69 | mA   |
|                 |                                                                                                                                                                                                   | 105 °C                   | 29.21 | mA   |
|                 |                                                                                                                                                                                                   | 125 °C                   | 33.02 | mA   |
| IDD_SLEEP_OD_1  | 1. CPU_CLK = OFF; SYSTEM_CLK = 180 MHz from FRO180M. VDD_CORE = 1.2 V from LDO_CORE Normal Drive. 2. All peripheral clocks disabled. 3. Core in WFI.                                              | 25 °C                    | 8.08  | mA   |
|                 |                                                                                                                                                                                                   | 105 °C                   | 11.68 | mA   |
|                 |                                                                                                                                                                                                   | 125 °C                   | 14.75 | mA   |
| IDD_SLEEP_OD_2  | 1. CPU_CLK = OFF; SYSTEM_CLK = 180 MHz from FRO180M. VDD_CORE = 1.2 V from LDO_CORE Normal Drive. 2. All peripheral clocks enabled. 3. Core in WFI.                                               | 25 °C                    | 9.16  | mA   |
|                 |                                                                                                                                                                                                   | 105 °C                   | 12.69 | mA   |
|                 |                                                                                                                                                                                                   | 125 °C                   | 15.78 | mA   |
| IDD_SLEEP_MD_1  | 1. CPU_CLK = OFF; SYSTEM_CLK = 45 MHz from FRO180M. VDD_CORE = 1.0V from LDO_CORE Normal Drive. 2. All peripheral clocks disabled. 3. Core in WFI.                                                | 25 °C                    | 2.16  | mA   |
|                 |                                                                                                                                                                                                   | 105 °C                   | 4.59  | mA   |
|                 |                                                                                                                                                                                                   | 125 °C                   | 6.81  | mA   |
| IDD_SLEEP_MD_2  | 1. CPU_CLK = OFF; SYSTEM_CLK = 45 MHz from FRO180M. VDD_CORE = 1.0V from                                                                                                                          | 25 °C                    | 2.41  | mA   |
|                 |                                                                                                                                                                                                   | 105 °C                   | 4.85  | mA   |

Table continues on the next page...

Table 14. Power consumption operating behaviors...continued

| Symbol                | Description                                                                                                                                                                                          | Condition <sup>[1]</sup> | Typ    | Unit |
|-----------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------|--------|------|
|                       | LDO_CORE Normal Drive. 2. All peripheral clocks enabled. 3. Core in WFI.                                                                                                                             | 125 °C                   | 7.07   | mA   |
| IDD_SLEEP_MD_3        | 1. CPU_CLK = OFF; SYSTEM_CLK = 12 MHz from FRO12M. VDD_CORE = 1.0 V from LDO_CORE Low Drive. 2. All peripheral clocks disabled. 3. Core in WFI.                                                      | 25 °C                    | 0.579  | mA   |
|                       |                                                                                                                                                                                                      | 105 °C                   | 3.04   | mA   |
|                       |                                                                                                                                                                                                      | 125 °C                   | 5.32   | mA   |
| IDD_DEEP_SLEEP_OD_1   | 1. CPU_CLK = OFF; SYSTEM_CLK = OFF; SLOW_CLK = OFF; VDD_CORE = 1.2 V from LDO_CORE Normal Drive; FRO12M disabled. 2. All peripheral clocks disabled; all on-chip SRAM in deep sleep. 3. Core in WFI. | 25 °C                    | 542.27 | μA   |
|                       |                                                                                                                                                                                                      | 105 °C                   | 3000   | μA   |
|                       |                                                                                                                                                                                                      | 125 °C                   | 5130   | μA   |
| IDD_DEEP_SLEEP_MD_1   | 1. CPU_CLK = OFF; SYSTEM_CLK = OFF; SLOW_CLK = OFF; VDD_CORE = 1.0 V from LDO_CORE Low Drive; FRO12M disabled. 2. All peripheral clocks disabled; all on-chip SRAM in deep sleep. 3. Core in WFI.    | 25 °C                    | 96.02  | μA   |
|                       |                                                                                                                                                                                                      | 105 °C                   | 1850   | μA   |
|                       |                                                                                                                                                                                                      | 125 °C                   | 3470   | μA   |
| IDD_DEEP_SLEEP_MD_2   | 1. CPU_CLK = OFF; SYSTEM_CLK = OFF; SLOW_CLK = OFF; VDD_CORE = 1.0 V from LDO_CORE Low Drive; FRO12M enabled. 2. All peripheral clocks disabled; all on-chip SRAM in deep sleep. 3. Core in WFI.     | 25 °C                    | 155.29 | μA   |
|                       |                                                                                                                                                                                                      | 105 °C                   | 1910   | μA   |
|                       |                                                                                                                                                                                                      | 125 °C                   | 3530   | μA   |
| IDD_POWER_DOWN_1      | 1. CPU_CLK = SYSTEM_CLK = OFF; VDD_CORE = 0.6V retention voltage from LDO_CORE Low Drive 2. All RAM retained; FRO16K disabled. 3. Core in WFI.                                                       | 25 °C                    | 31.95  | μA   |
|                       |                                                                                                                                                                                                      | 105 °C                   | 915.38 | μA   |
|                       |                                                                                                                                                                                                      | 125 °C                   | 1810   | μA   |
| IDD_DEEP_POWER_DOWN_1 | 1. CPU_CLK = SYSTEM_CLK = OFF; All VDD_CORE domains power off. 2. All RAM OFF; Wake timer disabled, FRO16K disabled. 3. Core in WFI.                                                                 | 25 °C                    | 0.473  | μA   |
|                       |                                                                                                                                                                                                      | 105 °C                   | 7.95   | μA   |
|                       |                                                                                                                                                                                                      | 125 °C                   | 18.62  | μA   |
| IDD_DEEP_POWER_DOWN_2 | 1. CPU_CLK = SYSTEM_CLK = OFF; All VDD_CORE domains power off. 2. All RAM OFF; Wake timer enabled, FRO16K enabled. 3. Core in WFI.                                                                   | 25 °C                    | 0.646  | μA   |
|                       |                                                                                                                                                                                                      | 105 °C                   | 8.15   | μA   |
|                       |                                                                                                                                                                                                      | 125 °C                   | 18.76  | μA   |
| IDD_DEEP_POWER_DOWN_3 | 1. CPU_CLK = SYSTEM_CLK = OFF; All VDD_CORE domains power off. 2. All RAM retained; Wake timer enabled, FRO16K enabled. 3. Core in WFI.                                                              | 25 °C                    | 3.4    | μA   |
|                       |                                                                                                                                                                                                      | 105 °C                   | 83.13  | μA   |
|                       |                                                                                                                                                                                                      | 125 °C                   | 183.28 | μA   |
| IDD_DEEP_POWER_DOWN_4 | 1. CPU_CLK = SYSTEM_CLK = OFF; All VDD_CORE domains power off. 2. RAM X0/X1/B0/B1, A0~A4 retained; Wake timer enabled, FRO16K enabled. 3. Core in WFI.                                               | 25 °C                    | 2.29   | μA   |
|                       |                                                                                                                                                                                                      | 105 °C                   | 50.43  | μA   |
|                       |                                                                                                                                                                                                      | 125 °C                   | 110.66 | μA   |
| IDD_DEEP_POWER_DOWN_5 | 1. CPU_CLK = SYSTEM_CLK = OFF; All VDD_CORE domains power off. 2. RAM                                                                                                                                | 25 °C                    | 1.66   | μA   |
|                       |                                                                                                                                                                                                      | 105 °C                   | 33.49  | μA   |

Table continues on the next page...

Table 14. Power consumption operating behaviors...continued

| Symbol                 | Description                                                                                                                                                                     | Condition <sup>[1]</sup> | Typ   | Unit |
|------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------|-------|------|
|                        | X0/X1/B0/B1/A0 retained; Wake timer enabled, FRO16K enabled. 3. Core in WFI.                                                                                                    | 125 °C                   | 74.02 | μA   |
| IDD_DEEP_POWER_DOWN_6  | 1. CPU_CLK = SYSTEM_CLK = OFF; All VDD_CORE domains power off. 2. RAM A0 retained; Wake timer enabled, FRO16K enabled. 3. Core in WFI.                                          | 25 °C                    | 0.849 | μA   |
|                        |                                                                                                                                                                                 | 105 °C                   | 11.41 | μA   |
|                        |                                                                                                                                                                                 | 125 °C                   | 25.7  | μA   |
| IDD_DEEP_POWER_DOWN_7  | 1. CPU_CLK = SYSTEM_CLK = OFF; All VDD_CORE domains power off. 2. RAM X0/X1/B0/B1 retained; Wake timer enabled, FRO16K enabled. 3. Core in WFI.                                 | 25 °C                    | 1.55  | μA   |
|                        |                                                                                                                                                                                 | 105 °C                   | 30.39 | μA   |
|                        |                                                                                                                                                                                 | 125 °C                   | 67.28 | μA   |
| IDD_DEEP_POWER_DOWN_8  | 1. CPU_CLK = SYSTEM_CLK = OFF; All VDD_CORE domains power off. 2. RAM A0 retained; RTC enabled, Wake timer disabled, FRO16K enabled. 3. Core in WFI.                            | 25 °C                    | 0.842 | μA   |
|                        |                                                                                                                                                                                 | 105 °C                   | 11.44 | μA   |
|                        |                                                                                                                                                                                 | 125 °C                   | 25.76 | μA   |
| IDD_DEEP_POWER_DOWN_9  | 1. CPU_CLK = SYSTEM_CLK = OFF; All VDD_CORE domains power off. 2. RAM A0 retained; RTC enabled, Wake timer enabled, FRO16K enabled. 3. Core in WFI.                             | 25 °C                    | 0.855 | μA   |
|                        |                                                                                                                                                                                 | 105 °C                   | 11.43 | μA   |
|                        |                                                                                                                                                                                 | 125 °C                   | 25.73 | μA   |
| IDD_DEEP_POWER_DOWN_10 | 1. CPU_CLK = SYSTEM_CLK = OFF; All VDD_CORE domains power off. 2. All RAM OFF; RTC enabled, Wake timer disabled, FRO16K enabled. 3. Core in WFI.                                | 25 °C                    | 0.651 | μA   |
|                        |                                                                                                                                                                                 | 105 °C                   | 8.11  | μA   |
|                        |                                                                                                                                                                                 | 125 °C                   | 18.77 | μA   |
| IDD_DEEP_POWER_DOWN_11 | 1. CPU_CLK = SYSTEM_CLK = OFF; All VDD_CORE domains power off. 2. All RAM OFF; RTC enabled, Wake timer disabled, FRO16K enabled, Digital Tamper (TDET) enabled. 3. Core in WFI. | 25 °C                    | 0.727 | μA   |
|                        |                                                                                                                                                                                 | 105 °C                   | 8.21  | μA   |
|                        |                                                                                                                                                                                 | 125 °C                   | 18.83 | μA   |

[1] Ambient temperature

[2] MD middle drive, core voltage is 1.0V. OD over drive, core voltage is 1.2V

### 3.2.7 EMC radiated emissions operating behaviors

EMC measurements to IC-level IEC standards are available from NXP on request.

### 3.2.8 Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:

1. Go to [nxp.com](http://nxp.com).
2. Perform a keyword search for “EMC design”.

### 3.2.9 Capacitance attributes

Table 15. Capacitance attributes

| Symbol | Description                     | Min | Typ | Max | Unit | Condition |
|--------|---------------------------------|-----|-----|-----|------|-----------|
| CIN_A  | Input capacitance: analog pins  | —   | —   | 7   | pF   | —         |
| CIN_D  | Input capacitance: digital pins | —   | —   | 7   | pF   | —         |

## 3.3 Switching specifications

### 3.3.1 Device clock specs

Table 16. Device clock specs

| Symbol  | Description                                            | Min | Typ | Max | Unit | Condition                                      |
|---------|--------------------------------------------------------|-----|-----|-----|------|------------------------------------------------|
| fCPU    | CPU clock (CPU_CLK)For<br>MCXA185/186/265/266          | —   | —   | 240 | MHz  | Over drive (OD) mode,<br>VDD_CORE = 1.2 V      |
| fSYSTEM | System clock<br>(SYSTEM_CLK)For<br>MCXA185/186/265/266 | —   | —   | 240 | MHz  | Over drive (OD) mode,<br>VDD_CORE = 1.2 V      |
| fSLOW   | Slow clock (SLOW_CLK)For<br>MCXA185/186/265/266        | —   | —   | 40  | MHz  | Over drive (OD) mode,<br>VDD_CORE = 1.2 V      |
| fCPU    | CPU clock (CPU_CLK)For<br>MCXA175/176/255/256          | —   | —   | 180 | MHz  | Over drive (OD) mode,<br>VDD_CORE = 1.2 V      |
| fSYSTEM | System clock<br>(SYSTEM_CLK)For<br>MCXA175/176/255/256 | —   | —   | 180 | MHz  | Over drive (OD) mode,<br>VDD_CORE = 1.2 V      |
| fSLOW   | Slow clock (SLOW_CLK)For<br>MCXA175/176/255/256        | —   | —   | 30  | MHz  | Over drive (OD) mode,<br>VDD_CORE = 1.2 V      |
| fCPU    | CPU clock (CPU_CLK)                                    | —   | —   | 45  | MHz  | Middle drive (MD)<br>mode VDD_CORE = 1.<br>0 V |
| fSYSTEM | SYSTEM clock (SYSTEM_CLK)                              | —   | —   | 45  | MHz  | Middle drive (MD)<br>mode VDD_CORE =<br>1.0 V  |
| fSLOW   | Slow clock (SLOW_CLK)                                  | —   | —   | 7.5 | MHz  | Middle drive (MD)<br>mode VDD_CORE = 1.<br>0 V |

### 3.3.2 General switching specifications

These general-purpose specifications apply to all signals configured for GPIO, LPUART, LPI2C, LPI3C, LPSPi functions.

#### 3.3.2.1 General switching specifications

**Note:** Refer to attached pinout spreadsheet.

Table 17. General switching specifications

| Symbol | Description                                                                  | Min | Typ | Max | Unit                      | Condition                                                       |
|--------|------------------------------------------------------------------------------|-----|-----|-----|---------------------------|-----------------------------------------------------------------|
| —      | GPIO pin interrupt pulse width<br>— Synchronous path <sup>[1]</sup>          | 1.5 | —   | —   | SYSTEM<br>clock<br>cycles | The synchronous and asynchronous timing must be met.            |
| —      | GPIO pin interrupt pulse width<br>— Asynchronous path                        | 150 | —   | —   | ns                        | —                                                               |
| —      | GPIO pin interrupt pulse width<br>— Asynchronous path                        | 50  | —   | —   | ns                        | —                                                               |
| —      | External RST pin interrupt pulse width<br>— Asynchronous path <sup>[2]</sup> | 330 | —   | —   | ns                        | This is the shortest pulse that is guaranteed to be recognized. |
| —      | GPIO pin interrupt pulse width<br>— Asynchronous path <sup>[2]</sup>         | 16  | —   | —   | ns                        | —                                                               |
| —      | Port rise/fall time for slow I/O pins <sup>[3][4]</sup>                      | 1   | —   | 7   | ns                        | $2.7 \leq VDD \leq 3.6$ V,<br>Fast slew rate (SRE = 0; DSE = 0) |
| —      | Port rise/fall time for slow I/O pins <sup>[3][4]</sup>                      | 3.5 | —   | 15  | ns                        | $2.7 \leq VDD \leq 3.6$ V,<br>Slow slew rate (SRE = 1; DSE = 0) |
| —      | Port rise/fall time for slow I/O pins <sup>[3][4]</sup>                      | 1   | —   | 7   | ns                        | $1.71 \leq VDD < 2.7$ V,<br>Fast slew rate (SRE = 0; DSE = 1)   |
| —      | Port rise/fall time for slow I/O pins <sup>[3][4]</sup>                      | 3.5 | —   | 25  | ns                        | $1.71 \leq VDD < 2.7$ V,<br>Slow slew rate (SRE = 1; DSE = 1)   |
| —      | Port rise/fall time for slow I/O pins, 5V Tolerant <sup>[3][4]</sup>         | 1   | —   | 7   | ns                        | $2.7 \leq VDD \leq 3.6$ V,<br>Fast slew rate (SRE = 0; DSE = 0) |
| —      | Port rise/fall time for slow I/O pins, 5V Tolerant <sup>[3][4]</sup>         | 3.5 | —   | 15  | ns                        | $2.7 \leq VDD \leq 3.6$ V,<br>Slow slew rate (SRE = 1; DSE = 0) |
| —      | Port rise/fall time for slow I/O pins, 5V Tolerant <sup>[3][4]</sup>         | 1   | —   | 7   | ns                        | $1.71 \leq VDD < 2.7$ V,<br>Fast slew rate (SRE = 0; DSE = 1)   |
| —      | Port rise/fall time for slow I/O pins, 5V Tolerant <sup>[3][4]</sup>         | 3.5 | —   | 25  | ns                        | $1.71 \leq VDD < 2.7$ V,<br>Fast slew rate (SRE = 1; DSE = 1)   |
| —      | Port rise/fall time for medium I/O pins <sup>[5][6]</sup>                    | 0.8 | —   | 4   | ns                        | $2.7 \leq VDD \leq 3.6$ V,<br>Fast slew rate (SRE = 0; DSE = 0) |

Table continues on the next page...

Table 17. General switching specifications...continued

| Symbol | Description                                               | Min | Typ | Max | Unit | Condition                                                                      |
|--------|-----------------------------------------------------------|-----|-----|-----|------|--------------------------------------------------------------------------------|
| —      | Port rise/fall time for medium I/O pins <sup>[5][6]</sup> | 1   | —   | 7   | ns   | $2.7 \leq VDD \leq 3.6$ V,<br>Slow slew rate (SRE = 1; DSE = 0)                |
| —      | Port rise/fall time for medium I/O pins <sup>[5][6]</sup> | 0.8 | —   | 4   | ns   | $1.71 \leq VDD < 2.7$ V,<br>Fast slew rate (SRE = 0; DSE = 1)                  |
| —      | Port rise/fall time for medium I/O pins <sup>[5][6]</sup> | 1   | —   | 7   | ns   | $1.71 \leq VDD < 2.7$ V,<br>Slow slew rate (SRE = 1; DSE = 1)                  |
| —      | HD pins <sup>[7]</sup>                                    | 2.2 | —   | 7   | ns   | $2.7 \leq VDD \leq 3.6$ V,<br>Normal drive, fast slew rate (SRE = 0; DSE = 0)  |
| —      | Port rise/fall time for HD pins <sup>[7]</sup>            | 1   | —   | 7   | ns   | $2.7 \leq VDD \leq 3.6$ V,<br>Normal drive (DSE = 0), fast slew rate (SRE = 0) |
| —      | Port rise/fall time for HD pins <sup>[7]</sup>            | 3.5 | —   | 15  | ns   | $2.7 \leq VDD \leq 3.6$ V,<br>Normal drive (DSE = 0), slow slew rate (SRE = 1) |
| —      | Port rise/fall time for HD pins <sup>[7]</sup>            | 1   | —   | 7   | ns   | $1.71 \leq VDD < 2.7$ V,<br>High drive (DSE = 1), Fast slew rate (SRE = 0)     |
| —      | Port rise/fall time for HD pins <sup>[7]</sup>            | 3.5 | —   | 25  | ns   | $1.71 \leq VDD < 2.7$ V,<br>High drive (DSE = 1), Slow slew rate (SRE = 1)     |
| —      | RST pins <sup>[4]</sup>                                   | 3   | —   | 8   | ns   | $2.7 \leq VDD \leq 3.6$ V                                                      |
| —      | RST pins <sup>[4]</sup>                                   | 3.6 | —   | 20  | ns   | $1.71 \leq VDD < 2.7$ V                                                        |

[1] The synchronous and asynchronous timing must be met.

[2] This is the shortest pulse that is guaranteed to be recognized

[3] For the HD I/O pins, setting DSE1 = 1 will support the same rise/fall time at 4x the load capacitance. For the 5VTOL I/O pins, setting DSE1=1 will support the same fall time at 2x the load capacitance, but the rise time will increase due to the increased loading

[4] Load is 25 pF.

[5] Assumes default values in CALIB1 and CALIB0 in PORTS

[6] 25 pF lumped load

[7] Load is 25 pF for DSE=0. Load is 100 pF for DSE=2 or DSE=3. Drive strength and slew rate are configured using PORTx\_PCRn[DSE1], PORTx\_PCRn[DSE], and PORTx\_PCRn[SRE].

### 3.4 Thermal specifications

### 3.4.1 Thermal operating requirements

Table 18. Thermal operating requirements

| Symbol | Description                                   | Min | Typ | Max | Unit | Condition |
|--------|-----------------------------------------------|-----|-----|-----|------|-----------|
| TA     | Ambient temperature <sup>[1]</sup>            | -40 | 25  | 125 | °C   | —         |
| TJ     | Die junction temperature <sup>[2][3][4]</sup> | —   | —   | 125 | °C   | —         |

[1] The device may operate at maximum TA rating as long as TJ maximum of 125 °C is not exceeded. The simplest method to determine TJ is:  $TJ = TA + R_{\theta JA} \times \text{chip power dissipation}$ .

[2] The device operating specification is not guaranteed beyond 125 °C TJ.

[3] The maximum operating requirement applies to all chapters unless otherwise specifically stated.

[4] Operating at maximum conditions for extended periods may affect device reliability. Refer to Product Lifetime Usage Estimates application note (AN14194)

### 3.4.2 Thermal attributes

Table 19. Thermal attributes

| Rating                                                                       | Board Type <sup>[1]</sup> | Symbol          | LQFP64 | LQFP100 | LQFP144 | WFBGA169 | Unit |
|------------------------------------------------------------------------------|---------------------------|-----------------|--------|---------|---------|----------|------|
| Junction to Ambient Thermal Resistance <sup>[2]</sup>                        | 2s2p                      | $R_{\theta JA}$ | 34.5   | 45.3    | 41.9    | 48.2     | °C/W |
| Junction-to-Top of Package Thermal Characterization Parameter <sup>[2]</sup> | 2s2p                      | $\Psi_{JT}$     | 2.2    | 0.7     | 1.3     | 1.6      | °C/W |
| Junction to Case Top Thermal Resistance <sup>[3]</sup>                       | 1s                        | $R_{\theta JC}$ | 18.9   | 15.4    | 14.5    | 19.2     | °C/W |

[1] Thermal test board meets JEDEC specification for this package (JESD51-9 for non-leaded package(BGA) while JESD 51-7 is for leaded package(QFN,QFP,SOIC))

[2] Determined in accordance to JEDEC JESD51-2A natural convection environment. Thermal resistance data in this report is solely for a thermal performance comparison of one package to another in a standardized specified environment. It is not meant to predict the performance of a package in an application-specific environment

[3] Junction-to-Case thermal resistance determined using an isothermal cold plate. For QFN package, case temperature refers to the exposed pad surface temperature at the package bottom side dead centre. For QFP/BGA packages, case temperature refers to the mold surface temperature at the package top side dead centre..

## 4 Peripheral operating requirements and behaviors

### 4.1 Core modules

#### 4.1.1 JTAG Debug Interface Timing

The following table gives the JTAG specifications in debug interface mode.

Table 20. JTAG Debug Interface Timing

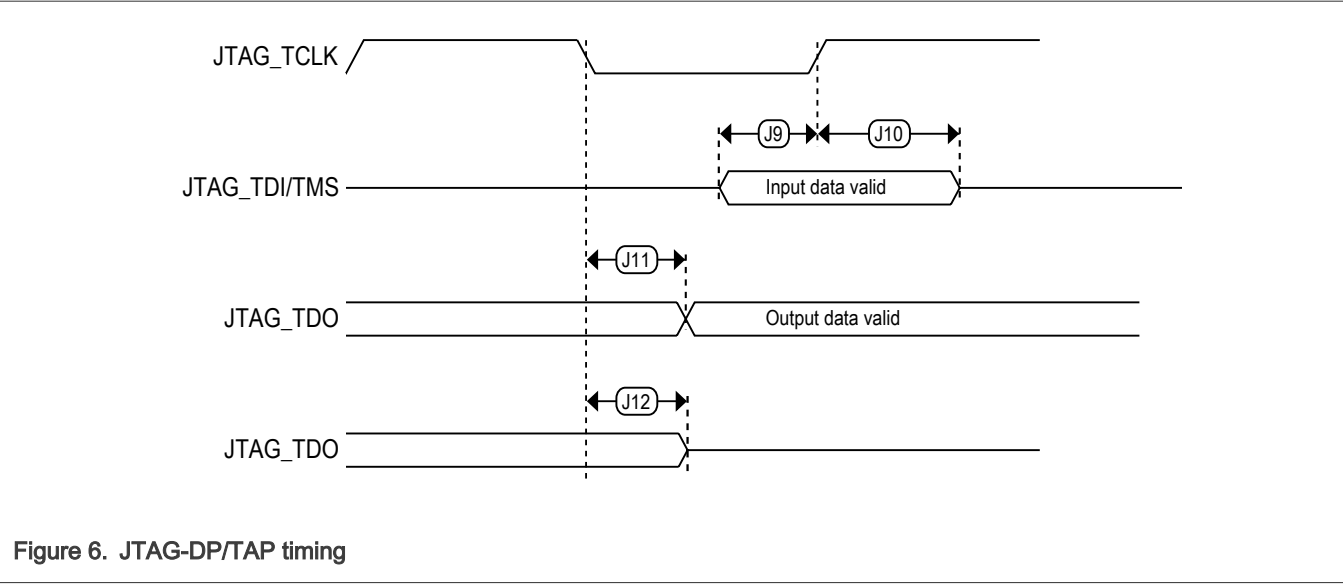
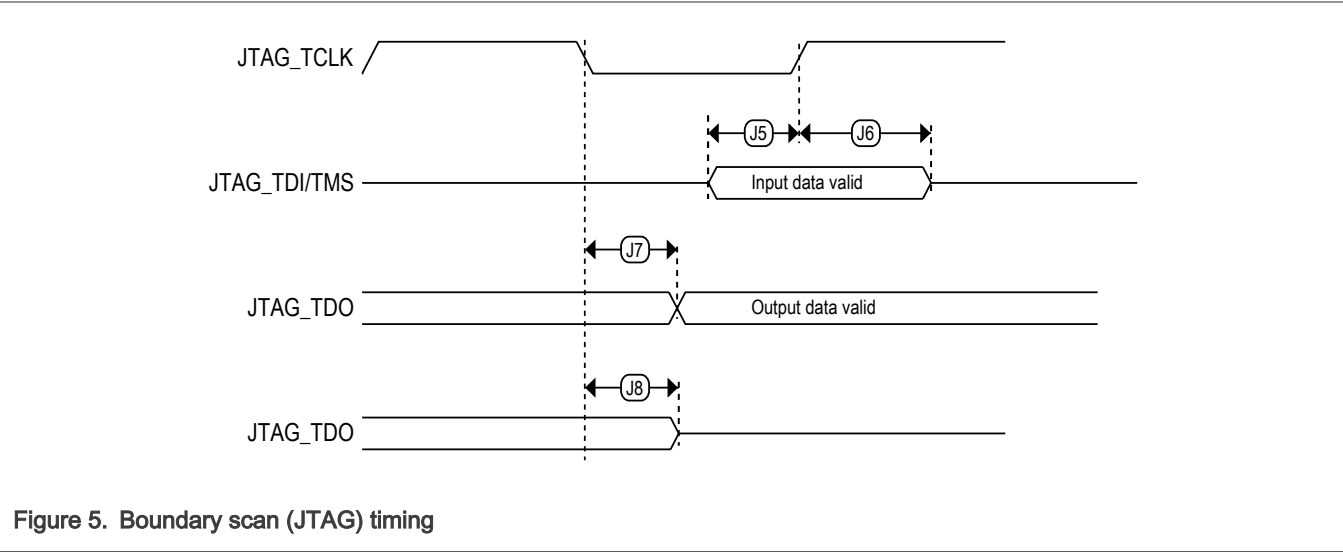
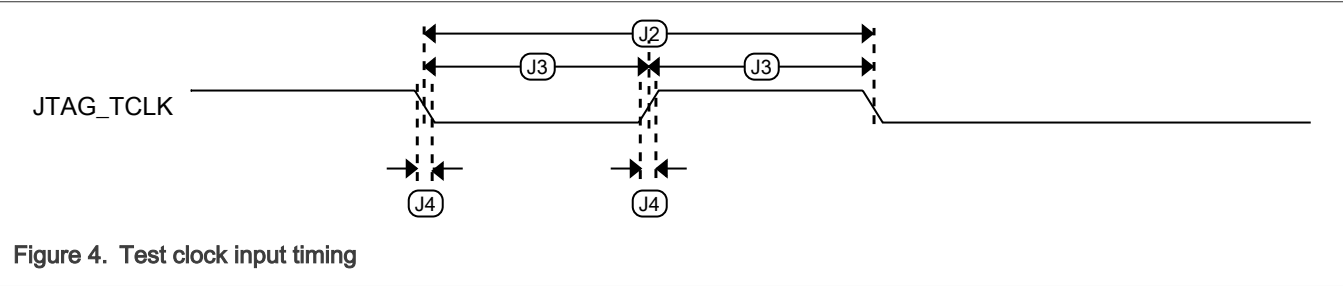
| Symbol | Description                 | Min  | Typ | Max  | Unit | Condition               |
|--------|-----------------------------|------|-----|------|------|-------------------------|
| —      | Operating voltage           | 1.71 | —   | 3.6  | V    | —                       |
| J1     | TCLK frequency of operation | —    | —   | 25   | MHz  | Boundary Scan (OD mode) |
| J1     | TCLK frequency of operation | —    | —   | 12.5 | MHz  | Boundary Scan (MD mode) |

Table continues on the next page...

Table 20. JTAG Debug Interface Timing...continued

| Symbol | Description                                               | Min     | Typ | Max  | Unit | Condition             |
|--------|-----------------------------------------------------------|---------|-----|------|------|-----------------------|
| J1     | TCLK frequency of operation                               | —       | —   | 25   | MHz  | JTAG-DP/TAP (OD mode) |
| J1     | TCLK frequency of operation                               | —       | —   | 12.5 | MHz  | JTAG-DP/TAP (MD mode) |
| J2     | TCLK cycle period                                         | 1000/J1 | —   | —    | ns   | —                     |
| J3     | TCLK clock pulse width                                    | J2/2    | —   | —    | ns   | —                     |
| J4     | TCLK rise and fall times                                  | —       | —   | 3    | ns   | —                     |
| J5     | Boundary scan input data setup time to TCLK rise          | —       | —   | 8    | ns   | OD mode               |
| J5     | Boundary scan input data setup time to TCLK rise          | —       | —   | 16   | ns   | MD mode               |
| J6     | Boundary scan input data hold time after TCLK rise        | 1       | —   | —    | ns   | OD mode               |
| J6     | Boundary scan input data hold time after TCLK rise        | 1       | —   | —    | ns   | MD mode               |
| J7     | TCLK low to boundary scan output data valid               | —       | —   | 18   | ns   | OD mode               |
| J7     | TCLK low to boundary scan output data valid               | —       | —   | 38   | ns   | MD mode               |
| J8     | TCLK low to boundary scan output high-Z                   | —       | —   | 18   | ns   | OD mode               |
| J8     | TCLK low to boundary scan output high-Z                   | —       | —   | 38   | ns   | MD mode               |
| J9     | JTAG-DP/TAP TMS, TDI input data setup time to TCLK rise   | —       | —   | 8    | ns   | OD mode               |
| J9     | JTAG-DP/TAP TMS, TDI input data setup time to TCLK rise   | —       | —   | 16   | ns   | MD mode               |
| J10    | JTAG-DP/TAP TMS, TDI input data hold time after TCLK rise | 1       | —   | —    | ns   | OD mode               |
| J10    | JTAG-DP/TAP TMS, TDI input data hold time after TCLK rise | 1       | —   | —    | ns   | MD mode               |
| J11    | TCLK low to JTAG-DP/TAP TDO data valid                    | —       | —   | 18   | ns   | OD mode               |
| J11    | TCLK low to JTAG-DP/TAP TDO data valid                    | —       | —   | 38   | ns   | MD mode               |
| J12    | TCLK low to JTAG-DP/TAP TDO high-Z                        | —       | —   | 18   | ns   | OD mode               |
| J12    | TCLK low to JTAG-DP/TAP TDO high-Z                        | —       | —   | 38   | ns   | MD mode               |

TDOC represents the TDO bit frame of the scan packet in compact JTAG 2-wire mode.



### 4.1.2 Serial Wire Debug (SWD) Timing

The following table gives the Serial Wire Debug specifications for the device.

Table 21. Serial Wire Debug (SWD) Timing

| Symbol | Description                                     | Min     | Typ | Max  | Unit | Condition |
|--------|-------------------------------------------------|---------|-----|------|------|-----------|
| —      | Operating voltage                               | 1.71    | —   | 3.6  | V    | —         |
| S1     | SWD_CLK frequency of operation                  | —       | —   | 25   | MHz  | OD mode   |
| S1     | SWD_CLK frequency of operation                  | —       | —   | 20   | MHz  | MD mode   |
| S2     | SWD_CLK cycle period                            | 1000/S1 | —   | —    | ns   | OD mode   |
| S2     | SWD_CLK cycle period                            | 1000/S1 | —   | —    | ns   | MD mode   |
| S3     | SWD_CLK clock pulse width                       | 20      | —   | —    | ns   | OD mode   |
| S3     | SWD_CLK clock pulse width                       | 25      | —   | —    | ns   | MD mode   |
| S4     | SWD_CLK rise and fall times                     | —       | —   | 3    | ns   | —         |
| S5     | SWD_DIO input data setup time to SWD_CLK rise   | —       | —   | 10   | ns   | OD mode   |
| S5     | SWD_DIO input data setup time to SWD_CLK rise   | —       | —   | 12.5 | ns   | MD mode   |
| S6     | SWD_DIO input data hold time after SWD_CLK rise | 0       | —   | —    | ns   | OD mode   |
| S6     | SWD_DIO input data hold time after SWD_CLK rise | 0       | —   | —    | ns   | MD mode   |
| S7     | SWD_CLK high to SWD_DIO data valid              | —       | —   | 25   | ns   | OD mode   |
| S7     | SWD_CLK high to SWD_DIO data valid              | —       | —   | 30   | ns   | MD mode   |
| S8     | SWD_CLK high to SWD_DIO high-Z                  | —       | —   | 25   | ns   | OD mode   |
| S8     | SWD_CLK high to SWD_DIO high-Z                  | —       | —   | 30   | ns   | MD mode   |

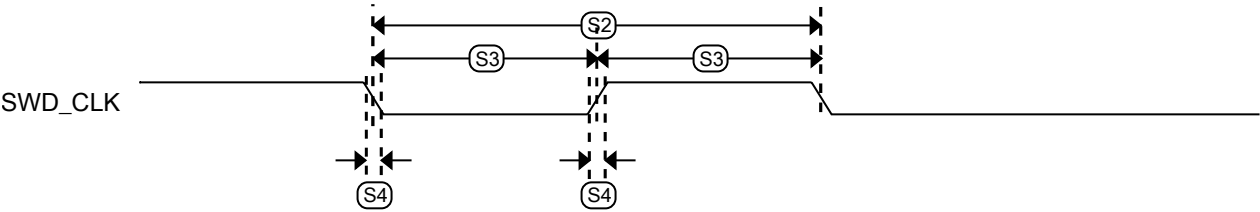
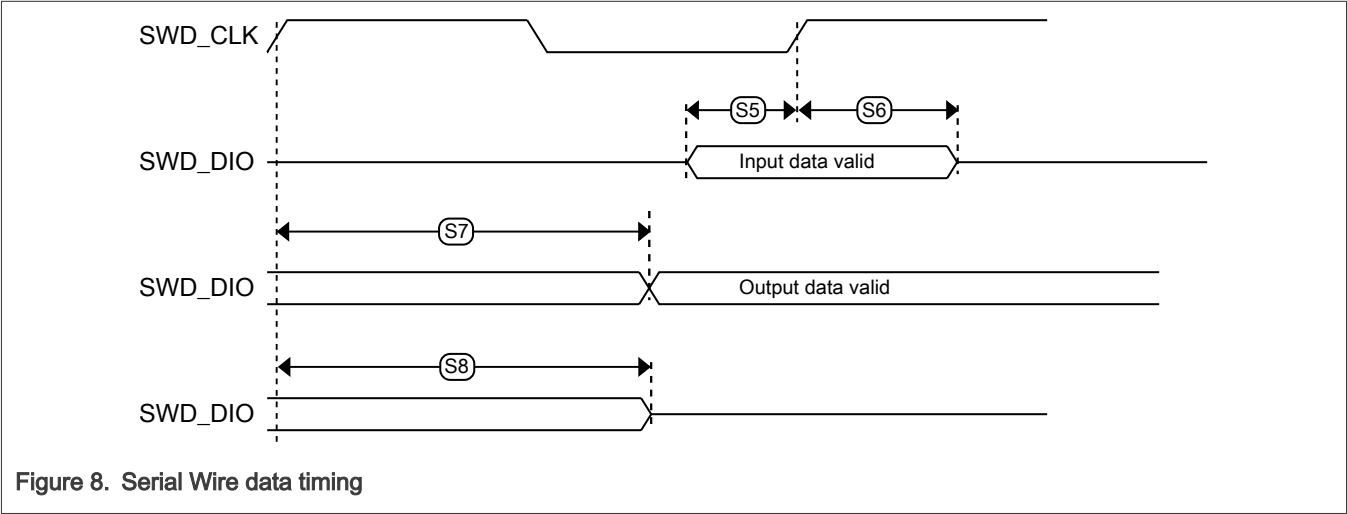


Figure 7. Serial Wire clock input timing



4.2 Clock modules

4.2.1 Reference Oscillator Specification

This chip is designed to meet targeted specifications with a  $\pm 40$  ppm frequency error over the life of the part, which includes the temperature, mechanical, and aging excursions.

The table below shows typical specifications for the Crystal Oscillator.

4.2.1.1 System Crystal Oscillator Specification

Table 22. System Crystal Oscillator Specification

| Symbol    | Description                                              | Min                                | Typ      | Max      | Unit | Condition           |
|-----------|----------------------------------------------------------|------------------------------------|----------|----------|------|---------------------|
| fosc      | Crystal Frequency                                        | 8                                  | —        | 50       | MHz  | —                   |
| Tol       | Frequency tolerance                                      | —                                  | $\pm 10$ | $\pm 40$ | ppm  | —                   |
| Jitosc    | Jitter                                                   | —                                  | 70       | —        | —    | Period jitter (RMS) |
| Vpp       | Peak-to-peak amplitude of oscillation <sup>[1]</sup>     | —                                  | 0.6      | —        | V    | —                   |
| fec       | Externally provided input clock frequency <sup>[2]</sup> | 0                                  | —        | 50       | MHz  | —                   |
| tDC_EXTAL | External clock duty cycle                                | 45                                 | 50       | 55       | %    | —                   |
| Vec       | Externally provided input clock amplitude <sup>[2]</sup> | Refer to VIH and VIL specification | —        | —        | —    | —                   |

[1] When a crystal is being used with the oscillator, the EXTAL and XTAL pins should only be connected to required oscillator components and must not be connected to any other devices.

[2] This specification is for an externally supplied clock driven to EXTAL and does not apply to any other clock input.

#### 4.2.1.2 System Oscillator Crystal Specifications.

Table 23. System Oscillator Crystal Specifications.

| Symbol | Description                          | Min | Typ | Max | Unit | Condition                                                                                     |
|--------|--------------------------------------|-----|-----|-----|------|-----------------------------------------------------------------------------------------------|
| Cin    | Parasitic capacitance of EXTAL       | —   | 2   | 8   | pF   | —                                                                                             |
| Cout   | Parasitic capacitance of XTAL        | —   | 2   | 10  | pF   | —                                                                                             |
| Tstart | Crystal start-up time <sup>[1]</sup> | —   | 186 | —   | μs   | Normal mode<br>fcrystal=16 MHz,<br>Rm=200 Ω, Cp=1 pF,<br>Cload=8 pF, Cm=0.008 pF, Lm=12.37 mH |
| IOSC   | Current consumption                  | —   | 200 | —   | μA   | Normal mode<br>fcrystal=16 MHz,<br>Rm=200 Ω, Cp=1 pF,<br>Cload=8 pF, Cm=0.008 pF, Lm=12.37 mH |
| IOSC   | Current consumption                  | —   | —   | 3   | μA   | Disable mode                                                                                  |

[1] Dependent on crystal specifications, proper PC board layout procedures must be followed to achieve specifications

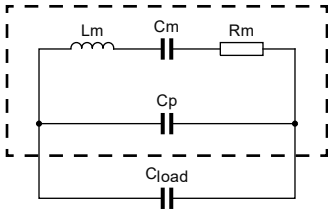


Figure 9. Crystal Electrical Block Diagram

#### 4.2.1.3 System Oscillator Crystal Specifications

Table 24. System Oscillator Crystal Specifications.

| Freq<br>Crystal<br>(MHz) | R <sub>m</sub> (ohms) | C <sub>p</sub> (pF) | C <sub>load</sub> (pF) | C <sub>m</sub> (pF) | L <sub>m</sub> (mH) | Typical<br>startup<br>(μs) <sup>[1]</sup> | Typical<br>Current<br>consumption<br>(μA) <sup>[1]</sup> | Drive level (μW) |     |
|--------------------------|-----------------------|---------------------|------------------------|---------------------|---------------------|-------------------------------------------|----------------------------------------------------------|------------------|-----|
|                          |                       |                     |                        |                     |                     |                                           |                                                          | min              | max |
| 8                        | 100                   | 5.00                | 18.0                   | 0.008               | 49.47               | 1240                                      | 168                                                      | 24               | 34  |
| 16                       | 80                    | 2.00                | 8.00                   | 0.008               | 12.37               | 215                                       | 168.3                                                    | 16               | 22  |
| 16                       | 200                   | 1.00                | 8.00                   | 0.008               | 12.37               | 186                                       | 200.4                                                    | 31               | 46  |
| 25                       | 60                    | 3.00                | 11.0                   | 0.008               | 5.07                | 224                                       | 245.6                                                    | 70               | 93  |
| 25                       | 60                    | 2.00                | 10.0                   | 0.008               | 5.07                | 128                                       | 232.5                                                    | 61               | 80  |
| 25                       | 100                   | 1.00                | 8.00                   | 0.008               | 5.07                | 73.6                                      | 232.7                                                    | 62               | 82  |
| 32                       | 60                    | 3.00                | 9.00                   | 0.008               | 3.09                | 233                                       | 269.6                                                    | 71               | 95  |
| 32                       | 60                    | 2.00                | 8.00                   | 0.008               | 3.09                | 116                                       | 253.2                                                    | 59               | 80  |

Table continues on the next page...

Table 24. System Oscillator Crystal Specifications. ...continued

|    |     |      |      |       |      |      |       |     |     |
|----|-----|------|------|-------|------|------|-------|-----|-----|
| 32 | 100 | 1.00 | 8.00 | 0.008 | 3.09 | 52.4 | 289.3 | 91  | 123 |
| 40 | 50  | 2.00 | 8.00 | 0.008 | 1.98 | 80.4 | 296.9 | 73  | 99  |
| 40 | 60  | 3.00 | 9.00 | 0.008 | 1.98 | 162  | 333.2 | 99  | 135 |
| 48 | 50  | 2.00 | 8.00 | 0.008 | 1.37 | 73.1 | 359.6 | 104 | 140 |
| 48 | 60  | 3.00 | 9.00 | 0.008 | 1.37 | 155  | 407.9 | 138 | 188 |

[1] This is based on simulation

## 4.2.2 FRO180M specifications

Table 25. FRO180M specifications

| Symbol    | Description                                       | Min  | Typ    | Max  | Unit | Condition                                             |
|-----------|---------------------------------------------------|------|--------|------|------|-------------------------------------------------------|
| jitper    | Period jitter RMS <sup>[1]</sup>                  | —    | 70     | —    | ps   | —                                                     |
| jitper    | Accumulated jitter over 10K cycles <sup>[1]</sup> | —    | 800    | —    | ps   | —                                                     |
| TJ        | Operation temperature                             | -40  | 27     | 125  | °C   | —                                                     |
| Vvdda     | Analog supply voltage                             | 1.71 | 3.3    | 3.63 | V    | —                                                     |
| Vvdd      | Digital supply voltage                            | 0.9  | 1.1    | 1.21 | V    | —                                                     |
| Ivdda     | 3.3v analog supply current                        | —    | 50     | —    | μA   | —                                                     |
| Ivdd      | 1.1v analog supply current                        | —    | 58     | —    | μA   | —                                                     |
| Ivdda_dis | 3.3v leakage current                              | —    | 5      | —    | nA   | —                                                     |
| Ivdd_dis  | 1.1v leakage current                              | —    | 40     | —    | nA   | —                                                     |
| Fclkout   | Clock frequency <sup>[2][3]</sup>                 | —    | 45/45  | —    | MHz  | freq_sel[2:0]=3'b001, set the FRO180M trim to 180 MHz |
| Fclkout   | Clock frequency <sup>[2][3]</sup>                 | —    | 60/45  | —    | MHz  | freq_sel[2:0]=3'b011, set the FRO180M trim to 180 MHz |
| Fclkout   | Clock frequency <sup>[2][3]</sup>                 | —    | 90/45  | —    | MHz  | freq_sel[2:0]=3'b101, set the FRO180M trim to 180 MHz |
| Fclkout   | Clock frequency <sup>[2][3]</sup>                 | —    | 180/45 | —    | MHz  | freq_sel[2:0]=3'b111, set the FRO180M trim to 180 MHz |
| Fclkout   | Clock frequency <sup>[2][3]</sup>                 | —    | 60/60  | —    | MHz  | freq_sel[2:0]=3'b001, set the FRO180M trim to 240 MHz |
| Fclkout   | Clock frequency <sup>[2][3]</sup>                 | —    | 80/60  | —    | MHz  | freq_sel[2:0]=3'b011, set the FRO180M trim to 240 MHz |

Table continues on the next page...

Table 25. FRO180M specifications...continued

| Symbol             | Description                                                         | Min   | Typ    | Max  | Unit | Condition                                             |
|--------------------|---------------------------------------------------------------------|-------|--------|------|------|-------------------------------------------------------|
| Fclkout            | Clock frequency <sup>[2][3]</sup>                                   | —     | 120/60 | —    | MHz  | freq_sel[2:0]=3'b101, set the FRO180M trim to 240 MHz |
| Fclkout            | Clock frequency <sup>[2][3]</sup>                                   | —     | 240/60 | —    | MHz  | freq_sel[2:0]=3'b111, set the FRO180M trim to 240 MHz |
| Δfclkout           | Frequency variation for packages other than WFBGA169 <sup>[4]</sup> | -1    | —      | 1    | %    | -40 °C ≤ T <sub>J</sub> ≤ 125 °C                      |
| Fclkout_closetloop | Close loop accuracy with autotrim from an accurate clock source     | -0.25 | —      | 0.25 | %    | —                                                     |
| Tstartup           | Start-up time from disable to 20% accuracy                          | —     | 2      | —    | μs   | —                                                     |
| Tsettle            | Settling time from disable to 1% accuracy                           | —     | —      | 50   | μs   | —                                                     |
| Fovershoot         | frequency overshoot during start-up and settling                    | —     | —      | 2    | %    | —                                                     |
| DC                 | Duty cycle of the clock                                             | 45    | —      | 55   | %    | —                                                     |

[1] Tested at 80 MHz

[2] Frequency in left of slash is fro-hf, and frequency in right of slash is clk\_45m in reference manual clocking chapter

[3] Guaranteed by design

[4] Guaranteed by characterization

### 4.2.3 FRO12M specifications

Table 26. FRO12M specifications

| Symbol   | Description                        | Min | Typ | Max  | Unit | Condition                                              |
|----------|------------------------------------|-----|-----|------|------|--------------------------------------------------------|
| ffro12m  | FRO12M frequency (nominal)         | —   | 12  | —    | MHz  | —                                                      |
| Δffro12m | Frequency deviation                | —   | —   | ±3   | %    | open loop                                              |
| Δffro12m | Frequency deviation                | —   | —   | ±0.6 | %    | closed loop (using accurate clock source as reference) |
| tstartup | Start-up time                      | —   | 5   | —    | μs   | —                                                      |
| fos      | Frequency overshoot during startup | —   | 10  | 20   | %    | —                                                      |
| lfro12m  | Current consumption                | —   | 7   | —    | μA   | —                                                      |

## 4.2.4 FRO16K specifications

Table 27. FRO16K specifications

| Symbol           | Description                                                                | Min | Typ    | Max     | Unit          | Condition |
|------------------|----------------------------------------------------------------------------|-----|--------|---------|---------------|-----------|
| ffro16k          | FRO16K frequency (nominal)                                                 | —   | 16.384 | —       | kHz           | —         |
| $\Delta$ ffro16k | Frequency deviation over $-40^{\circ}\text{C}$ to $125^{\circ}\text{C}$ Ta | —   | —      | $\pm 6$ | %             | open loop |
| TRIMstep         | Trimming step                                                              | —   | 1.5    | —       | %             | —         |
| tstartup         | Start-up time                                                              | —   | 310    | —       | $\mu\text{s}$ | —         |
| Ifro16k          | Current consumption                                                        | —   | 50     | —       | nA            | —         |

## 4.3 Memories and memory interfaces

### 4.3.1 Flash electrical specifications

This section describes the electrical characteristics of the flash memory module.

#### 4.3.1.1 Timing specifications

The following command times assume a flash bus clock frequency of 24 MHz. Command times will be increased by up to 10  $\mu\text{s}$  at 24 MHz if the module is exiting sleep mode when the command is launched. The time to abort a command is not included in the following table.

##### 4.3.1.1.1 Flash command time specifications

Table 28. Flash command time specifications

| Symbol      | Description                                         | Min | Typ | Max  | Unit          | Condition |
|-------------|-----------------------------------------------------|-----|-----|------|---------------|-----------|
| trd1all256k | Read 1s All execution time (256 KB)                 | —   | —   | 1700 | $\mu\text{s}$ | —         |
| trd1all512k | Read 1s All execution time (512 KB)                 | —   | —   | 3200 | $\mu\text{s}$ | —         |
| trd1all1MB  | Read 1s All execution time (1 MB)                   | —   | —   | 6200 | $\mu\text{s}$ | —         |
| trd1blk256k | Read 1s Block execution time (256 KB)               | —   | —   | 1500 | $\mu\text{s}$ | —         |
| trd1blk512k | Read 1s Block execution time (512KB)                | —   | —   | 3050 | $\mu\text{s}$ | —         |
| trd1blk1MB  | Read 1s Block execution time (1MB)                  | —   | —   | 6000 | $\mu\text{s}$ | —         |
| trd1scr     | Read 1s Sector execution time (8 KB) <sup>[1]</sup> | —   | —   | 50   | $\mu\text{s}$ | —         |
| trd1pg      | Read 1s Page execution time (128 B) <sup>[1]</sup>  | —   | —   | 4.4  | $\mu\text{s}$ | —         |
| trd1pglv    | Read 1s Page at low voltage execution time (128 B)  | —   | —   | 5.8  | $\mu\text{s}$ | —         |

Table continues on the next page...

Table 28. Flash command time specifications...continued

| Symbol           | Description                                                        | Min | Typ | Max  | Unit | Condition |
|------------------|--------------------------------------------------------------------|-----|-----|------|------|-----------|
| trd1phr          | Read 1s Phrase execution time (16B) <sup>[1]</sup>                 | —   | —   | 3.8  | μs   | —         |
| trd1phrlv        | Read 1s Phrase at low voltage execution time (16 B)                | —   | —   | 4.8  | μs   | —         |
| trdmisr8k        | Read into MISR (8 KB) <sup>[1]</sup>                               | —   | —   | 50   | μs   | —         |
| trdmisr256k      | Read into MISR (256 KB)                                            | —   | —   | 1500 | μs   | —         |
| trdmisr512k      | Read into MISR (512 KB)                                            | —   | —   | 3050 | μs   | —         |
| trdmisr1M        | Read into MISR (1 MB) <sup>[1]</sup>                               | —   | —   | 6000 | μs   | —         |
| trd1ipg          | Read 1s IFR Page execution time (128 B) <sup>[1]</sup>             | —   | —   | 4.4  | μs   | —         |
| trd1ipglv        | Read 1s IFR Page at low voltage execution time (128 B)             | —   | —   | 5.8  | μs   | —         |
| trd1iphr         | Read 1s IFR Phrase execution time (16 B) <sup>[1]</sup>            | —   | —   | 3.8  | μs   | —         |
| trd1iphrlv       | Read 1s IFR Phrase at low voltage execution time (16 B)            | —   | —   | 4.8  | μs   | —         |
| trdimisr8k       | Read IFR into MISR (8 KB) <sup>[1]</sup>                           | —   | —   | 50   | μs   | —         |
| trdimisr32k      | Read IFR into MISR (32 KB) <sup>[1]</sup>                          | —   | —   | 190  | μs   | —         |
| tpgmpg_initial   | Program Page execution time at < 1k cycles (128 B) <sup>[2]</sup>  | —   | 450 | 600  | μs   | —         |
| tpgmpg_lifetime  | Program Page execution time at > 1k cycles (128 B)                 | —   | 450 | 750  | μs   | —         |
| tpgmphr_initial  | Program Phrase execution time at < 1k cycles (16 B) <sup>[2]</sup> | —   | 135 | 180  | μs   | —         |
| tpgmphr_lifetime | Program Phrase execution time at > 1k cycles (16 B)                | —   | 135 | 225  | μs   | —         |
| tersall256k      | Erase All execution time (256 KB)                                  | —   | —   | 800  | ms   | —         |
| tersall512k      | Erase All execution time (512 KB)                                  | —   | —   | 1500 | ms   | —         |
| tersall1M        | Erase All execution time (1 MB)                                    | —   | —   | 2800 | ms   | —         |
| tmasers256k      | Mass Erase execution time ( via sideband) (256 KB)                 | —   | —   | 800  | ms   | —         |
| tmasers512k      | Mass Erase execution time ( via sideband) (512 KB)                 | —   | —   | 1500 | ms   | —         |
| tmasers1M        | Mass Erase execution time ( via sideband) (1 MB)                   | —   | —   | 2800 | ms   | —         |

Table continues on the next page...

Table 28. Flash command time specifications...continued

| Symbol  | Description                                       | Min | Typ | Max | Unit | Condition |
|---------|---------------------------------------------------|-----|-----|-----|------|-----------|
| terrscr | Erase Sector execution time (8 KB) <sup>[2]</sup> | —   | 2   | 22  | ms   | —         |

[1] Time to abort the command may significantly impact the time to execute the command.

[2] Measured from the time FSTAT[PERDY] is cleared.

#### 4.3.1.2 Flash high voltage current behavior

Table 29. Flash high voltage current behavior

| Symbol     | Description                                                                    | Min | Typ | Max | Unit | Condition |
|------------|--------------------------------------------------------------------------------|-----|-----|-----|------|-----------|
| IDD_IO_PGM | Average current adder to VDD during flash programming operation <sup>[1]</sup> | —   | —   | 6   | mA   | —         |
| IDD_IO_ERS | Average current adder to VDD during flash erase operation <sup>[1]</sup>       | —   | —   | 4   | mA   | —         |

[1] See the Power Management chapter in the reference manual for the specific VDD voltage supply powering the flash array.

#### 4.3.1.3 Flash reliability specifications.

Table 30. Flash reliability specifications.

| Symbol       | Description                                        | Min   | Typ   | Max | Unit   | Condition     |
|--------------|----------------------------------------------------|-------|-------|-----|--------|---------------|
| Tnvmretp10k  | tnvmretp10k                                        | 10    | 50    | —   | years  | Program Flash |
| Nnvmcycscr   | Sector cycling endurance <sup>[1]</sup>            | 10 K  | 500 K | —   | cycles | Program Flash |
| Tnvmretp1k   | Data retention after up to 1 K cycles              | 20    | 100   | —   | years  | Program Flash |
| Tnvmretp100k | Data retention after up to 100 K cycles            | 5     | 50    | —   | years  | Program Flash |
| Nnvmcyc256k  | Sector cycling endurance for 256 KB <sup>[2]</sup> | 100 K | 500 K | —   | cycles | Program Flash |

[1] Sector cycling endurance represents the number of Program/Erase cycles on a single sector at  $-40^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$ .

[2] For devices with a single flash block, sectors must be located within the last 256 KB of the flash main memory. For devices with two flash blocks, sectors must be located within the last 256 KB of each flash main memory but must not total more than 256 KB per device.

**Note:** Typical data retention values are based on measured response accelerated at high temperature and derated to a constant 25°C use profile.

## 4.4 Analog

### 4.4.1 ADC electrical specifications

## 4.4.1.1 ADC operating conditions

Table 31. ADC operating conditions

| Symbol       | Description                              | Min   | Typ   | Max   | Unit       | Condition                   |
|--------------|------------------------------------------|-------|-------|-------|------------|-----------------------------|
| VDDAD        | Supply voltage                           | 1.71  | —     | 3.6   | V          | —                           |
| VSSAD        | Ground voltage                           | -0.1  | 0     | 0.1   | V          | —                           |
| $\Delta VDD$ | — [1]                                    | -0.1  | 0     | 0.1   | V          | —                           |
| $\Delta VSS$ | — [1]                                    | -0.1  | 0     | 0.1   | V          | —                           |
| VREFH        | Reference Voltage High [2]               | 0.99  | VDDAD | VDDAD | V          | —                           |
| VREFL        | Reference Voltage Low [3]                | VSSAD | VSSAD | VSSAD | V          | —                           |
| VADIN        | Input Voltage [3][4][5]                  | VREFL | —     | VREFH | V          | —                           |
| FADCK        | ADC conversion clock frequency           | 6     | —     | 24    | MHz        | Low-power mode, PWRSEL=0    |
| FADCK        | ADC conversion clock frequency           | 6     | —     | 64    | MHz        | Normal Mode, 16b, PWRSEL=1  |
| FADCK        | ADC conversion clock frequency           | 6     | —     | 64    | MHz        | Normal Mode, 12b , PWRSEL=1 |
| RAS          | Analog source resistance (external) [6]  | —     | —     | 5     | k $\Omega$ | —                           |
| RADIN        | Input Resistance ADC channels 7:0 [7][8] | —     | —     | 1.65  | k $\Omega$ | VDDAD $\geq$ 1.71 V         |
| RADIN        | Input Resistance ADC channels 7:0 [7][8] | —     | —     | 1.525 | k $\Omega$ | VDDAD $\geq$ 2.1 V          |
| RADIN        | Input Resistance ADC channels 7:0 [7][8] | —     | 0.925 | 1.35  | k $\Omega$ | VDDAD $\geq$ 2.5 V          |
| CADIN        | Input Capacitance                        | —     | 1.92  | 2.4   | pF         | —                           |

[1] DC potential difference

[2] Minimum VDDAD/VREFH is 2.4 V in high-speed mode (when HS =1)

[3] For devices that do not have a dedicated VREFL and VSS\_ANA pins, VREFL and VSS\_ANA are tied to VSS internally.

[4] If VREFH is less than VDD\_ANA, then voltage inputs greater than VREFH but less than VDD\_ANA are allowed but result in a full-scale conversion result

[5] ADC selected inputs and unselected dedicated inputs must not exceed VDD\_ANA during an ADC conversion. Unselected muxed inputs may exceed VDD\_ANA but must not exceed the IO supply associated with the inputs (VDD) when a conversion is in progress. If an ADC input may exceed these levels, then a minimum of 1 K series resistance must be used between the source and the ADC input pin.

[6] This resistance is external to MCU. To achieve the best results, the analog source resistance must be kept as low as possible.

[7] There are several types of ADC inputs. To see which channels correspond to which type of ADC inputs, see channel index map in reference manual

[8] If the input come through a mux in the IO pad, add the IO Mux Resistance Adder value to the resistance for the channel type

## 4.4.1.2 I/O mux resistance table

Table 32. I/O mux resistance table

| Symbol | Description        | Min | Typ  | Max  | Unit       | Condition        |
|--------|--------------------|-----|------|------|------------|------------------|
| RIOMUX | I/O MUX Resistance | —   | —    | 5.35 | k $\Omega$ | VDD $\geq$ 1.71v |
| RIOMUX | I/O MUX Resistance | —   | —    | 1    | k $\Omega$ | VDD $\geq$ 2.1v  |
| RIOMUX | I/O MUX Resistance | —   | 0.35 | 0.66 | k $\Omega$ | VDD $\geq$ 2.5 v |

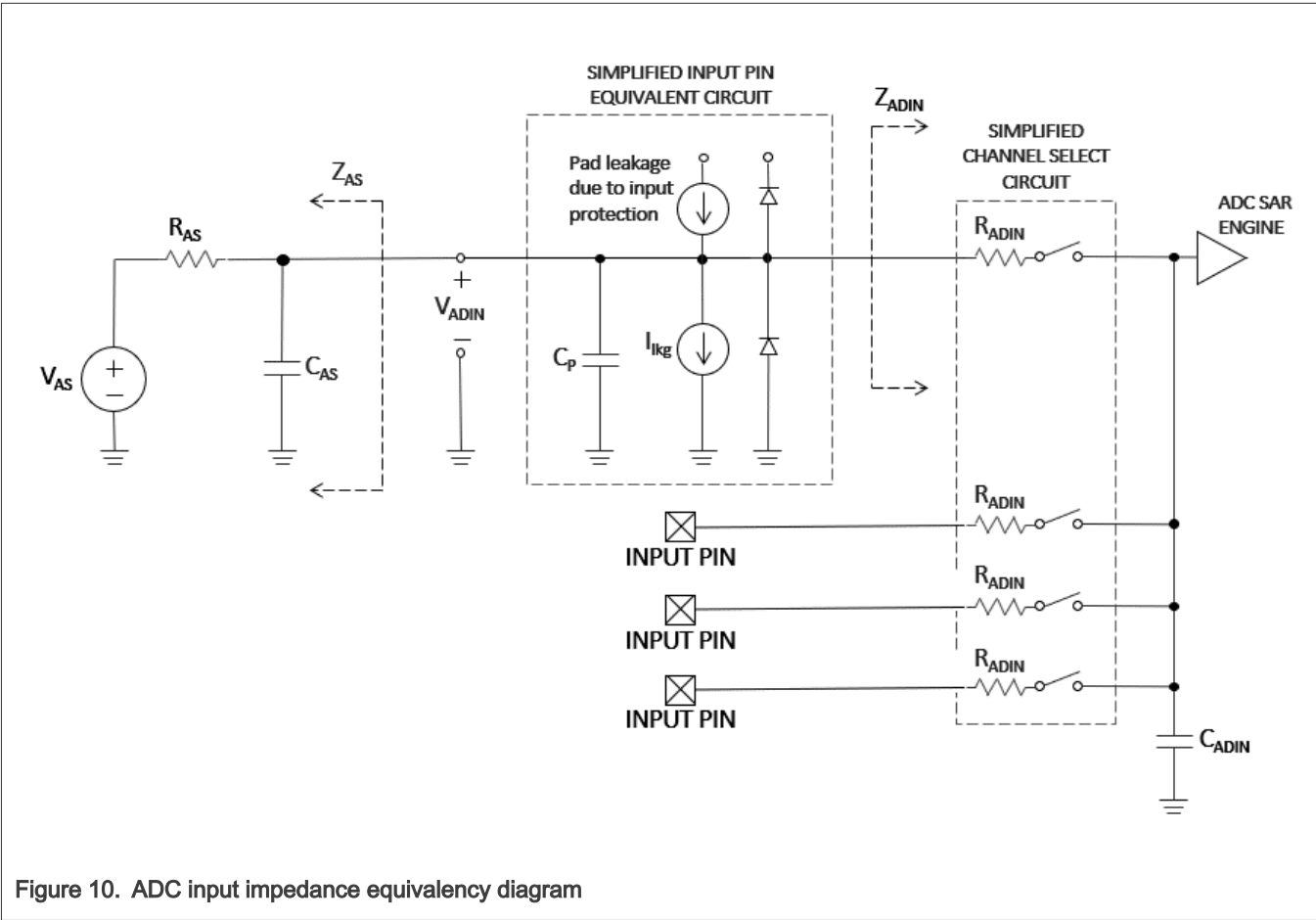


Figure 10. ADC input impedance equivalency diagram

#### 4.4.1.3 ADC electrical characteristics

**Note:** Typical values are for reference only and are not tested in production

Table 33. ADC electrical characteristics

| Symbol | Description                   | Min | Typ | Max | Unit | Condition                                              |
|--------|-------------------------------|-----|-----|-----|------|--------------------------------------------------------|
| —      | Supply current <sup>[1]</sup> | —   | 7   | —   | —    | PWREN=0,<br>Conversions triggered<br>at 10 kS/s        |
| IDDAD  | Supply current <sup>[1]</sup> | —   | 60  | —   | μA   | PWREN=1, No<br>Conversions                             |
| IDDAD  | Supply current <sup>[1]</sup> | —   | 194 | —   | μA   | Low-power mode,<br>6 MHz Clock,<br>PWRSEL=0, 16b mode  |
| IDDAD  | Supply current <sup>[1]</sup> | —   | 251 | —   | μA   | Low-power mode,<br>24 MHz clock,<br>PWRSEL=0, 16b mode |
| IDDAD  | Supply current <sup>[1]</sup> | —   | 658 | —   | μA   | Normal Mode, 64 MHz,<br>PWRSEL=1, 12b mode             |

Table continues on the next page...

Table 33. ADC electrical characteristics...continued

| Symbol   | Description                                                        | Min   | Typ       | Max   | Unit   | Condition                                                                              |
|----------|--------------------------------------------------------------------|-------|-----------|-------|--------|----------------------------------------------------------------------------------------|
| IDDAD    | Supply current <sup>[1]</sup>                                      | —     | 757       | —     | μA     | High Speed Mode, 64 MHz Clock, PWRSEL=1, HS=1, 12b mode                                |
| IDDTS    | Temp Sensor Supply Current                                         | —     | 50        | —     | μA     | Temperature Sensor Adder                                                               |
| CSMP     | ADC Sample cycles <sup>[2]</sup>                                   | 3.5   | —         | 131.5 | cycles | Low-power mode and High speed mode                                                     |
| Fconv    | ADC conversion rate <sup>[3]</sup>                                 | —     | —         | 4.0   | MS/s   | 12b mode, (HS=1)                                                                       |
| Fconv    | ADC conversion rate <sup>[3]</sup>                                 | —     | —         | 3.2   | MS/s   | 16b mode, (HS=1)                                                                       |
| TSMP_REQ | Required Sample Time <sup>[4]</sup>                                | —     | —         | —     | ns     | Use equation based on RAS, RIOMUX, RADIN, CADIN, RAS, CAS, CP and desired accuracy (B) |
| TSMP     | Sample Time <sup>[5]</sup>                                         | 145.8 | TSMP_R EQ | —     | ns     | Low-power mode                                                                         |
| TSMP     | Sample Time <sup>[6]</sup>                                         | 54.7  | TSMP_R EQ | —     | ns     | High-speed 16b mode                                                                    |
| TSMP     | Sample Time <sup>[6]</sup>                                         | 54.7  | TSMP_R EQ | —     | ns     | High-speed 12b mode                                                                    |
| TSMPINT  | Internal channel sample time inputs <sup>[7]</sup>                 | 2.0   | —         | —     | μs     | —                                                                                      |
| DNL      | Differential non-linearity <sup>[8][9][10]</sup>                   | —     | ±0.7      | ±0.9  | LSB    | 12b mode, N = 12 bits                                                                  |
| INL      | Integral non-linearity <sup>[8][9][10]</sup>                       | —     | ±0.5      | ±0.8  | LSB    | 12b mode, N = 12 bits                                                                  |
| DNL      | Differential non-linearity <sup>[8][9][10]</sup>                   | —     | ±0.5      | ±0.7  | LSB    | N = 14 bits, for 16-bit specification, multiply by 4.                                  |
| INL      | Integral non-linearity <sup>[8][9][10]</sup>                       | —     | ±0.5      | ±0.8  | LSB    | N = 14 bits, for 16-bit specification, multiply by 4.                                  |
| ZSE      | Zero-scale error (V_ADIN = V_REFL) <sup>[8][9]</sup>               | —     | ±1        | —     | LSB    | 12b mode                                                                               |
| FSE      | Full-scale error (V_ADIN = V_REFH) <sup>[8][9]</sup>               | —     | ±2        | —     | LSB    | 12b mode                                                                               |
| TUE      | Total Unadjusted Error <sup>[8][9]</sup>                           | —     | ±3        | —     | LSB    | 12b mode                                                                               |
| ENOB16   | Effective number of bits, 16b Mode, 1 kHz input <sup>[9][11]</sup> | —     | 15.0      | —     | bits   | 25.2 kS/s (FADCK = 64 MHz, HS =1, AVGS=0111)                                           |

Table continues on the next page...

Table 33. ADC electrical characteristics...continued

| Symbol   | Description                                                               | Min | Typ  | Max | Unit | Condition                                   |
|----------|---------------------------------------------------------------------------|-----|------|-----|------|---------------------------------------------|
| ENOB16   | Effective number of bits, 16b Mode, 1 kHz input <sup>[9][11]</sup>        | —   | 13.6 | —   | bits | 200 kS/s (FADCK = 64 MHz, HS=1, AVGS =0100) |
| ENOB16   | Effective number of bits, 16b Mode, 1 kHz input                           | —   | 12.7 | —   | bits | 800 kS/s (FADCK = 64 MHz, HS=1, AVGS =0010) |
| ENOB16   | Effective number of bits, 16b Mode, 1 kHz input                           | —   | 11.7 | —   | bits | 3.2 MS/s (FADCK = 64 MHz, HS=1, AVGS =0000) |
| ENOB12   | Effective number of bits, 12b Mode, 1 kHz input <sup>[9][11]</sup>        | —   | 11.5 | —   | bits | 1.0 MS/s (FADCK = 64 MHz, HS =1, AVGS=0010) |
| ENOB12   | Effective number of bits, 12b Mode, 1 kHz input <sup>[9][11]</sup>        | —   | 11.0 | —   | bits | 4.0 MS/s (FADCK = 64 MHz, HS =1, AVGS=0000) |
| SNDR16   | Signal-to-noise plus distortion, 16b Mode, 1 kHz input <sup>[9][11]</sup> | —   | 92.4 | —   | dB   | 25.2 kS/s (FADCK=64 MHz, HS=1, AVGS=0111)   |
| SNDR16   | Signal-to-noise plus distortion, 16b Mode, 1 kHz input <sup>[9][11]</sup> | —   | 84.1 | —   | dB   | 200 kS/s (FADCK=64 MHz, HS=1, AVGS=0100)    |
| SNDR16   | Signal-to-noise plus distortion, 16b Mode, 1 kHz input <sup>[9][11]</sup> | —   | 78.3 | —   | dB   | 800 kS/s (FADCK=64MHz, HS=1, AVGS=0010)     |
| SNDR16   | Signal-to-noise plus distortion, 16b Mode, 1 kHz input                    | —   | 72   | —   | dB   | 3.2 MS/s (FADCK=64 MHz, HS=1, AVGS=0000)    |
| SNDR12   | Signal-to-noise plus distortion, 12b Mode, 1 kHz input <sup>[9][11]</sup> | —   | 71.0 | —   | dB   | 1.0 MS/s (FADCK=64 MHz, HS=1, AVGS=0010)    |
| SNDR12   | Signal-to-noise plus distortion, 12b Mode, 1 kHz input <sup>[9][11]</sup> | —   | 68.0 | —   | dB   | 4.0 MS/s (FADCK=64 MHz, HS=1, AVGS=0000)    |
| SFDR     | Spurious free dynamic range <sup>[9][11]</sup>                            | —   | 88.0 | —   | dB   | 12b/16b Mode, 1kHz input, AVGS =0010        |
| SFDR     | Spurious free dynamic range <sup>[9][11]</sup>                            | —   | 82.0 | —   | dB   | 12b/16b Mode, 1kHz input, AVGS =0000        |
| tADCSTUP | Start-up time <sup>[10][12]</sup>                                         | 5   | —    | —   | μs   | —                                           |
| E_TS     | Temperature sensor error <sup>[13]</sup>                                  | —   | ±1   | ±3  | °C   | T <sub>j</sub> =−40 to 105 °C               |
| E_TS     | Temperature sensor error <sup>[13]</sup>                                  | —   | ±2   | ±4  | °C   | T <sub>j</sub> =−40 to 125 °C               |

Table continues on the next page...

Table 33. ADC electrical characteristics...continued

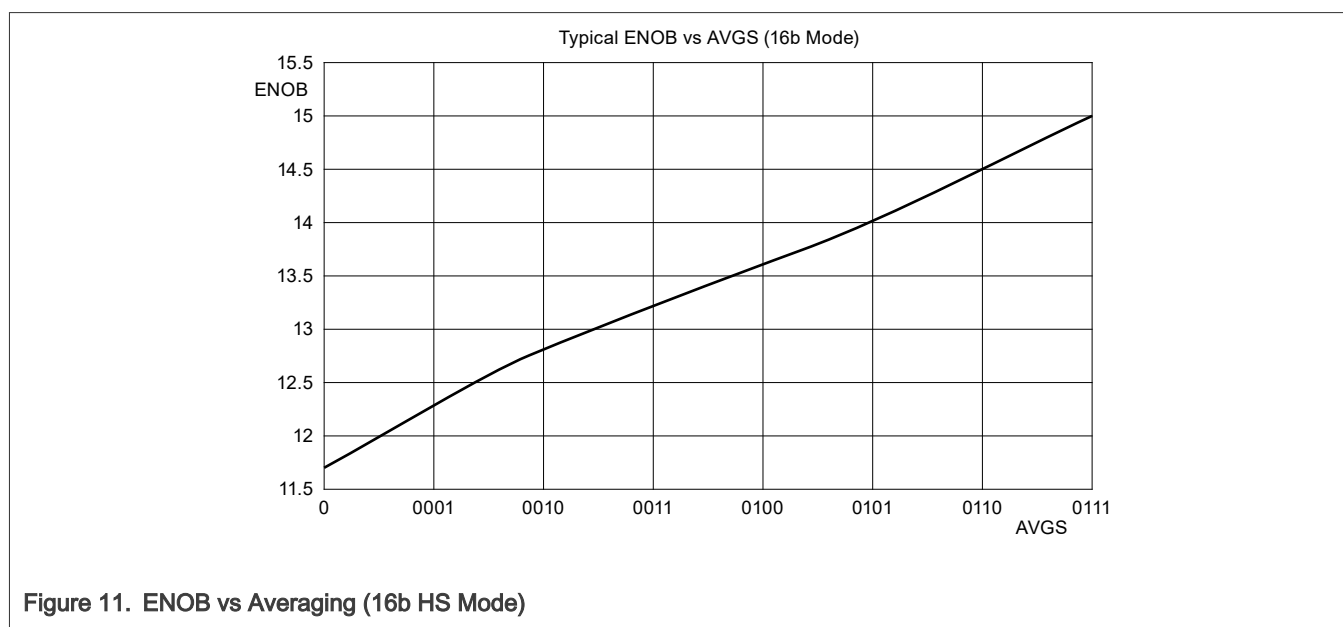
| Symbol   | Description                                             | Min | Typ   | Max | Unit | Condition |
|----------|---------------------------------------------------------|-----|-------|-----|------|-----------|
| A        | Temp Sensor Slope Constant <sup>[1]</sup> <sub>4]</sub> | —   | 738   | —   | °C   | —         |
| B        | Temp Sensor Offset Constant <sup>[14]</sup>             | —   | 287.5 | —   | °C   | —         |
| $\alpha$ | Temp Sensor Bandgap Constant <sup>[14]</sup>            | —   | 10.06 | —   | °C   | —         |

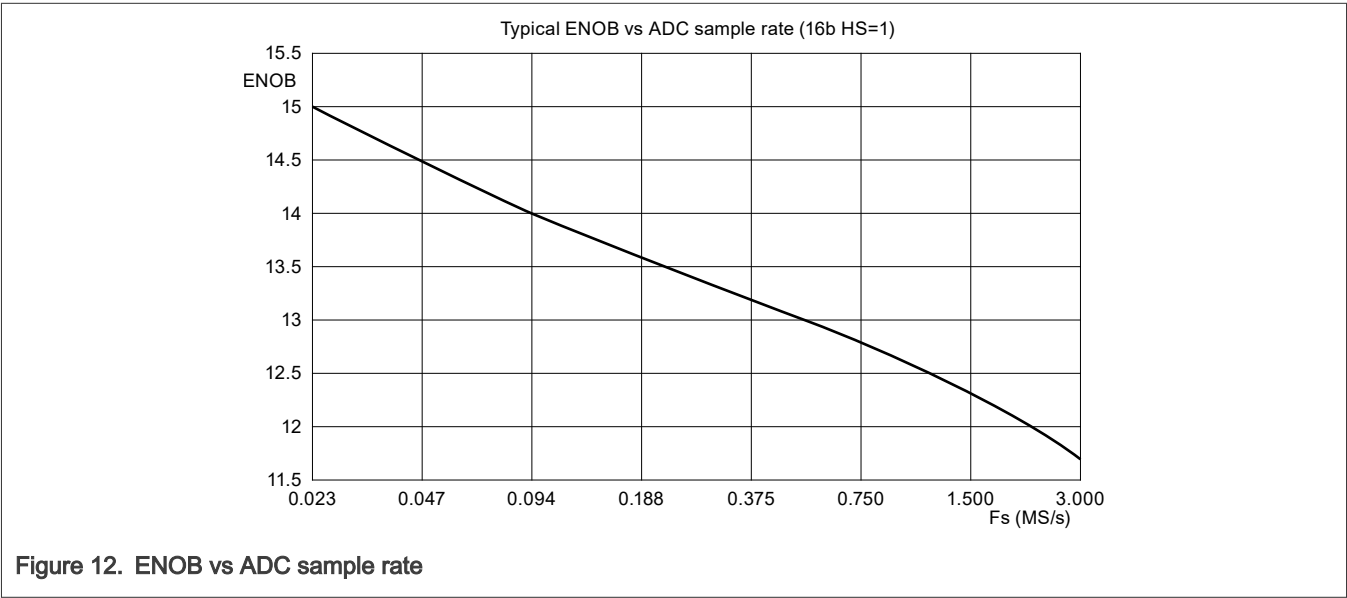
- [1] The ADC supply current depends on the ADC conversion clock speed, conversion rate, and power mode. Typical value show is at 6 MHz, 24 MHz, and 64 MHz. For lowest power operation, PWRSEL should be set to 0.
- [2] Must meet minimum TSMP requirement
- [3] fADCK=64 MHz (HS Mode)
- [4] Required sample time is dictated by external components RAS, CAS, internal components RADIN, CADIN, CP, and desired sample accuracy in bits (B). Calculate it with formula:  $TSMP\_REQ = B * \ln(2) * [RAS * (CAS + CP + CADIN) + (RAS + RIOMUX + RADIN) * CADIN(typ)]$ . RIOMUX=0 unless the ADC input channel goes through an analog mux in the IO"
- [5] Min based on 3.5 cycles
- [6] Min based on 3.5 cycles @ 64 MHz
- [7] Internal channel inputs are those that do not come from external source (temperature sensor, bandgap).
- [8]  $1 \text{ LSB} = (VREFH - VREFL) / 2^N$
- [9] All accuracy numbers assume that the ADC is calibrated with VREFH=VDD\_ANA and using a high- speed- dedicated input channel. Typical values assume VDD\_ANA = 3.0 V, Temp = 25 °C, fADCK = 24 MHz, sample time of 3.5 ADCK cycles (CMDHn[STS]=0h) unless otherwise stated. Typical values are for reference only, and are not tested in production.
- [10] Guaranteed by characterization
- [11] Dynamic results assume Fin=1 kHz sinewave, no averaging unless otherwise specified
- [12] Delay required if PWREN=0. Set the power-up delay (PUDLY) according to the ADC start-up time if PWREN=0.
- [13] The temperature sensor can be calibrated to a +/- 1 % precision after board assembly by using a 3-temperature calibration flow with accurate  $\pm 0.15 \%$  temperature chamber
- [14]  $T(^{\circ}\text{C}) = A * [\alpha(Vbe8 - Vbe1) / (Vbe8 + \alpha(Vbe8 - Vbe1))] - B$  where Vbe1 is the first value stored to FIFO as a result of the temperature sensor channel conversion, Vbe8 is the second value stored to FIFO as a result of the temperature sensor channel conversion, A is the slope factor, B is the offset factor,  $\alpha$  is the bandgap coefficient

Typical values are for reference only and are not tested in production

fADCK=60 MHz (HS Mode)

Min based on 3.5 cycles @ 60 MHz





#### 4.4.2 12-bit DAC electrical characteristics

##### 4.4.2.1 12-bit DAC operating requirements

Table 34. 12-bit DAC operating requirements

| Symbol     | Description                            | Min  | Typ | Max     | Unit | Condition |
|------------|----------------------------------------|------|-----|---------|------|-----------|
| VDD_ANA    | Supply voltage                         | 1.71 | —   | 3.6     | V    | —         |
| VDACR      | Reference Voltage                      | 0.97 | —   | VDD_ANA | V    | —         |
| CL         | Output load capacitance <sup>[1]</sup> | —    | 50  | 100     | pF   | —         |
| IL         | Output load current <sup>[2]</sup>     | -1   | —   | 1       | mA   | —         |
| DAC_c_rate | DAC conversion rate                    | —    | —   | 1       | MSPS | —         |

[1] A small load capacitance (50 pF) can improve the bandwidth performance of the DAC.

[2] Sink or source current availability

The DAC reference can be selected to be VDD\_ANA or VREFH, keep VDD\_ANA be the highest voltage.

##### 4.4.2.2 12-bit DAC operating behaviors

Table 35. 12-bit DAC operating behaviors

| Symbol  | Description                                              | Min | Typ | Max | Unit | Condition      |
|---------|----------------------------------------------------------|-----|-----|-----|------|----------------|
| IDD_DAC | Supply Current                                           | —   | 300 | 500 | μA   | Normal mode    |
| IDD_DAC | Supply Current                                           | —   | 100 | 150 | μA   | Low-power mode |
| IDD_DAC | Supply Current                                           | —   | 10  | —   | nA   | Disabled       |
| tDAC    | Full-scale settling time (0x100 to 0xF00) <sup>[1]</sup> | —   | 2.5 | 3   | μs   | Normal mode    |

Table continues on the next page...

Table 35. 12-bit DAC operating behaviors...continued

| Symbol   | Description                                                                       | Min       | Typ   | Max   | Unit  | Condition      |
|----------|-----------------------------------------------------------------------------------|-----------|-------|-------|-------|----------------|
| tDAC     | Full-scale settling time (0x100 to 0xF00) <sup>[1]</sup>                          | —         | 5     | 6     | μs    | Low-power mode |
| tccDAC   | Code-to-code settling time (0xBF8 to 0xC08) <sup>[1]</sup>                        | —         | 0.7   | 1     | μs    | —              |
| Vdacoutl | DAC output voltage range low<br>— high-speed mode, no load,<br>DAC set to 0x000   | —         | —     | 100   | mV    | —              |
| Vdacouth | DAC output voltage range high<br>— high-speed mode, no load,<br>DAC set to 0xFFFF | VDACR-100 | —     | VDACR | mV    | —              |
| INL      | Integral non-linearity error <sup>[2]</sup>                                       | —         | —     | ±3    | LSB   | —              |
| DNL      | Differential non-linearity error <sup>[3]</sup>                                   | —         | —     | ±1    | LSB   | —              |
| EOFFSET  | Offset error <sup>[4]</sup>                                                       | —         | ± 0.4 | ± 0.8 | %FSR  | —              |
| EG       | Gain error <sup>[4]</sup>                                                         | —         | ± 0.3 | ± 0.6 | %FSR  | VDACR < 2.1 V  |
| EG       | Gain error <sup>[4]</sup>                                                         | —         | ± 0.1 | ± 0.3 | %FSR  | VDACR > 2.1 V  |
| PSRR     | Power supply rejection ratio,<br>VDD_ANA ≥ 2.4 V                                  | —         | 70    | —     | dB    | —              |
| TCO      | Temperature coefficient offset<br>voltage at middle scale <sup>[5]</sup>          | —         | —     | —     | μV/C  | —              |
| TEO      | Temperature coefficient offset<br>error                                           | —         | 30    | —     | μV/C  | —              |
| TGE      | Temperature coefficient gain<br>error                                             | —         | 10    | —     | PPM/C | —              |
| ROP      | Output resistance (load = 10<br>kΩ)                                               | —         | 200   | —     | Ω     | —              |
| SR       | Slew rate 100 h -> F00 h or F00<br>h -> 100 h                                     | —         | 3.6   | —     | V/μs  | —              |
| SR       | Slew rate 100 h -> F00 h or F00<br>h -> 100 h                                     | —         | 0.5   | —     | V/μs  | —              |
| TPU      | Power-up time                                                                     | —         | 2.5   | —     | μs    | —              |

[1] Settling within ±1 LSB measured with a 47 pF load.

[2] The INL is measured for 0 + 100 mV to VDACR - 100 mV

[3] The DNL is measured for 0 + 100 mV to VDACR - 100 mV

[4] Calculated by a best fit curve from VSS\_ANA + 100 mV to VDACR - 100 mV

[5] VDD\_ANA = 3.0 V, reference select set for VDD\_ANA (DACx\_CO: DACRFS = 1), high- power mode (DACx\_C0: LPEN = 0), DAC set to 0x800, temperature range is across the full range of the device.

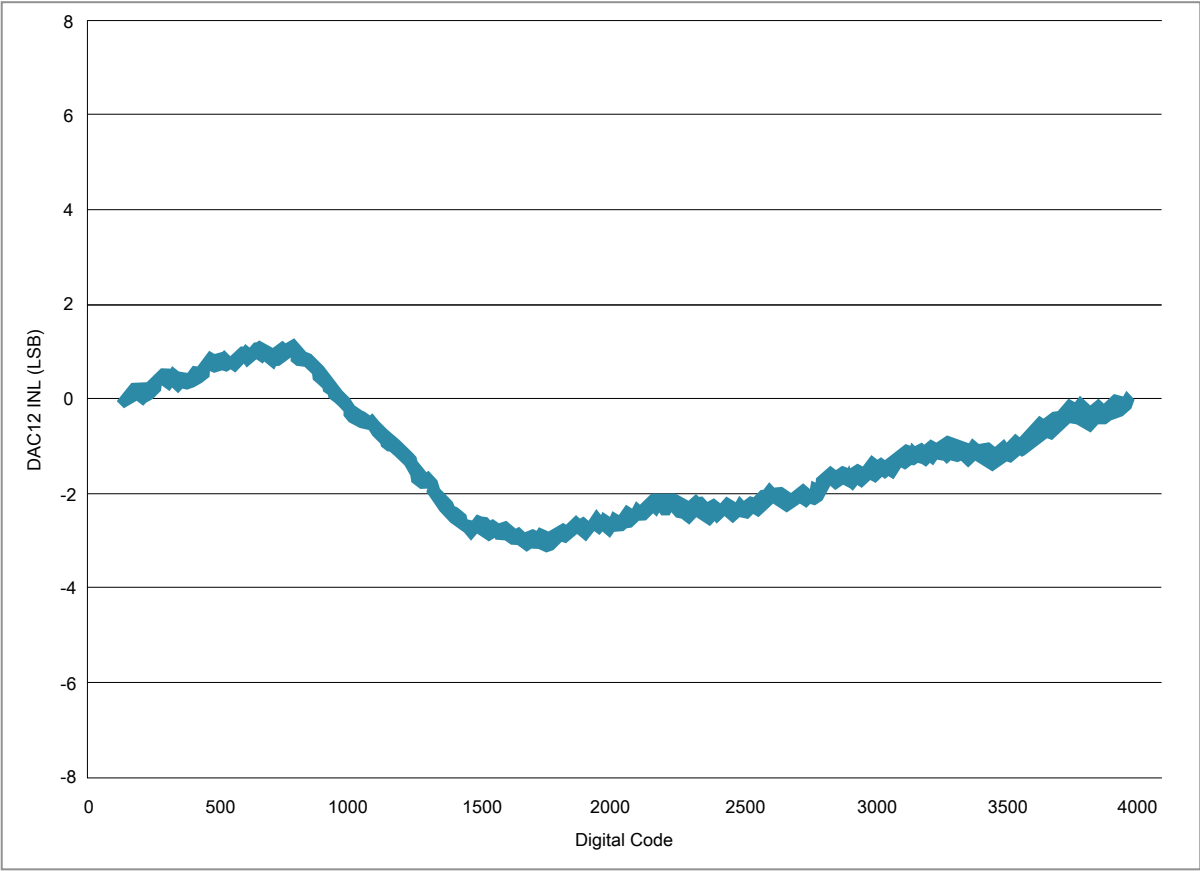


Figure 13. Typical INL error vs. digital code

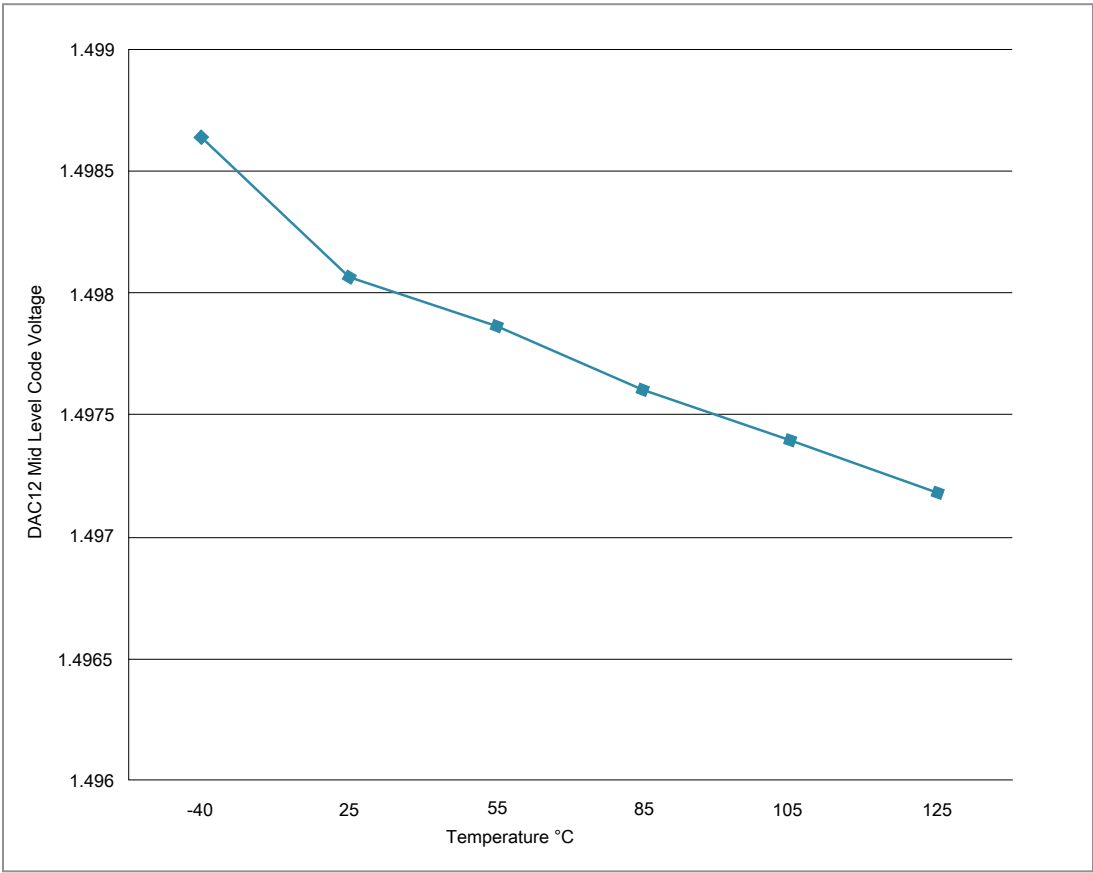


Figure 14. Offset at half scale vs. temperature

4.4.3 Comparator and 8-bit DAC electrical specifications

Table 36. Comparator and 8-bit DAC electrical specifications

| Symbol  | Description                      | Min  | Typ | Max | Unit | Condition                             |
|---------|----------------------------------|------|-----|-----|------|---------------------------------------|
| VDD     | Supply voltage                   | 1.71 | —   | 3.6 | V    | —                                     |
| VREFH   | 8-bit DAC reference voltage high | 0.97 | —   | VDD | V    | —                                     |
| IDD_CMP | Supply current                   | —    | 200 | —   | μA   | High speed mode (EN=1, HPMD=1)        |
| IDD_CMP | Supply current                   | —    | 10  | —   | μA   | Normal mode (EN=1, HPMD=0, NPMD=0)    |
| IDD_CMP | Supply current                   | —    | 400 | —   | nA   | Low-power mode (EN=1, HPMD=0, NPMD=1) |
| VAIN    | Analog input voltage             | VSS  | —   | VDD | V    | —                                     |
| VAIO    | Analog input offset voltage      | —    | —   | 20  | mV   | High speed mode                       |

Table continues on the next page...

Table 36. Comparator and 8-bit DAC electrical specifications...continued

| Symbol | Description                                           | Min       | Typ | Max  | Unit | Condition                                        |
|--------|-------------------------------------------------------|-----------|-----|------|------|--------------------------------------------------|
| VAIO   | Analog input offset voltage                           | —         | —   | 20   | mV   | Normal mode                                      |
| VAIO   | Analog input offset voltage                           | —         | —   | 40   | mV   | Low-power mode                                   |
| VH     | Analog comparator hysteresis <sup>[1]</sup>           | —         | 0   | —    | mV   | CR0[HYSTCTR] = 00                                |
| VH     | Analog comparator hysteresis <sup>[1]</sup>           | —         | 10  | —    | mV   | CR0[HYSTCTR] = 01                                |
| VH     | Analog comparator hysteresis <sup>[1]</sup>           | —         | 20  | —    | mV   | CR0[HYSTCTR] = 10                                |
| VH     | Analog comparator hysteresis <sup>[1]</sup>           | —         | 30  | —    | mV   | CR0[HYSTCTR] = 11                                |
| VCMPOh | Output high                                           | VDD - 0.2 | —   | —    | V    | —                                                |
| VCMPOI | Output low                                            | —         | —   | 0.2  | V    | —                                                |
| tD     | Propagation delay <sup>[2]</sup>                      | —         | —   | 25   | ns   | High speed mode, 100 mV overdrive, power > 1.71V |
| tD     | Propagation delay <sup>[2]</sup>                      | —         | —   | 50   | ns   | High speed mode, 30 mV overdrive, power > 1.71V  |
| tD     | Propagation delay <sup>[2]</sup>                      | —         | —   | 600  | ns   | Normal mode, 30 mV overdrive, power > 1.71V      |
| tD     | Propagation delay <sup>[2]</sup>                      | —         | —   | 5    | μs   | Low-power mode, 30 mV overdrive, power > 1.71V   |
| tinit  | Analog comparator initialization delay <sup>[3]</sup> | —         | —   | 40   | μs   | —                                                |
| IDAC8b | 8-bit DAC current adder (enabled)                     | —         | 10  | —    | μA   | High power mode (EN=1, PMODE=1)                  |
| IDAC8b | 8-bit DAC current consumption                         | —         | 1   | —    | μA   | Low power mode (EN=1, PMODE=0)                   |
| INL    | 8-bit DAC integral non-linearity <sup>[4]</sup>       | -1        | —   | +1.0 | LSB  | Low/High power mode, supply power > 1.71V        |
| DNL    | 8-bit DAC differential non-linearity                  | -1        | —   | +1.0 | LSB  | Low/High power mode, power > 1.71V               |

[1] Typical hysteresis is measured with input voltage range limited to 0.6 to VDD\_ANA-0.6 V.

[2] Overdrive does not include input offset voltage or hysteresis. The propagation delay is defined as the time delay between the change of the voltage on input pin and the output change of the comparator analog part

[3] Comparator initialization delay is defined as the time between software writes to change control inputs (Writes to CMP\_DACCR[DACEN], CMP\_DACCR[VRSEL], CMP\_DACCR[VOSEL], CMP\_MUXCR[PSEL], and CMP\_MUXCR[MSEL]) and the comparator output settling to a stable level.

[4] 1 LSB = Vreference/256

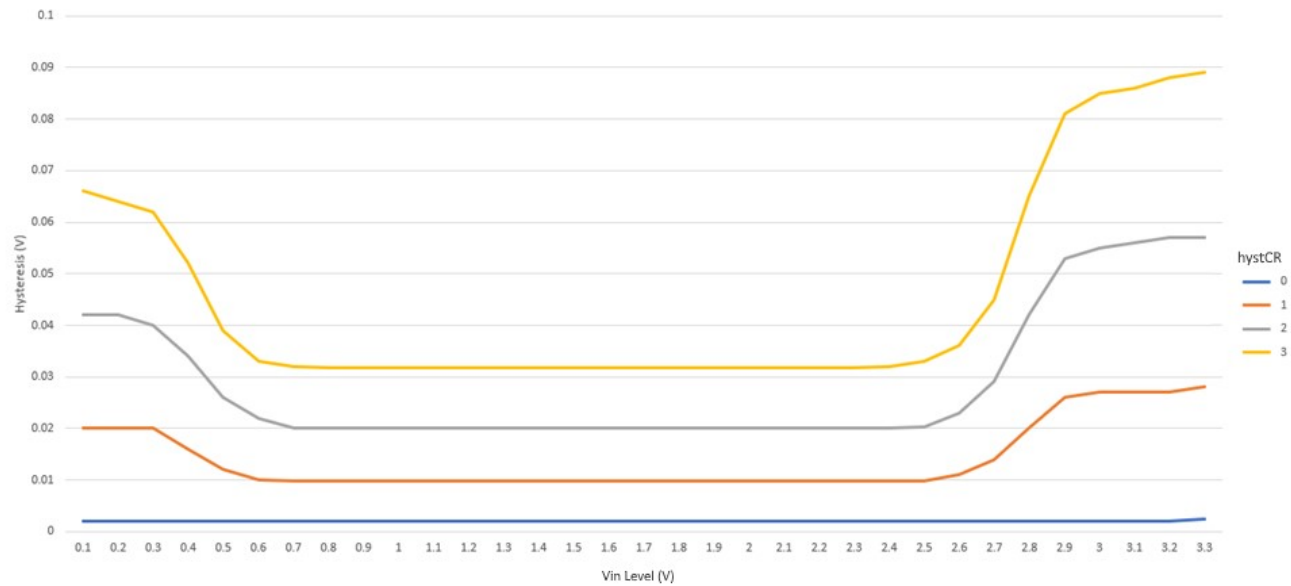


Figure 15. Typical hysteresis vs. Vin level (VDD = 3.3 V, HPMD = 1)

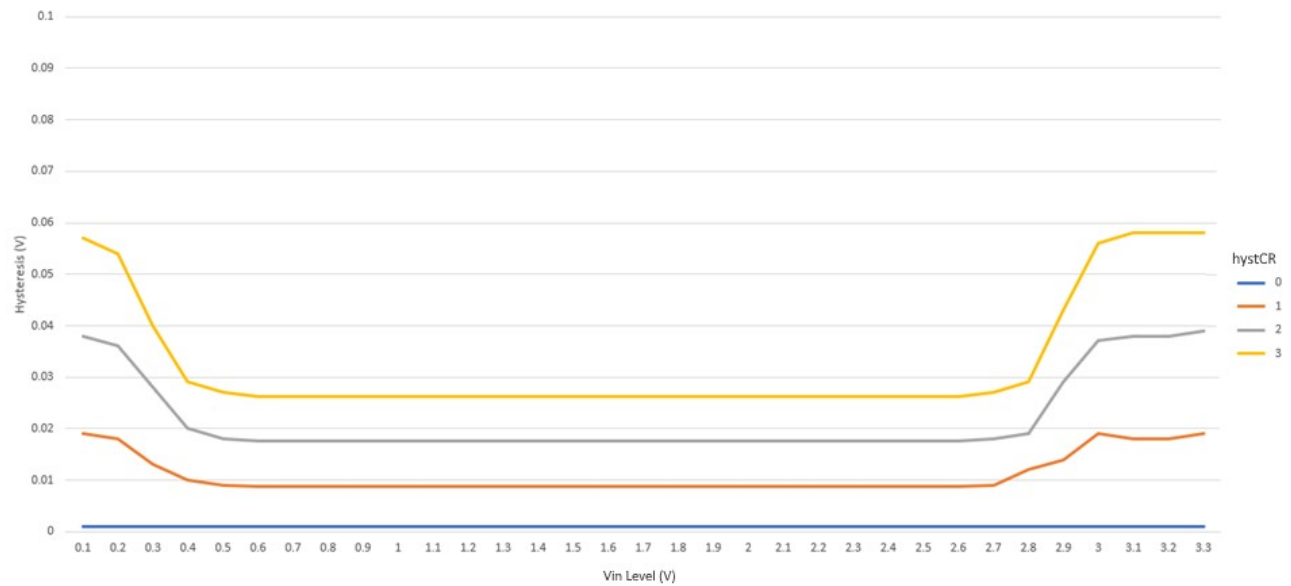


Figure 16. Typical hysteresis vs. Vin level (VDD = 3.3 V, HPMD = 0, NPMD = 0)

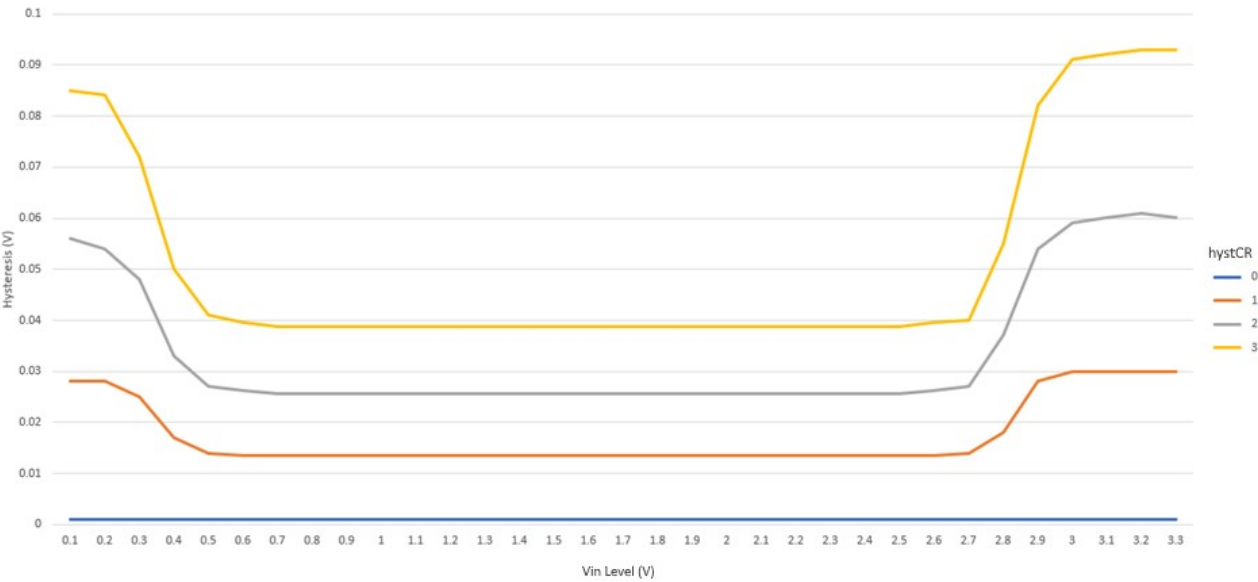


Figure 17. Typical hysteresis vs Vin level (VDD =3.3 V, HPMD = 0, NPMD = 1)

4.4.4 OpAmp electrical specifications

Table 37. OpAmp electrical specifications

| Symbol | Description            | Min  | Typ | Max  | Unit | Condition |
|--------|------------------------|------|-----|------|------|-----------|
| TJ     | Operation temperature  | -40  | 25  | 125  | °C   | —         |
| Vvdda  | Analog supply voltage  | 1.71 | 3   | 3.6  | V    | —         |
| Vvdd   | Digital supply voltage | 0.9  | 1.1 | 1.21 | V    | —         |

General

Table 38. OpAmp electrical specifications

| Symbol | Description                     | Min  | Typ | Max          | Unit | Condition |
|--------|---------------------------------|------|-----|--------------|------|-----------|
| Ivdda  | Analog supply current           | —    | 500 | —            | μA   | —         |
| Cin    | Input capacitance               | —    | —   | 5            | pF   | —         |
| Cload  | Load capacitance                | —    | —   | 20           | pF   | —         |
| Rload  | Load resistance                 | 3    | —   | 20           | KΩ   | —         |
| Vcm    | Input common mode voltage range | 0    | —   | Vvdda-1      | V    | —         |
| Vout   | Output voltage range            | 0.15 | —   | Vvdda - 0.15 | V    | —         |

Table continues on the next page...

Table 38. OpAmp electrical specifications...continued

| Symbol       | Description                       | Min | Typ   | Max | Unit          | Condition                   |
|--------------|-----------------------------------|-----|-------|-----|---------------|-----------------------------|
| Ishutdown_3v | Leakage current for vdda_3v pin   | —   | 1     | 80  | nA            | When Vvdda = 3V             |
| Vos          | Input offset voltage              | -7  | 0     | 7   | mV            | —                           |
| CMRR         | Input common mode rejection ratio | —   | 80    | —   | dB            | —                           |
| PSRR         | Power supply rejection ratio      | —   | 80    | —   | dB            | —                           |
| UGB          | Unity gain bandwidth              | —   | 8     | —   | MHz           | CC config=2'b00, gain=2     |
| UGB          | Unity gain bandwidth              | —   | 16    | —   | MHz           | CC config=2'b01, gain=4     |
| UGB          | Unity gain bandwidth              | —   | 32    | —   | MHz           | CC config=2'b10, gain=8     |
| UGB          | Unity gain bandwidth              | —   | 64    | —   | MHz           | CC config=2'b11, gain=16    |
| Av           | DC open loop voltage gain         | -   | 95    | -   | dB            | —                           |
| PM           | Phase marge                       | -   | 60    | -   | deg           | —                           |
| Tsettle      | Settling time                     | -   | 450   | -   | ns            | —                           |
| SR           | Slew rate                         | -   | 10    | -   | V/us          | —                           |
| Vn           | Voltage noise density @1KHz       | —   | 150   | —   | nV/<br>sqrtHz | Gain = 1                    |
| Zout         | Closed-loop output impedance      | —   | 1.703 | —   | Ohm           | cc config=2'b00, f = 200KHz |
| Zout         | Closed-loop output impedance      | —   | 14.72 | —   | Ohm           | cc config=2'b01, f = 200KHz |
| Zout         | Closed-loop output impedance      | —   | 8.514 | —   | Ohm           | cc config=2'b00, f = 1MHz   |
| Zout         | Closed-loop output impedance      | —   | 73.47 | —   | Ohm           | cc config=2'b01, f = 1MHz   |

## 4.5 Timers

See [General switching specifications](#).

## 4.6 Communication Interfaces

### 4.6.1 LPUART

See [General switching specifications](#).

### 4.6.2 LPSPI switching specifications

The Low Power Serial Peripheral Interface (LPSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The following tables provide timing characteristics for classic SPI timing modes.

## 4.6.2.1 LPSPI controller mode timing

Table 39. LPSPI controller mode timing

| Symbol | Description                                     | Min      | Typ | Max    | Unit    | Condition             |
|--------|-------------------------------------------------|----------|-----|--------|---------|-----------------------|
| LP1    | Frequency of operation <sup>[1]</sup>           | —        | —   | —      | MHz     | —                     |
| LP1    | LPSPi0 ~ LPSPi1 medium speed pad <sup>[2]</sup> | —        | —   | 50     | MHz     | Controller in OD mode |
| LP1    | LPSPi0 ~ LPSPi1 slow speed pad <sup>[2]</sup>   | —        | —   | 25     | MHz     | Controller in OD mode |
| LP1    | LPSPi0 ~ LPSPi1 medium speed pad <sup>[2]</sup> | —        | —   | 25     | MHz     | Controller in MD mode |
| LP1    | LPSPi0 ~ LPSPi1 slow speed pad <sup>[2]</sup>   | —        | —   | 25     | MHz     | Controller in MD mode |
| LP2    | SPSCK period                                    | 1000/LP1 | —   | —      | ns      | —                     |
| LP3    | Enable lead time <sup>[3]</sup>                 | 1/2      | —   | —      | tperiph | —                     |
| LP4    | Enable lag time <sup>[3]</sup>                  | 1/2      | —   | —      | tperiph | —                     |
| LP5    | Clock (SPSCK) high or low time                  | tSCK/2-3 | —   | tSCK/2 | ns      | —                     |
| LP6    | Data setup time (inputs)                        | —        | —   | —      | ns      | —                     |
| LP6    | LPSPi0 ~ LPSPi1 medium speed pad <sup>[2]</sup> | —        | —   | 4.2    | ns      | Controller in OD mode |
| LP6    | LPSPi0 ~ LPSPi1 slow speed pad <sup>[2]</sup>   | —        | —   | 4.4    | ns      | Controller in OD mode |
| LP6    | LPSPi0 ~ LPSPi1 medium speed pad <sup>[2]</sup> | —        | —   | 5.4    | ns      | Controller in MD mode |
| LP6    | LPSPi0 ~ LPSPi1 slow speed pad <sup>[2]</sup>   | —        | —   | 5.4    | ns      | Controller in MD mode |
| LP7    | Data hold time (inputs)                         | —        | —   | —      | ns      | —                     |
| LP7    | LPSPi0 ~ LPSPi1 medium speed pad <sup>[2]</sup> | 0        | —   | —      | ns      | Controller in OD mode |
| LP7    | LPSPi0 ~ LPSPi1 slow speed pad <sup>[2]</sup>   | 0        | —   | —      | ns      | Controller in OD mode |
| LP7    | LPSPi0 ~ LPSPi1 medium speed pad <sup>[2]</sup> | 0        | —   | —      | ns      | Controller in MD mode |
| LP7    | LPSPi0 ~ LPSPi1 slow speed pad <sup>[2]</sup>   | 0        | —   | —      | ns      | Controller in MD mode |
| LP8    | Data valid (after SPSCK edge)                   | —        | —   | —      | ns      | —                     |
| LP8    | LPSPi0 ~ LPSPi1 medium speed pad <sup>[2]</sup> | —        | —   | 6.4    | ns      | Controller in OD mode |
| LP8    | LPSPi0 ~ LPSPi1 slow speed pad <sup>[2]</sup>   | —        | —   | 12.8   | ns      | Controller in OD mode |

Table continues on the next page...

Table 39. LPSPI controller mode timing...continued

| Symbol | Description                                     | Min | Typ | Max  | Unit | Condition             |
|--------|-------------------------------------------------|-----|-----|------|------|-----------------------|
| LP8    | LPSPi0 ~ LPSPi1 medium speed pad <sup>[2]</sup> | —   | —   | 13.6 | ns   | Controller in MD mode |
| LP8    | LPSPi0 ~ LPSPi1 slow speed pad <sup>[2]</sup>   | —   | —   | 13.6 | ns   | Controller in MD mode |
| LP9    | Data hold time (outputs)                        | —   | —   | —    | ns   | —                     |
| LP9    | LPSPi0 ~ LPSPi1 medium speed pad <sup>[2]</sup> | -1  | —   | —    | ns   | Controller in OD mode |
| LP9    | LPSPi0 ~ LPSPi1 slow speed pad <sup>[2]</sup>   | -1  | —   | —    | ns   | Controller in OD mode |
| LP9    | LPSPi0 ~ LPSPi1 medium speed pad <sup>[2]</sup> | -1  | —   | —    | ns   | Controller in MD mode |
| LP9    | LPSPi0 ~ LPSPi1 slow speed pad <sup>[2]</sup>   | -1  | —   | —    | ns   | Controller in MD mode |

[1] The frequency of operation is also limited to a minimum of  $f_{periph}/2048$  and a max of  $f_{periph}/2$ , where  $f_{periph}$  is the LPSPI peripheral functional clock.

[2] OD mode is MCU at Over drive mode, MD mode is MCU at Middle drive mode.

[3]  $t_{periph} = 1/f_{periph}$

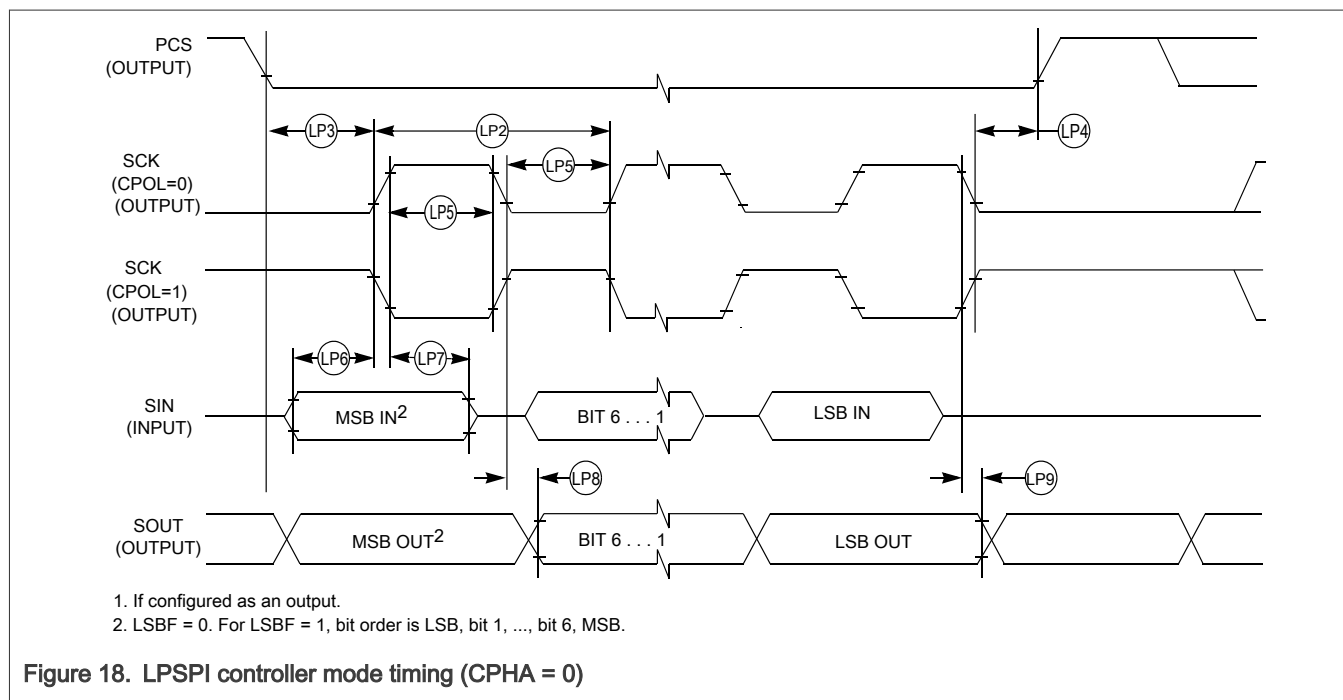


Figure 18. LPSPI controller mode timing (CPHA = 0)

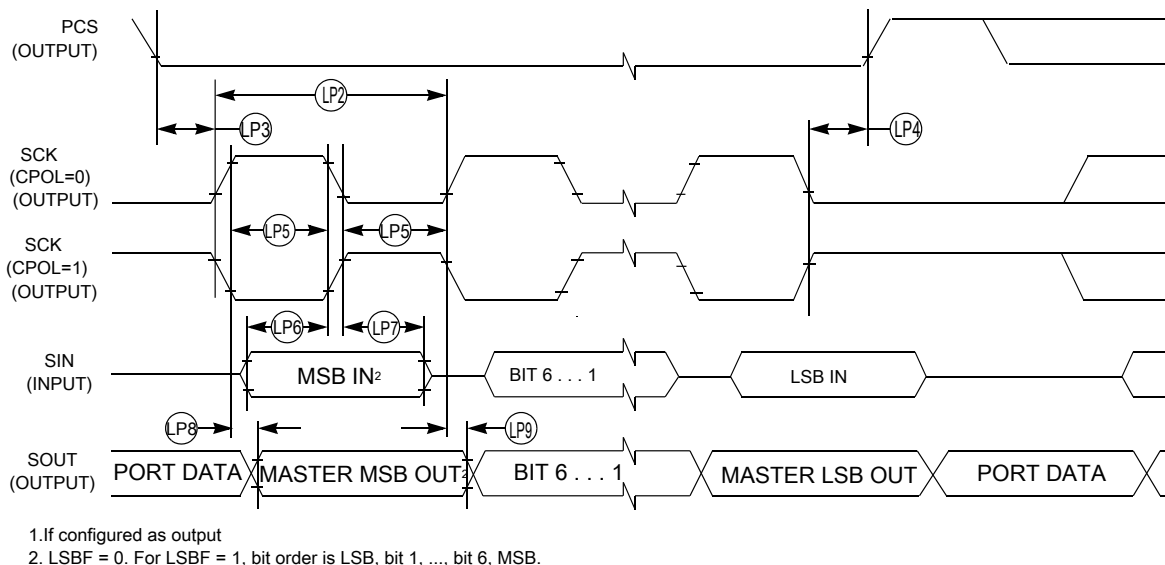


Figure 19. LPSPi controller mode timing (CPHA = 1)

## 4.6.2.2 LPSPi peripheral mode timing

Table 40. LPSPi peripheral mode timing

| Symbol | Description                                      | Min         | Typ | Max            | Unit    | Condition                |
|--------|--------------------------------------------------|-------------|-----|----------------|---------|--------------------------|
| LP1    | Frequency of operation in OD mode <sup>[1]</sup> | —           | —   | —              | —       | —                        |
| LP1    | lpspi0~lpspi1 medium speed pad <sup>[1]</sup>    | —           | —   | 25             | MHz     | Peripheral Tx in OD mode |
| LP1    | lpspi0~lpspi1 slow speed pad <sup>[1]</sup>      | —           | —   | 12.5           | MHz     | Peripheral Tx in OD mode |
| LP1    | lpspi0~lpspi1 medium speed pad                   | —           | —   | 50             | MHz     | Peripheral Rx in OD mode |
| LP1    | lpspi0~lpspi1 slow speed pad                     | —           | —   | 25             | MHz     | Peripheral Rx in OD mode |
| LP1    | lpspi0~lpspi1 medium speed pad                   | —           | —   | 12             | MHz     | Peripheral Tx in MD mode |
| LP1    | lpspi0~lpspi1 slow speed pad                     | —           | —   | 12             | MHz     | Peripheral Tx in MD mode |
| LP1    | lpspi0~lpspi1 medium speed pad                   | —           | —   | 12             | MHz     | Peripheral Rx in MD mode |
| LP1    | lpspi0~lpspi1 slow speed pad                     | —           | —   | 12             | MHz     | Peripheral Rx in MD mode |
| LP2    | SPSCK period                                     | 4 x tperiph | —   | 2048 x tperiph | ns      | —                        |
| LP3    | Enable lead time <sup>[2]</sup>                  | 1           | —   | —              | tperiph | —                        |

Table continues on the next page...

Table 40. LPSPi peripheral mode timing...continued

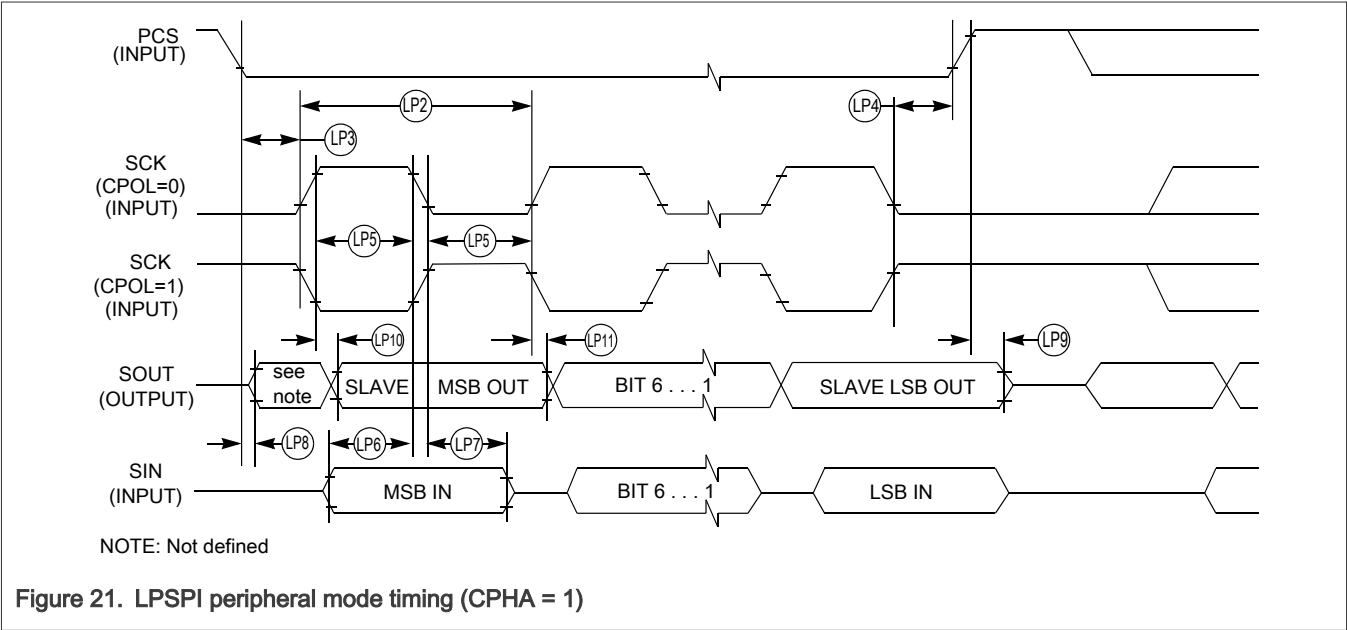
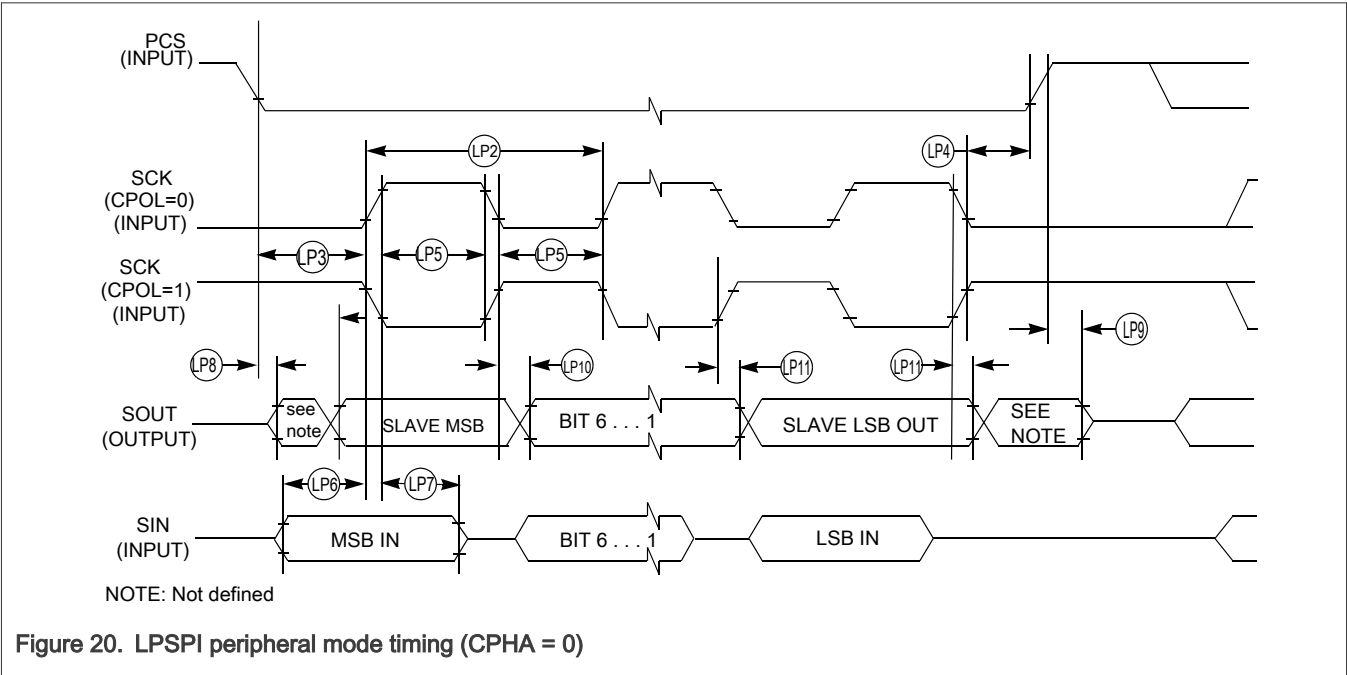
| Symbol | Description                                                   | Min                           | Typ | Max                       | Unit                | Condition                |
|--------|---------------------------------------------------------------|-------------------------------|-----|---------------------------|---------------------|--------------------------|
| LP4    | Enable lag time <sup>[2]</sup>                                | 1                             | —   | —                         | t <sub>periph</sub> | —                        |
| LP5    | Clock (SPSCK) high or low time                                | t <sub>SPSCK</sub> /<br>2 - 5 | —   | t <sub>SPSCK</sub> /<br>2 | ns                  | —                        |
| LP6    | Data setup time (inputs)                                      | —                             | —   | —                         | ns                  | —                        |
| LP6    | lpspi0~lpspi1 medium speed pad                                | —                             | —   | 3.6                       | ns                  | Peripheral Rx in OD mode |
| LP6    | lpspi0~lpspi1 slow speed pad                                  | —                             | —   | 7.2                       | ns                  | Peripheral Rx in OD mode |
| LP6    | lpspi0~lpspi1 medium speed pad                                | —                             | —   | 12.8                      | ns                  | Peripheral Rx in MD mode |
| LP6    | lpspi0~lpspi1 slow speed pad                                  | —                             | —   | 12.8                      | ns                  | Peripheral Rx in MD mode |
| LP7    | Data hold time (inputs)                                       | —                             | —   | —                         | ns                  | —                        |
| LP7    | lpspi0~lpspi1 medium speed pad                                | 0                             | —   | —                         | ns                  | Peripheral Rx in OD mode |
| LP7    | lpspi0~lpspi1 slow speed pad                                  | 0                             | —   | —                         | ns                  | Peripheral Rx in OD mode |
| LP7    | lpspi0~lpspi1 medium speed pad                                | 0                             | —   | —                         | ns                  | Peripheral Rx in MD mode |
| LP7    | lpspi0~lpspi1 slow speed pad                                  | 0                             | —   | —                         | ns                  | Peripheral Rx in MD mode |
| LP8    | Peripheral access time <sup>[2][3]</sup>                      | —                             | —   | t <sub>periph</sub>       | ns                  | —                        |
| LP9    | Peripheral MISO disable time <sup>[2]</sup><br><sup>[4]</sup> | —                             | —   | t <sub>periph</sub>       | ns                  | —                        |
| LP10   | Data valid (after SPSCK edge)                                 | —                             | —   | —                         | ns                  | —                        |
| LP10   | lpspi0~lpspi1 medium speed pad                                | —                             | —   | 15.6                      | ns                  | Peripheral Tx in OD mode |
| LP10   | lpspi0~lpspi1 slow speed pad                                  | —                             | —   | 31.2                      | —                   | Peripheral Tx in OD mode |
| LP10   | lpspi0~lpspi1 medium speed pad                                | —                             | —   | 29.2                      | ns                  | Peripheral Tx in MD mode |
| LP10   | lpspi0~lpspi1 slow speed pad                                  | —                             | —   | 29.2                      | ns                  | Peripheral Tx in MD mode |
| LP11   | Data hold time (outputs)                                      | —                             | —   | —                         | ns                  | —                        |
| LP11   | lpspi0~lpspi1 medium speed pad                                | 2                             | —   | —                         | ns                  | Peripheral Tx in OD mode |
| LP11   | lpspi0~lpspi1 slow speed pad                                  | 2                             | —   | —                         | ns                  | Peripheral Tx in OD mode |

Table continues on the next page...

Table 40. LPSPi peripheral mode timing...continued

| Symbol | Description                    | Min | Typ | Max | Unit | Condition                |
|--------|--------------------------------|-----|-----|-----|------|--------------------------|
| LP11   | lpspi0~lpspi1 medium speed pad | 2   | —   | —   | ns   | Peripheral Tx in MD mode |
| LP11   | lpspi0~lpspi1 slow speed pad   | 2   | —   | —   | ns   | Peripheral Tx in MD mode |

- [1] The frequency of operation is also limited to a minimum of  $f_{\text{periph}}/2048$  and a max of  $f_{\text{periph}}/4$ , where  $f_{\text{periph}}$  is the LPSPi peripheral functional clock.  
[2]  $t_{\text{periph}} = 1/f_{\text{periph}}$   
[3] Time to data active from high-impedance state  
[4] Hold time to high-impedance state



## 4.6.3 LPI2C timing

Table 41. LPI2C timing

| Symbol   | Description                                                                                                  | Min        | Typ | Max  | Unit | Condition |
|----------|--------------------------------------------------------------------------------------------------------------|------------|-----|------|------|-----------|
| fSCL     | SCL Clock Frequency in standard mode                                                                         | 0          | —   | 100  | kHz  | —         |
| fSCL     | SCL Clock Frequency in fast mode                                                                             | 0          | —   | 400  | kHz  | —         |
| tHD; STA | Hold time (repeated) START condition. After this period, the first clock pulse is generated in standard mode | 4          | —   | —    | μs   | —         |
| tHD; STA | Hold time (repeated) START condition. After this period, the first clock pulse is generated in fast mode     | 0.6        | —   | —    | μs   | —         |
| tLOW     | LOW period of the SCL clock in standard mode                                                                 | 4.7        | —   | —    | μs   | —         |
| tLOW     | LOW period of the SCL clock in fast mode                                                                     | 1.25       | —   | —    | μs   | —         |
| tHIGH    | HIGH period of the SCL clock in standard mode                                                                | 4          | —   | —    | μs   | —         |
| tHIGH    | HIGH period of the SCL clock in fast mode                                                                    | 0.6        | —   | —    | μs   | —         |
| tSU; STA | Set-up time for a repeated START condition in standard mode                                                  | 4.7        | —   | —    | μs   | —         |
| tSU; STA | Set-up time for a repeated START condition in fast mode                                                      | 0.6        | —   | —    | μs   | —         |
| tHD; DAT | Data hold time for I2C bus devices in standard mode <sup>[1][2]</sup>                                        | 0          | —   | 3.45 | μs   | —         |
| tHD; DAT | Data hold time for I2C bus devices in fast mode <sup>[1][3]</sup>                                            | 0          | —   | 0.9  | μs   | —         |
| tSU; DAT | Data set-up time in standard mode <sup>[4]</sup>                                                             | 250        | —   | —    | ns   | —         |
| tSU; DAT | Data set-up time in fast mode <sup>[2][5]</sup>                                                              | 100A       | —   | —    | ns   | —         |
| tr       | Rise time of SDA and SCL signals in standard mode <sup>[6]</sup>                                             | —          | —   | 1000 | ns   | —         |
| tr       | Rise time of SDA and SCL signals in fast mode <sup>[6]</sup>                                                 | 20 + 0.1Cb | —   | 300  | ns   | —         |
| tf       | Fall time of SDA and SCL signals in standard mode <sup>[5]</sup>                                             | —          | —   | 300  | ns   | —         |

Table continues on the next page...

Table 41. LPI2C timing...continued

| Symbol                | Description                                                                        | Min       | Typ | Max | Unit | Condition |
|-----------------------|------------------------------------------------------------------------------------|-----------|-----|-----|------|-----------|
| t <sub>f</sub>        | Fall time of SDA and SCL signal s in fast mode <sup>[5]</sup>                      | 20 +0.1Cb | —   | 300 | ns   | —         |
| t <sub>SU</sub> ; STO | Set-up time for STOP condition in standard mode                                    | 4         | —   | —   | μs   | —         |
| t <sub>SU</sub> ; STO | Set-up time for STOP condition in fast mode                                        | 0.6       | —   | —   | μs   | —         |
| t <sub>BUF</sub>      | Bus free time between STOP and START condition in standard mode                    | 4.7       | —   | —   | μs   | —         |
| t <sub>BUF</sub>      | Bus free time between STOP and START condition in fast mode                        | 1.3       | —   | —   | μs   | —         |
| t <sub>SP</sub>       | Pulse width of spikes that must be suppressed by the input filter in standard mode | N/A       | —   | N/A | ns   | —         |
| t <sub>SP</sub>       | Pulse width of spikes that must be suppressed by the input filter in fast mode     | 0         | —   | 50  | ns   | —         |

- [1] The controller mode I2C deasserts ACK of an address byte simultaneously with the falling edge of SCL. If no targets acknowledge this address byte, then a negative hold time can result, depending on the edge rates of the SDA and SCL lines.
- [2] The maximum t<sub>HD</sub>; DAT must be met only if the device does not stretch the LOW period (t<sub>LOW</sub>) of the SCL signal
- [3] Input signal Slew = 10 ns and Output Load = 50 pF
- [4] Set-up time in slave-transmitter mode is 1 IPBus clock period, if the TX FIFO is empty.
- [5] A Fast mode I2C bus device can be used in a Standard mode I2C bus system, but the requirement t<sub>SU</sub>; DAT ≥ 250 ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, then it must output the next data bit to the SDA line t<sub>rmx</sub> + t<sub>SU</sub>; DAT = 1000 + 250 = 1250 ns (according to the Standard mode I2C bus specification) before the SCL line is released.
- [6] Cb = total capacitance of the one bus line in pF.

#### 4.6.4 I2C 1 Mbps timing

Table 42. I2C 1 Mbps timing

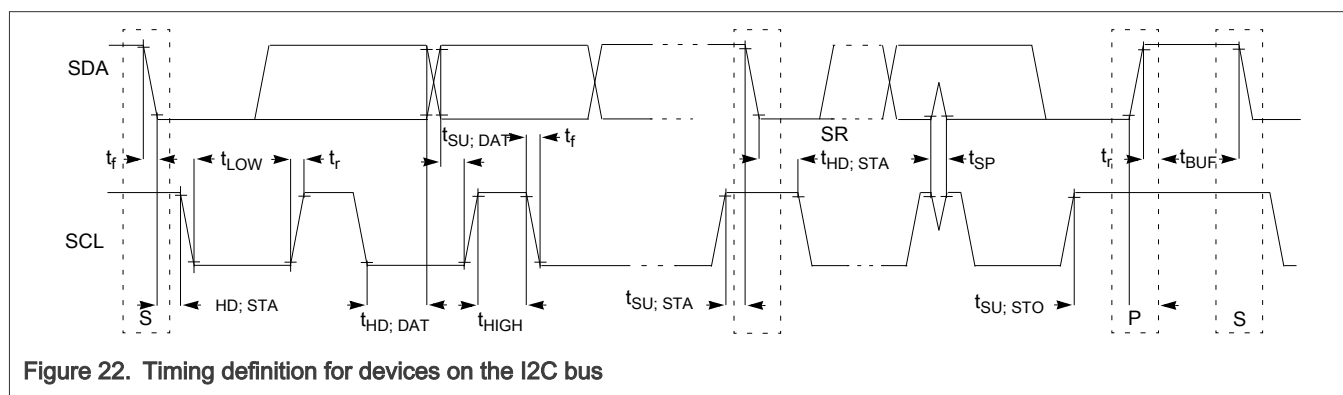
| Symbol                | Description                                                                                  | Min  | Typ | Max | Unit | Condition |
|-----------------------|----------------------------------------------------------------------------------------------|------|-----|-----|------|-----------|
| f <sub>SCL</sub>      | SCL Clock Frequency                                                                          | 0    | —   | 1   | MHz  | —         |
| t <sub>HD</sub> ; STA | Hold time (repeated) START condition. After this period, the first clock pulse is generated. | 0.26 | —   | —   | μs   | —         |
| t <sub>LOW</sub>      | LOW period of the SCL clock                                                                  | 0.5  | —   | —   | μs   | —         |
| t <sub>HIGH</sub>     | HIGH period of the SCL clock                                                                 | 0.26 | —   | —   | μs   | —         |
| t <sub>SU</sub> ; STA | Set-up time for a repeated START condition                                                   | 0.26 | —   | —   | μs   | —         |
| t <sub>HD</sub> ; DAT | Data hold time for I2C bus devices                                                           | 0    | —   | —   | μs   | —         |
| t <sub>SU</sub> ; DAT | Data set-up time                                                                             | 50   | —   | —   | ns   | —         |

Table continues on the next page...

Table 42. I2C 1 Mbps timing...continued

| Symbol        | Description                                                       | Min       | Typ | Max | Unit | Condition |
|---------------|-------------------------------------------------------------------|-----------|-----|-----|------|-----------|
| $t_r$         | Rise time of SDA and SCL signals <sup>[1]</sup>                   | 20 +0.1Cb | —   | 120 | ns   | —         |
| $t_f$         | Fall time of SDA and SCL signals <sup>[1]</sup>                   | 20 +0.1Cb | —   | 120 | ns   | —         |
| $t_{SU; STO}$ | Set-up time for STOP condition                                    | 0.26      | —   | —   | μs   | —         |
| $t_{BUF}$     | Bus free time between STOP and START condition                    | 0.5       | —   | —   | μs   | —         |
| $t_{SP}$      | Pulse width of spikes that must be suppressed by the input filter | 0         | —   | 50  | ns   | —         |

[1] Cb = total capacitance of the one bus line in pF for maximum value



#### 4.6.5 I2C HS mode timing

Table 43. I2C HS mode timing

| Symbol        | Description                                                                                  | Min       | Typ | Max | Unit | Condition |
|---------------|----------------------------------------------------------------------------------------------|-----------|-----|-----|------|-----------|
| fSCL          | SCL Clock Frequency                                                                          | 0         | —   | 3.4 | MHz  | —         |
| $t_{HD; STA}$ | Hold time (repeated) START condition. After this period, the first clock pulse is generated. | 0.26      | —   | —   | μs   | —         |
| $t_{LOW}$     | LOW period of the SCL clock                                                                  | 0.5       | —   | —   | μs   | —         |
| $t_{HIGH}$    | High period of the SCL clock                                                                 | 0.26      | —   | —   | μs   | —         |
| $t_{SU; STA}$ | Set-up time for a repeated START condition                                                   | 0.26      | —   | —   | μs   | —         |
| $t_{HD; DAT}$ | Data hold time for I2C bus devices <sup>[1]</sup>                                            | 0         | —   | —   | μs   | —         |
| $t_{SU; DAT}$ | Data setup time                                                                              | 34        | —   | —   | ns   | —         |
| $t_r$         | Rise time of SDA and SCL signals <sup>[2]</sup>                                              | 20 +0.1Cb | —   | 120 | ns   | —         |

Table continues on the next page...

Table 43. I2C HS mode timing...continued

| Symbol               | Description                                                       | Min          | Typ | Max | Unit | Condition |
|----------------------|-------------------------------------------------------------------|--------------|-----|-----|------|-----------|
| t <sub>f</sub>       | Fall time of SDA and SCL signals <sup>[2]</sup>                   | 20<br>+0.1Cb | —   | 120 | ns   | —         |
| t <sub>SU; STO</sub> | Setup time for STOP condition                                     | 0.26         | —   | —   | μs   | —         |
| t <sub>BUF</sub>     | Bus free time between STOP and START condition                    | 0.5          | —   | —   | μs   | —         |
| t <sub>SP</sub>      | Pulse width of spikes that must be suppressed by the input filter | 0            | —   | 50  | ns   | —         |

[1] A device must internally provide a data hold time to bridge the undefined part between VIH and VIL of the falling edge of the SCLH signal. An input circuit with a threshold as low as possible for the falling edge of the SCLH signal minimizes this hold time in maximum value.

[2] Cb = total capacitance of the one bus line in pF. The typical Cb value is 20 pF

#### 4.6.6 I3C Push-Pull Timing Parameters for SDR Mode

I3C interface is not supported on GPIO-Standard-plus pad type for 5 V operation. Measurements are with maximum output load of 30 pF, input transition of 1 ns. GPIO-Standard-plus pad configured with DSE = 1'b1 and GPIO-Medium pad with DSE = 1'b1 and SRE = 1'b1. SCL, SDA and PUR combination should be of same pad type. For e.g. I3C medium Data Pads to be used with I3C Medium Clock and PUR Pads Only. I3C Standard plus Data Pads to be used with I3C standard plus Clock and PUR pads only.

Table 44. I3C Push-Pull Timing Parameters for SDR Mode

| Symbol | Description                                                   | Min  | Typ  | Max                                       | Measurement Timing   | Unit | Condition                                           |
|--------|---------------------------------------------------------------|------|------|-------------------------------------------|----------------------|------|-----------------------------------------------------|
| fSCL   | SCL Clock Frequency                                           | 0.01 | 12.5 | 12.9                                      | —                    | MHz  | F <sub>SCL</sub> = 1 / (tDIG_L + tDIG_H)            |
| tDIG_L | SCL Clock Low Period <sup>[1]</sup>                           | 32   | —    | —                                         | —                    | ns   | —                                                   |
| tDIG_H | SCL Clock High Period <sup>[2]</sup>                          | 32   | —    | —                                         | —                    | ns   | —                                                   |
| tSCO   | Clock in to Data Out for Target <sup>[3][4]</sup>             | —    | —    | 12                                        | 21.51 <sup>[5]</sup> | ns   | in MD mode                                          |
|        |                                                               |      |      |                                           | 18.09 <sup>[5]</sup> | ns   | in OD mode                                          |
| tCR    | SCL Clock Rise Time <sup>[6]</sup>                            | —    | —    | 150e06<br>* 1 /<br>fSCL<br>(capped at 60) | —                    | ns   | —                                                   |
| tCF    | SCL Clock Fall Time                                           | —    | —    | —                                         | —                    | —    | —                                                   |
| tHD_PP | SDA Signal Data Hold in Push-Pull Mode, Target <sup>[7]</sup> | 0    | —    | —                                         | —                    | —    | Applicable for target and controller loopback modes |
| tSU_PP | SDA Signal Data Setup in Push-Pull Mode                       | 3    | —    | —                                         | —                    | ns   | Applicable for target and controller loopback modes |

[1] As both edges are used, the hold time needs to be satisfied for the respective edges; i.e., tCF + 3 for falling edge clocks, and tCR + 3 for rising edge clocks.

[2] tDIG\_L and tDIG\_H are the clock Low and High periods as seen at the receiver end of the I3C Bus using VIL and VIH (see Figure 30)

[3] Devices with more than 12ns of tSCO delay shall set the limitation bit in the BCR, and shall support the GETMXDS CCC to allow the Controller to read this value and adjust computations accordingly. For purposes of system design and test conformance, this parameter should be considered together with pad delay, bus capacitance, propagation delay, and clock triggering points.

- [4] Pad delay based on 90  $\Omega$  / 4 mA driver and 50 pF load. Note that Controller may be a Target in a multi-Controller system, and thus shall also adhere to this requirement
- [5] Guaranteed by design
- [6] The clock maximum rise/fall time is capped at 60 ns. For lower frequency rise and fall the maximum value is limited at 60 ns, and is not dependent upon the clock frequency.
- [7]  $t_{HD\_PP}$  is a Hold time parameter for Push-Pull Mode that has a different value for Controller mode vs. Target mode. In SDR Mode the Hold time parameter is referred to as  $t_{HD\_SDR}$ .

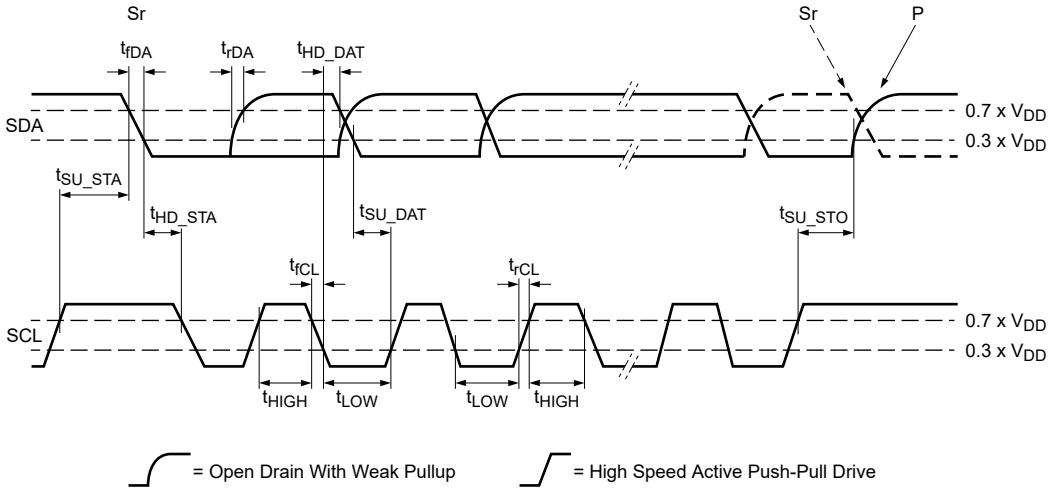


Figure 23. Legacy mode timing

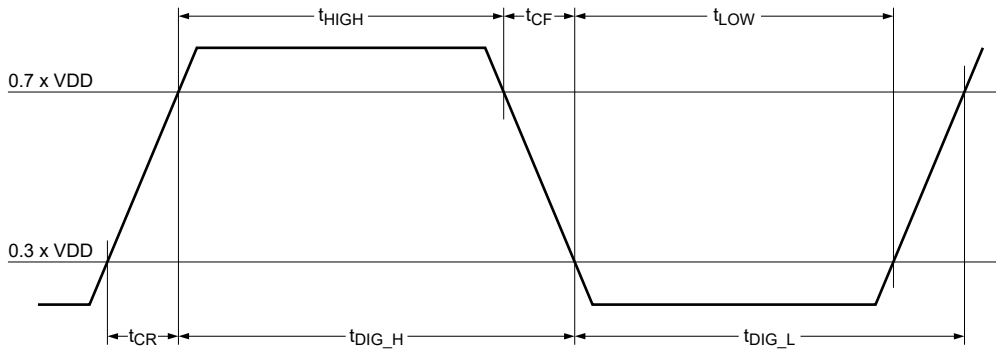


Figure 24.  $t_{DIG\_H}$  and  $t_{DIG\_L}$

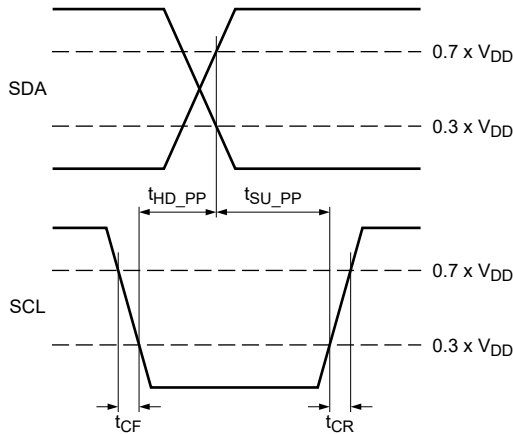


Figure 25. Controller out timing

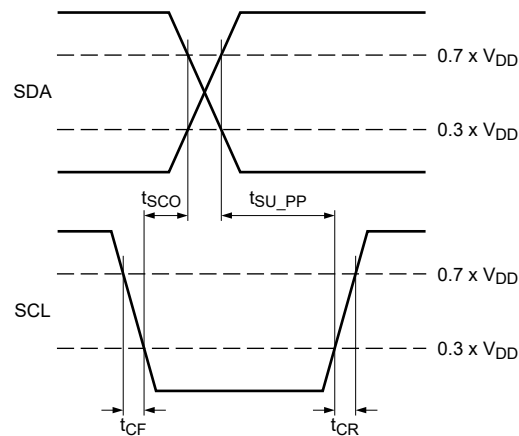


Figure 26. Target out timing

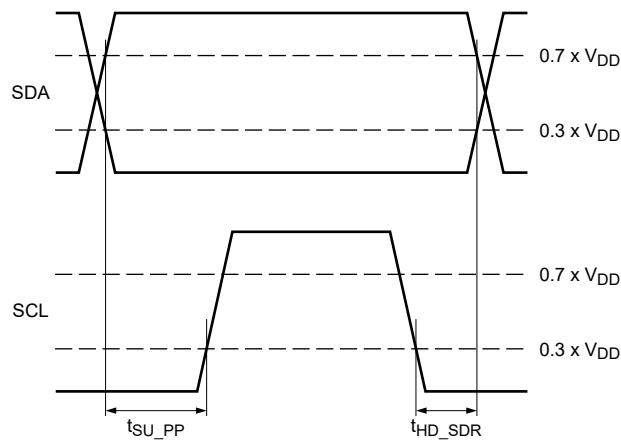


Figure 27. Controller SDR timing

#### 4.6.7 USB Full-speed device electrical specifications

This section describes the USB0 port Full Speed/Low Speed transceiver. The USB0 (FS/LS Transceiver) meets the electrical compliance requirements defined in the Universal Serial Bus Revision 2.0 Specification with the amendments below.

- USB ENGINEERING CHANGE NOTICE
  - Title: 5 V Short Circuit Withstand Requirement Change
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- Errata for USB Revision 2.0 April 27, 2000 as of 12/7/2000
- USB ENGINEERING CHANGE NOTICE
  - Title: Pull-up/Pull-down resistors
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- USB ENGINEERING CHANGE NOTICE
  - Title: Suspend Current Limit Changes
  - Applies to: Universal Serial Bus Specification, Revision 2.0

This SoC does not have a dedicated pin to monitor the state of the USB VBUS signal. Please refer to the USBFS chapter in the Reference Manual for methods which can be used for VBUS Session\_Valid detection with either a P4-12/ALT1 pin using an external resistive divider.

#### 4.6.8 Flexible I/O controller (FLEXIO) electrical specifications

The following table shows FlexIO timing specifications.

Table 45. Flexible I/O controller (FLEXIO) electrical specifications

| Symbol | Description                                                                                                            | Min | Typ | Max | Unit | Condition |
|--------|------------------------------------------------------------------------------------------------------------------------|-----|-----|-----|------|-----------|
| tODS   | Output delay skew between any two FlexIO_Dx pins configured as outputs that toggle on same internal clock cycle        | 0   | —   | 8   | ns   | —         |
| tIDS   | Input delay skew between any two FlexIO_Dx pins configured as inputs that are sampled on the same internal clock cycle | 0   | —   | 8   | ns   | —         |

#### 4.6.9 FlexCAN

See [General switching specifications](#).

### 4.7 Human Machine Interface (HMI) modules

#### 4.7.1 General Purpose Input/Output (GPIO)

See [General switching specifications](#).

#### 4.7.2 Segment LCD electrical specification

Table 46. Segment LCD electrical specification

| Symbol  | Description                                        | Min  | Typ | Max  | Unit | Condition   |
|---------|----------------------------------------------------|------|-----|------|------|-------------|
| TJ      | Operation temperature                              | -40  | 27  | 115  | °C   | —           |
| Vvdd_3v | Analog supply voltage                              | 2.7  | 3   | 3.3  | V    | —           |
| Vvdd_lv | Digital supply voltage                             | 0.81 | 1.1 | 1.21 | V    | —           |
| Cbypass | Bypass capacitor for Vlcd_vll2_3v and Vlcd_vll1_3v | 80   | 100 | 120  | nF   | —           |
| Rser    | Resistance in series with bypass capacitor         | —    | —   | 100  | Ω    | —           |
| Cglass  | LCD glass capacitor                                | —    | —   | 8    | nF   | —           |
| Fclk    | Clock signal                                       | —    | 16  | —    | kHz  | —           |
| Ivdd_3v | Current consumption at room temp                   | —    | 6   | —    | μA   | normal mode |
| Ivdd_3v | Current consumption at room temp                   | —    | 1   | —    | μA   | S&H mode    |

Table continues on the next page...

Table 46. Segment LCD electrical specification...continued

| Symbol           | Description                                                    | Min | Typ   | Max | Unit    | Condition |
|------------------|----------------------------------------------------------------|-----|-------|-----|---------|-----------|
| Ishutdown_3v     | Leakage current for vdd_3v pin                                 | —   | 1     | —   | nA      | Disabled  |
| Vlcd_vll3_3v     | LCD bias voltage level 3                                       | —   | 1     | —   | Vvdd_3v | —         |
| Vlcd_vll2_3v     | LCD bias voltage level 2                                       | —   | 0.67  | —   | Vvdd_3v | —         |
| Vlcd_vll1_3v     | LCD bias voltage level 1                                       | —   | 0.34  | —   | Vvdd_3v | —         |
| Vlcd_vll0_3v     | LCD bias voltage level 0                                       | —   | 0     | —   | Vvdd_3v | —         |
| Vlcd_error       | LCD bias voltage error                                         | -50 | 0     | 50  | mV      | —         |
| Vlcd_config_step | LCD bias voltage config step for Vlcd_vll2_3v and Vlcd_vll1_3v | —   | 1.67% | —   | Vvdd_3v | —         |
| Tstart           | Startup time                                                   | —   | —     | 10  | ms      | —         |
| Fframe           | LCD frame frequency                                            | 28  | 30    | 58  | Hz      | —         |

## 5 Package dimensions

### 5.1 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to [nxp.com](https://www.nxp.com) and perform a keyword search for the drawing's document number:

| If you want the drawing for this package | Then use this document number |
|------------------------------------------|-------------------------------|
| WFBGA169                                 | 98ASA02230D                   |
| LQFP144                                  | 98ASS23177W                   |
| LQFP100                                  | 98ASS23308W                   |
| LQFP64                                   | 98ASS23234W                   |

## 6 Pinout

### 6.1 MCX A175, A176, A185, A186, A255, A256, A265, and A266 Signal Multiplexing and Pin Assignments

The signal multiplexing and pin assignments are provided in an Excel file attached to this document:

1. Click the paperclip symbol on the left side of the PDF window.
2. Double-click on the Excel file to open it.
3. Select the "Pinout" tab.

The Port Control Module is responsible for selecting which ALT functionality is available on each pin.

However, the pinout table is as given below

Table 47. Pinmux

| Pin Name | MCXA26xA25xA<br>18xA17x<br>LQFP144 | MCXA26xA25xA<br>18xA17x<br>WFBGA169 | MCXA26xA25xA<br>18xA17x<br>LQFP100 | MCXA26xA25xA<br>18xA17x<br>LQFP64 | Pinmux Assignment                                                                                                                                                                                                                                                                | Pad Settings                                                               | Alternate Functions                                             |
|----------|------------------------------------|-------------------------------------|------------------------------------|-----------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------|-----------------------------------------------------------------|
| P1_8     | 1                                  | B2                                  | 1                                  | 2                                 | <b>ALT0</b> - P1_8<br><b>ALT1</b><br>- FREQME_CLK_IN0<br><b>ALT2</b> - LPUART1_RXD<br><b>ALT3</b> - LPI2C2_SDA<br><b>ALT4</b> - CT_INP8<br><b>ALT5</b> - CT0_MAT2<br><b>ALT6</b> - FLEXIO0_D16<br><b>ALT7</b> - SmartDMA_PIO4<br><b>ALT9</b> - LCD_P6<br><b>ALT10</b> - I3C0_SDA | <b>IO Supply</b> - VDD<br><b>Pad type</b> - HD+I3C<br><b>Default</b> - DIS | <b>ANALOG</b> - LCD_P6<br><b>VDD SYS</b> - WUU0_IN10            |
| P1_9     | 2                                  | B1                                  | 2                                  | 3                                 | <b>ALT0</b> - P1_9<br><b>ALT1</b><br>- FREQME_CLK_IN1<br><b>ALT2</b> - LPUART1_TXD<br><b>ALT3</b> - LPI2C2_SCL<br><b>ALT4</b> - CT_INP9<br><b>ALT5</b> - CT0_MAT3<br><b>ALT6</b> - FLEXIO0_D17<br><b>ALT7</b> - SmartDMA_PIO5<br><b>ALT9</b> - LCD_P7<br><b>ALT10</b> - I3C0_SCL | <b>IO Supply</b> - VDD<br><b>Pad type</b> - HD<br><b>Default</b> - DIS     | <b>ANALOG</b> - LCD_P7                                          |
| P1_10    | 3                                  | C2                                  | 3                                  | 4                                 | <b>ALT0</b> - P1_10<br><b>ALT2</b> - LPUART1_RTS_B<br><b>ALT3</b> - LPI2C2_SDAS<br><b>ALT4</b> - CT2_MAT0<br><b>ALT6</b> - FLEXIO0_D18<br><b>ALT7</b> - SmartDMA_PIO6<br><b>ALT8</b> - LPUART5_TXD<br><b>ALT9</b> - LCD_P8<br><b>ALT11</b> - CAN0_TXD                            | <b>IO Supply</b> - VDD<br><b>Pad type</b> - SLOW<br><b>Default</b> - DIS   | <b>ANALOG</b> -<br>ADC1_A8/LCD_P8                               |
| P1_11    | 4                                  | C1                                  | 4                                  | 5                                 | <b>ALT0</b> - P1_11<br><b>ALT1</b> - TRIG_OUT2<br><b>ALT2</b> - LPUART1_CTS_B<br><b>ALT3</b> - LPI2C2_SCLS<br><b>ALT4</b> - CT2_MAT1                                                                                                                                             | <b>IO Supply</b> - VDD<br><b>Pad type</b> - SLOW<br><b>Default</b> - DIS   | <b>ANALOG</b> -<br>ADC1_A9/LCD_P9<br><b>VDD SYS</b> - WUU0_IN11 |

Table continues on the next page...

Table 47. Pinmux...continued

| Pin Name | MCXA26xA25xA<br>18xA17x<br>LQFP144 | MCXA26xA25xA<br>18xA17x<br>WFBGA169 | MCXA26xA25xA<br>18xA17x<br>LQFP100 | MCXA26xA25xA<br>18xA17x<br>LQFP64 | Pinmux Assignment                                                                                                                                                                                                                                                               | Pad Settings                                                             | Alternate Functions                                               |
|----------|------------------------------------|-------------------------------------|------------------------------------|-----------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------|-------------------------------------------------------------------|
|          |                                    |                                     |                                    |                                   | <b>ALT6</b> - FLEXIO0_D19<br><b>ALT7</b> - SmartDMA_PIO7<br><b>ALT8</b> - LPUART5_RXD<br><b>ALT9</b> - LCD_P9<br><b>ALT10</b> - I3C0_PUR<br><b>ALT11</b> - CAN0_RXD                                                                                                             |                                                                          |                                                                   |
| P1_12    | 5                                  | D4                                  | 5                                  | 6                                 | <b>ALT0</b> - P1_12<br><b>ALT2</b> - LPI2C1_SDA<br><b>ALT3</b> - LPUART2_RXD<br><b>ALT4</b> - CT2_MAT2<br><b>ALT6</b> - FLEXIO0_D20<br><b>ALT7</b> - SmartDMA_PIO8<br><b>ALT8</b> - LPUART5_CTS_B<br><b>ALT9</b> - LCD_P10<br><b>ALT11</b> - CAN1_RXD                           | <b>IO Supply</b> - VDD<br><b>Pad type</b> - SLOW<br><b>Default</b> - DIS | <b>ANALOG</b> -<br>ADC1_A10/LCD_P10<br><b>VDD SYS</b> - WUU0_IN12 |
| P1_13    | 6                                  | D1                                  | 6                                  | 7                                 | <b>ALT0</b> - P1_13<br><b>ALT1</b> - TRIG_IN3<br><b>ALT2</b> - LPI2C1_SCL<br><b>ALT3</b> - LPUART2_TXD<br><b>ALT4</b> - CT2_MAT3<br><b>ALT6</b> - FLEXIO0_D21<br><b>ALT7</b> - SmartDMA_PIO9<br><b>ALT8</b> - LPUART5_RTS_B<br><b>ALT9</b> - LCD_P11<br><b>ALT11</b> - CAN1_TXD | <b>IO Supply</b> - VDD<br><b>Pad type</b> - SLOW<br><b>Default</b> - DIS | <b>ANALOG</b> -<br>ADC1_A11/LCD_P11                               |
| P1_14    | 7                                  | E2                                  | 7                                  | --                                | <b>ALT0</b> - P1_14<br><b>ALT2</b> - LPI2C1_SCLS<br><b>ALT3</b> - LPUART2_RTS_B<br><b>ALT5</b> - CT3_MAT0<br><b>ALT6</b> - FLEXIO0_D22<br><b>ALT7</b> - SmartDMA_PIO10<br><b>ALT9</b> - LCD_P12                                                                                 | <b>IO Supply</b> - VDD<br><b>Pad type</b> - SLOW<br><b>Default</b> - DIS | <b>ANALOG</b> -<br>ADC1_A12/LCD_P12                               |
| P1_15    | 8                                  | E1                                  | 8                                  | --                                | <b>ALT0</b> - P1_15<br><b>ALT2</b> - LPI2C1_SDAS                                                                                                                                                                                                                                | <b>IO Supply</b> - VDD<br><b>Pad type</b> - SLOW                         | <b>ANALOG</b> -<br>ADC1_A13/LCD_P13<br><b>VDD SYS</b> - WUU0_IN13 |

Table continues on the next page...

Table 47. Pinmux...continued

| Pin Name | MCXA26xA25xA<br>18xA17x<br>LQFP144 | MCXA26xA25xA<br>18xA17x<br>WFBGA169 | MCXA26xA25xA<br>18xA17x<br>LQFP100 | MCXA26xA25xA<br>18xA17x<br>LQFP64 | Pinmux Assignment                                                                                                                                                                                          | Pad Settings                                                             | Alternate Functions                                               |
|----------|------------------------------------|-------------------------------------|------------------------------------|-----------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------|-------------------------------------------------------------------|
|          |                                    |                                     |                                    |                                   | <b>ALT3</b> - LPUART2_CTS_B<br><b>ALT5</b> - CT3_MAT1<br><b>ALT6</b> - FLEXIO0_D23<br><b>ALT7</b><br>- SmartDMA_PIO11<br><b>ALT9</b> - LCD_P13                                                             | <b>Default</b> - DIS                                                     |                                                                   |
| P1_16    | 9                                  | D2                                  | --                                 | --                                | <b>ALT0</b> - P1_16<br><b>ALT4</b> - CT_INP12<br><b>ALT6</b> - FLEXIO0_D24<br><b>ALT7</b><br>- SmartDMA_PIO12<br><b>ALT8</b> - LPUART5_RXD<br><b>ALT9</b> - LCD_P14<br><b>ALT11</b> - CAN1_RXD             | <b>IO Supply</b> - VDD<br><b>Pad type</b> - SLOW<br><b>Default</b> - DIS | <b>ANALOG</b> -<br>ADC1_A14/LCD_P14<br><b>VDD SYS</b> - WUU0_IN14 |
| P1_17    | 10                                 | D3                                  | --                                 | --                                | <b>ALT0</b> - P1_17<br><b>ALT4</b> - CT_INP13<br><b>ALT6</b> - FLEXIO0_D25<br><b>ALT7</b><br>- SmartDMA_PIO13<br><b>ALT8</b> - LPUART5_TXD<br><b>ALT9</b> - LCD_P15<br><b>ALT11</b> - CAN1_TXD             | <b>IO Supply</b> - VDD<br><b>Pad type</b> - SLOW<br><b>Default</b> - DIS | <b>ANALOG</b> -<br>ADC1_A15/LCD_P15                               |
| P1_18    | 11                                 | E4                                  | --                                 | --                                | <b>ALT0</b> - P1_18<br><b>ALT1</b><br>- FREQME_CLK_IN0<br><b>ALT4</b> - CT3_MAT0<br><b>ALT6</b> - FLEXIO0_D26<br><b>ALT7</b><br>- SmartDMA_PIO14<br><b>ALT8</b> - LPUART5_RTS_B<br><b>ALT11</b> - CAN0_TXD | <b>IO Supply</b> - VDD<br><b>Pad type</b> - SLOW<br><b>Default</b> - DIS | <b>ANALOG</b> - ADC1_A16                                          |
| P1_19    | 12                                 | E3                                  | --                                 | --                                | <b>ALT0</b> - P1_19<br><b>ALT1</b><br>- FREQME_CLK_IN1<br><b>ALT4</b> - CT3_MAT1<br><b>ALT6</b> - FLEXIO0_D27                                                                                              | <b>IO Supply</b> - VDD<br><b>Pad type</b> - SLOW<br><b>Default</b> - DIS | <b>ANALOG</b> - ADC1_A17<br><b>VDD SYS</b> - WUU0_IN15            |

Table continues on the next page...

Table 47. Pinmux...continued

| Pin Name | MCXA26xA25xA<br>18xA17x<br>LQFP144 | MCXA26xA25xA<br>18xA17x<br>WFBGA169 | MCXA26xA25xA<br>18xA17x<br>LQFP100 | MCXA26xA25xA<br>18xA17x<br>LQFP64 | Pinmux Assignment                                                                                                                                            | Pad Settings                                                               | Alternate Functions      |
|----------|------------------------------------|-------------------------------------|------------------------------------|-----------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------|--------------------------|
|          |                                    |                                     |                                    |                                   | <b>ALT7</b><br>- SmartDMA_PIO15<br><b>ALT8</b> - LPUART5_CTS_B<br><b>ALT11</b> - CAN0_RXD                                                                    |                                                                            |                          |
| P1_29    | 13                                 | F2                                  | 9                                  | 8                                 | <b>ALT0</b> - P1_29<br><b>ALT1</b> - RESET_B<br><b>ALT2</b> - SPC_LPREQ                                                                                      | <b>IO Supply</b> - VDD<br><b>Pad type</b> - RST<br><b>Default</b> - ALT1   | <b>VDD SYS</b> - RESET_B |
| P1_30    | 14                                 | F1                                  | 10                                 | 9                                 | <b>ALT0</b> - P1_30<br><b>ALT1</b> - TRIG_OUT3<br><b>ALT3</b> - LPI2C0_SDA<br><b>ALT4</b> - CT_INP16<br><b>ALT6</b> - FLEXIO0_D30<br><b>ALT10</b> - I3C0_SDA | <b>IO Supply</b> - VDD<br><b>Pad type</b> - HD+I3C<br><b>Default</b> - DIS | <b>ANALOG</b> - XTAL48M  |
| P1_31    | 15                                 | G1                                  | 11                                 | 10                                | <b>ALT0</b> - P1_31<br><b>ALT1</b> - TRIG_IN4<br><b>ALT3</b> - LPI2C0_SCL<br><b>ALT4</b> - CT_INP17<br><b>ALT6</b> - FLEXIO0_D31<br><b>ALT10</b> - I3C0_SCL  | <b>IO Supply</b> - VDD<br><b>Pad type</b> - HD<br><b>Default</b> - DIS     | <b>ANALOG</b> - EXTAL48M |
| VSS      | 16                                 | C3                                  | 12                                 | 11                                |                                                                                                                                                              | <b>IO Supply</b> - VDD                                                     |                          |
| VREFL    | 17                                 | H5                                  | 12                                 | 11                                |                                                                                                                                                              | <b>IO Supply</b> - VDD                                                     |                          |
| VREFH    | 18                                 | G5                                  | 13                                 | 12                                |                                                                                                                                                              | <b>IO Supply</b> - VDD                                                     |                          |
| VDD_ANA  | 19                                 | G6                                  | 14                                 | 12                                |                                                                                                                                                              | <b>IO Supply</b> - VDD                                                     |                          |
| VDD      | 20                                 | E5                                  | 15                                 | 13                                |                                                                                                                                                              | <b>IO Supply</b> - VDD                                                     |                          |
| P4_0     | 21                                 | H1                                  | --                                 | --                                | <b>ALT0</b> - P4_0<br><b>ALT1</b> - TRIG_IN5<br><b>ALT5</b> - PWM0_A3<br><b>ALT6</b> - FLEXIO0_D8<br><b>ALT7</b><br>- SmartDMA_PIO20                         | <b>IO Supply</b> - VDD<br><b>Pad type</b> - MED<br><b>Default</b> - DIS    |                          |
| P4_1     | 22                                 | H2                                  | --                                 | --                                | <b>ALT0</b> - P4_1<br><b>ALT5</b> - PWM0_B3<br><b>ALT6</b> - FLEXIO0_D9                                                                                      | <b>IO Supply</b> - VDD<br><b>Pad type</b> - MED<br><b>Default</b> - DIS    |                          |

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Table 47. Pinmux...continued

| Pin Name | MCXA26xA25xA<br>18xA17x<br>LQFP144 | MCXA26xA25xA<br>18xA17x<br>WFBGA169 | MCXA26xA25xA<br>18xA17x<br>LQFP100 | MCXA26xA25xA<br>18xA17x<br>LQFP64 | Pinmux Assignment                                                                                                                                                                                                          | Pad Settings                                                            | Alternate Functions        |
|----------|------------------------------------|-------------------------------------|------------------------------------|-----------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------|----------------------------|
|          |                                    |                                     |                                    |                                   | <b>ALT7</b><br>- SmartDMA_PIO21                                                                                                                                                                                            |                                                                         |                            |
| P4_2     | 23                                 | J1                                  | 16                                 | --                                | <b>ALT0</b> - P4_2<br><b>ALT1</b> - CLKOUT<br><b>ALT2</b> - LPI2C2_SDAS<br><b>ALT3</b> - LPUART3_RXD<br><b>ALT4</b> - CT4_MAT0<br><b>ALT5</b> - PWM0_A2<br><b>ALT6</b> - FLEXIO0_D10<br><b>ALT7</b><br>- SmartDMA_PIO22    | <b>IO Supply</b> - VDD<br><b>Pad type</b> - MED<br><b>Default</b> - DIS | <b>VDD SYS</b> - WUU0_IN16 |
| P4_3     | 24                                 | J2                                  | 17                                 | --                                | <b>ALT0</b> - P4_3<br><b>ALT2</b> - LPI2C2_SCL<br><b>ALT3</b> - LPUART4_TXD<br><b>ALT4</b> - CT4_MAT1<br><b>ALT5</b> - PWM0_B2<br><b>ALT6</b> - FLEXIO0_D11<br><b>ALT7</b><br>- SmartDMA_PIO23                             | <b>IO Supply</b> - VDD<br><b>Pad type</b> - MED<br><b>Default</b> - DIS |                            |
| P4_4     | 25                                 | K1                                  | 18                                 | --                                | <b>ALT0</b> - P4_4<br><b>ALT2</b> - LPI2C2_SDA<br><b>ALT3</b> - LPUART4_RXD<br><b>ALT4</b> - CT4_MAT2<br><b>ALT5</b> - PWM0_A1<br><b>ALT6</b> - FLEXIO0_D12<br><b>ALT7</b><br>- SmartDMA_PIO24                             | <b>IO Supply</b> - VDD<br><b>Pad type</b> - MED<br><b>Default</b> - DIS | <b>VDD SYS</b> - WUU0_IN17 |
| P4_5     | 26                                 | K2                                  | 19                                 | --                                | <b>ALT0</b> - P4_5<br><b>ALT1</b> - TRIG_OUT3<br><b>ALT2</b> - LPI2C2_SCLS<br><b>ALT3</b> - LPUART3_TXD<br><b>ALT4</b> - CT4_MAT3<br><b>ALT5</b> - PWM0_B1<br><b>ALT6</b> - FLEXIO0_D13<br><b>ALT7</b><br>- SmartDMA_PIO25 | <b>IO Supply</b> - VDD<br><b>Pad type</b> - MED<br><b>Default</b> - DIS |                            |

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Table 47. Pinmux...continued

| Pin Name | MCXA26xA25xA<br>18xA17x<br>LQFP144 | MCXA26xA25xA<br>18xA17x<br>WFBGA169 | MCXA26xA25xA<br>18xA17x<br>LQFP100 | MCXA26xA25xA<br>18xA17x<br>LQFP64 | Pinmux Assignment                                                                                                                                                                                                                                      | Pad Settings                                                             | Alternate Functions                                   |
|----------|------------------------------------|-------------------------------------|------------------------------------|-----------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------|-------------------------------------------------------|
| P4_6     | 27                                 | L1                                  | 20                                 | --                                | <b>ALT0</b> - P4_6<br><b>ALT1</b> - TRIG_IN4<br><b>ALT2</b> - LPI2C2_HREQ<br><b>ALT3</b> - LPUART3_CTS_B<br><b>ALT4</b> - CT_INP6<br><b>ALT5</b> - PWM0_A0<br><b>ALT6</b> - FLEXIO0_D14<br><b>ALT7</b><br>- SmartDMA_PIO26                             | <b>IO Supply</b> - VDD<br><b>Pad type</b> - MED<br><b>Default</b> - DIS  |                                                       |
| P4_7     | 28                                 | L2                                  | 21                                 | --                                | <b>ALT0</b> - P4_7<br><b>ALT1</b> - TRIG_IN5<br><b>ALT3</b> - LPUART3_RTS_B<br><b>ALT4</b> - CT_INP7<br><b>ALT5</b> - PWM0_B0<br><b>ALT6</b> - FLEXIO0_D15<br><b>ALT7</b><br>- SmartDMA_PIO27                                                          | <b>IO Supply</b> - VDD<br><b>Pad type</b> - MED<br><b>Default</b> - DIS  |                                                       |
| NC       | 29                                 | --                                  | --                                 | --                                |                                                                                                                                                                                                                                                        |                                                                          |                                                       |
| NC       | 30                                 | --                                  | --                                 | --                                |                                                                                                                                                                                                                                                        |                                                                          |                                                       |
| NC       | 31                                 | --                                  | --                                 | --                                |                                                                                                                                                                                                                                                        |                                                                          |                                                       |
| NC       | 32                                 | --                                  | --                                 | --                                |                                                                                                                                                                                                                                                        |                                                                          |                                                       |
| P2_0     | 33                                 | M1                                  | 22                                 | 14                                | <b>ALT0</b> - P2_0<br><b>ALT1</b> - TRIG_IN6<br><b>ALT2</b> - LPUART0_RXD<br><b>ALT3</b> - LPUART4_CTS_B<br><b>ALT4</b> - CT_INP16<br><b>ALT5</b> - CT2_MAT0<br><b>ALT6</b> - FLEXIO0_D8<br><b>ALT7</b><br>- SmartDMA_PIO24<br><b>ALT11</b> - CAN1_RXD | <b>IO Supply</b> - VDD<br><b>Pad type</b> - SLOW<br><b>Default</b> - DIS | <b>ANALOG</b> - ADC0_A0<br><b>VDD SYS</b> - WUU0_IN18 |
| P2_1     | 34                                 | N1                                  | 23                                 | 15                                | <b>ALT0</b> - P2_0<br><b>ALT1</b> - TRIG_IN7<br><b>ALT2</b> - LPUART0_TXD<br><b>ALT3</b> - LPUART4_RTS_B                                                                                                                                               | <b>IO Supply</b> - VDD<br><b>Pad type</b> - SLOW<br><b>Default</b> - DIS | <b>ANALOG</b> - ADC1_A0                               |

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Table 47. Pinmux...continued

| Pin Name | MCXA26xA25xA<br>18xA17x<br>LQFP144 | MCXA26xA25xA<br>18xA17x<br>WFBGA169 | MCXA26xA25xA<br>18xA17x<br>LQFP100 | MCXA26xA25xA<br>18xA17x<br>LQFP64 | Pinmux Assignment                                                                                                                                                                                                            | Pad Settings                                                             | Alternate Functions                                                                                 |
|----------|------------------------------------|-------------------------------------|------------------------------------|-----------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------|
|          |                                    |                                     |                                    |                                   | <b>ALT4</b> - CT_INP17<br><b>ALT5</b> - CT2_MAT1<br><b>ALT6</b> - FLEXIO0_D9<br><b>ALT7</b><br>- SmartDMA_PIO25<br><b>ALT11</b> - CAN1_TXD                                                                                   |                                                                          |                                                                                                     |
| P2_2     | 35                                 | M2                                  | 24                                 | 16                                | <b>ALT0</b> - P2_2<br><b>ALT1</b> - TRIG_IN6<br><b>ALT2</b> - LPUART0_RTS_B<br><b>ALT3</b> - LPUART2_TXD<br><b>ALT4</b> - CT_INP12<br><b>ALT5</b> - CT2_MAT2<br><b>ALT6</b> - FLEXIO0_D10<br><b>ALT7</b><br>- SmartDMA_PIO26 | <b>IO Supply</b> - VDD<br><b>Pad type</b> - SLOW<br><b>Default</b> - DIS | <b>ISP</b> - UART_TXD<br><b>ANALOG</b><br>- ADC0_A4/CMP0_IN0/<br>DAC0_OUT/CMP1_INN4                 |
| P2_3     | 36                                 | N2                                  | 25                                 | 17                                | <b>ALT0</b> - P2_3<br><b>ALT1</b> - TRIG_IN7<br><b>ALT2</b> - LPUART0_CTS_B<br><b>ALT3</b> - LPUART2_RXD<br><b>ALT4</b> - CT_INP13<br><b>ALT5</b> - CT2_MAT3<br><b>ALT6</b> - FLEXIO0_D11<br><b>ALT7</b><br>- SmartDMA_PIO27 | <b>IO Supply</b> - VDD<br><b>Pad type</b> - SLOW<br><b>Default</b> - DIS | <b>ISP</b> - UART_RXD<br><b>ANALOG</b> - ADC0_A3/<br>CMP1_IN0/ADC1_A4<br><b>VDD SYS</b> - WUU0_IN19 |
| P2_4     | 37                                 | M3                                  | 26                                 | 18                                | <b>ALT0</b> - P2_4<br><b>ALT3</b> - LPUART2_CTS_B<br><b>ALT4</b> - CT_INP14<br><b>ALT5</b> - CT1_MAT0<br><b>ALT6</b> - FLEXIO0_D12<br><b>ALT7</b><br>- SmartDMA_PIO28                                                        | <b>IO Supply</b> - VDD<br><b>Pad type</b> - SLOW<br><b>Default</b> - DIS | <b>ANALOG</b> - ADC0_A1                                                                             |
| P2_5     | 38                                 | N3                                  | 27                                 | 19                                | <b>ALT0</b> - P2_5<br><b>ALT3</b> - LPUART2_RTS_B<br><b>ALT4</b> - CT_INP15<br><b>ALT5</b> - CT1_MAT1<br><b>ALT6</b> - FLEXIO0_D13                                                                                           | <b>IO Supply</b> - VDD<br><b>Pad type</b> - SLOW<br><b>Default</b> - DIS | <b>ANALOG</b> - ADC1_A1                                                                             |

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Table 47. Pinmux...continued

| Pin Name | MCXA26xA25xA<br>18xA17x<br>LQFP144 | MCXA26xA25xA<br>18xA17x<br>WFBGA169 | MCXA26xA25xA<br>18xA17x<br>LQFP100 | MCXA26xA25xA<br>18xA17x<br>LQFP64 | Pinmux Assignment                                                                                                                                                                                                           | Pad Settings                                                             | Alternate Functions                       |
|----------|------------------------------------|-------------------------------------|------------------------------------|-----------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------|-------------------------------------------|
|          |                                    |                                     |                                    |                                   | <b>ALT7</b><br>- SmartDMA_PIO29                                                                                                                                                                                             |                                                                          |                                           |
| P2_6     | 39                                 | M4                                  | 28                                 | 20                                | <b>ALT0</b> - P2_6<br><b>ALT1</b> - TRIG_OUT4<br><b>ALT2</b> - LPSP11_PCS1<br><b>ALT3</b> - LPUART4_RXD<br><b>ALT4</b> - CT_INP18<br><b>ALT5</b> - CT1_MAT2<br><b>ALT6</b> - FLEXIO0_D14<br><b>ALT7</b><br>- SmartDMA_PIO30 | <b>IO Supply</b> - VDD<br><b>Pad type</b> - SLOW<br><b>Default</b> - DIS | <b>ANALOG</b> - ADC1_A3                   |
| P2_7     | 40                                 | N4                                  | 29                                 | 21                                | <b>ALT0</b> - P2_7<br><b>ALT1</b> - TRIG_IN5<br><b>ALT3</b> - LPUART4_TXD<br><b>ALT4</b> - CT_INP19<br><b>ALT5</b> - CT1_MAT3<br><b>ALT6</b> - FLEXIO0_D15<br><b>ALT7</b><br>- SmartDMA_PIO31                               | <b>IO Supply</b> - VDD<br><b>Pad type</b> - SLOW<br><b>Default</b> - DIS | <b>ANALOG</b> - VREFI/<br>ADC1_A7/ADC0_A7 |
| P2_8     | 41                                 | L4                                  | --                                 | --                                | <b>ALT0</b> - P2_8<br><b>ALT1</b> - TRIG_OUT3<br><b>ALT4</b> - CT3_MAT0<br><b>ALT6</b> - FLEXIO0_D16                                                                                                                        | <b>IO Supply</b> - VDD<br><b>Pad type</b> - SLOW<br><b>Default</b> - DIS |                                           |
| P2_9     | 42                                 | K5                                  | --                                 | --                                | <b>ALT0</b> - P2_9<br><b>ALT1</b> - TRIG_IN4<br><b>ALT4</b> - CT3_MAT1<br><b>ALT6</b> - FLEXIO0_D17                                                                                                                         | <b>IO Supply</b> - VDD<br><b>Pad type</b> - SLOW<br><b>Default</b> - DIS |                                           |
| P2_10    | 43                                 | L5                                  | 30                                 | --                                | <b>ALT0</b> - P2_10<br><b>ALT1</b> - TRIG_OUT5<br><b>ALT3</b> - LPUART2_TXD<br><b>ALT4</b> - CT3_MAT2<br><b>ALT6</b> - FLEXIO0_D18<br><b>ALT7</b><br>- SmartDMA_PIO14                                                       | <b>IO Supply</b> - VDD<br><b>Pad type</b> - SLOW<br><b>Default</b> - DIS |                                           |
| P2_11    | 44                                 | K6                                  | 31                                 | --                                | <b>ALT0</b> - P2_11<br><b>ALT1</b> - TRIG_IN4                                                                                                                                                                               | <b>IO Supply</b> - VDD<br><b>Pad type</b> - SLOW                         |                                           |

Table continues on the next page...

Table 47. Pinmux...continued

| Pin Name | MCXA26xA25xA<br>18xA17x<br>LQFP144 | MCXA26xA25xA<br>18xA17x<br>WFBGA169 | MCXA26xA25xA<br>18xA17x<br>LQFP100 | MCXA26xA25xA<br>18xA17x<br>LQFP64 | Pinmux Assignment                                                                                                                                                                                                                                             | Pad Settings                                        | Alternate Functions                                                               |
|----------|------------------------------------|-------------------------------------|------------------------------------|-----------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------|-----------------------------------------------------------------------------------|
|          |                                    |                                     |                                    |                                   | <b>ALT3</b> - LPUART2_RXD<br><b>ALT4</b> - CT3_MAT3<br><b>ALT6</b> - FLEXIO0_D19<br><b>ALT7</b><br>- SmartDMA_PIO15                                                                                                                                           | Default - DIS                                       |                                                                                   |
| VSS      | 45                                 | C11                                 | 32                                 | --                                |                                                                                                                                                                                                                                                               | IO Supply - VDD                                     |                                                                                   |
| VDD      | 46                                 | E6                                  | 33                                 | --                                |                                                                                                                                                                                                                                                               | IO Supply - VDD                                     |                                                                                   |
| P2_12    | 47                                 | M5                                  | 34                                 | 22                                | <b>ALT0</b> - P2_12<br><b>ALT1</b><br>- USB0_VBUS_DET<br><b>ALT2</b> - LPSP11_SCK<br><b>ALT3</b> - LPUART1_RXD<br><b>ALT4</b> - CT4_MAT0<br><b>ALT5</b> - CT0_MAT0<br><b>ALT6</b> - FLEXIO0_D20<br><b>ALT7</b><br>- SmartDMA_PIO16<br><b>ALT11</b> - CAN0_RXD | IO Supply - VDD<br>Pad type - SLOW<br>Default - DIS | <b>ANALOG</b> -<br>ADC0_A5/OPAMP0_INP<br><b>VDD SYS</b> - WUU0_IN20               |
| P2_13    | 48                                 | N5                                  | 35                                 | 23                                | <b>ALT0</b> - P2_13<br><b>ALT1</b> - TRIG_IN8<br><b>ALT2</b> - LPSP11_SDO<br><b>ALT3</b> - LPUART1_TXD<br><b>ALT4</b> - CT4_MAT1<br><b>ALT5</b> - CT0_MAT1<br><b>ALT6</b> - FLEXIO0_D21<br><b>ALT7</b><br>- SmartDMA_PIO17<br><b>ALT11</b> - CAN0_TXD         | IO Supply - VDD<br>Pad type - SLOW<br>Default - DIS | <b>ANALOG</b> -<br>ADC1_A5/OPAMP0_INN                                             |
| P2_14    | 49                                 | L6                                  | --                                 | --                                | <b>ALT0</b> - P2_14<br><b>ALT4</b> - CT4_MAT2<br><b>ALT6</b> - FLEXIO0_D22                                                                                                                                                                                    | IO Supply - VDD<br>Pad type - SLOW<br>Default - DIS |                                                                                   |
| P2_15    | 50                                 | M6                                  | 36                                 | 24                                | <b>ALT0</b> - P2_15<br><b>ALT1</b> - TRIG_OUT4<br><b>ALT2</b> - LPSP11_SDI<br><b>ALT3</b> - LPUART1_RTS_B<br><b>ALT4</b> - CT4_MAT3                                                                                                                           | IO Supply - VDD<br>Pad type - SLOW<br>Default - DIS | <b>ANALOG</b><br>- OPAMP0_OUT/<br>ADC0_A2/CMP0_INP4<br><b>VDD SYS</b> - WUU0_IN21 |

Table continues on the next page...

Table 47. Pinmux...continued

| Pin Name | MCXA26xA25xA<br>18xA17x<br>LQFP144 | MCXA26xA25xA<br>18xA17x<br>WFBGA169 | MCXA26xA25xA<br>18xA17x<br>LQFP100 | MCXA26xA25xA<br>18xA17x<br>LQFP64 | Pinmux Assignment                                                                                                                                                                                                             | Pad Settings                                                             | Alternate Functions                  |
|----------|------------------------------------|-------------------------------------|------------------------------------|-----------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------|--------------------------------------|
|          |                                    |                                     |                                    |                                   | <b>ALT5</b> - CT0_MAT2<br><b>ALT6</b> - FLEXIO0_D23<br><b>ALT7</b><br>- SmartDMA_PIO18<br><b>ALT11</b> - CAN1_RXD                                                                                                             |                                                                          |                                      |
| P2_16    | 51                                 | N6                                  | 37                                 | --                                | <b>ALT0</b> - P2_16<br><b>ALT2</b> - LPSP11_SDI<br><b>ALT3</b> - LPUART1_RTS_B<br><b>ALT4</b> - CT3_MAT0<br><b>ALT5</b> - CT0_MAT2<br><b>ALT6</b> - FLEXIO0_D24<br><b>ALT7</b><br>- SmartDMA_PIO19<br><b>ALT11</b> - CAN1_TXD | <b>IO Supply</b> - VDD<br><b>Pad type</b> - SLOW<br><b>Default</b> - DIS | <b>ANALOG</b> - ADC0_A6              |
| P2_17    | 52                                 | N7                                  | 38                                 | --                                | <b>ALT0</b> - P2_17<br><b>ALT1</b> - TRIG_IN9<br><b>ALT2</b> - LPSP11_PCS0<br><b>ALT3</b> - LPUART1_CTS_B<br><b>ALT4</b> - CT3_MAT1<br><b>ALT5</b> - CT0_MAT3<br><b>ALT6</b> - FLEXIO0_D25<br><b>ALT7</b><br>- SmartDMA_PIO20 | <b>IO Supply</b> - VDD<br><b>Pad type</b> - SLOW<br><b>Default</b> - DIS | <b>ANALOG</b> - ADC1_A6              |
| P2_18    | 53                                 | K8                                  | --                                 | --                                | <b>ALT0</b> - P2_18<br><b>ALT4</b> - CT3_MAT2<br><b>ALT6</b> - FLEXIO0_D26                                                                                                                                                    | <b>IO Supply</b> - VDD<br><b>Pad type</b> - SLOW<br><b>Default</b> - DIS |                                      |
| P2_19    | 54                                 | M7                                  | 39                                 | --                                | <b>ALT0</b> - P2_19<br><b>ALT1</b> - TRIG_OUT5<br><b>ALT4</b> - CT3_MAT3<br><b>ALT6</b> - FLEXIO0_D27<br><b>ALT7</b><br>- SmartDMA_PIO21                                                                                      | <b>IO Supply</b> - VDD<br><b>Pad type</b> - SLOW<br><b>Default</b> - DIS | <b>ANALOG</b> -<br>ADC1_A2/CMP1_INP4 |
| P2_20    | 55                                 | N8                                  | 40                                 | --                                | <b>ALT0</b> - P2_20<br><b>ALT1</b> - TRIG_IN8<br><b>ALT2</b> - LPSP11_PCS2<br><b>ALT4</b> - CT2_MAT0                                                                                                                          | <b>IO Supply</b> - VDD<br><b>Pad type</b> - SLOW<br><b>Default</b> - DIS |                                      |

Table continues on the next page...

Table 47. Pinmux...continued

| Pin Name | MCXA26xA25xA<br>18xA17x<br>LQFP144 | MCXA26xA25xA<br>18xA17x<br>WFBGA169 | MCXA26xA25xA<br>18xA17x<br>LQFP100 | MCXA26xA25xA<br>18xA17x<br>LQFP64 | Pinmux Assignment                                                                                                                                                    | Pad Settings                                                             | Alternate Functions                                   |
|----------|------------------------------------|-------------------------------------|------------------------------------|-----------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------|-------------------------------------------------------|
|          |                                    |                                     |                                    |                                   | <b>ALT6</b> - FLEXIO0_D28<br><b>ALT7</b><br>- SmartDMA_PIO22                                                                                                         |                                                                          |                                                       |
| P2_21    | 56                                 | M8                                  | 41                                 | --                                | <b>ALT0</b> - P2_21<br><b>ALT1</b> - TRIG_IN9<br><b>ALT2</b> - LPSP11_PCS3<br><b>ALT4</b> - CT2_MAT1<br><b>ALT6</b> - FLEXIO0_D29<br><b>ALT7</b><br>- SmartDMA_PIO23 | <b>IO Supply</b> - VDD<br><b>Pad type</b> - SLOW<br><b>Default</b> - DIS |                                                       |
| P2_22    | 57                                 | L8                                  | --                                 | --                                | <b>ALT0</b> - P2_22<br><b>ALT4</b> - CT2_MAT2<br><b>ALT6</b> - FLEXIO0_D30                                                                                           | <b>IO Supply</b> - VDD<br><b>Pad type</b> - SLOW<br><b>Default</b> - DIS |                                                       |
| P2_23    | 58                                 | N9                                  | 42                                 | --                                | <b>ALT0</b> - P2_23<br><b>ALT1</b> - TRIG_OUT5<br><b>ALT4</b> - CT2_MAT3<br><b>ALT6</b> - FLEXIO0_D31                                                                | <b>IO Supply</b> - VDD<br><b>Pad type</b> - SLOW<br><b>Default</b> - DIS | <b>ANALOG</b> - CMP0_INN4                             |
| P2_24    | 59                                 | M9                                  | --                                 | --                                | <b>ALT0</b> - P2_24<br><b>ALT1</b> - TRIG_OUT6<br><b>ALT4</b> - CT_INP8                                                                                              | <b>IO Supply</b> - VDD<br><b>Pad type</b> - SLOW<br><b>Default</b> - DIS |                                                       |
| P2_25    | 60                                 | K9                                  | --                                 | --                                | <b>ALT0</b> - P2_25<br><b>ALT1</b> - TRIG_OUT7<br><b>ALT4</b> - CT_INP9                                                                                              | <b>IO Supply</b> - VDD<br><b>Pad type</b> - SLOW<br><b>Default</b> - DIS |                                                       |
| P2_26    | 61                                 | L9                                  | --                                 | --                                | <b>ALT0</b> - P2_26<br><b>ALT1</b> - TRIG_IN5<br><b>ALT4</b> - CT_INP10                                                                                              | <b>IO Supply</b> - VDD<br><b>Pad type</b> - SLOW<br><b>Default</b> - DIS |                                                       |
| NC       | 62                                 | --                                  | --                                 | --                                |                                                                                                                                                                      |                                                                          |                                                       |
| VSS      | 63                                 | L3                                  | --                                 | --                                |                                                                                                                                                                      | <b>IO Supply</b> - VDD                                                   |                                                       |
| VDD      | 64                                 | E8                                  | --                                 | --                                |                                                                                                                                                                      | <b>IO Supply</b> - VDD                                                   |                                                       |
| VDD_USB  | 65                                 | N11                                 | 43                                 | 25                                |                                                                                                                                                                      | <b>IO Supply</b> - VDD_USB                                               |                                                       |
| USB0_DM  | 66                                 | N10                                 | 44                                 | 26                                |                                                                                                                                                                      | <b>IO Supply</b> - VDD_USB<br><b>Pad type</b> - ANA                      | <b>ANALOG</b> - USB0_DM<br><b>VDD SYS</b> - WUU0_IN28 |
| USB0_DP  | 67                                 | M10                                 | 45                                 | 27                                |                                                                                                                                                                      | <b>IO Supply</b> - VDD_USB                                               | <b>ANALOG</b> - USB0_DP                               |

Table continues on the next page...

Table 47. Pinmux...continued

| Pin Name | MCXA26xA25xA<br>18xA17x<br>LQFP144 | MCXA26xA25xA<br>18xA17x<br>WFBGA169 | MCXA26xA25xA<br>18xA17x<br>LQFP100 | MCXA26xA25xA<br>18xA17x<br>LQFP64 | Pinmux Assignment                                                                                                                                                                                                              | Pad Settings                                                                 | Alternate Functions                                                     |
|----------|------------------------------------|-------------------------------------|------------------------------------|-----------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------|-------------------------------------------------------------------------|
|          |                                    |                                     |                                    |                                   |                                                                                                                                                                                                                                | <b>Pad type</b> - ANA                                                        | <b>VDD SYS</b> - WUU0_IN29                                              |
| VSS      | 68                                 | L11                                 | 46                                 | 28                                |                                                                                                                                                                                                                                | <b>IO Supply</b> - VDD                                                       |                                                                         |
| VDD      | 69                                 | E9                                  | 47                                 | 29                                |                                                                                                                                                                                                                                | <b>IO Supply</b> - VDD                                                       |                                                                         |
| P3_31    | 70                                 | M12                                 | 48                                 | 30                                | <b>ALT0</b> - P3_31<br><b>ALT1</b> - TRIG_IN10<br><b>ALT2</b> - LPI2C3_SDAS<br><b>ALT3</b> - LPUART4_CTS_B<br><b>ALT4</b> - CT0_MAT3<br><b>ALT6</b> - FLEXIO0_D31<br><b>ALT7</b> - PWM1_B0<br><b>ALT10</b><br>- SmartDMA_PIO31 | <b>IO Supply</b> - VDD<br><b>Pad type</b> - SLOW+TAM<br><b>Default</b> - DIS | <b>ANALOG</b> - ADC1_A20<br><b>VDD SYS</b> -<br>LPTMR0_ALT2/<br>TAMPER0 |
| P3_30    | 71                                 | N12                                 | 49                                 | 31                                | <b>ALT0</b> - P3_30<br><b>ALT1</b> - TRIG_OUT6<br><b>ALT2</b> - LPI2C3_SCLS<br><b>ALT3</b> - LPUART4_RTS_B<br><b>ALT4</b> - CT0_MAT2<br><b>ALT6</b> - FLEXIO0_D30<br><b>ALT7</b> - PWM1_A0<br><b>ALT10</b><br>- SmartDMA_PIO30 | <b>IO Supply</b> - VDD<br><b>Pad type</b> - SLOW<br><b>Default</b> - DIS     | <b>ANALOG</b> - ADC1_A21                                                |
| P3_29    | 72                                 | N13                                 | 50                                 | 32                                | <b>ALT0</b> - P3_29<br><b>ALT1</b> - ISPMODE_N<br><b>ALT2</b> - LPI2C3_HREQ<br><b>ALT4</b> - CT_INP3<br><b>ALT5</b> - CT3_MAT3<br><b>ALT6</b> - FLEXIO0_D29<br><b>ALT10</b><br>- SmartDMA_PIO29                                | <b>IO Supply</b> - VDD<br><b>Pad type</b> - SLOW+TAM<br><b>Default</b> - DIS | <b>ANALOG</b> - ADC1_A22<br><b>VDD SYS</b> -<br>WUU0_IN27/TAMPER1       |
| P3_28    | 73                                 | M13                                 | 51                                 | 33                                | <b>ALT0</b> - P3_28<br><b>ALT1</b> - TRIG_IN11<br><b>ALT2</b> - LPI2C3_SDA<br><b>ALT3</b> - LPUART4_RXD<br><b>ALT4</b> - CT_INP12<br><b>ALT5</b> - CT3_MAT2                                                                    | <b>IO Supply</b> - VDD<br><b>Pad type</b> - SVTOL<br><b>Default</b> - DIS    | <b>VDD SYS</b> - WUU0_IN26                                              |

Table continues on the next page...

Table 47. Pinmux...continued

| Pin Name | MCXA26xA25xA<br>18xA17x<br>LQFP144 | MCXA26xA25xA<br>18xA17x<br>WFBGA169 | MCXA26xA25xA<br>18xA17x<br>LQFP100 | MCXA26xA25xA<br>18xA17x<br>LQFP64 | Pinmux Assignment                                                                                                                                                                                                                                     | Pad Settings                                                                 | Alternate Functions        |
|----------|------------------------------------|-------------------------------------|------------------------------------|-----------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------|----------------------------|
|          |                                    |                                     |                                    |                                   | <b>ALT6</b> - FLEXIO0_D28<br><b>ALT7</b> - PWM1_B3<br><b>ALT10</b><br>- SmartDMA_PIO28                                                                                                                                                                |                                                                              |                            |
| P3_27    | 74                                 | L12                                 | 52                                 | 34                                | <b>ALT0</b> - P3_27<br><b>ALT1</b> - TRIG_OUT7<br><b>ALT2</b> - LPI2C3_SCL<br><b>ALT3</b> - LPUART4_TXD<br><b>ALT4</b> - CT_INP13<br><b>ALT5</b> - CT3_MAT1<br><b>ALT6</b> - FLEXIO0_D27<br><b>ALT7</b> - PWM1_A3<br><b>ALT10</b><br>- SmartDMA_PIO27 | <b>IO Supply</b> - VDD<br><b>Pad type</b> - 5VTOL<br><b>Default</b> - DIS    | <b>VDD SYS</b> - WUU0_IN30 |
| P3_26    | 75                                 | L13                                 | --                                 | --                                | <b>ALT0</b> - P3_26<br><b>ALT1</b> - TRIG_IN10<br><b>ALT4</b> - CT_INP14<br><b>ALT6</b> - FLEXIO0_D26<br><b>ALT10</b><br>- SmartDMA_PIO26                                                                                                             | <b>IO Supply</b> - VDD<br><b>Pad type</b> - SLOW+TAM<br><b>Default</b> - DIS | <b>VDD SYS</b> - TAMPER2   |
| P3_25    | 76                                 | K12                                 | --                                 | --                                | <b>ALT0</b> - P3_25<br><b>ALT1</b> - TRIG_OUT6<br><b>ALT4</b> - CT_INP15<br><b>ALT6</b> - FLEXIO0_D25<br><b>ALT10</b><br>- SmartDMA_PIO25                                                                                                             | <b>IO Supply</b> - VDD<br><b>Pad type</b> - SLOW+TAM<br><b>Default</b> - DIS | <b>VDD SYS</b> - TAMPER3   |
| P3_24    | 77                                 | K13                                 | --                                 | --                                | <b>ALT0</b> - P3_24<br><b>ALT1</b> - TRIG_IN11<br><b>ALT4</b> - CT_INP16<br><b>ALT6</b> - FLEXIO0_D24<br><b>ALT10</b><br>- SmartDMA_PIO24                                                                                                             | <b>IO Supply</b> - VDD<br><b>Pad type</b> - SLOW<br><b>Default</b> - DIS     |                            |
| NC       | 78                                 | --                                  | --                                 | --                                |                                                                                                                                                                                                                                                       |                                                                              |                            |
| NC       | 79                                 | --                                  | --                                 | --                                |                                                                                                                                                                                                                                                       |                                                                              |                            |
| P3_23    | 80                                 | J12                                 | --                                 | --                                | <b>ALT0</b> - P3_23<br><b>ALT3</b> - LPUART1_CTS_B                                                                                                                                                                                                    | <b>IO Supply</b> - VDD<br><b>Pad type</b> - SLOW                             |                            |

Table continues on the next page...

Table 47. Pinmux...continued

| Pin Name | MCXA26xA25xA<br>18xA17x<br>LQFP144 | MCXA26xA25xA<br>18xA17x<br>WFBGA169 | MCXA26xA25xA<br>18xA17x<br>LQFP100 | MCXA26xA25xA<br>18xA17x<br>LQFP64 | Pinmux Assignment                                                                                                                                                                                                                                    | Pad Settings                                                                 | Alternate Functions                                 |
|----------|------------------------------------|-------------------------------------|------------------------------------|-----------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------|-----------------------------------------------------|
|          |                                    |                                     |                                    |                                   | <b>ALT4</b> - CT_INP11<br><b>ALT6</b> - FLEXIO0_D31<br><b>ALT7</b> - PWM1_X3<br><b>ALT10</b><br>- SmartDMA_PIO23                                                                                                                                     | <b>Default</b> - DIS                                                         |                                                     |
| P3_22    | 81                                 | J13                                 | 53                                 | --                                | <b>ALT0</b> - P3_22<br><b>ALT3</b> - LPUART1_RTS_B<br><b>ALT4</b> - CT_INP10<br><b>ALT6</b> - FLEXIO0_D30<br><b>ALT7</b> - PWM1_X2<br><b>ALT10</b><br>- SmartDMA_PIO22                                                                               | <b>IO Supply</b> - VDD<br><b>Pad type</b> - SLOW<br><b>Default</b> - DIS     |                                                     |
| P3_21    | 82                                 | H12                                 | 54                                 | --                                | <b>ALT0</b> - P3_21<br><b>ALT1</b> - TRIG_OUT1<br><b>ALT2</b> - LPI2C3_SCL<br><b>ALT3</b> - LPUART1_TXD<br><b>ALT4</b> - CT2_MAT3<br><b>ALT5</b> - PWM0_X3<br><b>ALT6</b> - FLEXIO0_D29<br><b>ALT7</b> - PWM1_B3<br><b>ALT10</b><br>- SmartDMA_PIO21 | <b>IO Supply</b> - VDD<br><b>Pad type</b> - SLOW<br><b>Default</b> - DIS     |                                                     |
| P3_20    | 83                                 | H13                                 | 55                                 | --                                | <b>ALT0</b> - P3_20<br><b>ALT1</b> - TRIG_OUT0<br><b>ALT2</b> - LPI2C3_SDA<br><b>ALT3</b> - LPUART1_RXD<br><b>ALT4</b> - CT2_MAT2<br><b>ALT5</b> - PWM0_X2<br><b>ALT6</b> - FLEXIO0_D28<br><b>ALT7</b> - PWM1_A3<br><b>ALT10</b><br>- SmartDMA_PIO20 | <b>IO Supply</b> - VDD<br><b>Pad type</b> - SLOW<br><b>Default</b> - DIS     |                                                     |
| NC       | 84                                 | --                                  | --                                 | --                                |                                                                                                                                                                                                                                                      |                                                                              |                                                     |
| P3_19    | 85                                 | J11                                 | 56                                 | --                                | <b>ALT0</b> - P3_19<br><b>ALT2</b> - LPUART4_TXD<br><b>ALT4</b> - CT2_MAT1                                                                                                                                                                           | <b>IO Supply</b> - VDD<br><b>Pad type</b> - SLOW+TAM<br><b>Default</b> - DIS | <b>ANALOG</b> - LCD_P47<br><b>VDD SYS</b> - TAMPER4 |

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Table 47. Pinmux...continued

| Pin Name | MCXA26xA25xA<br>18xA17x<br>LQFP144 | MCXA26xA25xA<br>18xA17x<br>WFBGA169 | MCXA26xA25xA<br>18xA17x<br>LQFP100 | MCXA26xA25xA<br>18xA17x<br>LQFP64 | Pinmux Assignment                                                                                                                                                                                                      | Pad Settings                                                                 | Alternate Functions                                  |
|----------|------------------------------------|-------------------------------------|------------------------------------|-----------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------|------------------------------------------------------|
|          |                                    |                                     |                                    |                                   | <b>ALT5</b> - PWM0_X1<br><b>ALT6</b> - FLEXIO0_D27<br><b>ALT7</b> - PWM1_X1<br><b>ALT9</b> - LCD_P47<br><b>ALT10</b><br>- SmartDMA_PIO19                                                                               |                                                                              |                                                      |
| P3_18    | 86                                 | J10                                 | 57                                 | --                                | <b>ALT0</b> - P3_18<br><b>ALT2</b> - LPUART4_RXD<br><b>ALT4</b> - CT2_MAT0<br><b>ALT5</b> - PWM0_X0<br><b>ALT6</b> - FLEXIO0_D26<br><b>ALT7</b> - PWM1_X0<br><b>ALT9</b> - LCD_P46<br><b>ALT10</b><br>- SmartDMA_PIO18 | <b>IO Supply</b> - VDD<br><b>Pad type</b> - SLOW+TAM<br><b>Default</b> - DIS | <b>ANALOG</b> - LCD_P46<br><b>VDD SYS</b> - TAMPERS5 |
| P3_17    | 87                                 | H11                                 | 58                                 | --                                | <b>ALT0</b> - P3_17<br><b>ALT2</b> - LPUART4_CTS_B<br><b>ALT4</b> - CT_INP9<br><b>ALT6</b> - FLEXIO0_D25<br><b>ALT7</b> - PWM1_B0<br><b>ALT9</b> - LCD_P45<br><b>ALT10</b><br>- SmartDMA_PIO17                         | <b>IO Supply</b> - VDD<br><b>Pad type</b> - SLOW<br><b>Default</b> - DIS     | <b>ANALOG</b> - LCD_P45                              |
| P3_16    | 88                                 | H10                                 | 59                                 | --                                | <b>ALT0</b> - P3_16<br><b>ALT2</b> - LPUART4_RTS_B<br><b>ALT4</b> - CT_INP8<br><b>ALT6</b> - FLEXIO0_D24<br><b>ALT7</b> - PWM1_A0<br><b>ALT9</b> - LCD_P44<br><b>ALT10</b><br>- SmartDMA_PIO16                         | <b>IO Supply</b> - VDD<br><b>Pad type</b> - SLOW<br><b>Default</b> - DIS     | <b>ANALOG</b> - LCD_P44                              |
| P3_15    | 89                                 | G13                                 | 60                                 | 35                                | <b>ALT0</b> - P3_15<br><b>ALT2</b> - LPUART2_TXD<br><b>ALT3</b> - LPUART3_RTS_B<br><b>ALT4</b> - CT_INP7<br><b>ALT5</b> - PWM0_X3                                                                                      | <b>IO Supply</b> - VDD<br><b>Pad type</b> - SLOW<br><b>Default</b> - DIS     | <b>ANALOG</b> - LCD_P43                              |

Table continues on the next page...

Table 47. Pinmux...continued

| Pin Name | MCXA26xA25xA<br>18xA17x<br>LQFP144 | MCXA26xA25xA<br>18xA17x<br>WFBGA169 | MCXA26xA25xA<br>18xA17x<br>LQFP100 | MCXA26xA25xA<br>18xA17x<br>LQFP64 | Pinmux Assignment                                                                                                                                                                                                                                     | Pad Settings                                                             | Alternate Functions                                   |
|----------|------------------------------------|-------------------------------------|------------------------------------|-----------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------|-------------------------------------------------------|
|          |                                    |                                     |                                    |                                   | <b>ALT6</b> - FLEXIO0_D23<br><b>ALT7</b> - PWM1_B1<br><b>ALT9</b> - LCD_P43<br><b>ALT10</b><br>- SmartDMA_PIO15                                                                                                                                       |                                                                          |                                                       |
| P3_14    | 90                                 | F12                                 | 61                                 | 36                                | <b>ALT0</b> - P3_14<br><b>ALT2</b> - LPUART2_RXD<br><b>ALT3</b> - LPUART3_CTS_B<br><b>ALT4</b> - CT_INP6<br><b>ALT5</b> - PWM0_X2<br><b>ALT6</b> - FLEXIO0_D22<br><b>ALT7</b> - PWM1_A1<br><b>ALT9</b> - LCD_P42<br><b>ALT10</b><br>- SmartDMA_PIO14  | <b>IO Supply</b> - VDD<br><b>Pad type</b> - SLOW<br><b>Default</b> - DIS | <b>ANALOG</b> - LCD_P42<br><b>VDD SYS</b> - WUU0_IN25 |
| P3_13    | 91                                 | F13                                 | 62                                 | 37                                | <b>ALT0</b> - P3_13<br><b>ALT2</b> - LPUART2_CTS_B<br><b>ALT3</b> - LPUART3_RXD<br><b>ALT4</b> - CT1_MAT3<br><b>ALT5</b> - PWM0_X1<br><b>ALT6</b> - FLEXIO0_D21<br><b>ALT7</b> - PWM1_B2<br><b>ALT9</b> - LCD_P41<br><b>ALT10</b><br>- SmartDMA_PIO13 | <b>IO Supply</b> - VDD<br><b>Pad type</b> - SLOW<br><b>Default</b> - DIS | <b>ANALOG</b> - LCD_P41                               |
| P3_12    | 92                                 | E12                                 | 63                                 | 38                                | <b>ALT0</b> - P3_12<br><b>ALT2</b> - LPUART2_RTS_B<br><b>ALT3</b> - LPUART3_TXD<br><b>ALT4</b> - CT1_MAT2<br><b>ALT5</b> - PWM0_X0<br><b>ALT6</b> - FLEXIO0_D20<br><b>ALT7</b> - PWM1_A2<br><b>ALT9</b> - LCD_P40<br><b>ALT10</b><br>- SmartDMA_PIO12 | <b>IO Supply</b> - VDD<br><b>Pad type</b> - SLOW<br><b>Default</b> - DIS | <b>ANALOG</b> - LCD_P40                               |
| VSS      | 93                                 | C7                                  | 64                                 | --                                |                                                                                                                                                                                                                                                       | <b>IO Supply</b> - VDD                                                   |                                                       |

Table continues on the next page...

Table 47. Pinmux...continued

| Pin Name | MCXA26xA25xA<br>18xA17x<br>LQFP144 | MCXA26xA25xA<br>18xA17x<br>WFBGA169 | MCXA26xA25xA<br>18xA17x<br>LQFP100 | MCXA26xA25xA<br>18xA17x<br>LQFP64 | Pinmux Assignment                                                                                                                                                                                                                                                                   | Pad Settings                                                            | Alternate Functions                                   |
|----------|------------------------------------|-------------------------------------|------------------------------------|-----------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------|-------------------------------------------------------|
| VDD      | 94                                 | J5                                  | 65                                 | --                                |                                                                                                                                                                                                                                                                                     | <b>IO Supply</b> - VDD                                                  |                                                       |
| P3_11    | 95                                 | E13                                 | 66                                 | 39                                | <b>ALT0</b> - P3_11<br><b>ALT1</b> - TRIG_IN6<br><b>ALT2</b> - LPSP11_PCS0<br><b>ALT3</b> - LPUART1_CTS_B<br><b>ALT4</b> - CT1_MAT1<br><b>ALT5</b> - PWM0_B2<br><b>ALT6</b> - FLEXIO0_D19<br><b>ALT8</b> - LPUART5_RXD<br><b>ALT9</b> - LCD_P39<br><b>ALT10</b><br>- SmartDMA_PIO11 | <b>IO Supply</b> - VDD<br><b>Pad type</b> - MED<br><b>Default</b> - DIS | <b>ANALOG</b> - LCD_P39<br><b>VDD SYS</b> - WUU0_IN24 |
| P3_10    | 96                                 | D13                                 | 67                                 | 40                                | <b>ALT0</b> - P3_10<br><b>ALT1</b> - TRIG_IN5<br><b>ALT2</b> - LPSP11_SCK<br><b>ALT3</b> - LPUART1_RTS_B<br><b>ALT4</b> - CT1_MAT0<br><b>ALT5</b> - PWM0_A2<br><b>ALT6</b> - FLEXIO0_D18<br><b>ALT8</b> - LPUART5_TXD<br><b>ALT9</b> - LCD_P38<br><b>ALT10</b><br>- SmartDMA_PIO10  | <b>IO Supply</b> - VDD<br><b>Pad type</b> - MED<br><b>Default</b> - DIS | <b>ANALOG</b> - LCD_P38                               |
| P3_9     | 97                                 | D12                                 | 68                                 | 41                                | <b>ALT0</b> - P3_9<br><b>ALT1</b> - TRIG_IN4<br><b>ALT2</b> - LPSP11_SDI<br><b>ALT3</b> - LPUART1_TXD<br><b>ALT4</b> - CT_INP5<br><b>ALT5</b> - PWM0_B1<br><b>ALT6</b> - FLEXIO0_D17<br><b>ALT8</b> - LPUART5_RTS_B<br><b>ALT9</b> - LCD_P37<br><b>ALT10</b><br>- SmartDMA_PIO9     | <b>IO Supply</b> - VDD<br><b>Pad type</b> - MED<br><b>Default</b> - DIS | <b>ANALOG</b> - LCD_P37                               |
| P3_8     | 98                                 | C13                                 | 69                                 | 42                                | <b>ALT0</b> - P3_8<br><b>ALT1</b> - TRIG_IN3                                                                                                                                                                                                                                        | <b>IO Supply</b> - VDD<br><b>Pad type</b> - MED                         | <b>ANALOG</b> - LCD_P36<br><b>VDD SYS</b> - WUU0_IN23 |

Table continues on the next page...

Table 47. Pinmux...continued

| Pin Name | MCXA26xA25xA<br>18xA17x<br>LQFP144 | MCXA26xA25xA<br>18xA17x<br>WFBGA169 | MCXA26xA25xA<br>18xA17x<br>LQFP100 | MCXA26xA25xA<br>18xA17x<br>LQFP64 | Pinmux Assignment                                                                                                                                                                                                                                                                                                | Pad Settings                                                            | Alternate Functions     |
|----------|------------------------------------|-------------------------------------|------------------------------------|-----------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------|-------------------------|
|          |                                    |                                     |                                    |                                   | <b>ALT2</b> - LPSP11_SDO<br><b>ALT3</b> - LPUART1_RXD<br><b>ALT4</b> - CT_INP4<br><b>ALT5</b> - PWM0_A1<br><b>ALT6</b> - FLEXIO0_D16<br><b>ALT8</b> - LPUART5_CTS_B<br><b>ALT9</b> - LCD_P36<br><b>ALT10</b><br>- SmartDMA_PIO8<br><b>ALT12</b> - CLKOUT                                                         | <b>Default</b> - DIS                                                    |                         |
| P3_7     | 99                                 | C12                                 | 70                                 | 43                                | <b>ALT0</b> - P3_7<br><b>ALT1</b> - TRIG_IN2<br><b>ALT2</b> - LPSP11_PCS2<br><b>ALT3</b> - LPUART3_CTS_B<br><b>ALT4</b> - CT4_MAT3<br><b>ALT5</b> - PWM0_B3<br><b>ALT6</b> - FLEXIO0_D15<br><b>ALT7</b> - PWM1_B0<br><b>ALT9</b> - LCD_P35<br><b>ALT10</b><br>- SmartDMA_PIO7                                    | <b>IO Supply</b> - VDD<br><b>Pad type</b> - MED<br><b>Default</b> - DIS | <b>ANALOG</b> - LCD_P35 |
| P3_6     | 100                                | B13                                 | 71                                 | 44                                | <b>ALT0</b> - P3_6<br><b>ALT1</b> - CLKOUT<br><b>ALT2</b> - LPSP11_PCS3<br><b>ALT3</b> - LPUART3_RTS_B<br><b>ALT4</b> - CT4_MAT2<br><b>ALT5</b> - PWM0_A3<br><b>ALT6</b> - FLEXIO0_D14<br><b>ALT7</b> - PWM1_A0<br><b>ALT9</b> - LCD_P34<br><b>ALT10</b><br>- SmartDMA_PIO6<br><b>ALT12</b><br>- FREQME_CLK_OUT1 | <b>IO Supply</b> - VDD<br><b>Pad type</b> - MED<br><b>Default</b> - DIS | <b>ANALOG</b> - LCD_P34 |
| P3_5     | 101                                | F11                                 | --                                 | --                                | <b>ALT0</b> - P3_5<br><b>ALT4</b> - CT_INP19                                                                                                                                                                                                                                                                     | <b>IO Supply</b> - VDD<br><b>Pad type</b> - SLOW                        |                         |

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Table 47. Pinmux...continued

| Pin Name | MCXA26xA25xA<br>18xA17x<br>LQFP144 | MCXA26xA25xA<br>18xA17x<br>WFBGA169 | MCXA26xA25xA<br>18xA17x<br>LQFP100 | MCXA26xA25xA<br>18xA17x<br>LQFP64 | Pinmux Assignment                                                                                                                                                                                                                                                                  | Pad Settings                                                             | Alternate Functions     |
|----------|------------------------------------|-------------------------------------|------------------------------------|-----------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------|-------------------------|
|          |                                    |                                     |                                    |                                   | <b>ALT5</b> - PWM0_X3<br><b>ALT6</b> - FLEXIO0_D13<br><b>ALT10</b><br>- SmartDMA_PIO5                                                                                                                                                                                              | <b>Default</b> - DIS                                                     |                         |
| P3_4     | 102                                | F10                                 | --                                 | --                                | <b>ALT0</b> - P3_4<br><b>ALT4</b> - CT_INP18<br><b>ALT5</b> - PWM0_X2<br><b>ALT6</b> - FLEXIO0_D12<br><b>ALT10</b><br>- SmartDMA_PIO4                                                                                                                                              | <b>IO Supply</b> - VDD<br><b>Pad type</b> - SLOW<br><b>Default</b> - DIS |                         |
| P3_3     | 103                                | E11                                 | --                                 | --                                | <b>ALT0</b> - P3_3<br><b>ALT4</b> - CT4_MAT1<br><b>ALT5</b> - PWM0_X1<br><b>ALT6</b> - FLEXIO0_D11<br><b>ALT7</b> - PWM1_X3<br><b>ALT10</b><br>- SmartDMA_PIO3                                                                                                                     | <b>IO Supply</b> - VDD<br><b>Pad type</b> - SLOW<br><b>Default</b> - DIS |                         |
| P3_2     | 104                                | E10                                 | --                                 | --                                | <b>ALT0</b> - P3_2<br><b>ALT2</b> - LPSP11_PCS1<br><b>ALT4</b> - CT4_MAT0<br><b>ALT5</b> - PWM0_X0<br><b>ALT6</b> - FLEXIO0_D10<br><b>ALT7</b> - PWM1_X2<br><b>ALT10</b><br>- SmartDMA_PIO2                                                                                        | <b>IO Supply</b> - VDD<br><b>Pad type</b> - SLOW<br><b>Default</b> - DIS |                         |
| P3_1     | 105                                | B12                                 | 72                                 | 45                                | <b>ALT0</b> - P3_1<br><b>ALT1</b> - TRIG_IN1<br><b>ALT3</b> - LPUART3_TXD<br><b>ALT4</b> - CT_INP17<br><b>ALT5</b> - PWM0_B0<br><b>ALT6</b> - FLEXIO0_D9<br><b>ALT7</b> - PWM1_X1<br><b>ALT9</b> - LCD_P33<br><b>ALT10</b><br>- SmartDMA_PIO1<br><b>ALT12</b><br>- FREQME_CLK_OUT0 | <b>IO Supply</b> - VDD<br><b>Pad type</b> - HD<br><b>Default</b> - DIS   | <b>ANALOG</b> - LCD_P33 |

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Table 47. Pinmux...continued

| Pin Name | MCXA26xA25xA<br>18xA17x<br>LQFP144 | MCXA26xA25xA<br>18xA17x<br>WFBGA169 | MCXA26xA25xA<br>18xA17x<br>LQFP100 | MCXA26xA25xA<br>18xA17x<br>LQFP64 | Pinmux Assignment                                                                                                                                                                                                                             | Pad Settings                                                              | Alternate Functions                                   |
|----------|------------------------------------|-------------------------------------|------------------------------------|-----------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------|-------------------------------------------------------|
| P3_0     | 106                                | A13                                 | 73                                 | 46                                | <b>ALT0</b> - P3_0<br><b>ALT1</b> - TRIG_IN0<br><b>ALT3</b> - LPUART3_RXD<br><b>ALT4</b> - CT_INP16<br><b>ALT5</b> - PWM0_A0<br><b>ALT6</b> - FLEXIO0_D8<br><b>ALT7</b> - PWM1_X0<br><b>ALT9</b> - LCD_P32<br><b>ALT10</b><br>- SmartDMA_PIO0 | <b>IO Supply</b> - VDD<br><b>Pad type</b> - HD<br><b>Default</b> - DIS    | <b>ANALOG</b> - LCD_P32<br><b>VDD SYS</b> - WUU0_IN22 |
| VSS      | 107                                | D7                                  | 74                                 | 47                                |                                                                                                                                                                                                                                               | <b>IO Supply</b> - VDD                                                    |                                                       |
| VDD      | 108                                | J6                                  | 75                                 | 48                                |                                                                                                                                                                                                                                               | <b>IO Supply</b> - VDD                                                    |                                                       |
| P0_0     | 109                                | A12                                 | 76                                 | 49                                | <b>ALT0</b> - P0_0<br><b>ALT1</b> - TMS/SWDIO<br><b>ALT2</b> - LPUART0_RTS_B<br><b>ALT3</b> - LPSPi0_PCS0<br><b>ALT4</b> - CT_INP0<br><b>ALT6</b> - FLEXIO0_D0                                                                                | <b>IO Supply</b> - VDD<br><b>Pad type</b> - SLOW<br><b>Default</b> - ALT1 |                                                       |
| P0_1     | 110                                | B11                                 | 77                                 | 50                                | <b>ALT0</b> - P0_1<br><b>ALT1</b> - TCLK/SWCLK<br><b>ALT2</b> - LPUART0_CTS_B<br><b>ALT3</b> - LPSPi0_SDI<br><b>ALT4</b> - CT_INP1<br><b>ALT6</b> - FLEXIO0_D1                                                                                | <b>IO Supply</b> - VDD<br><b>Pad type</b> - SLOW<br><b>Default</b> - ALT1 |                                                       |
| P0_2     | 111                                | A11                                 | 78                                 | 51                                | <b>ALT0</b> - P0_2<br><b>ALT1</b> - TDO/SWO<br><b>ALT2</b> - LPUART0_RXD<br><b>ALT3</b> - LPSPi0_SCK<br><b>ALT4</b> - CT0_MAT0<br><b>ALT5</b> - UTICK_CAP0<br><b>ALT6</b> - FLEXIO0_D2<br><b>ALT10</b> - I3C0_PUR                             | <b>IO Supply</b> - VDD<br><b>Pad type</b> - SLOW<br><b>Default</b> - ALT1 |                                                       |
| P0_3     | 112                                | D10                                 | 79                                 | 52                                | <b>ALT0</b> - P0_3<br><b>ALT1</b> - TDI<br><b>ALT2</b> - LPUART0_TXD                                                                                                                                                                          | <b>IO Supply</b> - VDD<br><b>Pad type</b> - SLOW<br><b>Default</b> - ALT1 | <b>ANALOG</b> -<br>CMP1_IN1/ADC0_A14                  |

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Table 47. Pinmux...continued

| Pin Name | MCXA26xA25xA<br>18xA17x<br>LQFP144 | MCXA26xA25xA<br>18xA17x<br>WFBGA169 | MCXA26xA25xA<br>18xA17x<br>LQFP100 | MCXA26xA25xA<br>18xA17x<br>LQFP64 | Pinmux Assignment                                                                                                                                                                                                                              | Pad Settings                                                              | Alternate Functions                                |
|----------|------------------------------------|-------------------------------------|------------------------------------|-----------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------|----------------------------------------------------|
|          |                                    |                                     |                                    |                                   | <b>ALT3</b> - LPSPiO_SDO<br><b>ALT4</b> - CT0_MAT1<br><b>ALT5</b> - UTICK_CAP1<br><b>ALT6</b> - FLEXIO0_D3<br><b>ALT8</b> - CMP0_OUT                                                                                                           |                                                                           |                                                    |
| P0_4     | 113                                | A10                                 | --                                 | --                                | <b>ALT0</b> - P0_4<br><b>ALT4</b> - CT0_MAT2<br><b>ALT5</b> - UTICK_CAP2<br><b>ALT6</b> - FLEXIO0_D4<br><b>ALT7</b> - SmartDMA_PiO0<br><b>ALT8</b> - CMP1_OUT                                                                                  | <b>IO Supply</b> - VDD<br><b>Pad type</b> - SLOW<br><b>Default</b> - DIS  | <b>VDD SYS</b> - WUU0_IN0                          |
| P0_5     | 114                                | B9                                  | --                                 | --                                | <b>ALT0</b> - P0_5<br><b>ALT4</b> - CT0_MAT3<br><b>ALT5</b> - UTICK_CAP3<br><b>ALT6</b> - FLEXIO0_D5<br><b>ALT7</b> - SmartDMA_PiO1                                                                                                            | <b>IO Supply</b> - VDD<br><b>Pad type</b> - SLOW<br><b>Default</b> - DIS  |                                                    |
| P0_6     | 115                                | A9                                  | 80                                 | 53                                | <b>ALT0</b> - P0_6<br><b>ALT1</b> - ISPMODE_N<br><b>ALT2</b> - LPI2C0_HREQ<br><b>ALT3</b> - LPSPiO_PCS1<br><b>ALT4</b> - CT_INP2<br><b>ALT6</b> - FLEXIO0_D6<br><b>ALT7</b> - SmartDMA_PiO2<br><b>ALT8</b> - CMP1_OUT<br><b>ALT12</b> - CLKOUT | <b>IO Supply</b> - VDD<br><b>Pad type</b> - SLOW<br><b>Default</b> - ALT1 | <b>ISP</b> - ISPMODE_N<br><b>ANALOG</b> - ADC0_A15 |
| P0_7     | 116                                | D11                                 | --                                 | --                                | <b>ALT0</b> - P0_7<br><b>ALT4</b> - CT_INP3<br><b>ALT6</b> - FLEXIO0_D7<br><b>ALT7</b> - SmartDMA_PiO3                                                                                                                                         | <b>IO Supply</b> - VDD<br><b>Pad type</b> - SLOW<br><b>Default</b> - DIS  | <b>VDD SYS</b> - WUU0_IN1                          |
| NC       | 117                                | --                                  | --                                 | --                                |                                                                                                                                                                                                                                                | <b>IO Supply</b> - NC                                                     |                                                    |
| VSS      | 118                                | E7                                  | --                                 | --                                |                                                                                                                                                                                                                                                | <b>IO Supply</b> - VDD                                                    |                                                    |
| P0_12    | 119                                | C10                                 | --                                 | --                                | <b>ALT0</b> - P0_12<br><b>ALT4</b> - CT0_MAT2<br><b>ALT6</b> - FLEXIO0_D4                                                                                                                                                                      | <b>IO Supply</b> - VDD<br><b>Pad type</b> - SLOW<br><b>Default</b> - DIS  | <b>ANALOG</b> - LCD_P16                            |

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Table 47. Pinmux...continued

| Pin Name | MCXA26xA25xA<br>18xA17x<br>LQFP144 | MCXA26xA25xA<br>18xA17x<br>WFBGA169 | MCXA26xA25xA<br>18xA17x<br>LQFP100 | MCXA26xA25xA<br>18xA17x<br>LQFP64 | Pinmux Assignment                                                                                                                                                                  | Pad Settings                                          | Alternate Functions                    |
|----------|------------------------------------|-------------------------------------|------------------------------------|-----------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------|----------------------------------------|
|          |                                    |                                     |                                    |                                   | ALT9 - LCD_P16                                                                                                                                                                     |                                                       |                                        |
| P0_13    | 120                                | B10                                 | --                                 | --                                | ALT0 - P0_13<br>ALT4 - CT0_MAT3<br>ALT6 - FLEXIO0_D5<br>ALT9 - LCD_P17                                                                                                             | IO Supply - VDD<br>Pad type - SLOW<br>Default - DIS   | ANALOG - LCD_P17                       |
| P0_14    | 121                                | C9                                  | 81                                 | --                                | ALT0 - P0_14<br>ALT4 - CT_INP2<br>ALT5 - UTICK_CAP0<br>ALT6 - FLEXIO0_D6<br>ALT7 - SmartDMA_PIO4<br>ALT9 - LCD_P18                                                                 | IO Supply - VDD<br>Pad type - SLOW<br>Default - DIS   | ANALOG - LCD_P18                       |
| P0_15    | 122                                | D9                                  | 82                                 | --                                | ALT0 - P0_15<br>ALT4 - CT_INP3<br>ALT5 - UTICK_CAP1<br>ALT6 - FLEXIO0_D7<br>ALT7 - SmartDMA_PIO5<br>ALT9 - LCD_P19                                                                 | IO Supply - VDD<br>Pad type - SLOW<br>Default - DIS   | ANALOG - LCD_P19                       |
| P0_16    | 123                                | B8                                  | 83                                 | 54                                | ALT0 - P0_16<br>ALT2 - LPI2C0_SDA<br>ALT3 - LPSPi0_PCS2<br>ALT4 - CT0_MAT0<br>ALT5 - UTICK_CAP2<br>ALT6 - FLEXIO0_D0<br>ALT7 - SmartDMA_PIO6<br>ALT9 - LCD_P20<br>ALT10 - I3C0_SDA | IO Supply - VDD<br>Pad type - HD+I3C<br>Default - DIS | ANALOG - LCD_P20<br>VDD SYS - WUU0_IN2 |
| P0_17    | 124                                | A8                                  | 84                                 | 55                                | ALT0 - P0_17<br>ALT2 - LPI2C0_SCL<br>ALT3 - LPSPi0_PCS3<br>ALT4 - CT0_MAT1<br>ALT5 - UTICK_CAP3<br>ALT6 - FLEXIO0_D1<br>ALT7 - SmartDMA_PIO7<br>ALT9 - LCD_P21<br>ALT10 - I3C0_SCL | IO Supply - VDD<br>Pad type - HD<br>Default - DIS     | ANALOG - LCD_P21                       |

Table continues on the next page...

Table 47. Pinmux...continued

| Pin Name | MCXA26xA25xA<br>18xA17x<br>LQFP144 | MCXA26xA25xA<br>18xA17x<br>WFBGA169 | MCXA26xA25xA<br>18xA17x<br>LQFP100 | MCXA26xA25xA<br>18xA17x<br>LQFP64 | Pinmux Assignment                                                                                                                                                                          | Pad Settings                                                             | Alternate Functions                                              |
|----------|------------------------------------|-------------------------------------|------------------------------------|-----------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------|------------------------------------------------------------------|
| P0_18    | 125                                | A7                                  | 85                                 | --                                | <b>ALT0</b> - P0_18<br><b>ALT2</b> - LPI2C0_SCLS<br><b>ALT4</b> - CT0_MAT2<br><b>ALT6</b> - FLEXIO0_D2<br><b>ALT7</b> - SmartDMA_PIO8<br><b>ALT8</b> - CMP0_OUT<br><b>ALT9</b> - LCD_P22   | <b>IO Supply</b> - VDD<br><b>Pad type</b> - SLOW<br><b>Default</b> - DIS | <b>ANALOG</b> -<br>ADC0_A8/LCD_P22                               |
| P0_19    | 126                                | B7                                  | 86                                 | --                                | <b>ALT0</b> - P0_19<br><b>ALT2</b> - LPI2C0_SDAS<br><b>ALT4</b> - CT0_MAT3<br><b>ALT6</b> - FLEXIO0_D3<br><b>ALT7</b> - SmartDMA_PIO9<br><b>ALT8</b> - CMP1_OUT<br><b>ALT9</b> - LCD_P23   | <b>IO Supply</b> - VDD<br><b>Pad type</b> - SLOW<br><b>Default</b> - DIS | <b>ANALOG</b> -<br>ADC0_A9/LCD_P23<br><b>VDD SYS</b> - WUU0_IN3  |
| P0_20    | 127                                | A6                                  | 87                                 | --                                | <b>ALT0</b> - P0_20<br><b>ALT3</b> - LPUART0_RXD<br><b>ALT4</b> - CT_INP0<br><b>ALT6</b> - FLEXIO0_D4<br><b>ALT7</b> - SmartDMA_PIO10<br><b>ALT9</b> - LCD_P24                             | <b>IO Supply</b> - VDD<br><b>Pad type</b> - SLOW<br><b>Default</b> - DIS | <b>ANALOG</b> -<br>ADC0_A10/LCD_P24<br><b>VDD SYS</b> - WUU0_IN4 |
| P0_21    | 128                                | B6                                  | 88                                 | --                                | <b>ALT0</b> - P0_21<br><b>ALT3</b> - LPUART0_TXD<br><b>ALT4</b> - CT_INP1<br><b>ALT6</b> - FLEXIO0_D5<br><b>ALT7</b> - SmartDMA_PIO11<br><b>ALT9</b> - LCD_P25                             | <b>IO Supply</b> - VDD<br><b>Pad type</b> - SLOW<br><b>Default</b> - DIS | <b>ANALOG</b> -<br>ADC0_A11/LCD_P25                              |
| P0_22    | 129                                | C8                                  | 89                                 | --                                | <b>ALT0</b> - P0_22<br><b>ALT3</b> - LPUART0_RTS_B<br><b>ALT4</b> - CT_INP2<br><b>ALT5</b> - CT0_MAT0<br><b>ALT6</b> - FLEXIO0_D6<br><b>ALT7</b> - SmartDMA_PIO12<br><b>ALT9</b> - LCD_P26 | <b>IO Supply</b> - VDD<br><b>Pad type</b> - SLOW<br><b>Default</b> - DIS | <b>ANALOG</b> -<br>ADC0_A12/LCD_P26                              |

Table continues on the next page...

Table 47. Pinmux...continued

| Pin Name | MCXA26xA25xA<br>18xA17x<br>LQFP144 | MCXA26xA25xA<br>18xA17x<br>WFBGA169 | MCXA26xA25xA<br>18xA17x<br>LQFP100 | MCXA26xA25xA<br>18xA17x<br>LQFP64 | Pinmux Assignment                                                                                                                                                                                                                      | Pad Settings                                                                        | Alternate Functions                                                                       |
|----------|------------------------------------|-------------------------------------|------------------------------------|-----------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------|
| P0_23    | 130                                | D8                                  | 90                                 | --                                | <b>ALT0</b> - P0_23<br><b>ALT3</b> - LPUART0_CTS_B<br><b>ALT4</b> - CT_INP3<br><b>ALT5</b> - CT0_MAT1<br><b>ALT6</b> - FLEXIO0_D7<br><b>ALT7</b><br>- SmartDMA_PIO13<br><b>ALT9</b> - LCD_P27                                          | <b>IO Supply</b> - VDD<br><b>Pad type</b> - SLOW<br><b>Default</b> - DIS            | <b>ANALOG</b> -<br>ADC0_A13/LCD_P27<br><b>VDD SYS</b> - WUU0_IN5                          |
| P0_24    | 131                                | C6                                  | --                                 | --                                | <b>ALT0</b> - P0_24<br><b>ALT4</b> - CT0_MAT0<br><b>ALT8</b> - LPUART5_RXD<br><b>ALT9</b> - LCD_P28                                                                                                                                    | <b>IO Supply</b> - VDD<br><b>Pad type</b> - SLOW<br><b>Default</b> - DIS            | <b>ANALOG</b> - LCD_P28                                                                   |
| P0_25    | 132                                | D6                                  | --                                 | --                                | <b>ALT0</b> - P0_25<br><b>ALT4</b> - CT0_MAT1<br><b>ALT8</b> - LPUART5_TXD<br><b>ALT9</b> - LCD_P29                                                                                                                                    | <b>IO Supply</b> - VDD<br><b>Pad type</b> - SLOW<br><b>Default</b> - DIS            | <b>ANALOG</b> - LCD_P29                                                                   |
| P0_26    | 133                                | C5                                  | --                                 | --                                | <b>ALT0</b> - P0_26<br><b>ALT4</b> - CT0_MAT2<br><b>ALT8</b> - LPUART5_RTS_B<br><b>ALT9</b> - LCD_P30                                                                                                                                  | <b>IO Supply</b> - VDD<br><b>Pad type</b> - SLOW<br><b>Default</b> - DIS            | <b>ANALOG</b> - LCD_P30                                                                   |
| P0_27    | 134                                | D5                                  | --                                 | --                                | <b>ALT0</b> - P0_27<br><b>ALT4</b> - CT0_MAT3<br><b>ALT8</b> - LPUART5_CTS_B<br><b>ALT9</b> - LCD_P31                                                                                                                                  | <b>IO Supply</b> - VDD<br><b>Pad type</b> - SLOW<br><b>Default</b> - DIS            | <b>ANALOG</b> - LCD_P31                                                                   |
| P1_0     | 135                                | A5                                  | 91                                 | 56                                | <b>ALT0</b> - P1_0<br><b>ALT1</b> - TRIG_IN0<br><b>ALT2</b> - LPSPI0_SDO<br><b>ALT3</b> - LPI2C1_SDA<br><b>ALT4</b> - CT_INP4<br><b>ALT5</b> - CT0_MAT2<br><b>ALT6</b> - FLEXIO0_D8<br><b>ALT9</b> - LCD_P0<br><b>ALT11</b> - CAN1_RXD | <b>IO Supply</b> - VDD<br><b>Pad type</b><br>- MED+I2C_FILT<br><b>Default</b> - DIS | <b>ANALOG</b> - ADC0_A16/<br>CMP0_IN3/LCD_P0<br><b>VDD SYS</b> - WUU0_IN6/<br>LPTMR0_ALT3 |
| P1_1     | 136                                | B5                                  | 92                                 | 57                                | <b>ALT0</b> - P1_1<br><b>ALT1</b> - TRIG_IN1                                                                                                                                                                                           | <b>IO Supply</b> - VDD                                                              | <b>ANALOG</b> - ADC0_A17/<br>CMP1_IN3/LCD_P1                                              |

Table continues on the next page...

Table 47. Pinmux...continued

| Pin Name | MCXA26xA25xA<br>18xA17x<br>LQFP144 | MCXA26xA25xA<br>18xA17x<br>WFBGA169 | MCXA26xA25xA<br>18xA17x<br>LQFP100 | MCXA26xA25xA<br>18xA17x<br>LQFP64 | Pinmux Assignment                                                                                                                                                                                                                          | Pad Settings                                                            | Alternate Functions                                                         |
|----------|------------------------------------|-------------------------------------|------------------------------------|-----------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------|-----------------------------------------------------------------------------|
|          |                                    |                                     |                                    |                                   | <b>ALT2</b> - LPSPi0_SCK<br><b>ALT3</b> - LPI2C1_SCL<br><b>ALT4</b> - CT_INP5<br><b>ALT5</b> - CT0_MAT3<br><b>ALT6</b> - FLEXIO0_D9<br><b>ALT9</b> - LCD_P1<br><b>ALT11</b> - CAN1_TXD                                                     | <b>Pad type</b><br>- MED+I2C_FILT<br><b>Default</b> - DIS               |                                                                             |
| P1_2     | 137                                | A4                                  | 93                                 | 58                                | <b>ALT0</b> - P1_2<br><b>ALT1</b> - TRIG_OUT0<br><b>ALT2</b> - LPSPi0_SDI<br><b>ALT3</b> - LPI2C1_SDAS<br><b>ALT4</b> - CT1_MAT0<br><b>ALT5</b> - CT_INP0<br><b>ALT6</b> - FLEXIO0_D10<br><b>ALT9</b> - LCD_P2<br><b>ALT11</b> - CAN0_TXD  | <b>IO Supply</b> - VDD<br><b>Pad type</b> - MED<br><b>Default</b> - DIS | <b>ANALOG</b> -<br>ADC0_A18/LCD_P2                                          |
| P1_3     | 138                                | B4                                  | 94                                 | 59                                | <b>ALT0</b> - P1_3<br><b>ALT1</b> - TRIG_OUT1<br><b>ALT2</b> - LPSPi0_PCS0<br><b>ALT3</b> - LPI2C1_SCLS<br><b>ALT4</b> - CT1_MAT1<br><b>ALT5</b> - CT_INP1<br><b>ALT6</b> - FLEXIO0_D11<br><b>ALT9</b> - LCD_P3<br><b>ALT11</b> - CAN0_RXD | <b>IO Supply</b> - VDD<br><b>Pad type</b> - MED<br><b>Default</b> - DIS | <b>ANALOG</b> - ADC0_A19/<br>CMP0_IN1/LCD_P3<br><b>VDD SYS</b> - WUU0_IN7   |
| VDD      | 139                                | J8                                  | 95                                 | 60                                |                                                                                                                                                                                                                                            | <b>IO Supply</b> - VDD                                                  |                                                                             |
| VSS      | 140                                | F7                                  | 96                                 | 61                                |                                                                                                                                                                                                                                            | <b>IO Supply</b> - VDD                                                  |                                                                             |
| P1_4     | 141                                | A3                                  | 97                                 | 62                                | <b>ALT0</b> - P1_4<br><b>ALT1</b><br>- FREQME_CLK_IN0<br><b>ALT2</b> - LPSPi0_PCS3<br><b>ALT3</b> - LPUART2_RXD<br><b>ALT4</b> - CT1_MAT2<br><b>ALT6</b> - FLEXIO0_D12<br><b>ALT7</b> - SmartDMA_PiO0                                      | <b>IO Supply</b> - VDD<br><b>Pad type</b> - MED<br><b>Default</b> - DIS | <b>ANALOG</b> - ADC0_A20/<br>CMP0_IN2/LCD_VLL2<br><b>VDD SYS</b> - WUU0_IN8 |

Table continues on the next page...

Table 47. Pinmux...continued

| Pin Name | MCXA26xA25xA<br>18xA17x<br>LQFP144 | MCXA26xA25xA<br>18xA17x<br>WFBGA169                                          | MCXA26xA25xA<br>18xA17x<br>LQFP100 | MCXA26xA25xA<br>18xA17x<br>LQFP64 | Pinmux Assignment                                                                                                                                                                                                                                                          | Pad Settings                                                            | Alternate Functions                                             |
|----------|------------------------------------|------------------------------------------------------------------------------|------------------------------------|-----------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------|-----------------------------------------------------------------|
| P1_5     | 142                                | B3                                                                           | 98                                 | 63                                | <b>ALT0</b> - P1_5<br><b>ALT1</b><br>- FREQME_CLK_IN1<br><b>ALT2</b> - LPSPi0_PCS2<br><b>ALT3</b> - LPUART2_TXD<br><b>ALT4</b> - CT1_MAT3<br><b>ALT6</b> - FLEXIO0_D13<br><b>ALT7</b> - SmartDMA_PIO1                                                                      | <b>IO Supply</b> - VDD<br><b>Pad type</b> - MED<br><b>Default</b> - DIS | <b>ANALOG</b> - ADC0_A21/<br>CMP1_IN2/LCD_VLL1                  |
| P1_6     | 143                                | A2                                                                           | 99                                 | 64                                | <b>ALT0</b> - P1_6<br><b>ALT1</b> - TRIG_IN2<br><b>ALT2</b> - LPSPi0_PCS1<br><b>ALT3</b> - LPUART2_RTS_B<br><b>ALT4</b> - CT_INP6<br><b>ALT5</b> - CT4_MAT0<br><b>ALT6</b> - FLEXIO0_D14<br><b>ALT7</b> - SmartDMA_PIO2<br><b>ALT9</b> - LCD_P4<br><b>ALT11</b> - CAN1_TXD | <b>IO Supply</b> - VDD<br><b>Pad type</b> - MED<br><b>Default</b> - DIS | <b>ANALOG</b> -<br>ADC0_A22/LCD_P4                              |
| P1_7     | 144                                | A1                                                                           | 100                                | 1                                 | <b>ALT0</b> - P1_7<br><b>ALT1</b> - TRIG_OUT2<br><b>ALT3</b> - LPUART2_CTS_B<br><b>ALT4</b> - CT_INP7<br><b>ALT5</b> - CT4_MAT1<br><b>ALT6</b> - FLEXIO0_D15<br><b>ALT7</b> - SmartDMA_PIO3<br><b>ALT9</b> - LCD_P5<br><b>ALT11</b> - CAN1_RXD                             | <b>IO Supply</b> - VDD<br><b>Pad type</b> - MED<br><b>Default</b> - DIS | <b>ANALOG</b> -<br>ADC0_A23/LCD_P5<br><b>VDD SYS</b> - WUU0_IN9 |
|          | --                                 | G7,H7,J7,K7,L7,<br>G2,G3,G4,G10,<br>G11,G12,F5,F6,<br>F8,F9,H6,H8,H9,<br>M11 | --                                 | --                                |                                                                                                                                                                                                                                                                            |                                                                         |                                                                 |
|          | --                                 | J9                                                                           | --                                 | --                                |                                                                                                                                                                                                                                                                            |                                                                         |                                                                 |
|          | --                                 | C4, F3, F4, G8,<br>G9, H3, H4, J3,<br>J4, K3, K4, K10,<br>K11, L10           | --                                 | --                                |                                                                                                                                                                                                                                                                            |                                                                         |                                                                 |

## Note:

- +I3C in Pad Type represents that strong pull up resistor is implemented on the pin. PV bit is implemented in Pin Control register of the pin.
- 2. +I2C\_FILT in Pad Type represents that I2C filter is implemented on the pin. PFE bit is implemented in Pin Control register of the pin.
- 3. HD in Pad Type represents that the pin can support up to 20mA drive strength. I2C filter is implemented on the pin. PFE bit is implemented in Pin Control register of the pin.
- 5VTOL in Pad Type represents that the pin is 5V tolerant.
- DIS in default column represents that the pin's input buffer is disabled by default
- RST pads support passive filter and 1M ohm pull resistor. PFE and PV bits are implemented in Pin Control register of the pin.
- PE, PS, SRE, ODE and DSE are supported in Pin Control register of all types of IO.
- 5VTol and HD pads support two DSE bits in Pin Control register of the pin.
- SLOW in Pad Type represents the IO supports 25MHz. MED in Pad Type represents the IO supports 50MHz.
- +TAM in Pad Type represents the IO supports 1M ohm pull resistor.
- CAN1, LPUART5, SLCD are not available in MCXA17x and MCXA25x.
- P0\_6 is the ISP\_ENTRY pin to for WFBGA169, LQFP144, LQFP100, and LQFP64 package. P3\_29 is the ISP\_ENTRY pin for QFN32 package.

## 6.2 MCX A175, A176, A185, A186, A255, A256, A265, and A266 Pinouts

The pinout diagrams are provided in an Excel file attached to this document:

1. Click the paperclip symbol on the left side of the PDF window.
2. Double-click on the Excel file to open it.
3. Select the respective package tab.

Many signals may be multiplexed onto a single pin. To determine what signals can be used on which pin, refer to the "Pinout" tab in the Excel file.

## 6.3 Recommended connection for unused analog and digital pins

Table 48 shows the recommended connections for pins if those pins are not used in the customer's application

Table 48. Recommended connection for unused analog and digital pins

| Pin Type | Pin Function | Recommendation                                                                                      | Comments                                                                                                             |
|----------|--------------|-----------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------|
| Power    | VDD          | Must be powered                                                                                     | VDD is the IO supply of P0,P1,P2 and P4, and supplies internal modules including Flash, CMP, and etc.. It must be on |
| Power    | VDD_ANA      | Must be powered                                                                                     | VDD_ANA must be same level with VDD, and ramps up together with VDD                                                  |
| Power    | VDD_USB      | Tie to ground through a 10 kΩ resistor if VDD_USB is an independent pin in the package version used |                                                                                                                      |

*Table continues on the next page...*

Table 48. Recommended connection for unused analog and digital pins...continued

| Pin Type        | Pin Function             | Recommendation                      | Comments                              |
|-----------------|--------------------------|-------------------------------------|---------------------------------------|
| Power           | VREFH                    | Always connect to VDD_ANA potential | Always connect to VDD_ANA potential   |
| Power           | VREFL                    | Always connect to VSS potential     | Always connect to VSS potential       |
| Power           | VSS_ANA                  | Always connect to VSS potential     | Always connect to VSS potential       |
| Power           | VSS_USB                  | Always connect to VSS potential     | Always connect to VSS potential       |
| Analog/non-GPIO | ADC $n_x$                | Float                               |                                       |
| Analog/non-GPIO | ADC $n_x$ /DAC $n_{OUT}$ | Float                               |                                       |
| Analog/non-GPIO | EXTAL                    | Float                               |                                       |
| Analog/non-GPIO | XTAL                     | Float                               | Analog output - Float                 |
| Analog/non-GPIO | USB0_DP                  | Float                               | Float                                 |
| Analog/non-GPIO | USB0_DM                  | Float                               | Float                                 |
| GPIO/Analog     | Px/ADC $n_x$             | Float                               | Float (default is analog input)       |
| GPIO/Analog     | Px/CMP $n_{INx}$         | Float                               | Float (default is analog input)       |
| GPIO/Digital    | JTAG_TCLK                | Float                               | Float (default is JTAG with pulldown) |
| GPIO/Digital    | JTAG_TDI                 | Float                               | Float (default is JTAG with pullup)   |
| GPIO/Digital    | JTAG_TDO                 | Float                               | Float (default is JTAG with pullup)   |
| GPIO/Digital    | JTAG_TMS                 | Float                               | Float (default is JTAG with pullup)   |
| GPIO/Digital    | Px                       | Float                               | Float (default is disabled)           |

## 7 Ordering parts

### 7.1 Determining valid orderable parts

Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to [nxp.com](https://www.nxp.com) and perform a part number search for the following device numbers: MCXA256

## 8 Part identification

Part numbers for the device have fields that identify the specific part. Use the values of these fields to determine the specific part.

### 8.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

### 8.2 Part number format

Part numbers for this device have the following format:

B PS F C D FS T PG SR PT

Table 49. Part number fields descriptions

| Field | Description                     | Values                                                                                                                                                                                                                                                                                                                                                                                   |
|-------|---------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| B     | Brand                           | <ul style="list-style-type: none"> <li>• MCX</li> </ul>                                                                                                                                                                                                                                                                                                                                  |
| PS    | Product series name             | <ul style="list-style-type: none"> <li>• A</li> </ul>                                                                                                                                                                                                                                                                                                                                    |
| F     | Family                          | <ul style="list-style-type: none"> <li>• 1 = Baseline</li> <li>• 2 = Baseline Enhance</li> </ul>                                                                                                                                                                                                                                                                                         |
| C     | Core Features                   | <ul style="list-style-type: none"> <li>• 5 = 180 MHz, 2xADC, 2xMotor PWM, 5xUART, 1xCAN, 1xUSB, 1xFlexIO, Security</li> <li>• 6 = 240 MHz, 2xADC, 2xMotor PWM, 6xUART, 2xCAN, 1xUSB, 1xFlexIO, SLCD, Security</li> <li>• 7 = 180 MHz, 2xADC, 2x Motor PWM, 5xUART, 1x CAN, 1xUSB, 1xFlexIO</li> <li>• 8 = 240 MHz, 2xADC, 2x Motor PWM, 6xUART, 2x CAN, 1xUSB, 1xFlexIO, SLCD</li> </ul> |
| FS    | Flash Size                      | <ul style="list-style-type: none"> <li>• 5 = 512 KB</li> <li>• 6 = 1024 KB</li> </ul>                                                                                                                                                                                                                                                                                                    |
| T     | Junction Temperature range (°C) | <ul style="list-style-type: none"> <li>• V = -40 to 125 °C</li> </ul>                                                                                                                                                                                                                                                                                                                    |
| PG    | Package                         | <ul style="list-style-type: none"> <li>• LH = LQFP64</li> <li>• LL = LQFP100</li> <li>• LQ = LQFP144</li> <li>• PN = WFBGA169</li> </ul>                                                                                                                                                                                                                                                 |
| SR    | Silicon Revision                | <ul style="list-style-type: none"> <li>• A = Initial Mask set</li> <li>• B = 1st Major spin</li> <li>• C = 2nd Major spin</li> </ul>                                                                                                                                                                                                                                                     |
| PT    | Package Type                    | <ul style="list-style-type: none"> <li>• R = Tape and Reel</li> <li>• T = Tray</li> </ul>                                                                                                                                                                                                                                                                                                |

### 8.3 Example

This is an example part number:

MCXA256VLH

### 8.4 Small package marking

### 8.4.1 Package marking information

Table 50. Package Marking

| Line        | LQFP144    | LQFP100    | LQFP64     | WFBGA169 |
|-------------|------------|------------|------------|----------|
| First Line  | AAAAAAAAAA | AAAAAAAAAA | AAAAAAA    | AAAAA    |
| Second Line | MMMMM      | MMMMM      | AAA MMMMM  | MMMMM    |
| Third Line  | XXXXYYWWXX | XXXXYYWWXX | XXXXYYWWXX | XXXYWXX  |

Table 51. Package marking

| Identifier | Description                                     |
|------------|-------------------------------------------------|
| A          | Part number code, refer to Ordering Information |
| M          | Mask set                                        |
| Y          | Year                                            |
| W          | Work week                                       |
| X          | NXP internal use                                |

## 9 Terminology and guidelines

### 9.1 Definitions

Key terms are defined in the following table:

Table 52. Definitions

| Term                  | Definition                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|-----------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Rating                | <p>A minimum or maximum value of a technical characteristic that, if exceeded, may cause permanent chip failure:</p> <ul style="list-style-type: none"> <li>• <i>Operating ratings</i> apply during operation of the chip.</li> <li>• <i>Handling ratings</i> apply when the chip is not powered.</li> </ul> <p><b>Note:</b> The likelihood of permanent chip failure increases rapidly as soon as a characteristic begins to exceed one of its operating ratings.</p> |
| Operating requirement | A specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip                                                                                                                                                                                                                                                                          |
| Operating behavior    | A specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions                                                                                                                                                                                                                                                                                     |
| Typical value         | <p>A specified value for a technical characteristic that:</p> <ul style="list-style-type: none"> <li>• Lies within the range of values specified by the operating behavior</li> <li>• Is representative of that characteristic during operation when you meet the <a href="#">typical-value conditions</a> or other specified conditions</li> </ul> <p><b>Note:</b> Typical values are provided as design guidelines and are neither tested nor guaranteed.</p>        |

9.2 Examples

Operating rating:

| Symbol          | Description               | Min. | Max. | Unit |
|-----------------|---------------------------|------|------|------|
| V <sub>DD</sub> | 1.0 V core supply voltage | −0.3 | 1.2  | V    |

Operating requirement:

| Symbol          | Description               | Min. | Max. | Unit |
|-----------------|---------------------------|------|------|------|
| V <sub>DD</sub> | 1.0 V core supply voltage | 0.9  | 1.1  | V    |

Operating behavior that includes a typical value:

| Symbol          | Description                              | Min. | Typ. | Max. | Unit |
|-----------------|------------------------------------------|------|------|------|------|
| I <sub>WP</sub> | Digital I/O weak pullup/pulldown current | 10   | 70   | 130  | μA   |

Figure 28. Examples

9.3 Typical-value conditions

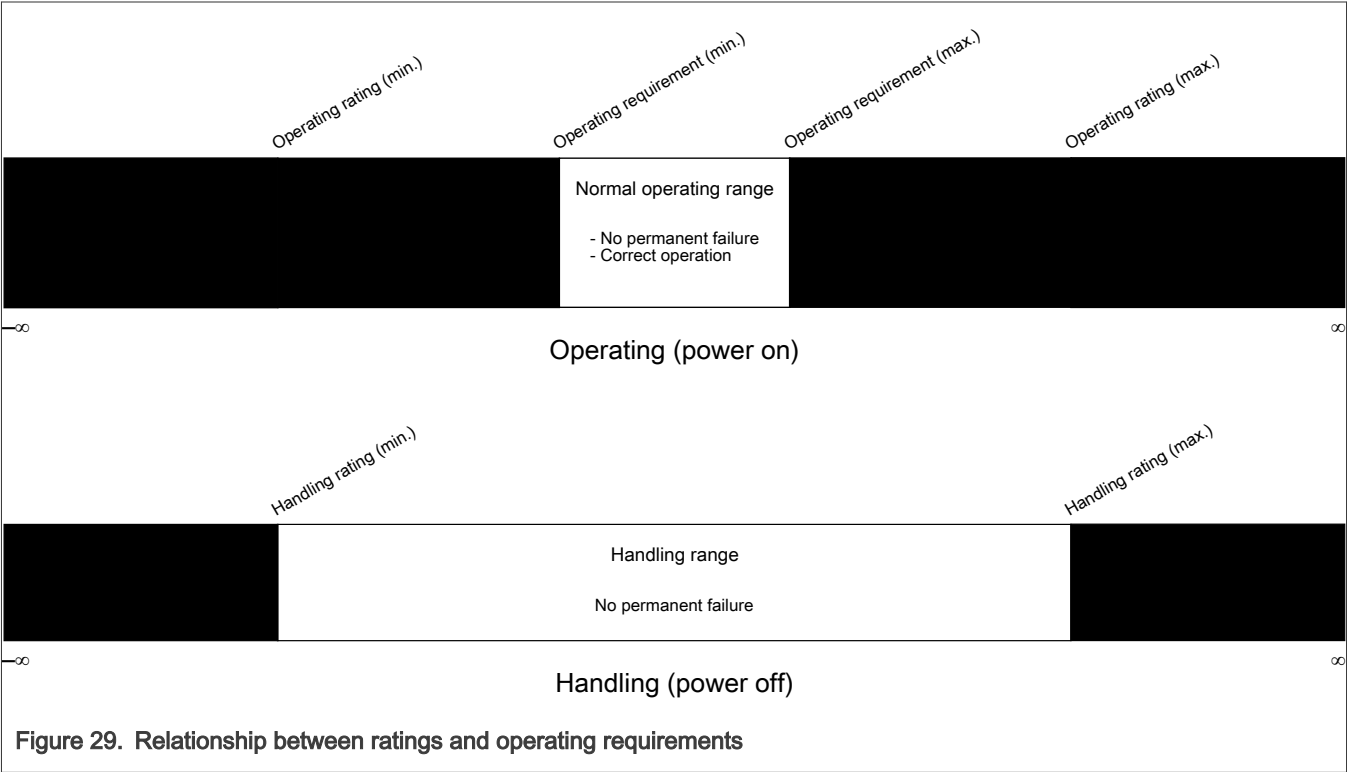
Typical values assume you meet the following conditions (or other conditions as specified):

Table 53. Typical-value conditions

| Symbol          | Description         | Value | Unit |
|-----------------|---------------------|-------|------|
| T <sub>A</sub>  | Ambient temperature | 25    | °C   |
| V <sub>DD</sub> | Supply voltage      | 3.3   | V    |

**Note:** Typical values are based on characterization but not covered by test limits in production.

9.4 Relationship between ratings and operating requirements



9.5 Guidelines for ratings and operating requirements

Follow these guidelines for ratings and operating requirements:

- Never exceed any of the chip’s ratings.
- During normal operation, don’t exceed any of the chip’s operating requirements.
- If you must exceed an operating requirement at times other than during normal operation (for example, during power sequencing), limit the duration as much as possible.

9.6 Specification Test Methods

Each specification is tested using one of these methods.

Table 54. Specification test methods

| Code | Method                                                      | Description                                                                                                                                              |
|------|-------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------|
| P    | Production direct                                           | On every chip during production, testing the specification                                                                                               |
| I    | Production indirect                                         | On every chip during production, testing parts of a module that affect whether the chip meets the specification but not testing the specification itself |
| C    | Characterization on a production tester                     | Measuring a statistically significant number of sample chips across process (matrix lot), voltage, and temperature                                       |
| L    | Characterization on lab equipment or a nonproduction tester |                                                                                                                                                          |

Table continues on the next page...

Table 54. Specification test methods...continued

| Code | Method               | Description                                                                                                                                                                                                              |
|------|----------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|      |                      | <b>Note:</b> Typical values are not necessarily characterized across process.                                                                                                                                            |
| D    | Guaranteed by design | Specification based on scientific and engineering principles                                                                                                                                                             |
| O    | Other                | Using methods such as: <ul style="list-style-type: none"> <li>• Performing silicon simulations</li> <li>• Performing package thermal simulations</li> <li>• Calculating specifications using reliability data</li> </ul> |

## 10 Revision History

The following table provides a revision history for this document.

Table 55. Revision History

| Document ID         | Release Date     | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|---------------------|------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| MCXAP144M240F61 v.3 | 14 November 2025 | <ul style="list-style-type: none"> <li>• Updated descriptions of FRO180M, Code Watchdog and CTimer in Section Features</li> <li>• Added MCXA18x and MCXA26x parts in the data sheet</li> <li>• Updated the front matter and feature comparison section</li> <li>• Updated Related resources table and Ordering Information table</li> <li>• Updated the block diagram and bus matrix diagram</li> <li>• Updated Power consumption operating behaviours</li> <li>• Updated Device clock specifications</li> <li>• Added units in JTAG debug interface timing</li> <li>• Updated System Oscillator Crystal Specifications table</li> <li>• Updated Table. FRO180M specifications</li> <li>• Updated INL and DNL parameters of ADC electrical characteristics</li> <li>• Updated second reference of LP9 from slow speed to medium speed in LPSPI controller mode timing</li> <li>• Updated the condition of third instance of LP1 from Peripheral Rx to Peripheral Tx in OD mode in LPSPI peripheral mode timing</li> <li>• Added Segment LCD electrical specifications</li> <li>• Updated the pinout table</li> <li>• Updated Part number fields descriptions table</li> </ul> |

Table continues on the next page...

Table 55. Revision History...continued

| Document ID         | Release Date | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|---------------------|--------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| MCXAP144M240F61 v.2 | 11 June 2025 | <ul style="list-style-type: none"> <li>Updated MCXA275 and MCXA276 by MCXA255 and MCXA256 all over the document</li> <li>Updated the block diagram and bus matrix</li> <li>Removed the part number list box in front matter</li> <li>Updated TBDs in front matter</li> <li>Updated Feature Comparison table</li> <li>Updated Ordering Information</li> <li>Removed the Note after block diagram</li> <li>Updated Thermal attributes section</li> <li>Added I/O mux resistance table</li> <li>Removed CT parameter from 12-bit DAC operating behaviors</li> <li>Updated FIRC to FRO180M in power mode transition operating behaviours section</li> <li>Removed INL and DNL parameters for the power supply below 1.71V from Comparator and 8-bit DAC electrical specifications</li> <li>Added figures of Comparator and 8-bit DAC electrical specifications</li> <li>Updated I2C HS mode timing electrical specifications</li> <li>Updated Op-amp to OpAmp and OpAmp electrical specifications</li> <li>Updated I3C Push-Pull Timing Parameters for SDR mode</li> <li>Updated the maximum value of Tstart in System oscillator crystal electrical specifications</li> <li>Added document number of package drawing of WFBGA169</li> <li>Updated the Package marking information section</li> <li>Added space between MCX and A to unify the device name and family in data sheet</li> <li>Updated master to controller and slave to peripheral in LPSPI module to align with inclusive language</li> <li>Updated the values in Power mode transition operating behaviours table</li> <li>Updated the values in Power consumption operating behaviours table</li> <li>Updated Thermal attributes section</li> <li>Removed Debug trace operating behaviours table</li> <li>Updated the values of JTAG Debug Interface Timing</li> <li>Added S4 and updated the other values in Serial Wire Debug (SWD) Timing specifications</li> <li>Updated the operator in description of tpgmpg_lifetime for 128 B and tpgmphr_initial for 16 B in Flash commandtime specifications</li> </ul> |

Table continues on the next page...

Table 55. Revision History...continued

| Document ID         | Release Date  | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|---------------------|---------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                     |               | <ul style="list-style-type: none"><li>• Updated TBDs and added K to Nnvmcyc256k in Flash reliability specifications table</li><li>• Updated the values in LPSPI controller mode timing and LPSPI peripheral mode timing</li><li>• Added FlexCAN description</li><li>• Removed Segment LCD electrical specification</li><li>• Updated the pinout table</li><li>• Updated comments in VDD_ANA in Recommended connection for unused analog and digital pins</li><li>• Removed leakage current for all pins in Voltage and current operating behaviours</li><li>• Added Note in package diagram in front page "All information on the package WFBGA169 is preliminary and pending qualification"</li></ul> |
| MCXAP144M240F61 v.1 | December 2024 | <ul style="list-style-type: none"><li>• Initial version</li></ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |

## Legal information

### Data sheet status

| Document status <sup>[1][2]</sup> | Product status <sup>[3]</sup> | Definition                                                                            |
|-----------------------------------|-------------------------------|---------------------------------------------------------------------------------------|
| Objective [short] data sheet      | Development                   | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet    | Qualification                 | This document contains data from the preliminary specification.                       |
| Product [short] data sheet        | Production                    | This document contains the product specification.                                     |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <https://www.nxp.com>.

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