REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Remove footnote 5/ reference from paragraph 1.4 and footnote 5/ at bottom of page 3. Correct truth table in figure 2. Remove paragraph 4.3.1. - CFS	01-12-11	Thomas M. Hess
B	Change lead temperature in section 1.3. Add section 1.5, radiation features. Update boilerplate to MIL-PRF-38535 requirements and to include radiation hardness assured requirements. Editorial changes throughout. - LTG	04-11-05	Thomas M. Hess
C	Update radiation features in section 1.5. Add SEP test table IB and paragraph 4.4.4.2. – jak	11-05-02	David J. Corbett
D	Delete class M requirements. Update boilerplate paragraphs to current requirements of MIL-PRF-38535. - LTG	17-12-20	Thomas M. Hess
E	Add device with case outline Y for grounded lid for class V device. Update device supplier's information and boilerplate paragraphs as required by the MIL-PRF-38535. – MAA	19-03-11	Thomas M. Hess

REV																				
SHEET																				
REV																				
SHEET																				
REV STATUS				REV			E	E	E	E	E	E	E	E	E	E	E	E	E	E
OF SHEETS				SHEET			1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

PREPARED BY
Charles F. Saffle

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
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STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
Charles F. Saffle

APPROVED BY
Thomas M. Hess

DRAWING APPROVAL DATE
01-06-27

REVISION LEVEL
E

MICROCIRCUIT, DIGITAL, ADVANCED CMOS, QUAD 2-INPUT NOR GATE, TTL COMPATIBLE INPUTS, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-89791**

SHEET 1 OF 14

DSCC FORM 2233
APR 97

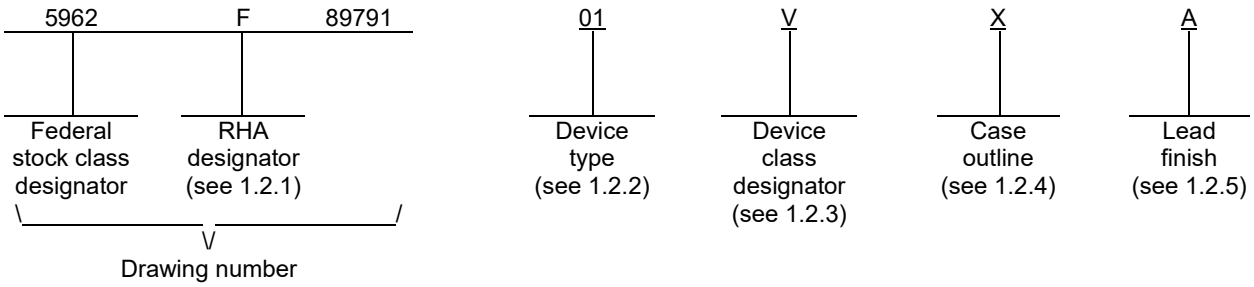
5962-E210-19

DISTRIBUTION STATEMENT A. Approved for public release. Distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	54ACT02	Quad 2-input NOR gate, TTL compatible inputs

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	CDFP3-F14	14	Flat pack
Y	CDFP3-F14	14	Flat pack 1/

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V.

1/ Package case outline Y flat pack with grounded lid.

1.3 Absolute maximum ratings. 1/ 2/ 3/

Supply voltage range (V_{CC})	-0.5 V dc to +7.0 V dc
DC input voltage range (V_{IN})	-0.5 V dc to V_{CC} + 0.5 V dc
DC output voltage range (V_{OUT})	-0.5 V dc to V_{CC} + 0.5 V dc
DC input clamp current (I_{IK}) (V_{IN} < 0.0 V or V_{IN} > V_{CC})	±20 mA
DC output clamp current (I_{OK}) (V_{OUT} < 0.0 V or V_{OUT} > V_{CC})	±20 mA
Continuous output current (I_{OUT}) (V_{OUT} = 0 to V_{CC})	±50 mA
Continuous current through V_{CC} or GND	±200 mA
Maximum power dissipation (P_D)	500 mW
Storage temperature range (T_{STG})	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+260°C
Thermal resistance, junction-to-case (θ_{JC})	See MIL-STD-1835
Junction temperature (T_J)	+175°C 4/

1.4 Recommended operating conditions. 2/ 3/

Supply voltage range (V_{DD})	+4.5 V dc to +5.5 V dc
Input voltage range (V_{IN})	+0.0 V dc to V_{CC}
Output voltage range (V_{OUT})	+0.0 V dc to V_{CC}
Case operating temperature range (T_C)	-55°C to +125°C
Input rise or fall time rate ($\Delta t/\Delta V$) (V_{CC} = 4.5 V to 5.5 V)	0 to 8 ns/V

1.5 Radiation features.

Device type 01:

Maximum total dose available (dose rate = 50 – 300 rad (Si)/s)	300 krad(Si)

Single event phenomenon (SEP):

Effective LET, no latch-up (SEL) (see 4.4.4.2)	≤ 93 MeV-cm^2/mg 5/
Effective LET, no upsets (SEU) (see 4.4.4.2)	≤ 93 MeV-cm^2/mg 5/

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2/ Unless otherwise noted, all voltages are referenced to GND.

3/ The limits for the parameters specified herein shall apply over the full specified V_{CC} range and case temperature range of -55°C to +125°C.

4/ Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883.

5/ These limits were obtained during technology characterization and qualification, and are guaranteed by design or process, but not production tested unless specified by the customer through the purchase order or contract.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://quicksearch.dla.mil).

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents cited in the solicitation or contract.

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JESD20 - Standard for Description of 54/74ACXXXXX and 54/74ACTXXXXX Advanced High-Speed CMOS Devices.

(Copies of these documents are available online at http://www.jedec.org or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240-S Arlington, VA 22201-2107).

ASTM INTERNATIONAL (ASTM)

ASTM F1192 - Standard Guide for the Measurement of Single Event Phenomena (SEP) Induced by Heavy Ion Irradiation of Semiconductor Devices.

(Copies of this document is available online at http://www.astm.org/ or from ASTM International, 100 Barr Harbor Drive, P. O. Box C700, West Conshohocken, PA 19428-2959).

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Logic diagram. The logic diagram shall be as specified on figure 3.

3.2.5 Switching waveforms and test circuit. The switching waveforms and test circuit shall be as specified on figure 4.

3.2.6 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table IA and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table IA.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 hereinThe certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

TABLE IA. Electrical performance characteristics.

Test and MIL-STD-883 test method 1/	Symbol	Test conditions 2/ 3/ $-55°C \le T_C \le +125°C$ $+4.5\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified	Device type and device class	V_{CC}	Group A subgroups	Limits 4/		Unit
						Min	Max	
Positive input clamp voltage 3022	V_{IC+}	For input under test, I_{IN} = 1.0 mA	All V	0.0 V	1	0.4	1.5	V
Negative input clamp voltage 3022	V_{IC-}	For input under test, I_{IN} = -1.0 mA	All V	Open	1	-0.4	-1.5	V
High level input voltage	V_{IH} 5/		All All	4.5 V and 5.5 V	1, 2, 3	2.0		V
Low level input voltage	V_{IL} 5/		All All	4.5 V and 5.5 V	1, 2, 3		0.8	V
High level output voltage 3006	V_{OH} 6/	$V_{IN} = V_{IH}$ = 2.0 V or V_{IL} = 0.8 V I_{OH} = -50 µA	All All	4.5 V	1, 2, 3	4.4		V
			All All	5.5 V	1, 2, 3	5.4		
		$V_{IN} = V_{IH}$ = 2.0 V or V_{IL} = 0.8 V I_{OH} = -24 mA	All All	4.5 V	1	3.86		
					2, 3	3.70		
			All All	5.5 V	1	4.86		
					2, 3	4.70		
		$V_{IN} = V_{IH}$ = 2.0 V or V_{IL} = 0.8 V I_{OH} = -50 mA	All All	5.5 V	1, 2, 3	3.85		
Low level output voltage 3007	V_{OL} 6/	$V_{IN} = V_{IH}$ = 2.0 V or V_{IL} = 0.8 V I_{OL} = 50 µA	All All	4.5 V	1, 2, 3		0.1	V
			All All	5.5 V	1, 2, 3		0.1	
		$V_{IN} = V_{IH}$ = 2.0 V or V_{IL} = 0.8 V I_{OL} = 24 mA	All All	4.5 V	1		0.36	
					2, 3		0.50	
			All All	5.5 V	1		0.36	
					2, 3		0.50	
		$V_{IN} = V_{IH}$ = 2.0 V or V_{IL} = 0.8 V I_{OL} = 50 mA	All All	5.5 V	1, 2, 3		1.65	
Input leakage current low 3009	I_{IL}	V_{IN} = 0.0 V	All All	5.5 V	1		-0.1	µA
					2, 3		-1.0	
Input leakage current high 3010	I_{IH}	V_{IN} = 5.5 V	All All	5.5 V	1		0.1	µA
					2, 3		1.0	
Quiescent supply current delta, TTL input levels 3005	ΔI_{CC} 7/	For input under test, $V_{IN} = V_{CC}$ - 2.1 V For all other inputs, $V_{IN} = V_{CC}$ or GND	All All	5.5 V	1, 2, 3		1.6	mA

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method 1/	Symbol	Test conditions 2/ 3/ $-55°C \le T_C \le +125°C$ $+4.5\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified	Device type and device class	V_{CC}	Group A subgroups	Limits 4/ Min	Limits 4/ Max	Unit
Quiescent supply current, output high 3005	I_{CCH}	$V_{IN} = V_{CC}$ or GND	All	5.5 V	1		2	µA
			All		2, 3		40	
		M, D, P, L, R, F 8/	01 Q, V		1		50	
Quiescent supply current, output low 3005	I_{CCL}	$V_{IN} = V_{CC}$ or GND	All	5.5 V	1		2	µA
			All		2, 3		40	
		M, D, P, L, R, F 8/	01 Q, V		1		50	
Input capacitance 3012	C_{IN}	See 4.4.1c $T_C = +25°C$	All All	5.0 V	4		8	pF
Power dissipation capacitance	C_{PD} 9/	See 4.4.1c $T_C = +25°C$, f = 1 MHz	All All	5.0 V	4		55	pF
Functional tests 3014	10/	See 4.4.1b $V_{IN} = V_{IH}$ or V_{IL} Verify output V_{OUT}	All All	4.5 V	7, 8	L	H	
				5.5 V	7, 8	L	H	
Propagation delay time, mA, mB to mY 3003	t_{PLH}, t_{PHL} 11/	$C_L = 50$ pF minimum $R_L = 500\Omega$ See figure 5	All All	4.5 V	9	1.5	8.0	ns
			All All		10, 11	1.0	11.0	
			All All	5.5 V	9	1.5	8.0	
			All All		10, 11	1.0	11.0	

1/ For tests not listed in the referenced MIL-STD-883, [e.g. V_{IH}, V_{IL}], utilize the general test procedure under the conditions listed herein.

2/ Each input/output, as applicable, shall be tested at the specified temperature, for the specified limits, to the tests in table IA herein. Output terminals not designated shall be high level logic, low level logic, or open, except as follows:

a. V_{IC} (pos) tests, the GND terminal can be open. $T_C = +25°C$.
b. V_{IC} (neg) tests, the V_{CC} terminal shall be open. $T_C = +25°C$.
c. All I_{CC} and ΔI_{CC} tests, the output terminal shall be open. When performing these tests, the current meter shall be placed in the circuit such that all current flows through the meter.

3/ RHA devices supplied to this drawing have been characterized through all levels M, D, P, L, R, and F of irradiation. However, this device is only tested at the 'R' level. Pre and Post irradiation values are identical unless otherwise specified in Table IA. When performing post irradiation electrical measurements for any RHA level, $T_A = +25°C$.

4/ For negative and positive voltage and current values, the sign designates the potential difference in reference to GND and the direction of current flow, respectively; and the absolute value of the magnitude, not the sign, is relative to the minimum and maximum limits, as applicable, listed herein. All devices shall meet or exceed the limits specified in table IA, as applicable, at $4.5\ V \le V_{CC} \le 5.5\ V$.

5/ The V_{IH} and V_{IL} tests are not required if applied as forcing functions for V_{OH} and V_{OL} tests.

6/ The V_{OH} and V_{OL} tests shall be tested at $V_{CC} = 4.5$ V. The V_{OH} and V_{OL} tests are guaranteed, if not tested, for $V_{CC} = 5.5$ V. Limits shown apply to operation at $V_{CC} = 5.0\ V \pm 0.5\ V$. Tests with input current at +50 mA or -50 mA are performed on only one input at a time with duration not to exceed 10 ms. Transmission driving tests may be performed using $V_{IN} = V_{CC}$ or GND. When $V_{IN} = V_{CC}$ or GND is used, the test is guaranteed for $V_{IN} = V_{IH}$ minimum and V_{IL} maximum. Values for subgroup 1 shall be guaranteed, if not tested, to the limits specified in table IA, herein.

7/ This test may be performed either one input at a time (preferred method) or with all input pins simultaneously at $V_{IN} = V_{CC} - 2.1$ V (alternate method). Classes Q and V shall use the preferred method. When the test is performed using the alternate test method, the maximum limit is equal to the number of inputs at a high TTL input level times 1.6 mA; and the preferred method and limits are guaranteed.

8/ The maximum limit for this parameter at 100 krads (Si) is 2 μA.

9/ Power dissipation capacitance (C_{PD}) determines the no load dynamic power consumption (P_D) and dynamic current consumption (I_S). Where:

$P_D = (C_{PD} + C_L) (V_{CC} \times V_{CC})f + (I_{CC} \times V_{CC}) + (n \times d \times \Delta I_{CC} \times V_{CC})$.

$I_S = (C_{PD} + C_L)V_{CC}f + I_{CC} + (n \times d \times \Delta I_{CC})$.

For both P_D and I_S, n is the number of device inputs at TTL levels, f is the frequency of the input signal, d is the duty cycle of the input signal, and C_L is the external output load capacitance.

10/ Tests shall be performed in sequence, attributes data only. Functional tests shall include the truth table and other logic patterns used for fault detection. The test vectors used to verify the truth table shall, at a minimum, test all functions of each input and output. All possible input to output logic patterns per function shall be guaranteed, if not tested, to the truth table in figure 2 herein. Functional tests shall be performed in sequence as approved by the qualifying activity on qualified devices. After incorporating allowable tolerances in accordance with MIL-STD-883, V_{IL} = 0.4 V and V_{IH} = 2.4 V. For outputs, L ≤ 0.8 V; H ≥ 2.0 V.

11/ AC limits at V_{CC} = 5.5 V are equal to the limits at V_{CC} = 4.5 V and guaranteed by testing at V_{CC} = 4.5 V. Minimum ac limits for V_{CC} = 5.5 V are 1.0 ns and guaranteed by guard-banding the V_{CC} = 4.5 V minimum limits to 1.5 ns. For propagation delay tests, all paths must be tested.

TABLE IB. SEP test limits. 1/ 2/

Device type	V_{CC} = 4.5 V 3/	Bias V_{CC} = 5.5 V For latch-up test no latch-up occur at effective LET = 4/ 5/ [MeV/(mg/cm^2)]
	Effective LET no upsets [MeV/(mg/cm^2)]	
01	LET ≤ 93 6/	≤ 93

1/ For SEP test conditions, see 4.4.4.2 herein.
2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end-of-line testing. Test plan must be approved by TRB and qualifying activity.
3/ Tested for upsets at operating temperature, T_A = +25°C ±10°C.
4/ Tested at operating temperature, T_A = +125°C ±10°C for latch-up.
5/ Tested to a LET of ≤ 93 MeV/(mg/cm^2) with no latch-up (SEL).
6/ Tested to a LET of ≤ 93 MeV/(mg/cm^2) with no single event upsets (SEU).

Device type	01
Case outline	X and Y
Terminal number	Terminal symbol
1	1Y
2	1A
3	1B
4	2Y
5	2A
6	2B
7	GND
8	3A
9	3B
10	3Y
11	4A
12	4B
13	4Y
14	V_{CC}

Note: Package case outline X flat pack with isolated lid. Package case outline Y flat pack with grounded lid.

Pin description	
Terminal symbol	Description
mA (m = 1 to 4)	Data inputs
mB (m = 1 to 4)	Data inputs
mY (m = 1 to 4)	Data outputs

FIGURE 1. Terminal connections.

Inputs		Outputs
mA	mB	mY
L	L	H
L	H	L
H	L	L
H	H	L

H = High voltage level
L = Low voltage level

FIGURE 2. Truth table.

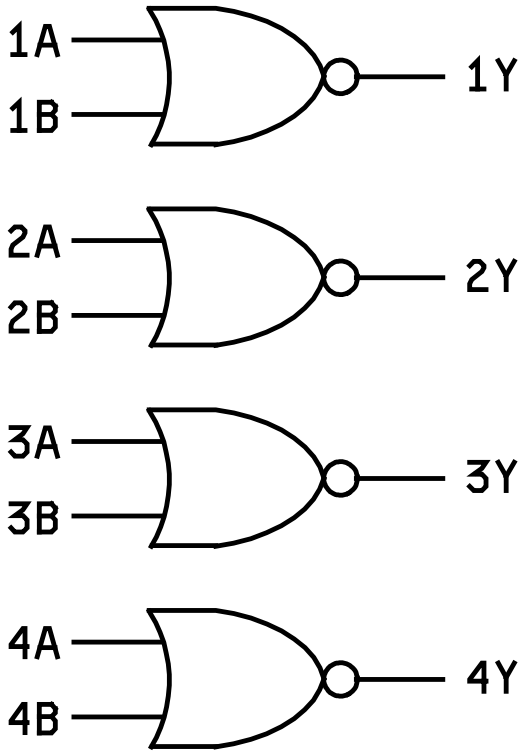
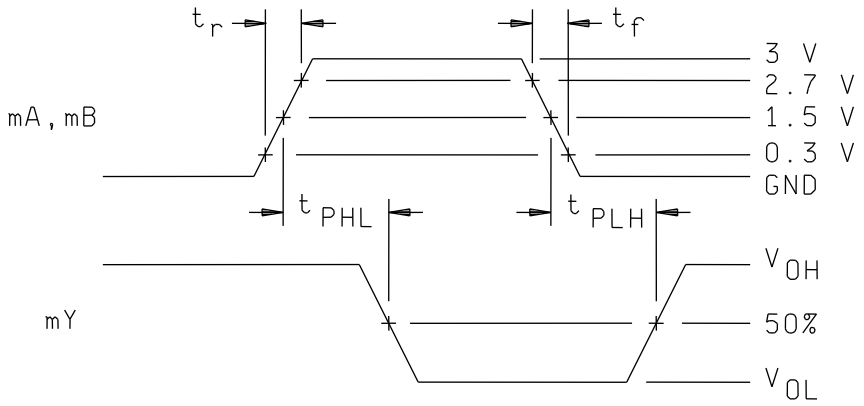
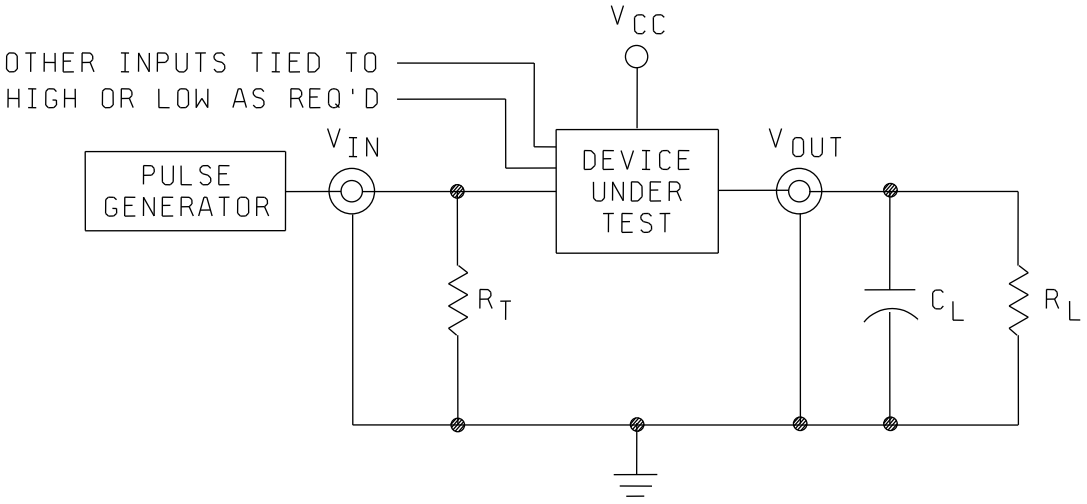


FIGURE 3. Logic diagram.





NOTES:
1. C_L = 50 pF or equivalent (includes test jig and probe capacitance).
2. R_T = 50Ω or equivalent. R_L = 500Ω or equivalent.
3. Input signal from pulse generator: V_{IN} = 0.0 V to 3.0 V; PRR ≤ 1 MHz; Z_O = 50Ω; t_r ≤ 3.0 ns; t_f ≤ 3.0 ns; t_r and t_f shall be measured from 0.3 V to 2.7 V and from 2.7 V to 0.3 V, respectively; duty cycle = 50 percent.
4. Timing parameters shall be tested at a minimum input frequency of 1MHz.
5. The outputs are measured one at a time with one transition per measurement.

FIGURE 4. Switching waveforms and test circuit.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections, and as specified herein.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

c. C_{IN} and C_{PD} shall be measured only for initial qualification and after process or design changes which may affect capacitance. C_{IN} shall be measured between the designated terminal and GND at a frequency of 1 MHz. C_{PD} shall be tested in accordance with the latest revision of JESD- 20 and table I herein. For C_{IN} and C_{PD}, test all applicable pins on five devices with zero failures.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table IA at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-PRF-38535, table IIB)	
	Device class Q	Device class V
Interim electrical parameters (see 4.2)		1
Final electrical parameters (see 4.2)	1/ 1, 2, 3, 7, 8, 9, 10, 11	2/ 3/ 1, 2, 3, 7, 8, 9, 10, 11
Group A test requirements (see 4.4)	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 2, 3	3/ 1, 2, 3, 7, 8, 9, 10, 11
Group D end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3, 7, 9
Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1, 7, and deltas.
3/ Delta limits, as specified in table IIB herein, shall be required, and the delta limits shall be completed with reference to the zero hour electrical parameters.

TABLE IIB. Burn-in and operating life test, delta parameters (+25°C).

Parameter 1/	Symbol	Delta limits
Supply current	I_{CCH}, I_{CCL}	±150 nA
Supply current delta	ΔI_{CC}	±0.4 mA
Input current low level	I_{IL}	±20 nA
Input current high level	I_{IH}	±20 nA
Output voltage low level V_{CC} = 5.5 V, I_{OL} = +24 mA	V_{OL}	±0.04 V
Output voltage high level V_{CC} = 5.5 V, I_{OH} = -24 mA	V_{OH}	±0.20 V

1/ These parameters shall be recorded before and after the required burn-in and life tests to determine the delta limits.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883, method 1019 condition A, and as specified herein.

1. Inputs tested high, V_{CC} = 5.5 V dc +5%, R_{CC} = 10Ω ±20%, V_{IN} = 5.0 V dc +5%, R_{IN} = 1 kΩ ±20%, and all outputs are open.

2. Inputs tested low, V_{CC} = 5.5 V dc +5%, R_{CC} = 10Ω ±20%, V_{IN} = 0.0 V dc, R_{IN} = 1 kΩ ±20%, and all outputs are open.

4.4.4.1.1 Accelerated annealing testing. Accelerated annealing testing shall be performed on all devices requiring a RHA level greater than 5k rads (Si). The post-anneal end-point electrical parameter limits shall be as specified in table I herein and shall be the pre-irradiation end-point electrical parameter limits at 25°C ±5°C. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.4.2 Single event phenomena (SEP). When specified in the purchase order or contract, SEP testing shall be required on class V devices. SEP testing shall be performed on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. Test 4 devices with zero failures. ASTM F1192 may be used as a guideline when performing SEP testing. The recommended test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. $0° \leq$ angle $\leq 60°$). No shadowing of the ion beam due to fixturing or package related affects is allowed.

b. The fluence shall be ≥ 100 errors or $\geq 10^7$ ions/cm^2.

c. The flux shall be between 10^2 and 10^5 ions/cm^2/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be ≥ 20 microns in silicon.

e. The test temperature shall be +25°C for the upset measurements and the maximum rated operating temperature ±10°C for the latchup measurents.

f. Bias conditions shall be V_{DD} = 4.5 V dc for the upset measurements and V_{DD} = 5.5 V dc for the latchup measurements.

g. For SEP test limits, see table IB herein.

4.5 Methods of inspection. Methods of inspection shall be specified as follows:

4.5.1 Voltage and current. Unless otherwise specified, all voltages given are referenced to the microcircuit GND terminal. Currents given are conventional current and positive when flowing into the referenced terminal.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 19-03-11

Approved sources of supply for SMD 5962-89791 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8979101QXA	3/	54ACT02K02Q
5962-8979101VXA	3/	54ACT02K02V
5962F8979101QXA	F8859	RHFACT02K02Q
5962F8979101QXC	F8859	RHFACT02K01Q
5962F8979101VXA	F8859	RHFACT02K02V
5962F8979101VYA	F8859	RHFACT02K04V
5962F8979101VXC	F8859	RHFACT02K01V
5962F8979101VYC	F8859	RHFACT02K03V

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
3/ Not available from an approved source of supply.

Vendor CAGE number	Vendor name and address
F8859	ST Microelectronics 3 rue de Suisse BP4199 35041 RENNES cedex2 - France

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.