

FEATURES

- 1.8GHz min. count frequency
- Extended 100E VEE range of -4.2V to -5.5V
- Synchronous and asynchronous enable pins
- Differential clock input and data output pins
- VBB output for single-ended use
- Asynchronous Master Reset
- Internal 75KΩ input pull-down resistors
- Available in 28-pin PLCC package

PIN NAMES

Pin	Function
CLK, $\overline{\text{CLK}}$	Differential Clock Inputs
Q0-Q7, $\overline{\text{Q0-Q7}}$	Differential Q Outputs
A_Start	Asynchronous Enable Input
EN1, EN2	Synchronous Enable Inputs
MR	Asynchronous Master Reset
VBB	Switching Reference Output
VCCO	Vcc to Output

DESCRIPTION

The SY10/100E137 are very high speed binary ripple counters. The two least significant bits were designed with very fast edge rates, while the more significant bits maintain standard ECLinPS output edge rates. This allows the counters to operate at very high frequencies, while maintaining a moderate power dissipation level.

The devices are ideally suited for multiple frequency clock generation, as well as for counters in high-performance ATE time measurement boards.

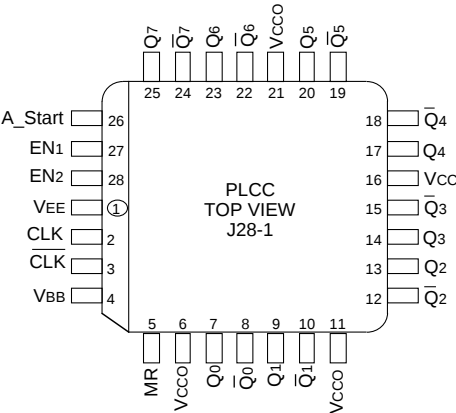
Both asynchronous and synchronous enables are available to maximize the device's flexibility for various applications. The asynchronous enable input, A_Start, when asserted, enables the counter while overriding any synchronous enable signals. The E137 features XOR'ed enable inputs, EN1 and EN2, which are synchronous to the CLK input. When only one synchronous enable is asserted, the counter becomes disabled on the next CLK transition. All outputs remain in the previous state poised for the other synchronous enable or A_Start to be asserted in order to re-enable the counter. Asserting both synchronous enables causes the counter to become enabled on the next transition of the CLK. EN1 (or EN2) and CLK edges are coincident. Sufficient delay has been inserted in the CLK path (to compensate for the XOR gate delay and the internal D-flip-flop set-up time) to ensure that the synchronous enable signal is clocked correctly; hence, the counter is disabled.

The E137 can also be driven single-endedly utilizing the VBB output supply as the voltage reference for the CLK input signal. If a single-ended signal is to be used, the VBB pin should be connected to the $\overline{\text{CLK}}$ input and bypassed to ground via a 0.01μF capacitor. VBB can only source/sink 0.5mA; therefore, it should be used as a switching reference for the E137 only.

All input pins left open will be pulled LOW via an input pull-down resistor. Therefore, do not leave the differential CLK inputs open. Doing so causes the current source transistor of the input clock gate to become saturated, thus upsetting the internal bias regulators and jeopardizing the stability of the device.

The asynchronous Master Reset resets the counter to an all zero state upon assertion.

PACKAGE/ORDERING INFORMATION



28-Pin PLCC (J28-1)

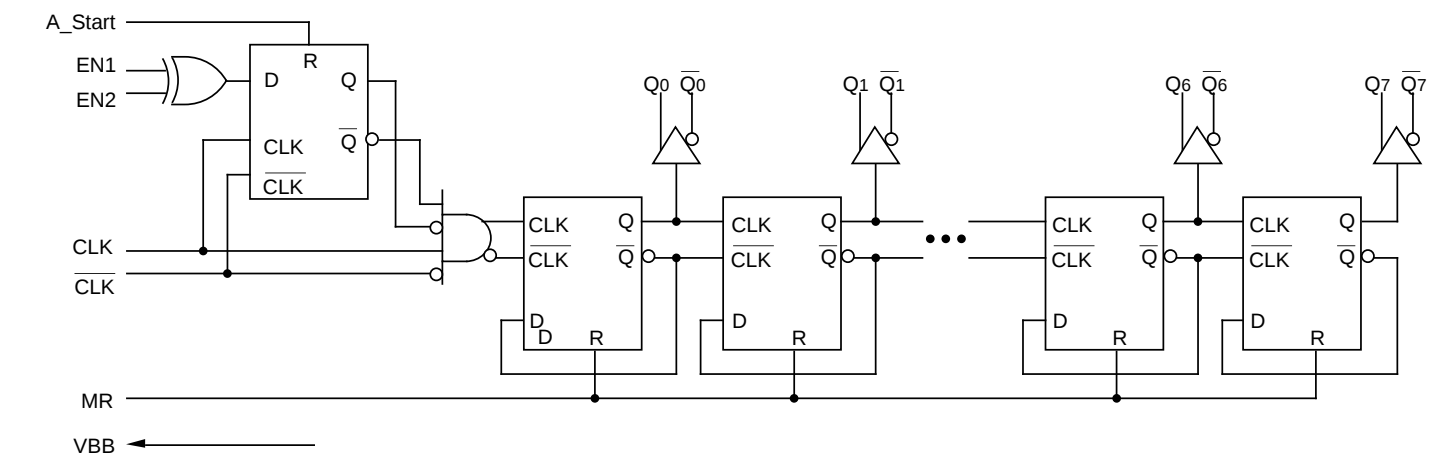
Ordering Information⁽¹⁾

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY10E137JC	J28-1	Commercial	SY10E137JC	Sn-Pb
SY10E137JCTR ⁽²⁾	J28-1	Commercial	SY10E137JC	Sn-Pb
SY100E137JC	J28-1	Commercial	SY100E137JC	Sn-Pb
SY100E137JCTR ⁽²⁾	J28-1	Commercial	SY100E137JC	Sn-Pb
SY10E137JZ ⁽³⁾	J28-1	Commercial	SY10E137JZ with Pb-Free bar-line indicator	Matte-Sn
SY10E137JZTR ^(2, 3)	J28-1	Commercial	SY10E137JZ with Pb-Free bar-line indicator	Matte-Sn
SY100E137JZ ⁽³⁾	J28-1	Commercial	SY100E137JZ with Pb-Free bar-line indicator	Matte-Sn
SY100E137JZTR ^(2, 3)	J28-1	Commercial	SY100E137JZ with Pb-Free bar-line indicator	Matte-Sn

Notes:

1. Contact factory for die availability. Dice are guaranteed at T_A = 25°C, DC Electricals only.
2. Tape and Reel.
3. Pb-Free package is recommended for new designs.

BLOCK DIAGRAM



SEQUENTIAL TRUTH TABLE⁽¹⁾

Function	EN1	EN2	A_Start	MR	CLK	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0
Reset	X	X	X	H	X	L	L	L	L	L	L	L	L
Count	L	L	L	L	Z	L	L	L	L	L	L	L	H
	L	L	L	L	Z	L	L	L	L	L	L	H	L
	L	L	L	L	Z	L	L	L	L	L	L	H	H
Stop	H	L	L	L	Z	L	L	L	L	L	L	H	H
	H	L	L	L	Z	L	L	L	L	L	L	H	H
Async. Start	H	L	H	L	Z	L	L	L	L	L	H	L	L
	H	L	H	L	Z	L	L	L	L	L	H	L	H
	L	L	H	L	Z	L	L	L	L	L	H	H	L
Count	L	L	L	L	Z	L	L	L	L	L	H	H	H
	L	L	L	L	Z	L	L	L	L	H	L	L	L
	L	L	L	L	Z	L	L	L	L	H	L	L	H
Stop	L	H	L	L	Z	L	L	L	L	H	L	L	H
	L	H	L	L	Z	L	L	L	L	H	L	L	H
Sync. Start	H	H	L	L	Z	L	L	L	L	H	L	H	L
	H	H	L	L	Z	L	L	L	L	H	L	H	H
	H	H	L	L	Z	L	L	L	L	H	H	L	L
Stop	H	L	L	L	Z	L	L	L	L	H	H	L	L
	H	L	L	L	Z	L	L	L	L	H	H	L	L
Count	L	L	L	L	Z	L	L	L	L	H	H	L	H
	L	L	L	L	Z	L	L	L	L	H	H	H	L
	L	L	L	L	Z	L	L	L	L	H	H	H	H
Reset	X	X	X	H	X	L	L	L	L	L	L	L	L

Note:

1. Z = LOW-to-HIGH transition

DC ELECTRICAL CHARACTERISTICSV_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

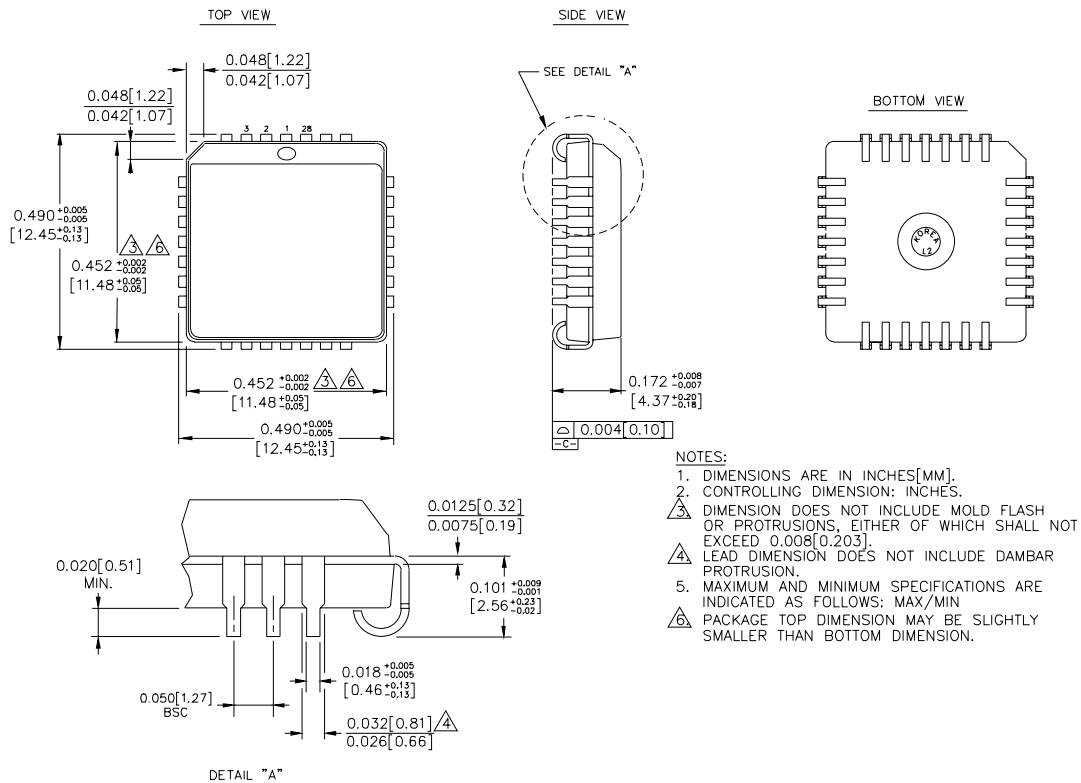
Symbol	Parameter	T _A = 0°C			T _A = +25°C			T _A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
V _{BB}	Output Reference Voltage	10E 100E	—	—	—	—	—	—	—	—	V	—
I _{IH}	Input HIGH Current	—	—	150	—	—	150	—	—	150	μA	—
I _{EE}	Power Supply Current	10E 100E	121 121	145 145	— —	121 121	145 145	— —	121 139	145 167	mA	—

AC ELECTRICAL CHARACTERISTICSV_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

Symbol	Parameter	T _A = 0°C			T _A = +25°C			T _A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
f _{COUNT}	Max. Count Frequency	1800	2200	—	1800	2200	—	1800	2200	—	MHz	—
t _{PD}	Propagation Delay to Output CLK to Q ₀ CLK to Q ₁ CLK to Q ₂ CLK to Q ₃ CLK to Q ₄ CLK to Q ₅ CLK to Q ₆ CLK to Q ₇ A_Start to Q ₀ MR to Q ₀	1300 1600 1950 2275 2625 2950 3250 3575 950 700	1700 2025 2425 2750 3125 3450 3775 4075 1325 1000	2150 2500 2925 3350 3750 4150 4450 4800 1700 1300	1300 1600 1950 2275 2625 2950 3250 3575 950 700	1700 2050 2450 2775 3150 3475 3800 4125 1325 1000	2150 2500 2925 3350 3750 4150 4450 4800 1700 1300	1350 1650 2025 2350 2700 3050 3375 3700 950 700	1750 2100 2500 2850 3225 3550 3925 4250 1325 1000	2200 2550 3000 3425 3625 4250 4600 4950 1700 1300	ps	—
t _s	Set-up Time (EN ₁ , EN ₂)	0	—150	—	0	—150	—	0	—150	—	ps	—
t _H	Hold Time (EN ₁ , EN ₂)	300	150	—	300	150	—	300	150	—	ps	—
t _{RR}	Reset Recovery Time MR, A_Start	400	200	—	400	200	—	400	200	—	ps	—
t _{PW}	Minimum Pulse Width CLK, MR, A_Start	400	—	—	400	—	—	400	—	—	ps	—
V _{PP}	Minimum Input Swing (CLK)	0.25	—	1.0	0.25	—	1.0	0.25	—	1.0	V	1
V _{CMR}	Com. Mode Range (CLK)	—0.4	—	—2.0	—0.4	—	—2.0	—0.4	—	—2.0	V	—
t _r t _f	Rise/Fall Time, 20% to 80% Q ₀ , Q ₁ Q ₂ –Q ₇	150 275	— —	400 600	150 275	— —	400 600	150 275	— —	400 600	ps	—

Note:

1. Minimum input swing for which AC parameters are guaranteed. Full DC ECL output swings will be generated with only 50mV input swings.

28-PIN PLCC (J28-1)

Rev. 03

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