

The documentation and process conversion measures necessary to comply with this revision shall be completed by 17 December 2015.

INCH-POUND

MIL-PRF-19500/754A
17 September 2015
SUPERSEDING
MIL-PRF-19500/754
13 August 2009

PERFORMANCE SPECIFICATION SHEET

* SEMICONDUCTOR DEVICE, DIODE, SILICON, SCHOTTKY, DUAL, COMMON CATHODE, TYPE 1N7064CCU3 and 1N7064CCU3C, JAN, JANTX, JANTXV, AND JANS

This specification is approved for use by all Departments and Agencies of the Department of Defense.

The requirements for acquiring the product described herein shall consist of this specification sheet and [MIL-PRF-19500](#).

1. SCOPE

- * 1.1 Scope. This specification covers the performance requirements for silicon, Schottky center tap power rectifier diodes for use in high frequency switching power supplies and resonant power converters. Four levels of product assurance (JAN, JANTX, JANTXV, and JANS) are provided for each device type.
- * 1.2 Package outlines. The device package outlines are as follows: U3 and U3C (ceramic lid) package in accordance with [figure 1](#) for all encapsulated device types.

1.3 Maximum ratings. Unless otherwise specified, $T_A = +25^\circ\text{C}$.

Column 1	Column 2	Column 3	Column 4	Column 5		Column 6
Types	V _{RWM}	I _O (1)(2) $T_C = +100^\circ\text{C}$	I _{FSM} (3) $t_p = 8.3 \text{ ms}$ $T_C = +25^\circ\text{C}$	$R_{\Theta JC}$ (2)	$R_{\Theta JC}$ (3)	T_{STG} and T_J
	V dc	A dc	A (pk)	°C/W	°C/W	°C
1N7064CCU3 1N7064CCU3C	45	30	85	1.75	3.5	-65 to +150

- (1) See temperature-current derating curves on [figure 2](#).
- (2) Entire package.
- (3) Each leg.

1.4 Primary electrical characteristics. $R_{\Theta JC} = 1.75^\circ\text{C}/\text{W}$ maximum entire package; $R_{\Theta JC} = 3.5^\circ\text{C}/\text{W}$ maximum each leg ([figure 3](#)).

* Comments, suggestions, or questions on this document should be addressed to DLA Land and Maritime, ATTN: VAC, P.O. Box 3990, Columbus, OH 43218-3990, or emailed to Semiconductor@dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at <https://assist.dla.mil>.



- * 1.5 Part or Identifying Number (PIN). The PIN is in accordance with [MIL-PRF-19500](#), and as specified herein. See [6.4](#) for PIN construction example and [6.5](#) for a list of available PINs.
- * 1.5.1 JAN certification mark and quality level for encapsulated devices. The quality level designators for encapsulated devices that are applicable for this specification sheet from the lowest to the highest level are as follows: "JAN", "JANTX", "JANTXV" and "JANS".
- * 1.5.2 Device type. The designation system for the device types of diodes covered by this specification sheet are as follows.
- * 1.5.2.1 First number and first letter symbols. The diodes of this specification sheet use the first number and letter symbols "1N".
- * 1.5.2.2 Second number symbols. The second number symbols for the diodes covered by this specification sheet are as follows: "7064CC".
- * 1.5.2.3 Suffix letters. The suffix letters "U3" and "U3C" are used on devices that are packaged in the package of [figure 1](#).
- * 1.5.3 Lead finish. The lead finishes applicable to this specification sheet are listed on [QPDSIS-19500](#).

2. APPLICABLE DOCUMENTS

- * 2.1 General. The documents listed in this section are specified in sections 3 and 4 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3 and 4 of this specification, whether or not they are listed.

2.2 Government documents.

- 2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

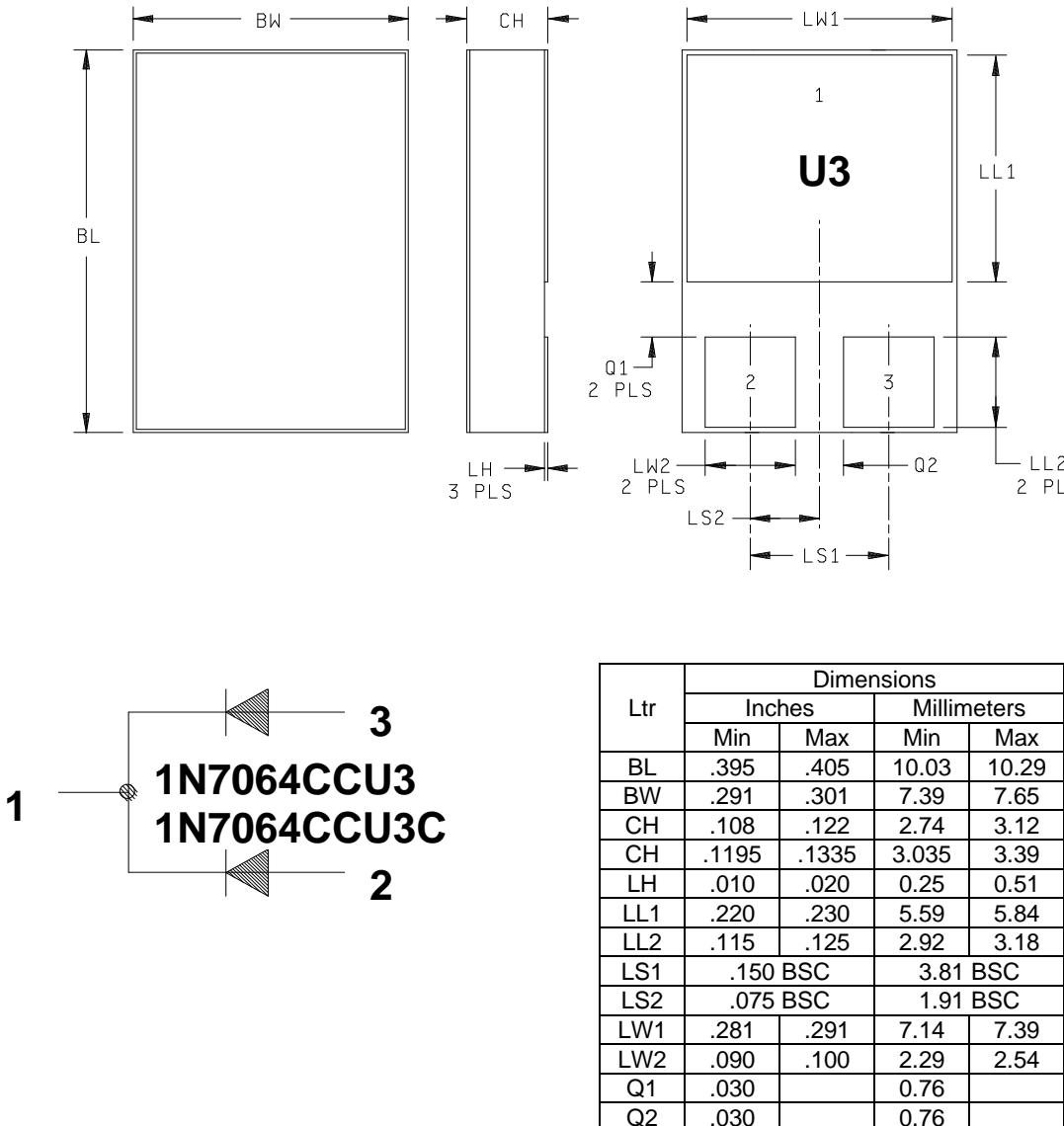
[MIL-PRF-19500](#) - Semiconductor Devices, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

[MIL-STD-750](#) - Test Methods for Semiconductor Devices.

- * (Copies of these documents are available online at <http://quicksearch.dla.mil/>).

- 2.3 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.



NOTES:

1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. In accordance with ASME Y14.5M, diameters are equivalent to Φx symbology.

FIGURE 1. Dimensions and configuration, 1N7064CCU3 and 1N7064CCU3C.

3. REQUIREMENTS

3.1 General. The individual item requirements shall be as specified in [MIL-PRF-19500](#) and as modified herein.

3.2 Qualification. Devices furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturer's list (QML) before contract award (see [4.2](#) and [6.3](#)).

3.3 Abbreviations, symbols, and definitions. Abbreviations, symbols, and definitions used herein shall be as specified in [MIL-PRF-19500](#).

3.4 Interface and physical dimensions. The interface and physical dimensions shall be as specified in [MIL-PRF-19500](#), and on [figure 1](#) herein.

3.4.1 Polarity. Polarity and terminal configuration shall be in accordance with [figure 1](#) herein.

3.4.2 Lead finish. Lead finish shall be solderable in accordance with [MIL-PRF-19500](#), [MIL-STD-750](#), and herein. Where a choice of finish is desired, it shall be specified in the acquisition document (see [6.2](#)).

3.5 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in [1.3](#), [1.4](#), and [table I](#) herein.

3.6 Electrical test requirements. The electrical test requirements shall be as specified in tables I and II herein.

3.7 Marking. Marking shall be in accordance with [MIL-PRF-19500](#) and herein.

3.8 Workmanship. Semiconductor devices shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.

4. VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

- a. Qualification inspection (see [4.2](#)).
- b. Screening (see [4.3](#)).
- c. Conformance inspection (see [4.4](#) and [tables I](#) and [II](#) herein).

4.2 Qualification inspection. Qualification inspection shall be in accordance with [MIL-PRF-19500](#) and as specified herein.

4.2.1 Group E qualification. Group E inspection shall be performed for qualification or re-qualification only. In case qualification was awarded to a prior revision of the specification sheet that did not request the performance of [table III](#) tests, the tests specified in [table III](#) herein that were not performed in the prior revision shall be performed on the first inspection lot of this revision to maintain qualification.

4.3 Screening (JANS, JANTXV, and JANTX levels). Screening shall be in accordance with table E-IV of [MIL-PRF-19500](#) and as specified herein. The following measurements shall be made in accordance with [table I](#) herein. Devices that exceed the limits of [table I](#) herein shall not be acceptable.

Screen (table E-IV of MIL-PRF-19500)	Measurement	
	JANS level	JANTX and JANTXV levels
3b	Method 4066 of MIL-STD-750 , condition A, one pulse, $t_p = 8.3$ ms, $I_O = 0$, $V_{RWM} = 0$, $I_{FSM} = \text{see 1.3 herein}$.	Method 4066 of MIL-STD-750 , condition A, one pulse, $t_p = 8.3$ ms, $I_O = 0$, $V_{RWM} = 0$, $I_{FSM} = \text{see 1.3 herein}$.
3c	Thermal impedance (see 4.3.2).	Thermal impedance (see 4.3.2).
3d	Avalanche energy test (see 4.3.3).	Avalanche energy test (see 4.3.3).
9, 10	Not applicable.	Not applicable.
11	V_{F1} and I_{R1} .	V_{F1} and I_{R1} .
12	See 4.3.1 .	See 4.3.1 .
13	Subgroups 2 and 3, of table I herein, V_{F1} and I_{R1} ; $\Delta V_{F2} = \pm 50$ mV (pk); $\Delta I_{R1} = \pm 100$ percent from the initial value or ± 10 uA, whichever is greater.	Subgroup 2, of table I herein; V_{F1} and I_{R1} ; $\Delta V_{F2} = \pm 50$ mV (pk); $\Delta I_{R1} = \pm 100$ percent from the initial value or ± 10 uA, whichever is greater.

4.3.1 High temperature reverse bias. Reverse bias conditions are as follows: Method 1038 of [MIL-STD-750](#), test condition A, $V_R = 36$ V dc; $T_J = +125^\circ\text{C}$.

4.3.2 Thermal impedance. The thermal impedance measurements shall be performed in accordance with method 3101 of [MIL-STD-750](#) using the guidelines in that method for determining I_M , I_H , t_H , and t_{MD} . Measurement delay time (t_{MD}) = 70 μs max. See [table III](#), subgroup 4, and [figure 3](#) herein.

4.3.3 Avalanche energy test. The avalanche energy test is to be performed in accordance with method 4064 of [MIL-STD-750](#) using the circuit as shown on [figure 4](#) or equivalent. The Schottky rectifier under test must be capable of absorbing the reverse energy, as follows: $I_{AS} = 1\text{A}$, $V_{br} = 45$ V minimum, $L = 100$ μH .

4.4 Conformance inspection. Conformance inspection shall be in accordance with [MIL-PRF-19500](#).

4.4.1 Group A inspection. Group A inspection shall be conducted in accordance with table E-V of [MIL-PRF-19500](#), and [table I](#) herein. Electrical measurements (end-points) and delta requirements shall be in accordance with the applicable steps of [table II](#) herein.

4.4.2 Group B inspection. Group B inspection shall be conducted in accordance with the conditions specified for subgroup testing in tables E-VIA (JANS) and E-VIB (JAN, JANTX, and JANTXV) of [MIL-PRF-19500](#) and as follows. Electrical measurements (end-points) shall be in accordance with [table I](#), subgroup 2, forward voltage test (V_F) and reverse leakage test (I_R) herein. Delta measurements shall be in accordance with [table II](#) herein.

- * 4.4.2.1 Quality level JANS, table E-VIA of [MIL-PRF-19500](#).

<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
B4	1037	$\Delta T_C = +85^\circ\text{C}$, $I_F = 2 \text{ A}$ minimum.
B5	1038	Condition A, $V_R = 36 \text{ V dc}$, $T_J = +125^\circ\text{C}$, $t = 340 \text{ hours min}$; heat sinking allowed. This test shall be extended to 1,000 hours for each wafer lot.

- * 4.4.2.2 Quality levels JAN, JANTX and JANTXV, table E-VIB (JAN, JANTX, and JANTXV) of [MIL-PRF-19500](#).

<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
B3	1037	$\Delta T_C = +85^\circ\text{C}$, $I_F = 2 \text{ A}$ minimum.

4.4.3 Group C inspection. Group C inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VII of [MIL-PRF-19500](#). Electrical measurements (end-points) shall be in accordance with [table I](#), subgroup 2, forward voltage test (V_F) and reverse leakage test (I_R) herein. Delta measurements shall be in accordance with [table II](#) herein.

<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
C2	2036	Not required.
C5	4081	Limit for thermal resistance is $3.5^\circ\text{C}/\text{W}$ for each diode.
*	C6	$\Delta T_C = +85^\circ\text{C}$, $I_F = 2 \text{ A}$ minimum.
C6	1038	Condition A, $V_R = 36 \text{ V dc}$, $T_J = +125^\circ\text{C}$, $t = 1,000 \text{ hours min}$; heat sinking allowed. (for TX and TXV only).

4.4.4 Group E inspection. Group E inspection shall be conducted in accordance with the tests and conditions specified for subgroup testing in table E-IX of [MIL-PRF-19500](#), and [table III](#) herein. Delta measurements shall be in accordance with [table II](#) herein.

4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables as follows.

4.5.1 Pulse measurements. Conditions for pulse measurement shall be as specified in section 4 of [MIL-STD-750](#).

*

TABLE I. Group A inspection.

Inspection 1/	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 1</u>						
Visual and mechanical examination	2071					
<u>Subgroup 2</u>						
Forward voltage	4011	Pulsed test (see 4.5.1), condition B, $I_F = 10 \text{ A (pk)}$	V_{F1}		0.68	V dc
Forward voltage	4011	Pulsed test (see 4.5.1), condition B, $I_F = 15 \text{ A (pk)}$	V_{F2}		0.80	V dc
Forward voltage	4011	Pulsed test (see 4.5.1), condition B, $I_F = 30 \text{ A (pk)}$	V_{F3}		1.09	V dc
Reverse current	4016	DC method; $V_R = 45 \text{ V}$	I_{R1}		0.08	mA dc
<u>Subgroup 3</u>						
High temperature operation:		$T_C = +125 \text{ }^\circ\text{C}$				
Forward voltage	4011	Pulsed test (see 4.5.1), condition B, $I_F = 10 \text{ A (pk)}$	V_{F4}		0.62	V dc
Forward voltage	4011	Pulsed test (see 4.5.1), condition B, $I_F = 15 \text{ A (pk)}$	V_{F5}		0.72	V dc
Forward voltage	4011	Pulsed test (see 4.5.1), condition B, $I_F = 30 \text{ A (pk)}$	V_{F6}		0.95	V dc
Reverse current	4016	DC method; $V_R = 45 \text{ V}$	I_{R2}		10.0	mA dc
Low temperature operation:		$T_C = -55 \text{ }^\circ\text{C}$				
Forward voltage	4011	Pulsed test (see 4.5.1), condition B, $I_F = 10 \text{ A (pk)}$	V_{F7}		0.72	V dc
Forward voltage	4011	Pulsed test (see 4.5.1), condition B, $I_F = 15 \text{ A (pk)}$	V_{F8}		0.81	V dc
Forward voltage	4011	Pulsed test (see 4.5.1), condition B, $I_F = 30 \text{ A (pk)}$	V_{F9}		1.09	V dc

See footnotes at end of table.

* TABLE I. Group A inspection - Continued.

Inspection 1/	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 4</u> Junction capacitance	4001	$V_R = 5 \text{ V dc}$, $f = 1 \text{ MHz}$, $V_{SIG} = 50 \text{ mV (p-p)}$	CJ		375	pF
<u>Subgroup 5</u> Not applicable						
<u>Subgroup 6</u> Surge	4066	See 1.3, column 4 herein, ten surges each diode. 60 seconds between surges, (see 4.5.1)				
Electrical measurements		See table I, subgroup 2 herein				
<u>Subgroup 7</u> Dielectric withstanding voltage 3/	1016	$V_R = 500 \text{ V dc}$; all leads shorted; measure from leads to case	DWV		10	μA
Scope display evaluation	4023	Stable only				
Electrical measurements		See table I, subgroup 2 herein				

1/ For sampling plan, see [MIL-PRF-19500](#).

2/ Electrical characteristics apply to all package styles and polarities.

3/ Not required for 1N7064CCU3C

TABLE II. Groups B, C, and E delta requirements. 1/ 2/ 3/ 4/ 5/ 6/

Step	Inspection	MIL-STD-750		Symbol	Limits		Unit	
		Method	Conditions		Min	Max		
1.	Forward voltage	4011	Condition B, $I_F = 15 \text{ A (pk)}$ pulsed (see 4.5.1)	ΔV_{F2}	$\pm 50 \text{ mV dc}$ from initial reading.			
2.	Reverse current	4016	$V_R = 45 \text{ V}_{dc}$	ΔI_{R1}	± 100 percent from initial reading or $\pm 10 \mu\text{A}$ whichever is greater.			
3.	Thermal impedance	3101	See 4.3.2	$Z_{\Theta JX}$				

1/ Each individual diode.

2/ The delta measurements for table E-VIA (JANS) of **MIL-PRF-19500** are as follows:

- a. Subgroup 4, see [table II](#) herein, steps 1, 2, and 3.
- b. Subgroup 5, see [table II](#) herein, steps 1 and 2.

3/ The delta measurements for table E-VIB (JAN, JANTX and JANTXV) of **MIL-PRF-19500** are as follows:

- a. Subgroup 2, see [table II](#) herein, steps 1, 2, and 3.
- b. Subgroup 3, see [table II](#) herein, steps 1, 2, and 3.
- c. Subgroup 6, see [table II](#) herein, steps 1 and 2.

4/ The delta measurements for table E-VII of **MIL-PRF-19500** are as follows:

- a. Subgroups 2 and 3, see [table II](#) herein, steps 1, 2, and 3 for all levels.
- b. Subgroup 6, see [table II](#) herein, steps 1, 2, and 3 for all levels.

5/ Devices which exceed the [table I](#) limits for this test shall not be accepted.6/ The delta measurements for table E-IX of **MIL-PRF-19500** are as follows:

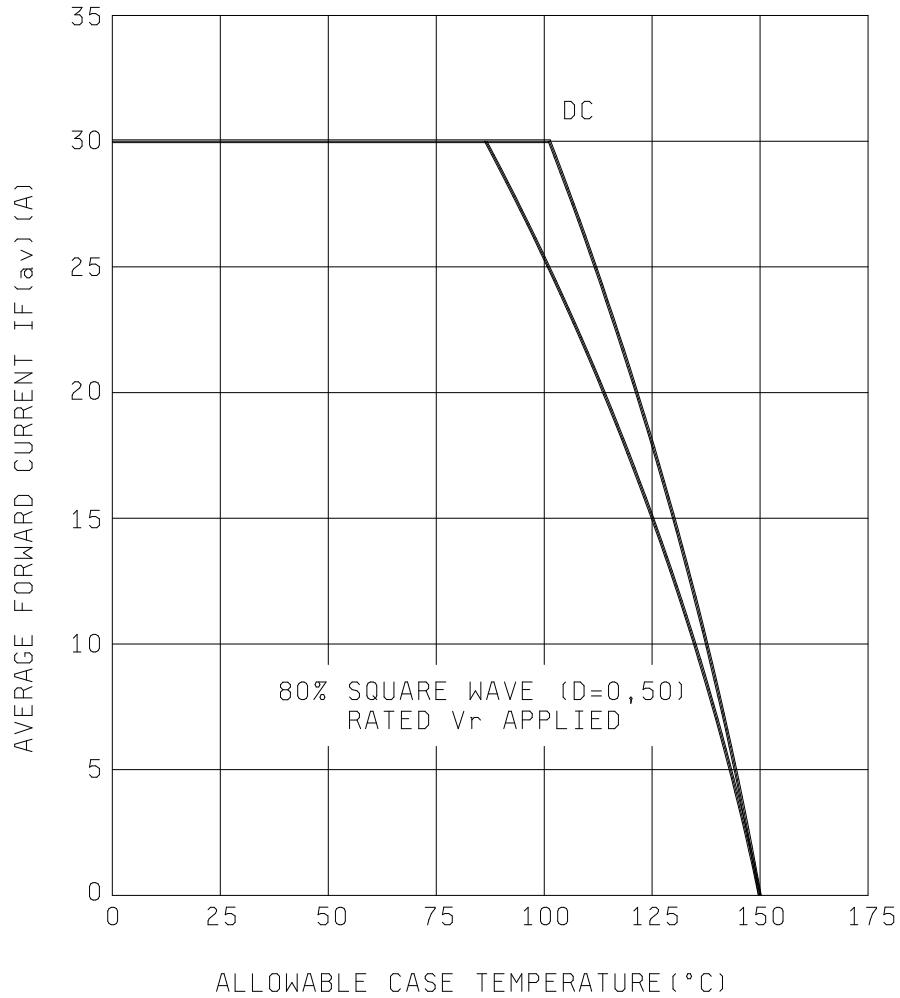
- a. Subgroup 1, see [table III](#) herein, steps 1, 2, and 3.
- b. Subgroup 2, see [table III](#) herein, steps 1 and 2.

* TABLE III. Group E inspection (all quality levels) – for qualification and requalification only.

Inspection	MIL-STD-750		Qualification
	Method	Conditions	
<u>Subgroup 1</u> Temperature cycling (air to air) Hermetic seal Electrical measurements	1051	Test condition G, 500 cycles, -55°C to +150°C. See table I , subgroup 2 and table II herein.	45 devices, c = 0
			45 devices, c = 0
<u>Subgroup 2</u> Life test Electrical measurements	1048	t = 1,000 hours, $T_J = +125^\circ\text{C}$, $V_R = 80\%$ rated voltage (see 1.3 , column 2 herein). See table I subgroup 2 and table II herein.	5 devices, c = 0
<u>Subgroup 4</u> Thermal impedance curves		See MIL-PRF-19500 .	5 devices, c = 0
<u>Subgroup 10 1/</u> Surge Electrical measurements	4066	Condition A, $T_A = +25^\circ\text{C}$, $I_{FSM} = 85\text{ A}$, 100 surges of 8.3 ms half sine wave. $V_R = 0$; $I_O = 0\text{ A}$ pk. See table I subgroup 2 (V_F and I_R only).	5 devices, c = 0

1/ Each individual diode.

TEMPERATURE-CURRENT DERATING CURVE
1N7064CCU3 and 1N7064CCU3C



Switch mode operation, 80 percent duty cycle: T_C ($^{\circ}\text{C}$) (case).

$R_{\Theta JC} = 1.75$ $^{\circ}\text{C}/\text{W}$.

NOTES:

1. All devices are capable of operating at $\leq T_J$ specified on this curve. Any parallel line to this curve will intersect the appropriate current for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperature ($T_J \leq 150^{\circ}\text{C}$) and current rating specified. (See 1.3 herein.)
3. Derate design curve chosen at $T_J \leq 125^{\circ}\text{C}$, where the maximum temperature of electrical test is performed.
4. Derate design curves chosen at $T_J \leq 125^{\circ}\text{C}$, and 110°C to show current rating where most users want to limit T_J in their application.

FIGURE 2. Temperature-current derating curve (per package) for 1N7064CCU3 and 1N7064CCU3C.

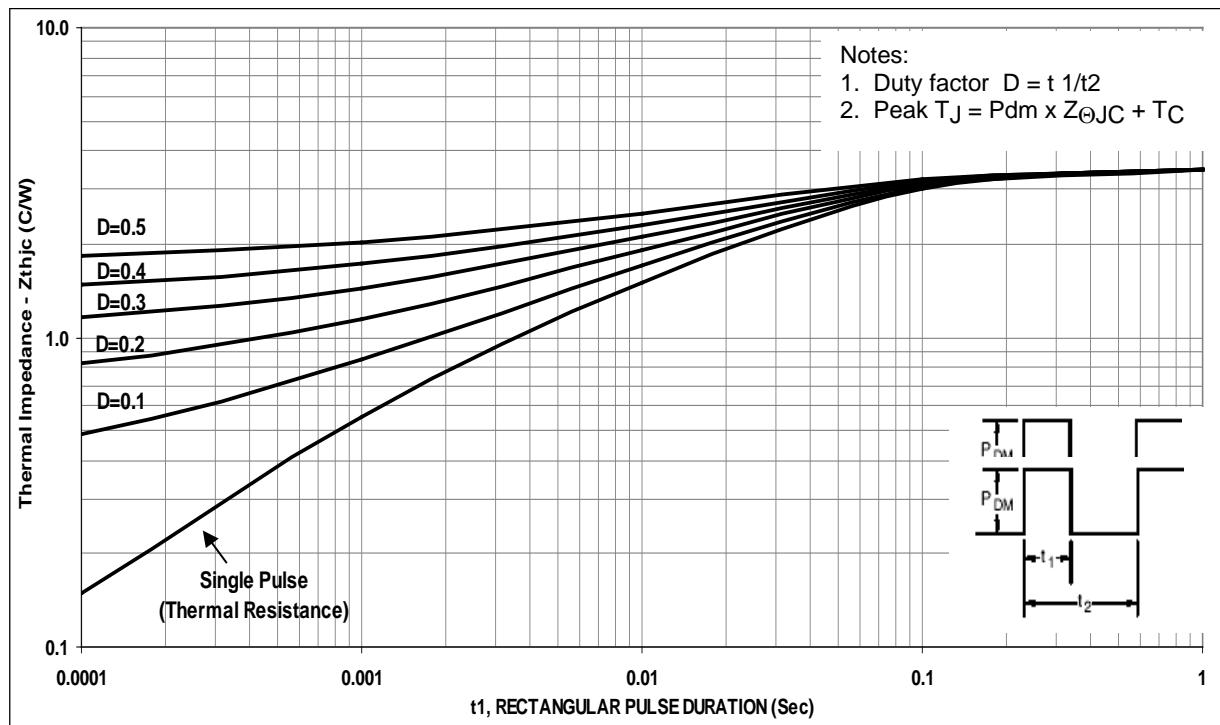
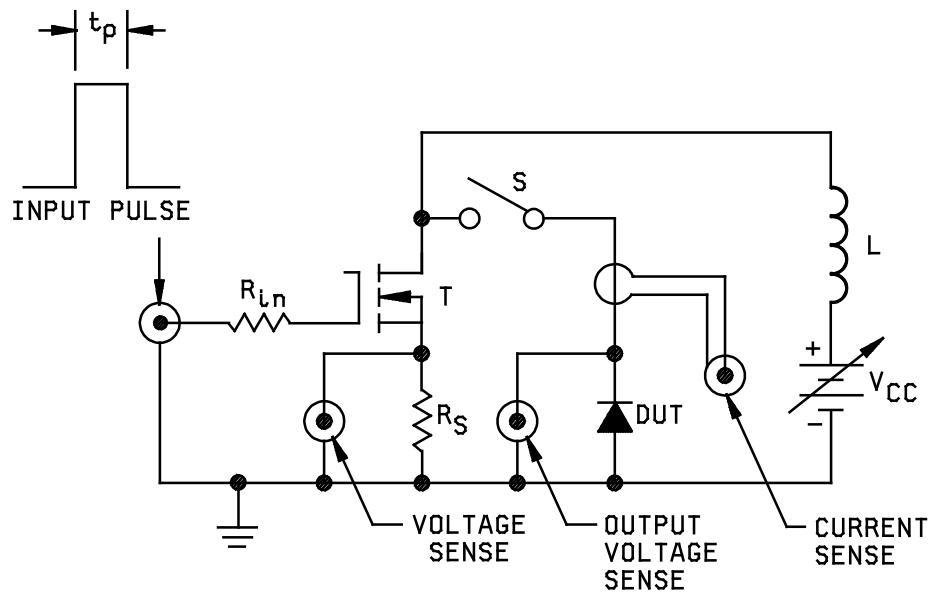


FIGURE 3. Thermal impedance (for each leg), 1N7064CCU3 and 1N7064CCU3C.



Input pulse $R_{in} = 50$ ohms
 $V_G = 10$ Volts, $R_S = 0.1$ ohms
 $Z_G = 50$ ohms
 $L = 100 \mu\text{H}$
 Duty cycle ≤ 1 percent, $T = \text{IRF350/2N6768 or equivalent}$

Procedure:

1. With S open, adjust pulse width to test current of 1 amp through R_S .
2. Close S , verify test current with current sense.
3. Read peak output voltage (see 4.3.3).

FIGURE 4. Avalanche energy test circuit.

5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory. The notes specified in [MIL-PRF-19500](#) are applicable to this specification.)

6.1 Intended use. Semiconductors conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

6.2 Acquisition requirements. Acquisition documents should specify the following:

- a. Title, number, and date of this specification.
- b. Packaging requirements (see 5.1).
- c. Lead material, finish, and formation (see 3.4.2).

* d. The complete PIN, see 1.5 and 6.5.

* 6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List ([QML 19500](#)) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DLA Land and Maritime, ATTN: VQE, P.O. Box 3990, Columbus, OH 43218-3990 or e-mail vqe.chief@dla.mil. An online listing of products qualified to this specification may be found in the Qualified Products Database (QPD) at <https://assist.dla.mil>.

* 6.4 PIN construction example.

* 6.4.1 Encapsulated devices The PINs for encapsulated devices are constructed using the following form.

<u>JANTXV</u>	<u>1N</u>	<u>7064CC</u>	<u>U3</u>
JAN certification mark and quality level (see 1.5.1)			
First number and first letter symbols (see 1.5.2.1)			
Second number symbols (see 1.5.2.2)			
First suffix symbol (see 1.5.2.3)			

- * 6.5 List of PINs.
- * 6.5.1 List of PINs for encapsulated devices. The following is a list of possible PINs for encapsulated devices available on this specification sheet.

PINs for devices of the base quality level	PINs for devices of the "TX" quality level	PINs for devices of the "TXV" quality level	PINs for devices of the "S" quality level
JAN1N7064CCU3	JANTX1N7064CCU3	JANTXV1N7064CCU3	JANS1N7064CCU3
JAN1N7064CCU3C	JANTX1N7064CCU3C	JANTXV1N7064CCU3C	JANS1N7064CCU3C

6.6 Cross reference substitution list. A PIN for PIN replacement table follows, and these devices are directly interchangeable.

Non-preferred PIN	Preferred PIN
30CLJQ045	JANS, JANTXV, JANTX, JAN1N7064CCU3
30CLJCQ045	JANS, JANTXV, JANTX, JAN1N7064CCU3C

6.7 Changes from previous issue. The margins of this specification are marked with asterisks to indicate where changes from the previous issue were made. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the last previous issue.

Custodians:
 Army - CR
 Navy - EC
 Air Force - 85
 NASA - NA
 DLA - CC

Preparing activity:
 DLA - CC
 (Project 5961-2015-090)

- * NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at <https://assist.dla.mil>.