15W STEREO CLASS-D AUDIO POWER AMPLIFIER WITH POWER LIMIT

Description

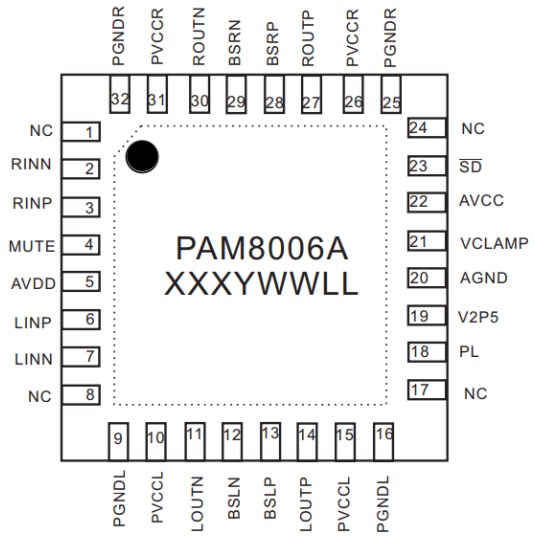
The PAM8006A is a 15W (per channel) stereo Class-D audio amplifier which offers low THD+N (0.2%), low EMI and good PSRR thus high-quality sound reproduction.

The PAM8006A runs off an 8V to 18V supply at much higher efficiency than competitors' ICs.

The PAM8006A only requires very few external components, significantly saving cost and board space.

The PAM8006A is available in a W-QFN5050-32 (Standard) package.

Pin Assignments



Top View of W-QFN5050-32 (Standard)

Features

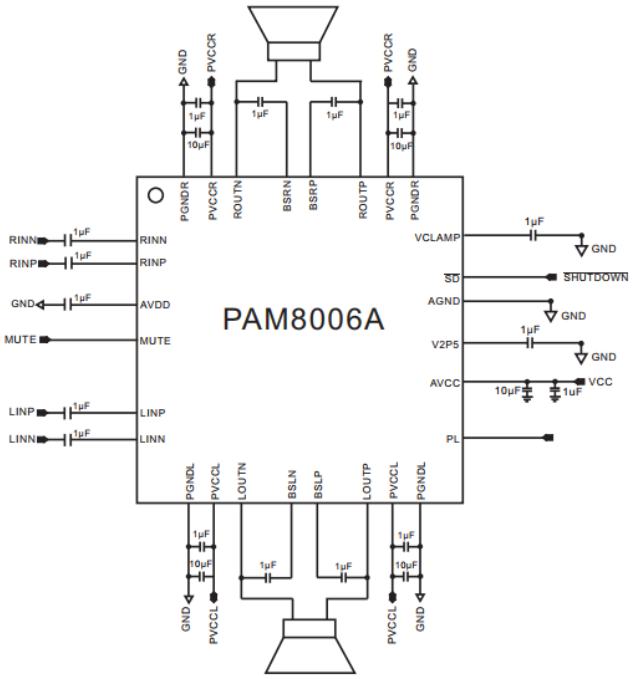
- 15W x2 into an 8Ω Speaker
- Low Noise: -90dB
- Over 90% Efficiency
- With Shutdown/Mute Function
- Overcurrent, OVP, UVLO, Thermal and Short-Circuit Protection
- Low THD+N
- Power Limit with Non-Clip
- Low Quiescent Current
- Pop Noise Suppression
- Small Package Outlines: W-QFN5050-32 (Standard)
- Pb-Free Package (RoHS Compliant)
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/104/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative. https://www.diodes.com/quality/product-definitions/**

Applications

- Flat monitors/LCD TVs
- Multi-media speaker systems
- DVD players, game machines
- Boom boxes
- Music instruments

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

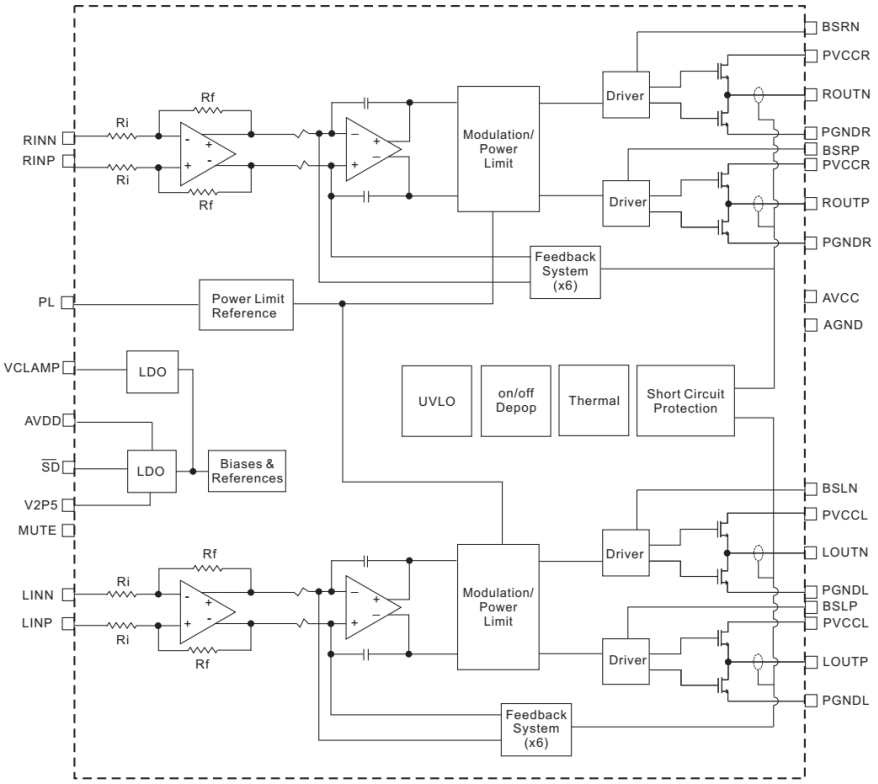
Typical Applications Circuit



Pin Descriptions

Pin Number	Pin Name	Function
1, 8, 17, 24	NC	Not Connected
2	RINN	Negative Differential Audio Input for Right Channel.
3	RINP	Positive Differential Audio Input for Right Channel.
4	MUTE	A logic high on this pin disables the outputs and a logic low enables the outputs.
5	AVDD	5V Analog Supply
6	LINP	Positive Differential Audio Input for Left Channel.
7	LINN	Negative Differential Audio Input for Left Channel.
9, 16	PGNDL	Power Ground for Left Channel H-Bridge.
10, 15	PVCCL	Power Supply for Left Channel H-Bridge, Not Connected to PVCCR or AVCC.
11	LOUTN	Class-D 1/2-H-Bridge Negative Output for Left Channel.
12	BSLN	Bootstrap I/O for Left Channel, Negative High-Side FET.
13	BSLP	Bootstrap I/O for Left Channel, Positive High-Side FET.
14	LOUTP	Class-D 1/2-H-Bridge Positive Output for Left Channel.
18	PL	Reference Voltage for Power Limit Function.
19	V2P5	2.5V Reference for Analog Cells.
20	AGND	Analog Ground
21	VCLAMP	Internally Generated Voltage Supply for Bootstrap Capacitors.
22	AVCC	High-Voltage Analog Power Supply (8V to 18V)
23	$\overline{SD}$	Shutdown Signal for IC (low = shutdown, high = operational). TTL logic levels with compliance to V_{CC}.
25, 32	PGNDR	Power Ground for Right Channel H-Bridge.
26, 31	PVCCR	Power Supply for Right Channel H-Bridge, Not Connected to PVCCL or AVCC.
27	ROUTP	Class-D 1/2-H-Bridge Positive Output for Right Channel.
28	BSRP	Bootstrap I/O for Right Channel, Positive High-Side FET.
29	BSRN	Bootstrap I/O for Right Channel, Negative High-Side FET.
30	ROUTN	Class-D 1/2-H-Bridge Negative Output for Right Channel.
33	Thermal Pad	Connect to Ground. Thermal pad should be soldered down on all applications to secure the device properly to the printed wiring board.

Functional Block Diagram



Note: 4. Maximum gain: R_I = 12.5k, R_F = 100k.
Power limit function: R_I and R_F are adjustable.

Absolute Maximum Ratings (@T_A = +25°C, unless otherwise specified.) (Note 5)

Parameter	Rating	Unit
Supply Voltage V_{CC}	-0.3 to +28.0	V
Input Voltage Range V_I		
MUTE, PL	0 to 6.0	V
$\overline{SD}$	-0.3 to V_{CC}	V
RINN, RINP, LINN, LINP	-0.3 to +6.0	V
Junction Temperature Range, T_J	-40 to +125	°C
Storage Temperature	-65 to +150	°C
Lead Temperature	+260 (5 sec)	°C

Note: 5. Stresses greater than those listed under *Absolute Maximum Ratings* can cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to *Absolute Maximum Ratings* for extended periods can affect device reliability. All voltages are with respect to ground.

Recommended Operating Conditions (@T_A = +25°C, unless otherwise specified.)

Parameter		Rating	Unit
Supply Voltage V_{CC}		8 to 18	V
Input Pin Voltage		0 to 5.5	V
High-Level Input Voltage	$\overline{SD}$	2.0 to V_{CC}	V
	MUTE	2.0 to 5.5	V
Low-Level Input Voltage	$\overline{SD}$	0 to 0.3	V
	MUTE	0 to 0.3	V
Ambient Operating Temperature		-20 to +85	°C

Thermal Information (Note 6)

Parameter	Package	Symbol	Maximum	Unit
Thermal Resistance (Junction to Case)	W-QFN5050-32 (Standard)	θ_{JC}	5.0	°C/W
Thermal Resistance (Junction to Ambient)	W-QFN5050-32 (Standard)	θ_{JA}	16.1	

Note: 6. The exposed PAD must be soldered to a thermal land on the PCB.

Electrical Characteristics (@T_A = +25°C, V_{CC} = 12V, R_L = 8Ω, unless otherwise specified.)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
P_O	Continuous Output Power	THD+N = 0.12%, f = 1kHz, R_L = 8Ω		—	6	—	W
		THD+N = 1%, f = 1kHz, R_L = 8Ω		—	8.5	—	
		THD+N = 10%, f = 1kHz, R_L = 8Ω		—	10	—	
I_{DD}	Quiescent Current	No Load		—	16.5	25	mA
I_{SD}	Supply Quiescent Current in Shutdown Mode	Shutdown = 0		—	4	10	μA
$R_{DS(ON)}$	Drain-Source On-State Resistance	I_O = 0.5A, T_J = +25°C	High Side	—	210	—	mΩ
			Low Side	—	210	—	
			Total	—	420	—	
PSRR	Power Supply Ripple Rejection Ratio	$1V_{PP}$ Ripple, f = 1kHz, Inputs AC-Coupled to Ground		—	-65	—	dB
f_{OSC}	Oscillator Frequency	—		—	300	—	kHz
Vn	Output Integrated Noise Floor	20Hz to 22kHz, A-Weighting		—	-100	—	dB
CS	Crosstalk	P_O = 3W, R_L = 8Ω, f = 1kHz		—	-95	—	dB
SNR	Signal to Noise Ratio	Maximum Output at THD+N < 0.5%, f = 1kHz		—	90	—	dB
—	Gain	—		—	32	—	dB
$\lvert V_{OS} \rvert$	Output Offset Voltage (measured differentially)	INN and INP Connected Together		—	30	—	mV
V2P5	2.5V Bias Voltage	No Load		—	2.5	—	V
AVDD	Internal Analog Supply Voltage	V_{CC} = 8V to 18V		—	5	5.5	V
OTS	Overtemperature Shutdown	—		—	+160	—	°C
OTH	Thermal Hysteresis	—		—	+50	—	°C

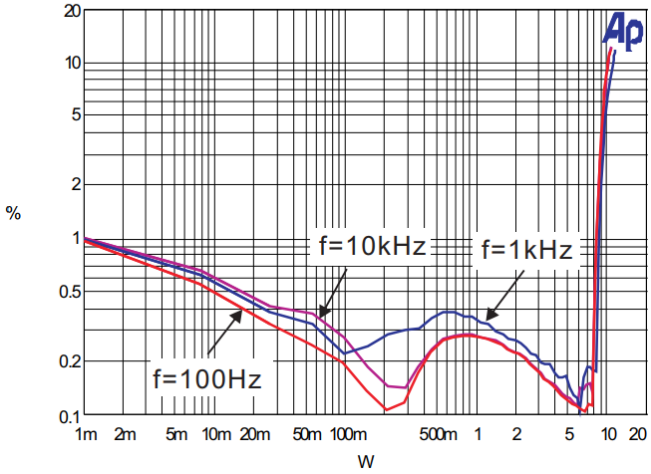
Electrical Characteristics (@T_A = +25°C, V_{CC} = 18V, R_L = 8Ω, unless otherwise specified.)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
P_O	Continuous Output Power	THD+N = 0.12%, f = 1kHz, R_L = 8Ω		—	2.2	—	W
		THD+N = 0.18%, f = 1kHz, R_L = 8Ω		—	15	—	
THD+N	Total Harmonic Distortion plus Noise	P_O = 10W, f = 1kHz, R_L = 8Ω		—	0.28	—	%
I_{DD}	Quiescent Current	No Load		—	18	25	mA
I_{SD}	Supply Quiescent Current in Shutdown Mode	Shutdown = 0		—	—	50	μA
$R_{DS(ON)}$	Drain-Source On-State Resistance	I_O = 0.5A T_J = +25°C	High Side	—	210	—	mΩ
			Low Side	—	210	—	
			Total	—	420	—	
PSRR	Power Supply Ripple Rejection Ratio	$1V_{PP}$ Ripple, f = 1kHz Inputs AC-Coupled to Ground		—	-65	—	dB
f_{OSC}	Oscillator Frequency	—		—	300	—	kHz
Vn	Output Integrated Noise Floor	20Hz to 22kHz, A-Weighting		—	-100	—	dB
CS	Crosstalk	P_O = 3W, R_L = 8Ω, f = 1kHz		—	-95	—	dB
SNR	Signal to Noise Ratio	Maximum Output at THD+N < 0.5% f = 1kHz		—	90	—	dB
—	Gain	—		—	32	—	dB
$\lvert V_{OS} \rvert$	Output Offset Voltage (measured differentially)	INN and INP Connected Together		—	30	—	mV
V2P5	2.5V Bias Voltage	No Load		—	2.5	—	V
AVDD	Internal Analog Supply Voltage	V_{CC} = 8V to 18V		—	5	5.5	V
OTS	Overtemperature Shutdown	—		—	+160	—	°C
OTH	Thermal Hysteresis	—		—	+50	—	°C

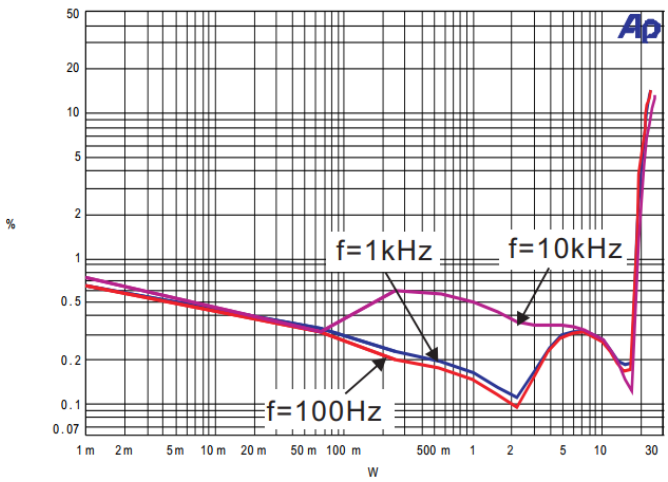
Typical Performance Characteristics

(V_{CC} = 18V, R_L = 8Ω, G_V = 32dB, T_A = +25°C, V_{CC} = 12V, R_L = 8Ω, unless otherwise specified.)

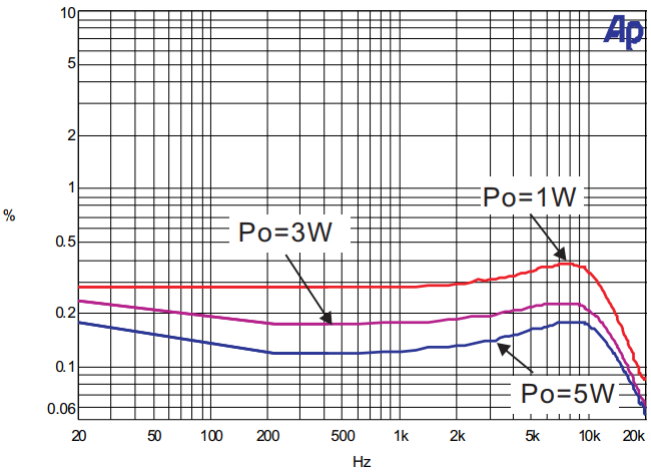
1. THD+N vs Power (VCC=12V)



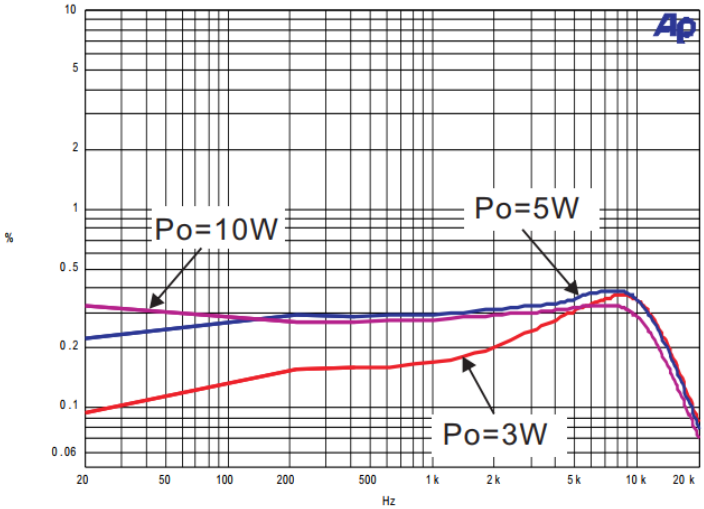
2. THD+N vs Power (VCC=18V)



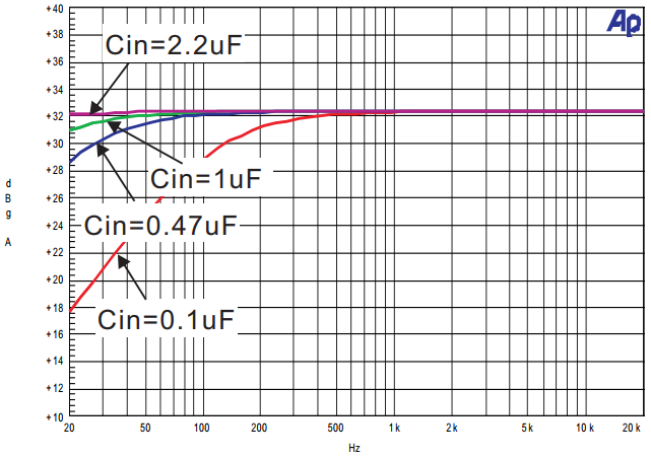
3. THD+N vs Frequency (VCC=12V)



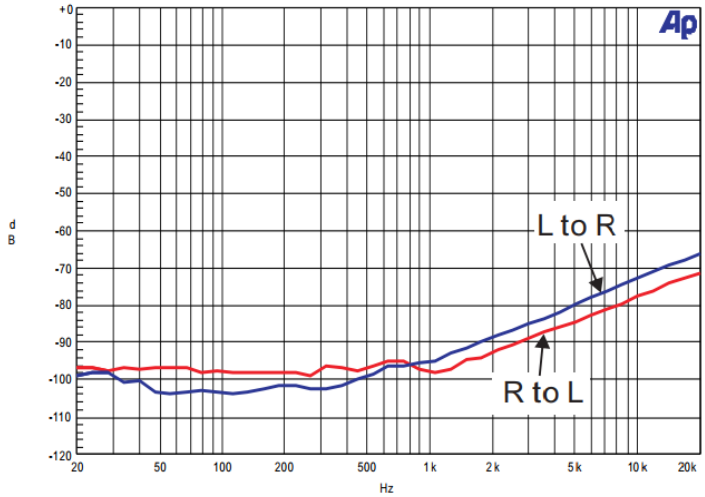
4. THD+N vs Frequency (VCC=18V)



5. Frequency Response



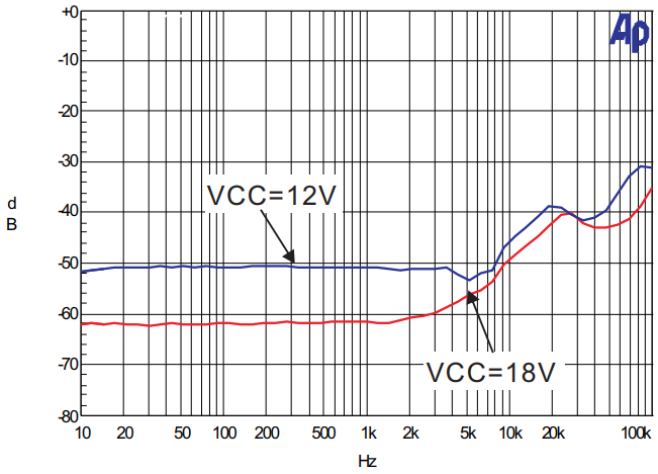
6. Crosstalk



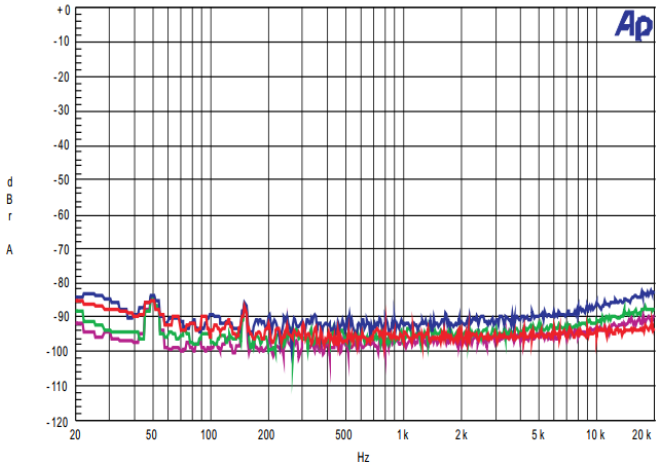
Typical Performance Characteristics (continued)

(V_{CC} = 18V, R_L = 8Ω, G_V = 32dB, T_A = +25°C, V_{CC} = 12V, R_L = 8Ω, unless otherwise specified.)

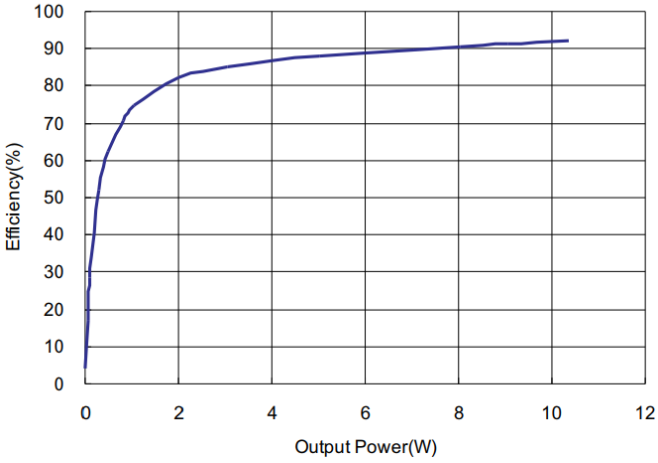
7. PSRR



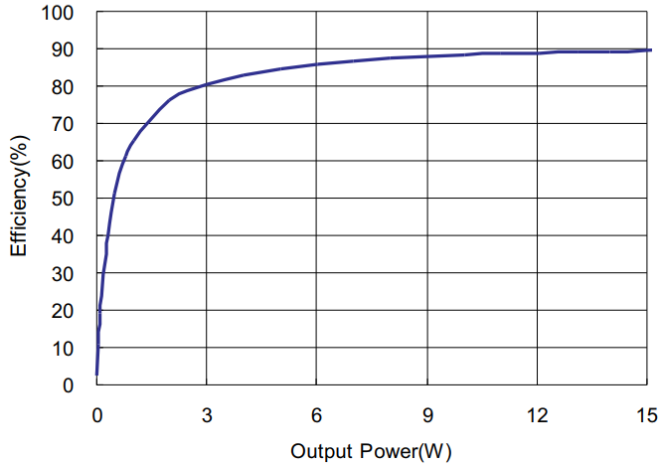
8. Noise Floor



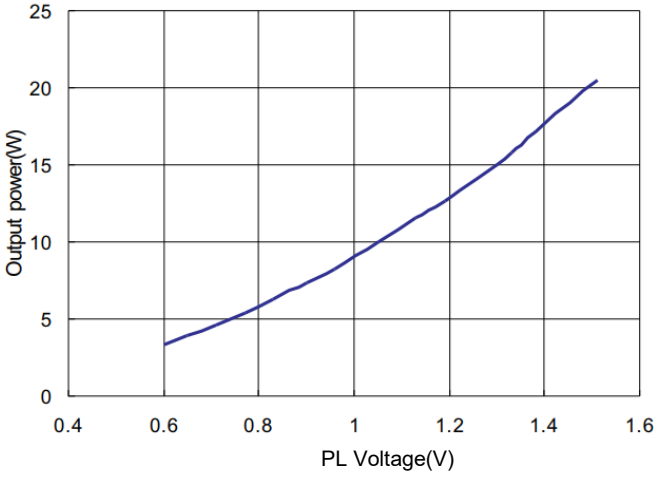
9. Efficiency vs Output Power (VCC=12V)



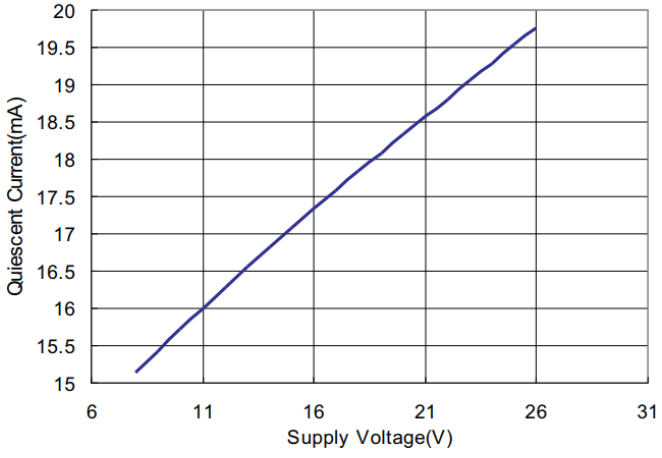
10. Efficiency vs Output Power (VCC=18V)



11. PL Voltage vs Output Power

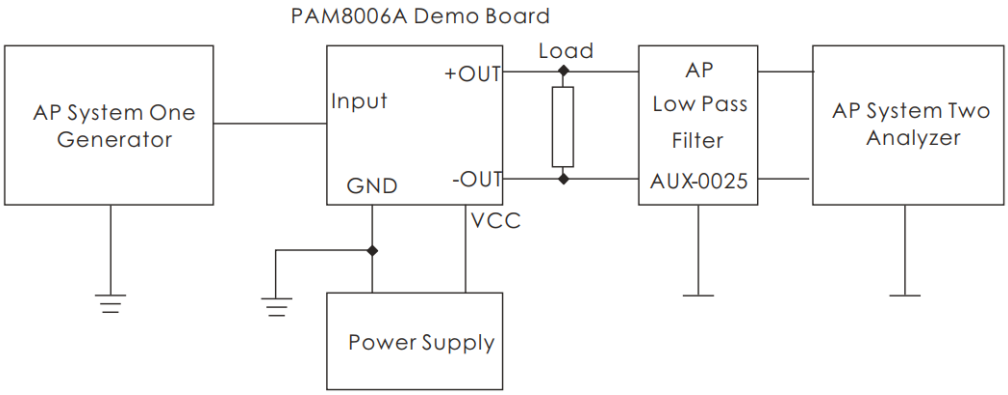


12. Quiescent Current vs Supply Voltage



Application Information

Test Setup for Performance Testing



Notes: 7. The AP AUX-0025 low pass filter is necessary for class-D amplifier measurement with AP analyzer.
8. Two 22μH inductors are used in series with load resistor to emulate the small speaker for efficiency measurement.

MUTE Operation

The MUTE pin is an input for controlling the output state of the PAM8006A. A logic high on this pin disables the outputs and low enables the outputs. This pin may be used as a quick disable or enable of the outputs without a volume fade.

Shutdown Operation

The PAM8006A employs a shutdown operation mode to reduce supply current to the absolute minimum level during periods of non-use to save power. The $\overline{SD}$ input terminal should be held high during normal operation when the amplifier is in use. Pulling $\overline{SD}$ low causes the outputs to be muted and the amplifier to enter a low-current state. $\overline{SD}$ should never be left unconnected to prevent the amplifier from unpredictable operation.

For the best power-off pop performance, the amplifier should be set in shutdown mode prior to removing the power supply voltage.

Internal 2.5V Bias Generator Capacitor Selection

The internal 2.5V bias generator (V2P5) provides the internal bias for the preamplifier stage. The external input capacitors and this internal reference allow the inputs to be biased within the optimal common-mode range of the input preamplifiers.

The selection of the capacitor value on the V2P5 terminal is critical for achieving the best device performance. During startup or recovery from shutdown state, the V2P5 capacitor determines the rate at which the amplifier starts up. When the voltage on the V2P5 capacitor equals 0.75 x V2P5, or 75% of its final value, the device turns on and the Class-D outputs start switching. The startup time is not critical for the best de-pop performance since any heard pop sound is the result of the Class-D output switching-on other than that of the startup time. However, at least a 0.47μF capacitor is recommended for the V2P5 capacitor.

Another function of the V2P5 capacitor is to filter high frequency noise on the internal 2.5V bias generator.

Power Supply Decoupling, C_S

The PAM8006A is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD) as low as possible. Power supply decoupling also prevents oscillations caused by long lead between the amplifier and the speaker. The optimum decoupling is achieved by using two capacitors of different types that target different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series resistance (ESR) ceramic capacitor, typically 1μF, is recommended, placed as close as possible to the device's VCC lead. To filter lower frequency noises, a large aluminum electrolytic capacitor of 10μF or greater is recommended, placed near the audio power amplifier. The 10μF capacitor also serves as a local storage capacitor for supplying current during large signal transients on the amplifier outputs.

BSN and BSP Capacitors

The full H-bridge output stages use nMOS transistors only. They therefore require bootstrap capacitors for the high side of each output to turn on correctly. An at least 220nF ceramic capacitor, rated for at least 25V, must be connected from each output to its corresponding bootstrap input. Specifically, one 220nF capacitor must be connected from xOUTP to xBSP, and another 220nF capacitor from xOUTN to xBSN. It is recommended to use 1μF BST capacitor to replace 220nF or lower than 100Hz applications.

Application Information (continued)

VCLAMP Capacitors

To ensure that the maximum gate-to-source voltage for the nMOS output transistors not exceeded, internal regulators are used to clamp the gate voltage. A 1µF capacitors must be connected from VCLAMP to ground and must be rated for at least 25V. The voltages at the VCLAMP terminals vary with V_{CC} and may not be used to power any other circuitry.

Internal Regulated 5V Supply (AVDD)

The AVDD terminal is the output of an internally generated 5V supply, used for the oscillator, amplifier, power limit circuitry and logic control circuitry. It requires a 0.1µF to 1µF capacitor, placed very close to the pin to ground to keep the regulator stable. The regulator may not be used to power any external circuitry.

Differential Input Power Limit

The differential input stage of the amplifier eliminates noises that appear on the two input lines of the channel. To use the PAM8006A with a differential source, connect the positive lead of the audio source to the INP input and the negative lead from the audio source to the INN input. To use the PAM8006A with a single-ended source, AC ground the INP input through a capacitor equal in value to the input capacitor on INN and apply the audio source to the INN input. In a single-ended input application, the INP input should be AC grounded at the audio source other than at the device input for best noise performance.

Using Low-ESR Capacitors

Low-ESR capacitors are recommended throughout this application section. A real (with respect to ideal) capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of this resistance the more the real capacitor behaves as an ideal capacitor.

Short-Circuit Protection

The PAM8006A has short-circuit protection circuitry on the outputs to prevent damage to the device when output-to-output shorts, output-to-GND shorts, or output-to-VCC shorts occur. Once a short-circuit is detected on the outputs, the output drive is immediately disabled. This is a latched fault and must be reset by cycling the voltage on the $\overline{SD}$ pin to a logic low and back to the logic high state for normal operation. This will clear the short-circuit flag and allow for normal operation if the short was removed. If the short was not removed, the protection circuitry will again be activated.

Thermal Protection

Thermal protection on the PAM8006A prevents damage to the device when the internal die temperature exceeds +160°C. There is a ±15 degree tolerance on this trip point from device to device. Once the die temperature exceeds the set thermal point, the device enters the shutdown state and the outputs are disabled. This is not a latched fault. The thermal fault is cleared once the temperature of the die is reduced by 50°C. The device begins normal operation at this point without external system intervention.

Power Limit

The voltage at PL pin can be used to limit the power to levels below that which is possible based on the supply rail. Add a resistor from PL to ground to set the voltage at the PL pin. An external reference may also be used if tighter tolerance is required. Also add a 1µF capacitor from PL pin to ground. The PL circuit sets a limit on the output peak-to-peak voltage. The gain of Class-D amplifier will automatically be reduced if the output power is higher than setting value to make output power less than limited value and also provide good sound quality.

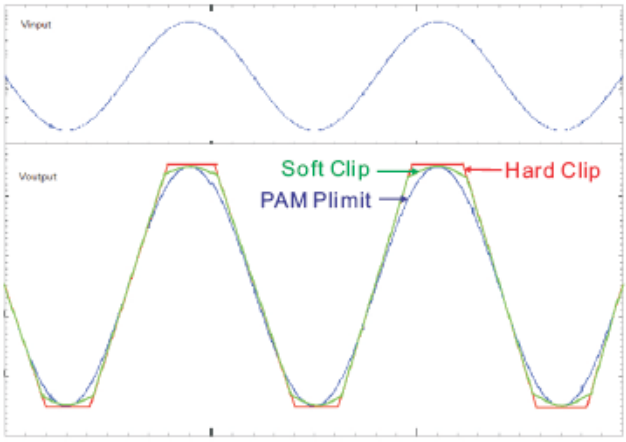
Application Information (continued)

Power Limit (continued)

The output power vs. PL pin resistor value as below.

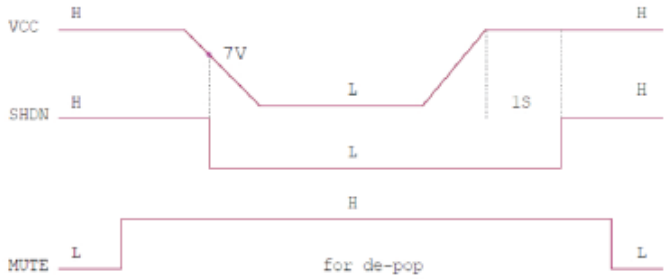
V_{CC} = 12V, R_{LOAD} = 8Ω

R (Ω)	PL (V)	PL (W)	R (Ω)	PL (V)	PL (W)
56K	0.61	3.1	100K	0.99	8.1
62K	0.67	3.7	110K	1.07	9.0
68K	0.73	4.3	120K	1.15	9.6
75K	0.79	5.1	130K	1.22	10.0
82K	0.85	6.0	140K	1.36	10.7
91K	0.92	7.0	—	—	—



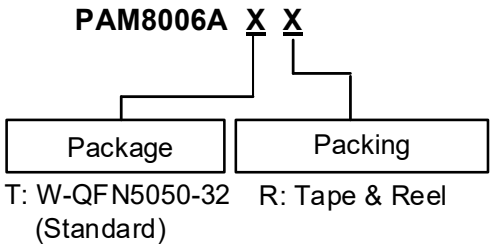
Power-Up/Down Sequence

The PAM8006A employs a shutdown operation mode to reduce supply current to the absolute minimum level during periods of non-use to save power. The $\overline{SD}$ input terminal should be held high during normal operation when the amplifier is in use. Pulling $\overline{SD}$ low causes the outputs to be muted and the amplifier to enter a low-current state. $\overline{SD}$ should never be left unconnected to prevent the amplifier from unpredictable operation. Suggested PL starting voltage is greater than 5V.



Startup/power-down sequencer recommended.

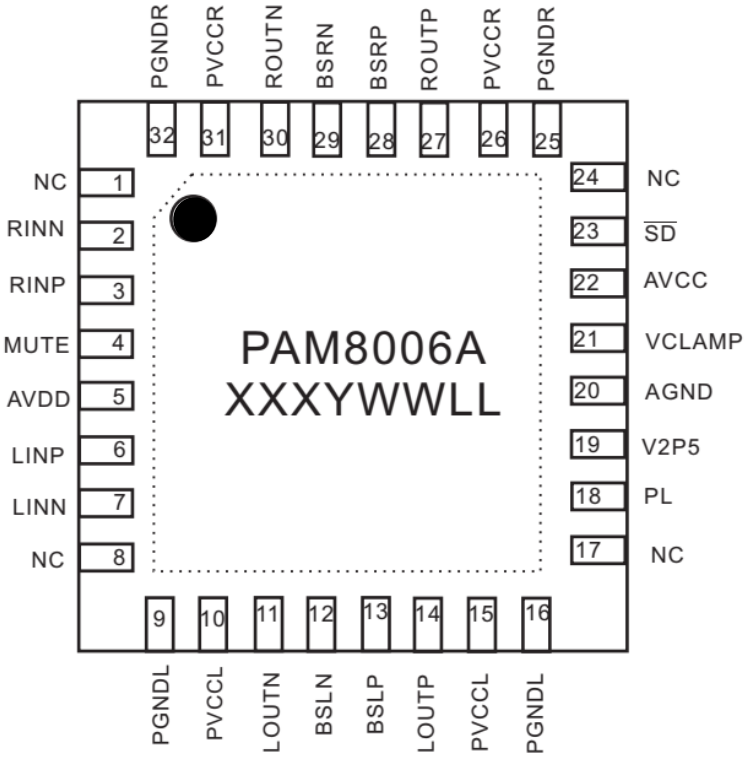
Ordering Information (Note 9)



Orderable Part Number	Part Marking	Package	Packing	
			Qty.	Carrier
PAM8006ATR	PAM8006A XXXYWWLL	W-QFN5050-32 (Standard)	3000 Units	Tape & Reel

Note: 9. For packaging details, go to our website at https://www.diodes.com/design/support/packaging/diodes-packaging/.

Marking Information

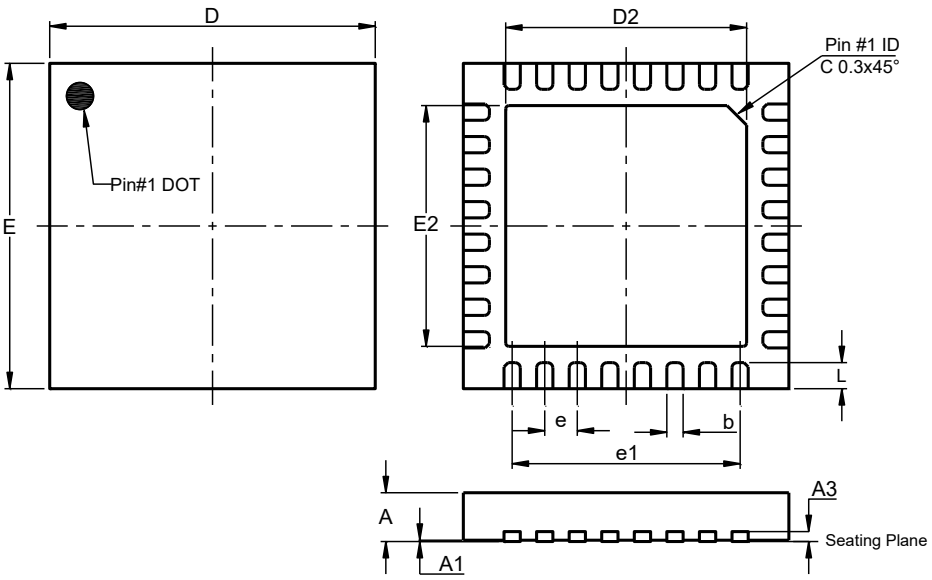


XXX: Internal Code
Y: Year (ex: 5 = 2025)
WW: Week: 01 to 52
52 represents week 52 and 53
LL: Internal Code

Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

W-QFN5050-32 (Standard)



W-QFN5050-32 (Standard)			
Dim	**Min**	**Max**	**Typ**
A	0.55	0.80	0.75
A1	0.00	0.05	--
A3	0.203 REF		
b	0.20	0.30	0.25
D	4.95	5.05	5.00
D2	3.65	3.75	3.70
E	4.95	5.05	5.00
E2	3.65	3.75	3.70
e	0.50 BSC		
e1	3.50 REF		
L	0.35	0.45	0.40
All Dimensions in mm			

Suggested Pad Layout

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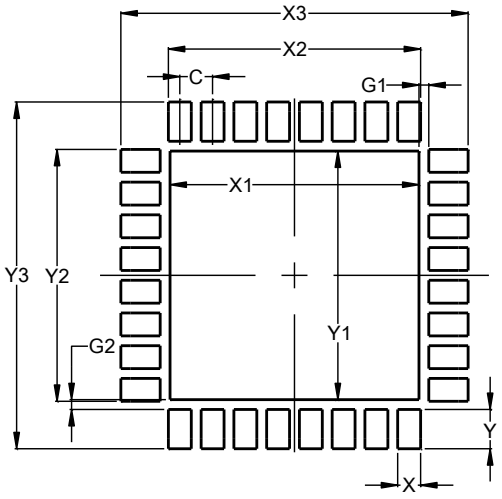
W-QFN5050-32 (Standard)



Dimensions	Value (in mm)
C	0.500
G1	0.150
G2	0.150
X	0.350
X1	3.800
X2	3.850
X3	5.300
Y	0.600
Y1	3.800
Y2	3.850
Y3	5.300

Mechanical Data

- Moisture Sensitivity: Level 3 per J-STD-020
- Terminals: Finish – Matte Tin Plated Leads, Solderable per MIL-STD-202, Method 208 e3
- Weight: 0.065 grams (Approximate)

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