



General Description

- Latest Trench Power AlphaMOS (αMOS LV) technology
- Very Low $R_{DS(ON)}$ at 2.5V V_{GS}
- Low Gate Charge
- ESD protection
- RoHS and Halogen-Free Compliant

Application

- Load switch, battery switch in portable devices

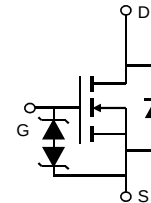
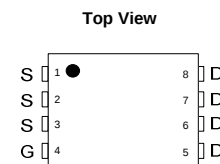
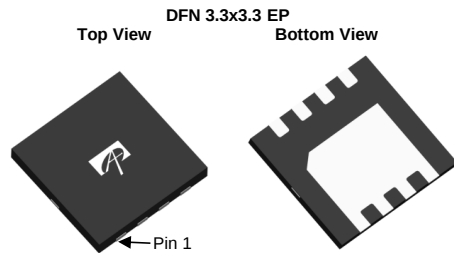
Product Summary

V_{DS}	30V
I_D (at $V_{GS}=10V$)	50A
$R_{DS(ON)}$ (at $V_{GS}=10V$)	< 1.8mΩ
$R_{DS(ON)}$ (at $V_{GS}=4.5V$)	< 2.1mΩ
$R_{DS(ON)}$ (at $V_{GS}=2.5V$)	< 3.1mΩ

Typical ESD protection

HBM Class 2

100% UIS Tested
100% R_g Tested



Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Parameter		Symbol	Maximum	Units
Drain-Source Voltage		V _{DS}	30	V
Gate-Source Voltage		V _{GS}	±12	V
Continuous Drain Current ^G	T _C =25°C	I _D	50	A
	T _C =100°C		39	
Pulsed Drain Current ^C		I _{DM}	200	
Continuous Drain Current	T _A =25°C	I _{DSM}	48	A
	T _A =70°C		38	
Avalanche Current ^C		I _{AS}	60	A
Avalanche energy L=0.05mH ^C		E _{AS}	90	mJ
V _{DS} Spike	100ns	V _{SPIKE}	36	V
Power Dissipation ^B	T _C =25°C	P _D	83.3	W
	T _C =100°C		33.3	
Power Dissipation ^A	T _A =25°C	P _{DSM}	6.2	W
	T _A =70°C		4	
Junction and Storage Temperature Range		T _J , T _{STG}	-55 to 150	°C

Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	16	20	$^\circ\text{C/W}$
$t \leq 10\text{s}$				
Maximum Junction-to-Ambient ^{A D}		45	55	$^\circ\text{C/W}$
Steady-State				
Maximum Junction-to-Case	$R_{\theta JC}$	1.1	1.5	$^\circ\text{C/W}$
Steady-State				

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	ID=250μA, V _{GS} =0V	30			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =30V, V _{GS} =0V T _J =125°C			1 5	μA
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} =±10V			±10	μA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250μA	0.5	0.85	1.2	V
R _{DS(on)}	Static Drain-Source On-Resistance	V _{GS} =10V, I _D =20A T _J =125°C		1.45 2.05	1.8 2.6	mΩ
		V _{GS} =4.5V, I _D =20A		1.66	2.1	
		V _{GS} =2.5V, I _D =20A		2.35	3.1	
g _{FS}	Forward Transconductance	V _{DS} =5V, I _D =20A		125		S
V _{SD}	Diode Forward Voltage	I _S =1A, V _{GS} =0V		0.61	1	V
I _S	Maximum Body-Diode Continuous Current ^G				50	A
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =15V, f=1MHz		4175		pF
C _{oss}	Output Capacitance			1505		pF
C _{rss}	Reverse Transfer Capacitance			300		pF
R _g	Gate resistance	V _{GS} =0V, V _{DS} =0V, f=1MHz	0.5	1	1.5	Ω
SWITCHING PARAMETERS						
Q _{g(10V)}	Total Gate Charge	V _{GS} =10V, V _{DS} =15V, I _D =20A		77.5	105	nC
Q _{g(4.5V)}	Total Gate Charge			37	50	nC
Q _{gs}	Gate Source Charge			6		nC
Q _{gd}	Gate Drain Charge			12.5		nC
t _{D(on)}	Turn-On DelayTime	V _{GS} =10V, V _{DS} =15V, R _L =0.75Ω, R _{GEN} =3Ω		6.5		ns
t _r	Turn-On Rise Time			7		ns
t _{D(off)}	Turn-Off DelayTime			58.5		ns
t _f	Turn-Off Fall Time			17.5		ns
t _{rr}	Body Diode Reverse Recovery Time	I _F =20A, dI/dt=500A/μs		20.3		ns
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =20A, dI/dt=500A/μs		40.7		nC

- A. The value of R_{θJA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C. The Power dissipation P_{DSM} is based on R_{θJA} ≤ 10s and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design.
- B. The power dissipation P_D is based on T_{J(MAX)}=150° C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.
- C. Single pulse width limited by junction temperature T_{J(MAX)}=150° C.
- D. The R_{θJA} is the sum of the thermal impedance from junction to case R_{θJC} and case to ambient.
- E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.
- F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T_{J(MAX)}=150° C. The SOA curve provides a single pulse rating.
- G. The maximum current rating is package limited.
- H. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C.

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

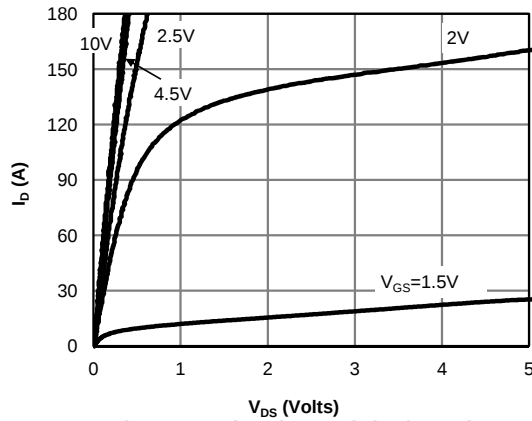


Fig 1: On-Region Characteristics (Note E)

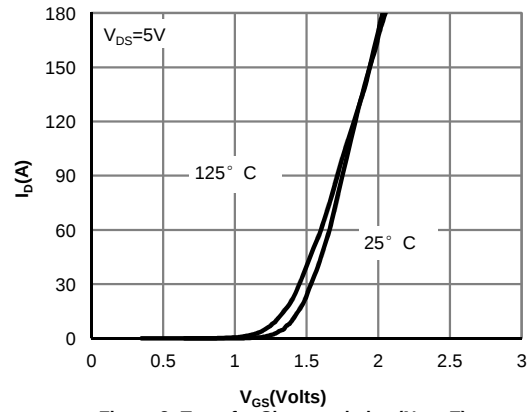


Figure 2: Transfer Characteristics (Note E)

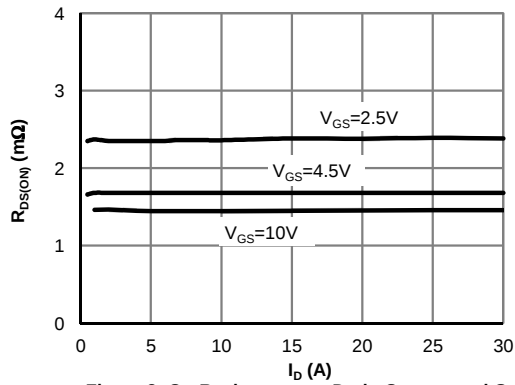


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

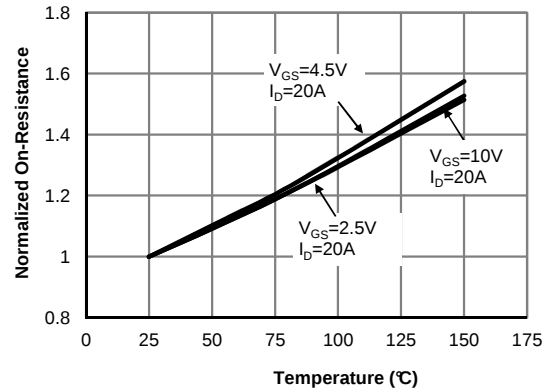


Figure 4: On-Resistance vs. Junction Temperature (Note E)

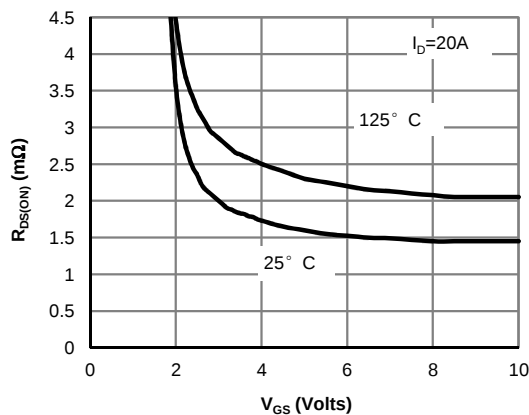


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

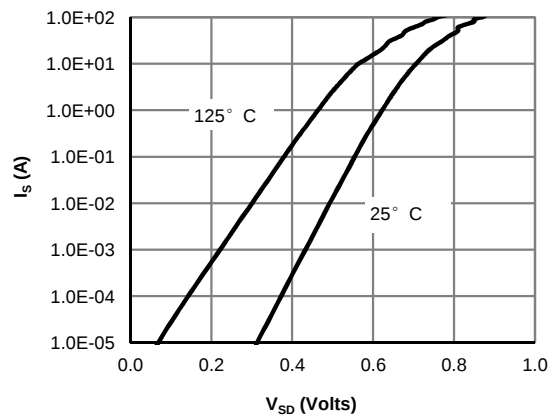


Figure 6: Body-Diode Characteristics (Note E)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

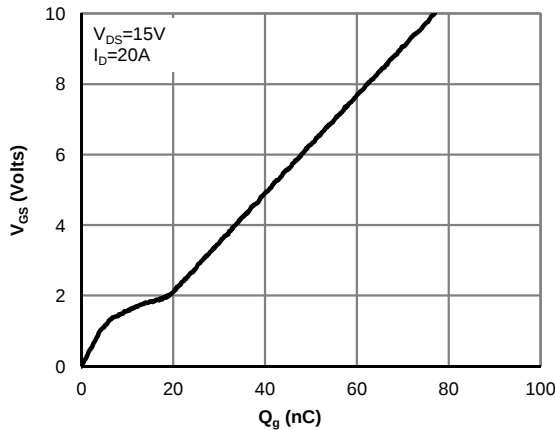


Figure 7: Gate-Charge Characteristics

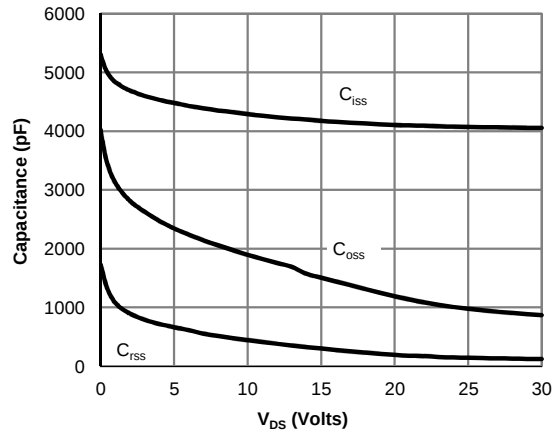


Figure 8: Capacitance Characteristics

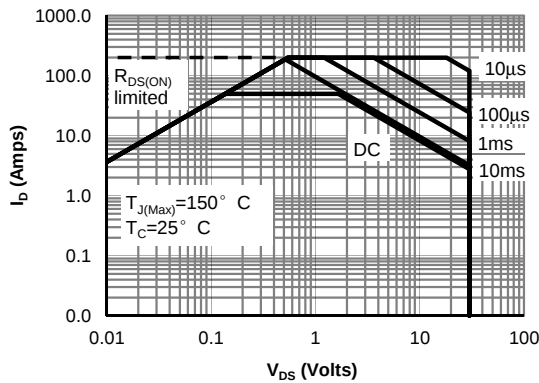


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

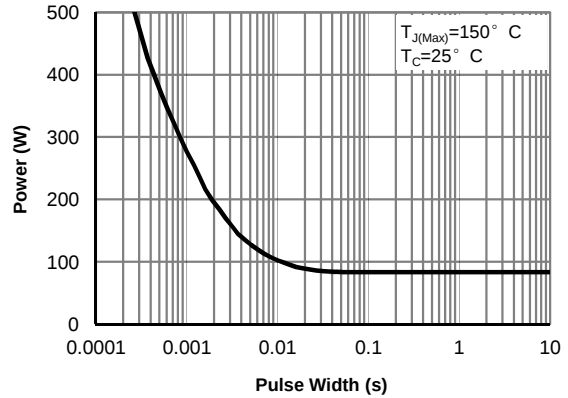


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

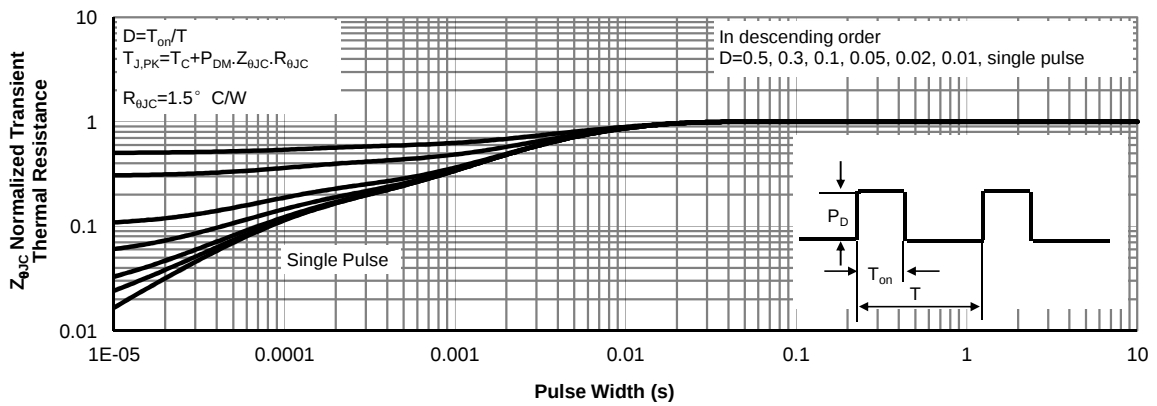


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

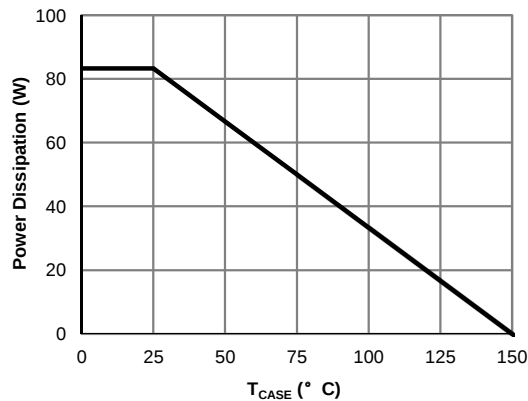


Figure 12: Power De-rating (Note F)

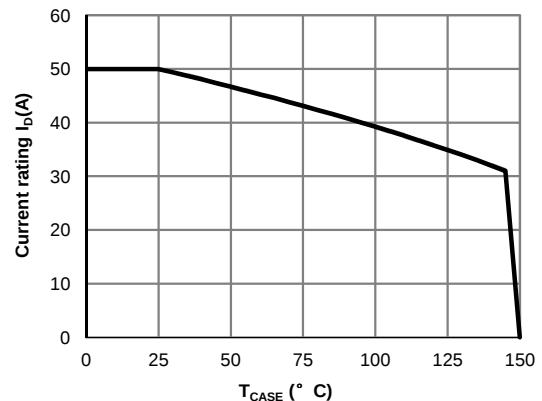


Figure 13: Current De-rating (Note F)

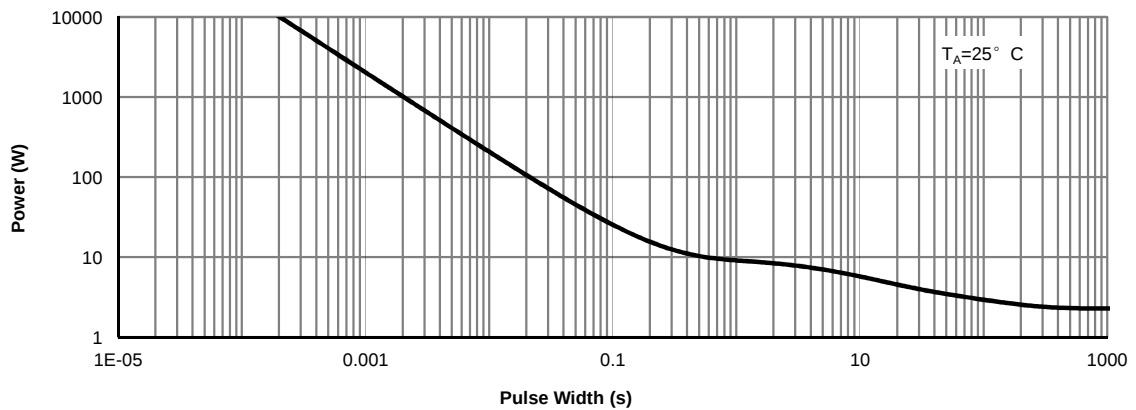


Figure 14: Single Pulse Power Rating Junction-to-Ambient (Note H)

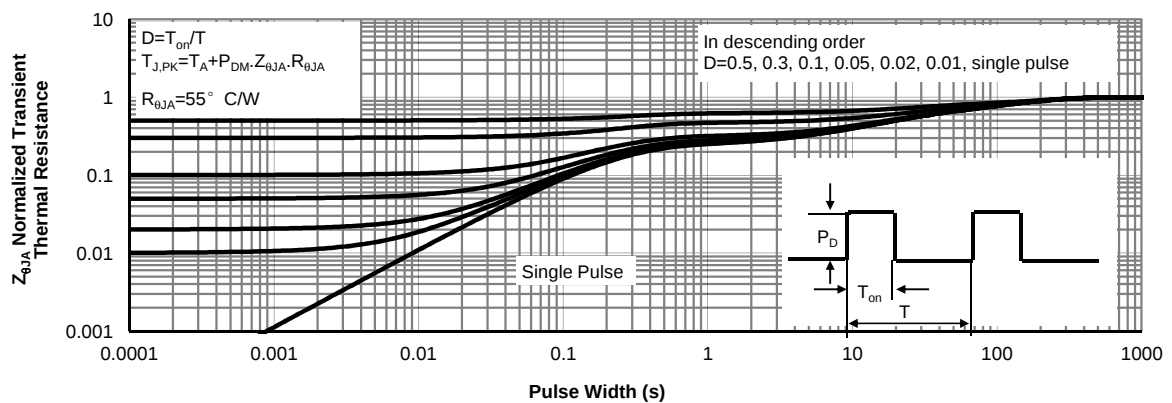
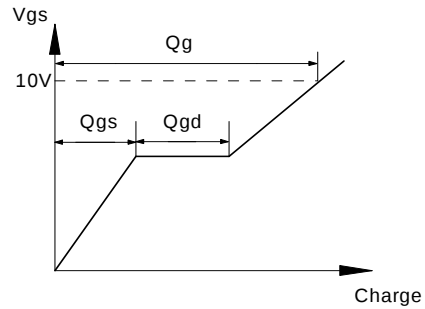
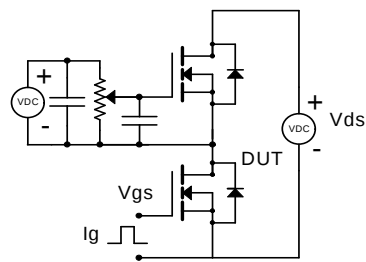
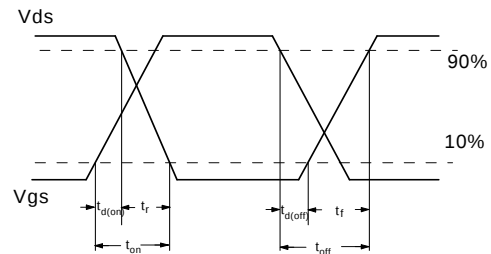
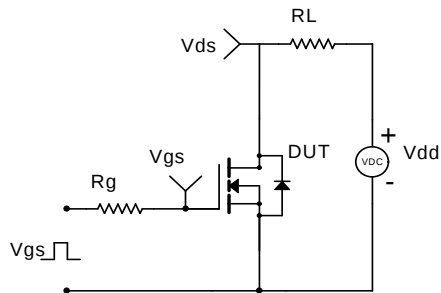


Figure 15: Normalized Maximum Transient Thermal Impedance (Note H)

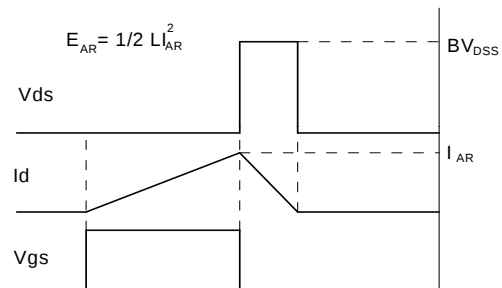
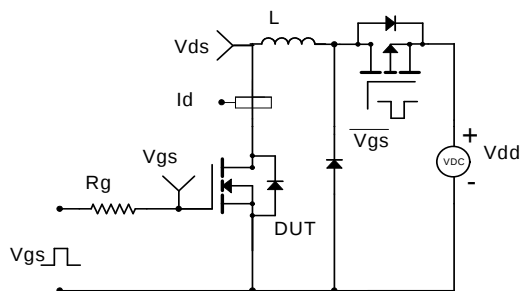
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

