Data Sheet

LT3046

20V, 200mA, Ultra-Low Noise, Ultra-High PSRR, Linear Regulator

FEATURES

- Ultra-Low RMS Noise: 0.8µV_{RMS} (10Hz to 100kHz)
- Ultra-Low Noise: 2.2nV/√Hz at 10kHz
- Ultra-Low 1/f Noise: 2.5µV_{P-P} (0.1Hz to 10Hz)
- Ultra-High PSRR: 82dB at 1MHz
- Output Current: 200mA
- Wide Input-Voltage Range: 2.2V to 20V
- Single Capacitor Improves Noise and PSRR
- SET Pin Current: 100µA, ±0.5% Initial Accuracy
- Single Resistor Programs Output Voltage
- Programmable Current Limit
- Low Dropout Voltage: 300mV
- Output-Voltage Range: 0.2V to 19V
- Programmable Power Good
- Fast Start-Up Capability
- Precision Enable/UVLO
- Parallelable for Lower Noise and Higher Current
- Internal Current Limit with Foldback
- Minimum Output Capacitor: 4.7µF Ceramic
- Compact, Low-Profile, 12-Lead, 3mm × 3mm, DFN Package and 11-Ball, 1.621mm × 1.680mm, WLCSP Package

APPLICATIONS

- RF Power Supplies: PLLs, VCOs, Mixers, LNAs, PAs
- Very Low-Noise Instrumentation
- High-Speed/High-Precision Data Converters
- Post-Regulator for Switching Supplies

GENERAL DESCRIPTION

The LT3046 is a high-performance, low-dropout linear regulator featuring Analog Devices, Inc. ultra-low noise and ultra-high PSRR architecture for powering noise-sensitive applications. Designed as a precision current reference followed by a high-performance voltage buffer, the LT3046 can be easily paralleled to further reduce noise, increase output current, and spread heat on the PCB.

The device supplies 200mA at a typical 300mV dropout voltage. Operating quiescent current is nominally 3.7mA and drops to 26µA in shutdown. The LT3046's wide output-voltage range (0.2V to 19V) while maintaining unity-gain operation provides virtually constant output noise, PSRR, bandwidth, and load regulation, independent of the programmed output voltage. Additionally, the regulator features programmable current limit, fast start-up capability, and programmable power good to indicate output voltage regulation.

Built-in protection includes reverse-battery protection, reverse-current protection, internal current limit with foldback and thermal limit with hysteresis. The LT3046 is available in thermally enhanced, 12-lead, 3mm × 3mm, DFN and 11-Ball, 1.621mm × 1.680mm, WLCSP packages.

TYPICAL APPLICATION

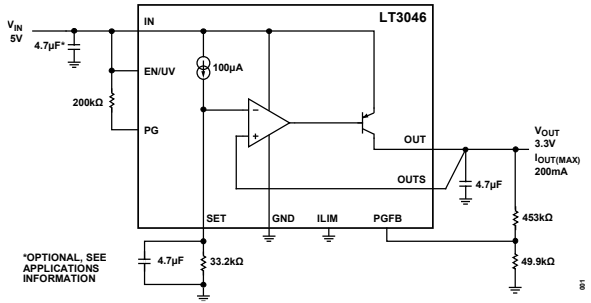

Figure 1. Typical Application

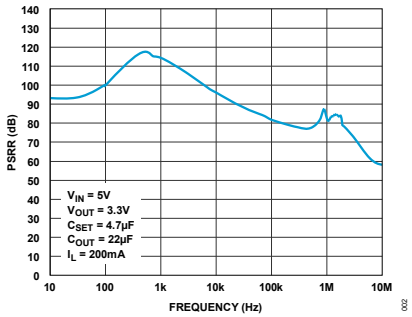

Figure 2. PSRR vs. Frequency

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0	10/23	Initial Release	—
A	04/25	WLCSP Addition:	
		Updated Features and General Description	1
		Updated Revision History Table	2
		Updated ESD Table Title	8
		Updated Figure 3 Caption	9
		Included Figure 4	9
		Updated Pin Description Table	10, 11
		Updated Output Sensing and Stability	25
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B	04/25	Added Package Number to WLCSP Package	48
		Replaced WLCSP to WLP in Selector Guide table	48

SPECIFICATIONS

Table 1. Electrical Characteristics

(T_J = -40°C to +125°C for the minimum and maximum values, T_A = +25°C for the typical values, output capacitance (C_{OUT}) = 4.7µF ceramic capacitor, and SET capacitance (C_{SET}) = 4.7µF, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS/COMMENTS		MIN	TYP	MAX	UNITS
Input-Voltage Range	V_{IN}			2.2		20	V
Minimum IN Pin Voltage[1]					2.05	2.2	V
Output-Voltage Range	V_{OUT}	$V_{IN} > V_{OUT}$		0.2		19	V
SET Pin Current	I_{SET}	V_{IN} = 2.2V, I_L = 1mA, V_{OUT} = 1.3V	T_A = +25°C	99.5	100	100.5	µA
		2.2V < V_{IN} < 20V, 0.2V < V_{OUT} < 19V, 1mA < I_L < 200mA[2]		99	100	101	
Fast Startup	I_{SET}	V_{PGFB} = 289mV, V_{IN} = 2.8V, V_{SET} = 1.3V			2.2		mA
Output Offset Voltage[3]	V_{OS}	V_{IN} = 2.2V, I_L = 1mA, V_{OUT} = 1.3V	T_A = +25°C	-1		+1	mV
		2.2V < V_{IN} < 20V, 0.2V < V_{OUT} < 19V, 1mA < I_L < 200mA[2]		-2		+2	
Line Regulation	ΔI_{SET}	V_{IN} = 2.2V to 20V, I_L = 1mA, V_{OUT} = 1.3V			0.25	±10	nA/V
	ΔV_{OS}	V_{IN} = 2.2V to 20V, I_L = 1mA, V_{OUT} = 1.3V[3]			1	±20	µV/V
Load Regulation	ΔI_{SET}	I_L = 1mA to 200mA, V_{IN} = 2.2V, V_{OUT} = 1.3V			5		nA
	ΔV_{OS}	I_L = 1mA to 200mA, V_{IN} = 2.2V, V_{OUT} = 1.3V[3]			0.1	0.7	mV
Change in I_{SET} with V_{SET}[4]		V_{SET} = 1.3V to 19V, V_{IN} = 20V, I_L = 1mA			175	500	nA
		V_{SET} = 0.2V to 0.75V, V_{IN} = 20V, I_L = 1mA			10	200	
Change in V_{OS} with V_{SET}[4]		V_{SET} = 1.3V to 19V, V_{IN} = 20V, I_L = 1mA[3]			0.06	0.6	mV
		V_{SET} = 0.2V to 0.75V, V_{IN} = 20V, I_L = 1mA[3]			0.01	0.2	
Error Amplifier Switchover Point (PNP-to-NPN Input Pair Switchover)		V_{IN} = 2.2V, I_L = 1mA, V_{SET} rising			957		mV
		V_{IN} = 2.2V, I_L = 1mA, V_{SET} falling			929		
		Hysteresis			28		
Dropout Voltage[5]		I_L = 1mA and 20mA	T_A = +25°C		290	370	mV
						450	
		I_L = 100mA	T_A = +25°C		295	375	
						460	
		I_L = 200mA	T_A = +25°C		300	380	

(T_J = -40°C to +125°C for the minimum and maximum values, T_A = +25°C for the typical values, output capacitance (C_{OUT}) = 4.7µF ceramic capacitor, and SET capacitance (C_{SET}) = 4.7µF, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS/COMMENTS	MIN	TYP	MAX	UNITS
					470	
GND Pin Current[6]		I_L = 10µA		3.7		mA
		I_L = 1mA		3.75	6.6	
		I_L = 20mA		4.2	8	
		I_L = 100mA		5.6	10.5	
		I_L = 200mA		8	15	
Output-Noise Spectral Density[3,7]		I_L = 200mA, frequency = 10Hz, C_{SET} = 0.47µF, V_{OUT} = 3.3V		148		nV/√Hz
		I_L = 200mA, frequency = 10Hz, C_{SET} = 4.7µF, 1.3V ≤ V_{OUT} ≤ 19V		24		
		I_L = 200mA, frequency = 10kHz, C_{SET} = 0.47µF, 1.3V ≤ V_{OUT} ≤ 19V		2.2		
		I_L = 200mA, frequency = 10kHz, C_{SET} = 0.47µF, 0.2V ≤ V_{OUT} < 1.3V		5		
Output RMS Noise[3,7]		I_L = 200mA, BW = 10Hz to 100kHz, C_{SET} = 0.47µF, V_{OUT} = 3.3V		1.7		$µV_{RMS}$
		I_L = 200mA, BW = 10Hz to 100kHz, C_{SET} = 4.7µF, 1.3V ≤ V_{OUT} ≤ 19V		0.8		
		I_L = 200mA, BW = 10Hz to 100kHz, C_{SET} = 4.7µF, 0.2V ≤ V_{OUT} < 1.3V		1.6		
Output Peak-to-Peak 1/f Noise[3,7]		I_L = 200mA, BW = 0.1Hz to 10Hz, C_{SET} = 4.7µF, V_{OUT} = 3.3V		4		$µV_{P-P}$
		I_L = 200mA, BW = 0.1Hz to 10Hz, C_{SET} = 22µF, V_{OUT} = 3.3V		2.5		
Reference Current RMS Output Noise[3,7]		BW = 10Hz to 100kHz		6		nA_{RMS}
Ripple Rejection 1.3V ≤ V_{OUT} ≤ 19V (V_{IN} - V_{OUT} = 1.7V (Avg)[3,7])		V_{RIPPLE} = 500mV_{P-P}, f_{RIPPLE} = 120Hz, I_L = 200mA		102		dB
		V_{RIPPLE} = 150mV_{P-P}, f_{RIPPLE} = 10kHz, I_L = 200mA		96		
		V_{RIPPLE} = 150mV_{P-P}, f_{RIPPLE} = 100kHz, I_L = 200mA		82		
		V_{RIPPLE} = 150mV_{P-P}, f_{RIPPLE} = 1MHz, I_L = 200mA		74		
		V_{RIPPLE} = 80mV_{P-P}, f_{RIPPLE} = 10MHz, I_L = 200mA		60		

(T_J = -40°C to +125°C for the minimum and maximum values, T_A = +25°C for the typical values, output capacitance (C_{OUT}) = 4.7µF ceramic capacitor, and SET capacitance (C_{SET}) = 4.7µF, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS/COMMENTS		MIN	TYP	MAX	UNITS
Ripple Rejection 0.2V ≤ V_{OUT} < 1.3V (V_{IN} - V_{OUT} = 1.7V (Avg) or $V_{IN(MIN)}$ = 2.2V[3,7])		V_{RIPPLE} = 500mV_{P-P}, f_{RIPPLE} = 120Hz, I_L = 200mA			92		dB
		V_{RIPPLE} = 50mV_{P-P}, f_{RIPPLE} = 10kHz, I_L = 200mA			88		
		V_{RIPPLE} = 50mV_{P-P}, f_{RIPPLE} = 100kHz, I_L = 200mA			77		
		V_{RIPPLE} = 50mV_{P-P}, f_{RIPPLE} = 1MHz, I_L = 200mA			69		
		V_{RIPPLE} = 50mV_{P-P}, f_{RIPPLE} = 10MHz, I_L = 200mA			60		
EN/UV Pin Threshold		EN/UV trip-point rising (turn-on), V_{IN} = 2.2V		1.19	1.27	1.35	V
EN/UV Pin Hysteresis		EN/UV trip-point hysteresis, V_{IN} = 2.2V			110		mV
EN/UV Pin Current		$V_{EN/UV}$ = 0V, V_{IN} = 20V				±1	µA
		$V_{EN/UV}$ = 1.27V, V_{IN} = 20V			0.04		
		$V_{EN/UV}$ = 20V, V_{IN} = 0V			1.7	8	
Quiescent Current in Shutdown ($V_{EN/UV}$ = 0V)		V_{IN} = 6V	T_A = +25°C		26	100	µA
Internal Current Limit[8]		V_{IN} = 2.2V, V_{OUT} = 0V		215	250	285	mA
		V_{IN} = 12V, V_{OUT} = 0V			210		
		V_{IN} = 20V, V_{OUT} = 0V		160	205	250	
Programmable Current Limit		Programming scale factor: 2.2V < V_{IN} < 20V[9]			150		mA × kΩ
		V_{IN} = 2.2V, V_{OUT} = 0V, R_{ILIM} = 750Ω		180	200	220	mA
		V_{IN} = 2.2V, V_{OUT} = 0V, R_{ILIM} = 1.5kΩ		90	100	110	
PGFB Trip Point		PGFB trip point rising		288.5	298	308.5	mV
PGFB Hysteresis		PGFB trip point hysteresis			7		mV
PGFB Pin Current		V_{IN} = 2.2V, V_{PGFB} = 298mV			25		nA
PG Output Low Voltage		I_{PG} = 100µA			35	110	mV
PG Leakage Current		V_{PG} = 20V				1	µA
Reverse Input Current		V_{IN} = -20V, $V_{EN/UV}$ = 0V, V_{OUT} = 0V, V_{SET} = 0V				200	µA
Reverse Output Current		V_{IN} = 0V, V_{OUT} = 5V, SET = open	T_A = +25°C		22	1000	µA
Thermal Shutdown		T_J rising			+165		°C
		Hysteresis			6		

(T_J = -40°C to +125°C for the minimum and maximum values, T_A = +25°C for the typical values, output capacitance (C_{OUT}) = 4.7µF ceramic capacitor, and SET capacitance (C_{SET}) = 4.7µF, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS/COMMENTS	MIN	TYP	MAX	UNITS
Start-Up Time		$V_{OUT(NOM)}$ = 5V, I_L = 200mA, C_{SET} = 0.47µF, V_{IN} = 6V, V_{PGFB} = 6V		55		ms
		$V_{OUT(NOM)}$ = 5V, I_L = 200mA, C_{SET} = 4.7µF, V_{IN} = 6V, V_{PGFB} = 6V		550		
		$V_{OUT(NOM)}$ = 5V, I_L = 200mA, C_{SET} = 4.7µF, V_{IN} = 6V, R_{PG1} = 50kΩ, R_{PG2} = 700kΩ (with fast startup to 90% of V_{OUT})		10		
Thermal Regulation		10ms pulse		-0.01		%/W

1 The EN/UV pin threshold must be met to ensure device operation.

2 The maximum T_J limits operating conditions. The regulated output-voltage specification does not apply for all possible combinations of input voltage and output current, especially due to the internal current-limit foldback, which starts to decrease current limit at V_{IN} - V_{OUT} > 11 V. If operating at the maximum output current, limit the input-voltage range. If operating at the maximum input voltage, limit the output-current range.

3 OUTS ties directly to OUT.

4 Changes in I_{SET} and V_{OS} with V_{SET} are tested at 0.2V, 0.75V, 1.3V, and 19V to ensure operation over the 0.2V to 19V SET pin voltage range.

5 The dropout voltage is the minimum input-to-output differential voltage needed to maintain regulation at a specified output current. The dropout voltage is measured when output is 1% out of regulation. This definition results in a higher dropout voltage compared to hard dropout, which is measured when V_{IN} = $V_{OUT(NOMINAL)}$. For output voltages less than 1.7V, the dropout voltage is limited by the minimum input-voltage specification. See *Figure 19* for the dropout voltage as a function of the output current and for temperature, see *Figure 20*, which was measured in a typical application circuit.

6 The GND pin current is tested with V_{IN} = $V_{OUT(NOMINAL)}$ and a current source load. Therefore, the LT3046 is tested while operating in dropout, which is the worst-case GND pin current. The GND pin current decreases at higher input voltages. Note that the GND pin current does not include the SET pin or the ILIM pin current; however, quiescent current does include the SET and ILIM pins.

7 Adding a capacitor across the SET pin resistor decreases the output voltage noise. Adding this capacitor bypasses the thermal noise of the resistor on the SET pin as well as the noise of the reference current. The output noise then equals the error-amplifier noise. Use of a SET pin bypass capacitor also increases the start-up time.

8 The internal back-up current-limit circuitry incorporates foldback protection that decreases current limit for V_{IN} - V_{OUT} > 11 V. Some level of output current is provided at all V_{IN} - V_{OUT} differential voltages. See *Figure 33* for the current limit as a function of V_{IN} - V_{OUT}.

9 The current-limit programming scale factor is specified while the internal backup current limit is not active. Note that the internal current limit has foldback protection for V_{IN} - V_{OUT} differentials greater than 11V.

ABSOLUTE MAXIMUM RATINGS

T_A = +25°C, unless otherwise specified.

Table 2. Absolute Maximum Ratings

PARAMETER	RATING
IN Pin Voltage	-22V to +22V
EN/UV Pin Voltage	-22V to +22V
IN-to-EN/UV Differential	-22V to +22V
PG Pin Voltage[1]	-0.3V to +22V
ILIM Pin Voltage[1]	-0.3V to +1V
PGFB Pin Voltage[1]	-0.3V to +22V
PGFB Pin Current	-20mA to +20mA
SET Pin Voltage[1]	-0.3V to +20V
SET Pin Current[2]	-20mA to +20mA
OUTS Pin Voltage[1]	-0.3V to +20V
OUTS Pin Current[2]	-20mA to +20mA
OUT Pin Voltage[1]	-0.3V to +20V
OUT-to-OUTS Differential[3]	-1.2V to +1.2V
IN-to-OUT Differential	-22V to +22V
IN-to-OUTS Differential	-22V to +22V
Output Short-Circuit Duration	Indefinite
Operating Junction Temperature[4]	-40°C to +125°C
Storage Temperature Range	-65°C to +150°C

1 Parasitic diodes exist internally between the ILIM, PG, PGFB, SET, OUTS, and OUT pins and the GND pin. Do not drive the ILIM, PG, PGFB, SET, OUTS, and OUT pins more than 0.3V less than the GND pin during a fault condition. The ILIM, PG, PGFB, SET, OUTS, and OUT pins must remain at a voltage more positive than GND during normal operation.

2 SET and OUTS pins are clamped using diodes and two 25Ω series resistors. For less than 5ms transients, this clamp circuitry can carry more than the rated current. See *Figure 67* and the *Protection Features* section for more information.

3 Maximum OUT-to-OUTS differential is guaranteed by design.

4 The LT3046 is tested and specified under pulse load conditions such that $T_J \approx T_A$. The LT3046 is tested at T_A = +25°C. Performance of the LT3046 over the full -40°C to +125°C operating temperature range is assured by design, characterization, and correlation with statistical process controls. The LT3046 is guaranteed over the full -40°C to +125°C operating T_J range.

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Thermal Resistance

Thermal performance is directly linked to PCB design and operating environment. Close attention to PCB thermal design is required. See the *Thermal Considerations* section for additional information.

Electrostatic Discharge (ESD)

The following ESD information is provided for handling of ESD-sensitive devices in an ESD-protected area only. Human body model (HBM) per ANSI/ESDA/JEDEC JS-001. Charged device model (CDM) per ANSI/ESDA/JEDEC JS-002.

ESD Ratings

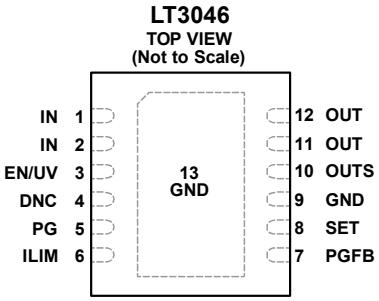
Table 3. LT3046, 12-Lead, 3mm x 3mm, DFN, and 11-Ball, 1.621mm x 1.680mm, WLCSP

ESD MODEL	WITHSTAND THRESHOLD (V)	CLASS
HBM	±1500	1C
CDM	±1250	C3

ESD Caution

Electrostatic discharge (ESD)-sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high-energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

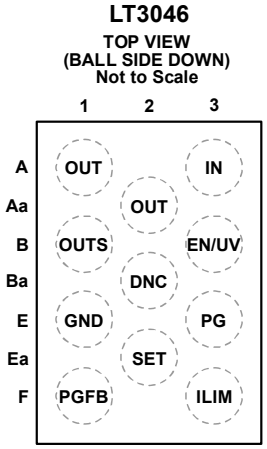
PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS



NOTES
1. DNC = DO NOT CONNECT.
2. EXPOSED PAD. THE EXPOSED PAD IS AN ELECTRICAL CONNECTION TO GND. TO ENSURE PROPER ELECTRICAL AND THERMAL PERFORMANCE, SOLDER THE EXPOSED BACKSIDE TO THE PCB GROUND AND CONNECT IT DIRECTLY TO THE GND PIN.

DFN PACKAGE
12-LEAD (3mm × 3mm)
T_{JMAX} = 125°C, θ_{JA} = 35°C/W, θ_{JCBOT} = 4°C/W, θ_{JCTOP} = 28°C/W
THERMAL RESISTANCE (θ) VALUES ARE DETERMINED PER JESD51 CONDITIONS. 003

Figure 3. 12-Lead DFN Pin Configuration



NOTES
1. DNC = DO NOT CONNECT.

WLCSP PACKAGE
11-BALL (1.621mm × 1.680mm)
T_{JMAX} = 125°C, θ_{JA} = 73°C/W
THERMAL RESISTANCE (θ) VALUES ARE DETERMINED PER JESD51 CONDITIONS. 004

Figure 4. 11-Ball WLCSP Pin Configuration

Table 4. Pin Descriptions

PIN		NAME	DESCRIPTION
DFN	WLCSP		
1, 2	A3	IN	Input. The IN pins supply power to the regulator. The LT3046 requires a bypass capacitor at the IN pin. In general, the output impedance of a battery rises with frequency; therefore, it is best practice to include a bypass capacitor in battery-powered applications. While a 4.7µF input bypass capacitor generally suffices, applications with large load transients can require higher input capacitance to prevent input supply droop. See the Stability and Input Capacitance and PSRR and Input Capacitance sections for the proper use of an input capacitor and its effect on circuit performance, in particular PSRR. The LT3046 withstands reverse voltages on IN with respect to GND, OUTS, and OUT. In the case of a reversed input, which occurs if a battery is plugged-in backwards, the LT3046 acts as if a diode is in series with its input. Therefore, no reverse-current flows into the LT3046 and no negative voltage appears at the load. The device protects itself and the load.
3	B3	EN/UV	Enable and UVLO. Pulling the EN/UV pin low moves the LT3046 to shutdown mode. Quiescent current in shutdown mode drops to 26µA and the output voltage turns off. Alternatively, the EN/UV pin can set an input supply undervoltage lockout (UVLO) threshold by using a resistor divider between IN, EN/UV, and GND. The LT3046 typically turns on when the EN/UV voltage exceeds 1.27V on its rising edge, with a 110mV hysteresis on its falling edge. The EN/UV pin can be driven above the input voltage and maintain proper functionality. If unused, connect EN/UV to IN. Do not float the EN/UV pin.
4	Ba2	DNC	Do not connect.
5	E3	PG	Power Good. PG is an open-drain flag that indicates output voltage regulation. PG pulls low if PGFB is less than 298mV. If the power good functionality is not needed, float the PG pin. A parasitic substrate diode exists between PG and GND pins of the LT3046; therefore, do not drive PG more than 0.3V below GND during normal operation or during a fault condition. The PG flag status is valid even if the LT3046 is in shutdown with the PG pin being pulled low.
6	F3	ILIM	Current Limit Programming Pin. Connecting a resistor between ILIM and GND programs the current limit. For best accuracy, Kelvin connect this resistor directly to the GND pin of the LT3046. The programming scale factor is nominally 150mA x kΩ. The ILIM pin sources current proportional (1:520) to the output current. Therefore, ILIM also serves as a current monitoring pin with a 0V to 290mV range. If the programmable current limit functionality is not needed, connect ILIM to GND. A parasitic substrate diode exists between the ILIM and GND pins of the LT3046; therefore, do not drive ILIM more than 0.3V below GND during normal operation or during a fault condition.

PIN		NAME	DESCRIPTION
DFN	WLCSP		
7	F1	PGFB	Power Good Feedback. The PG pin pulls high if PGFB increases beyond 298mV on its rising edge, with 7mV hysteresis on its falling edge. Connecting an external resistor divider between OUT, PGFB, and GND sets the programmable power good threshold with the following transfer function: 0.298V × (1 + R_{PG2}/R_{PG1}). As discussed further in the *Fast Startup* section, PGFB also activates the fast start-up circuitry. Connect PGFB to IN if the power good and fast start-up functions are not needed. In addition, if reverse input protection is additionally required, connect the anode of a 1N4148 diode to IN and its cathode to PGFB. See *Figure 79* for further details. A parasitic substrate diode exists between the PGFB and GND pins of the LT3046; therefore, do not drive PGFB more than 0.3V below GND during normal operation or during a fault condition.
8	Ea2	SET	The inverting input of the error amplifier and the regulation set-point for the LT3046. SET sources a precision 100µA current that flows through an external resistor connected between SET and GND. The output voltage of the LT3046 is determined by $V_{SET} = I_{SET} \times R_{SET}$. The output voltage range is from 0.2V to 19V. Adding a capacitor from SET to GND improves noise, PSRR and transient response at the expense of increased start-up time. For optimum load regulation, Kelvin connect the ground side of the SET pin resistor directly to the load. A parasitic substrate diode exists between the SET and GND pins of the LT3046; therefore, do not drive SET more than 0.3V below GND during normal operation or during a fault condition.
9	E1	GND	Ground.
10	B1	OUTS	Output Sense. The OUTS pin is the noninverting input to the error amplifier. For optimal transient performance and load regulation, Kelvin connect OUTS directly to the output capacitor and the load. In addition, connect the GND connections of the output capacitor and the SET pin capacitor directly together. A parasitic substrate diode exists between the OUTS and GND pins of the LT3046; therefore, do not drive OUTS more than 0.3V below GND during normal operation or during a fault condition.
11, 12	A1, Aa2	OUT	Output. The OUT pins supply power to the load. For stability, use a minimum 4.7µF output capacitor with an ESR below 20mΩ and an ESL below 2nH. Large load transients require larger output capacitance to limit peak voltage transients. See the *Stability and Output Capacitance* section for more information on output capacitance. A parasitic substrate diode exists between the OUT and GND pins of the LT3046; therefore, do not drive OUT more than 0.3V below GND during normal operation or during a fault condition.
13	N/A	EPAD (GND)	Exposed Pad. The exposed pad is an electrical connection to GND. To ensure proper electrical and thermal performance, solder the exposed backside to the PCB ground and connect it directly to the GND pin.

TYPICAL PERFORMANCE CHARACTERISTICS

(T_J = +25°C, unless otherwise noted.)

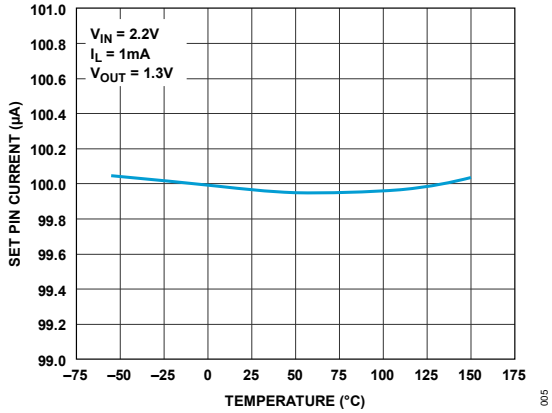


Figure 5. SET Pin Current vs. Temperature

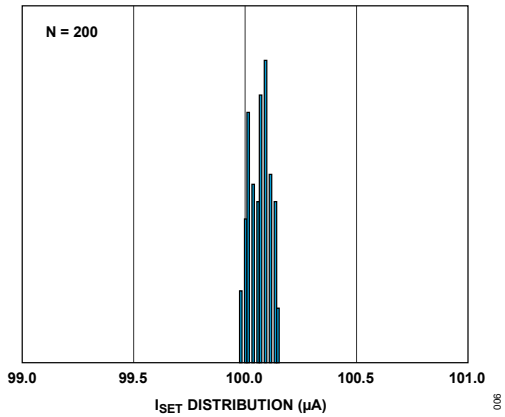


Figure 6. I_{SET} Distribution

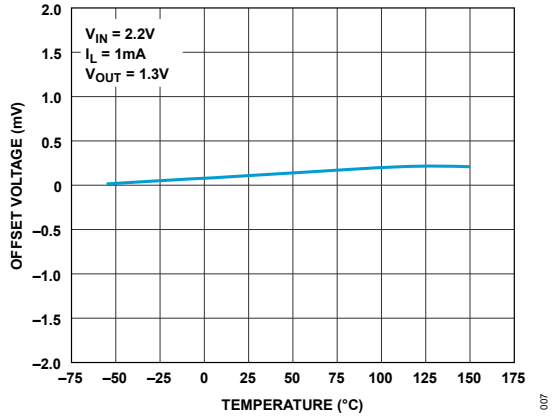


Figure 7. Offset Voltage (V_{OUT} - V_{SET}) vs. Temperature

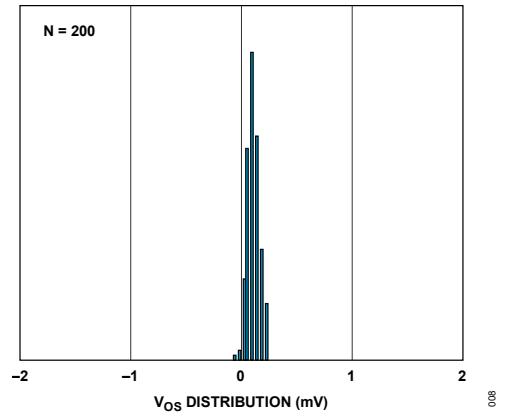


Figure 8. Offset Voltage (V_{OS}) Distribution

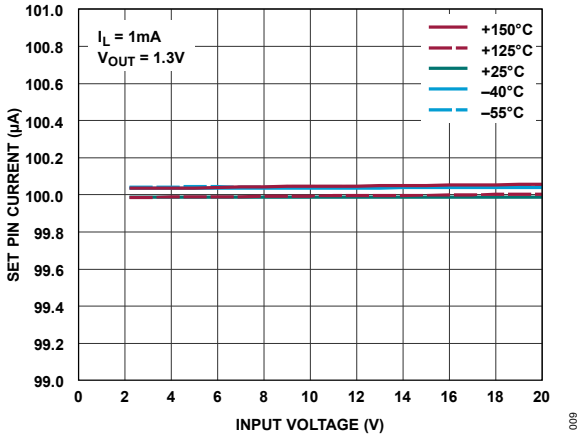


Figure 9. SET Pin Current vs. Input Voltage

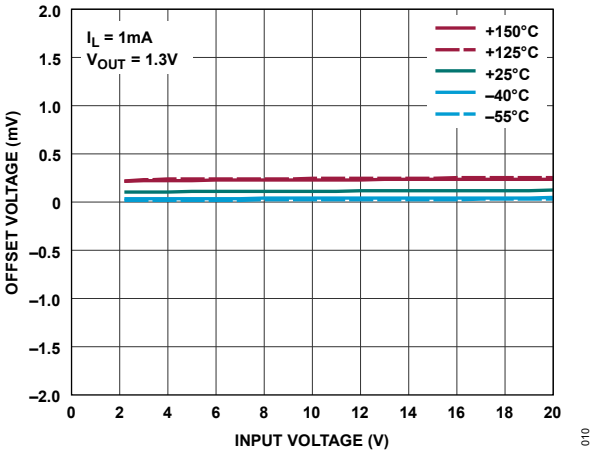


Figure 10. Offset Voltage (V_{OUT} - V_{SET}) vs. Input Voltage

(T_J = +25°C, unless otherwise noted.)

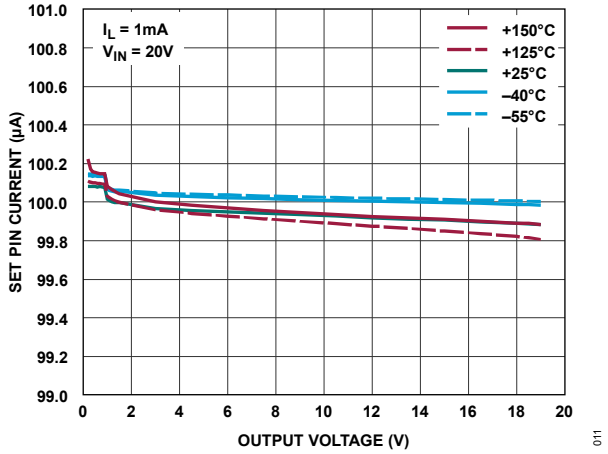


Figure 11. SET Pin Current vs. Output Voltage

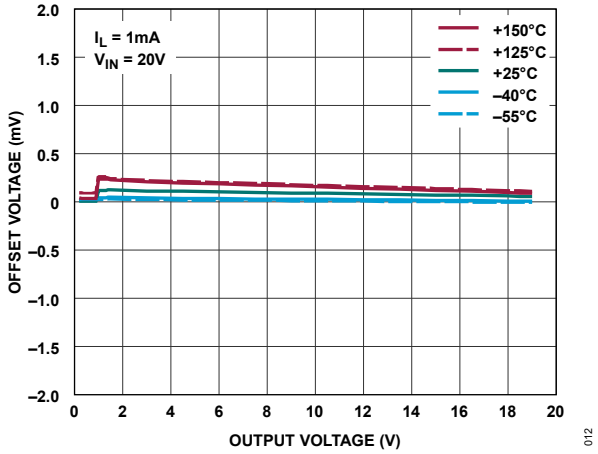


Figure 12. Offset Voltage (V_{OUT} - V_{SET}) vs. Output Voltage

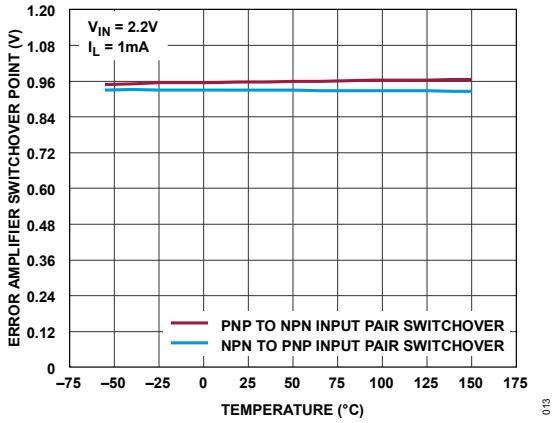


Figure 13. Error Amplifier Switchover Point vs. Temperature

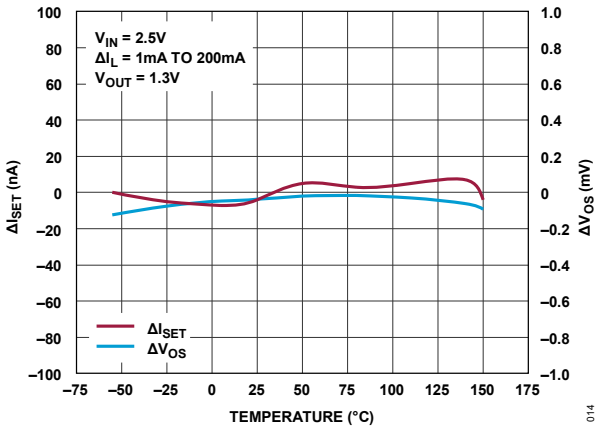


Figure 14. ΔI_{SET} and ΔV_{OS} Load Regulation vs. Temperature

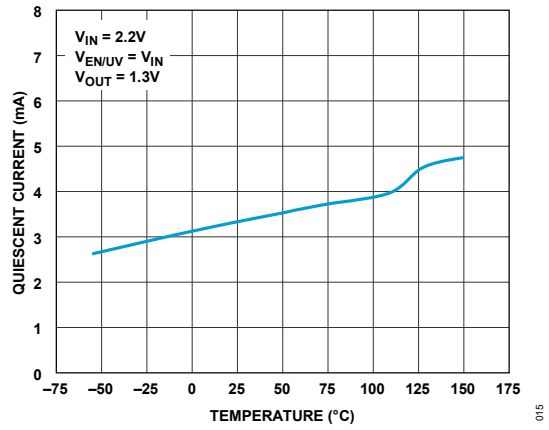


Figure 15. Quiescent Current vs. Temperature ($V_{EN/UV}$ = V_{IN})

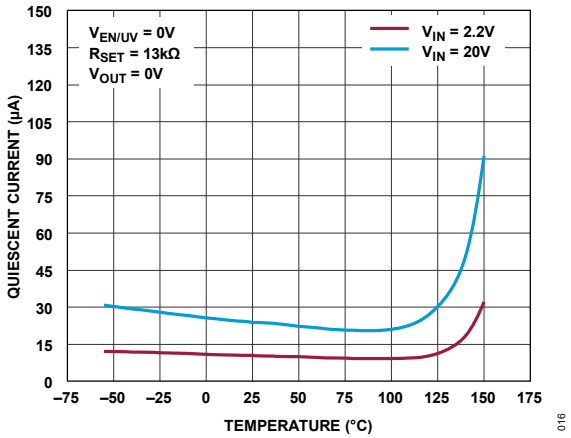


Figure 16. Quiescent Current vs. Temperature ($V_{EN/UV}$ = 0V)

(T_J = +25°C, unless otherwise noted.)

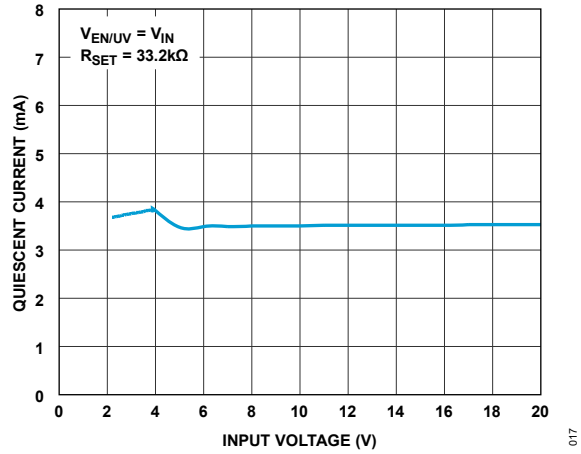


Figure 17. Quiescent Current vs. Input Voltage

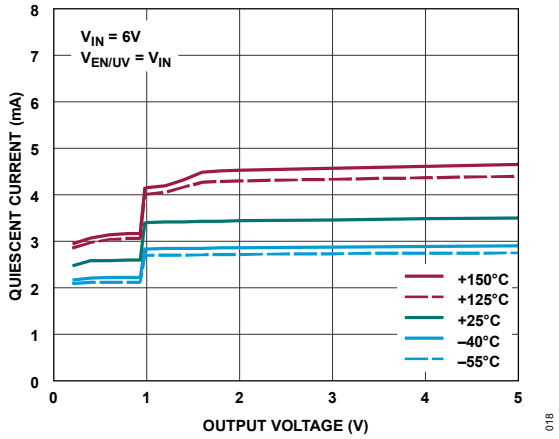


Figure 18. Quiescent Current vs. Output Voltage

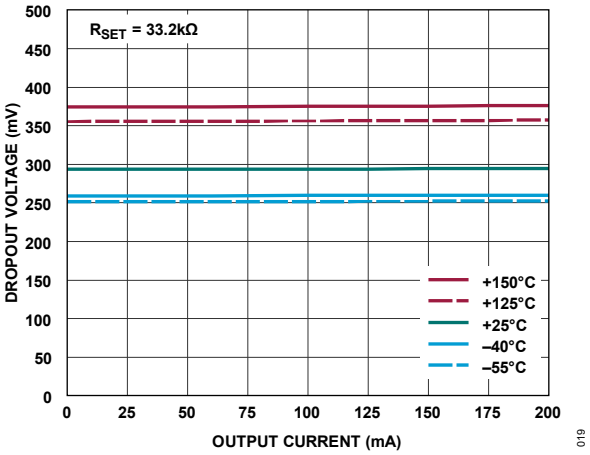


Figure 19. Dropout Voltage vs. Output Current

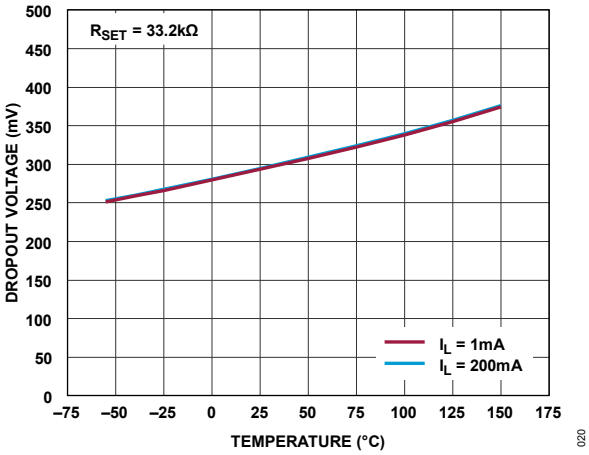


Figure 20. Dropout Voltage vs. Temperature

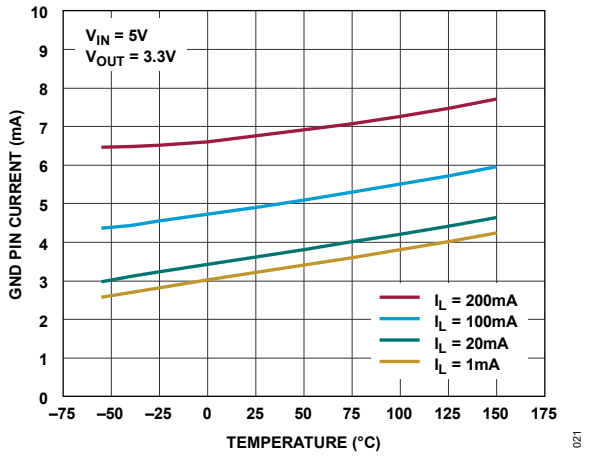


Figure 21. GND Pin Current vs. Temperature

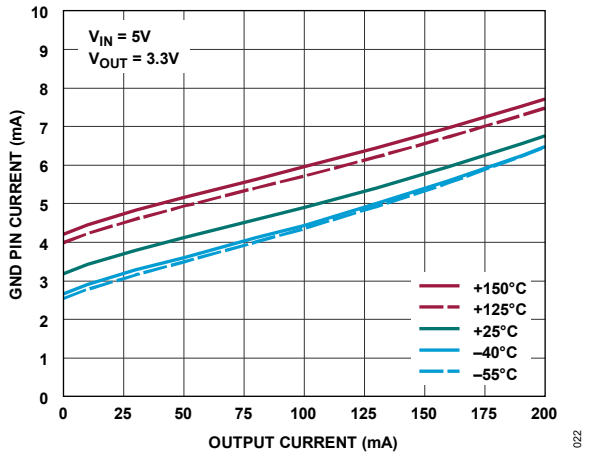


Figure 22. GND Pin Current vs. Output Current

(T_J = +25°C, unless otherwise noted.)

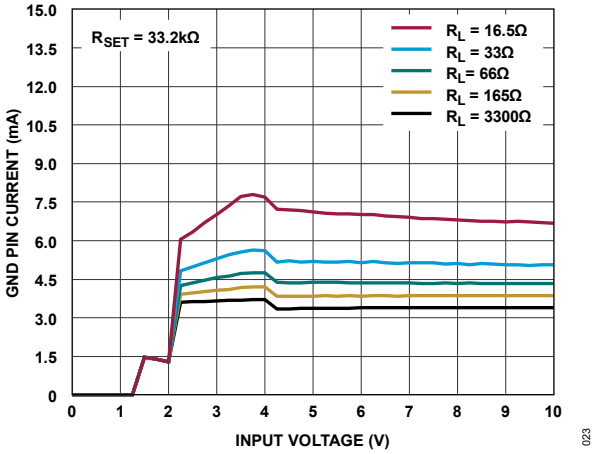


Figure 23. GND Pin Current vs. Input Voltage

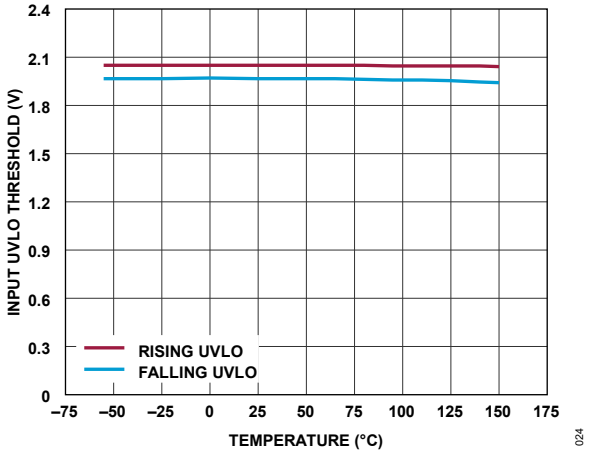


Figure 24. Input UVLO Threshold vs. Temperature

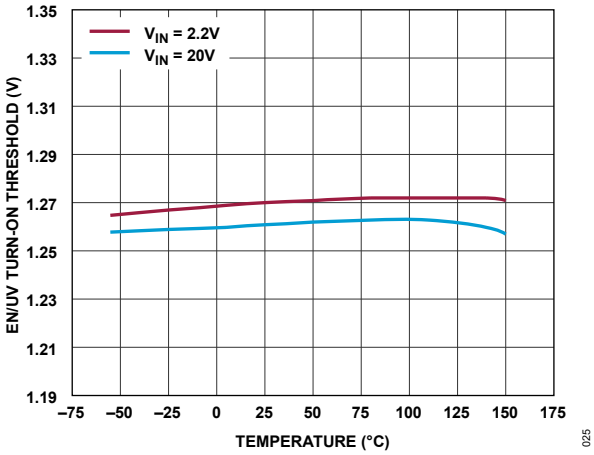


Figure 25. EN/UV Turn-On Threshold vs. Temperature

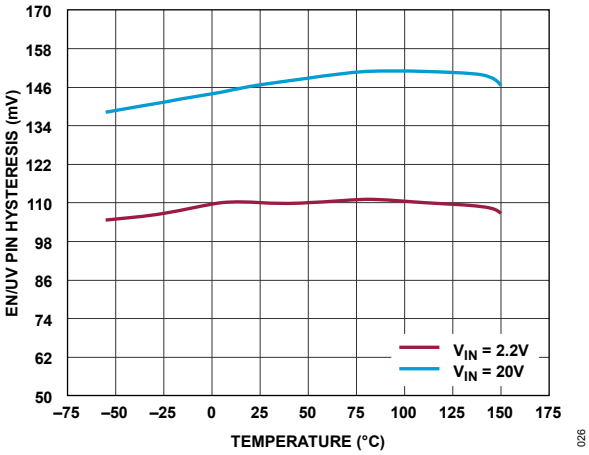


Figure 26. EN/UV Pin Hysteresis vs. Temperature

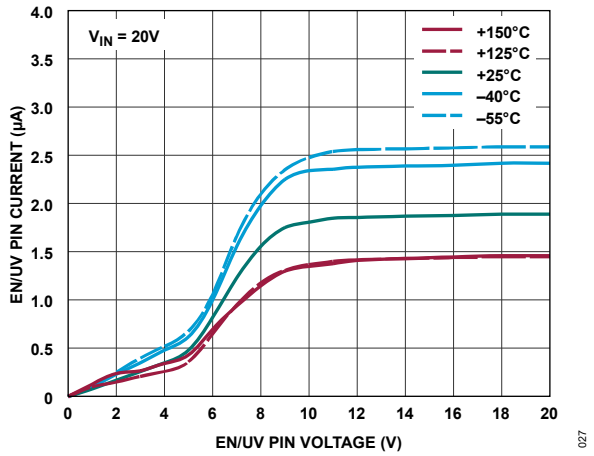


Figure 27. EN/UV Pin Current vs. EN/UV Pin Voltage (Temperature Steps)

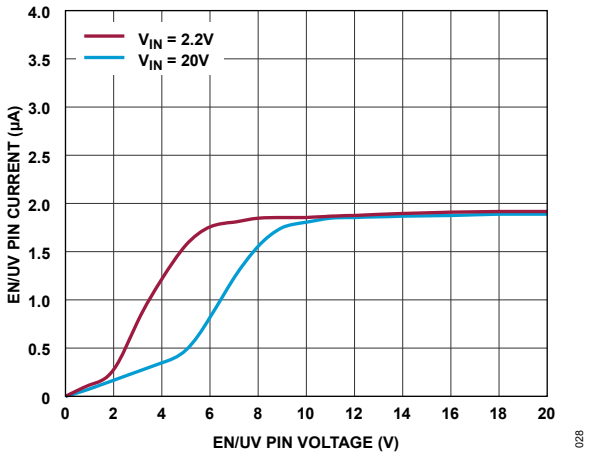


Figure 28. EN/UV Pin Current vs. EN/UV Pin Voltage (V_{IN} Steps)

(T_J = +25°C, unless otherwise noted.)

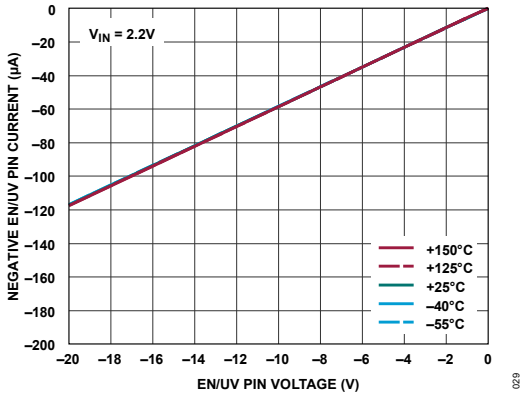


Figure 29. Negative EN/UV Pin Current vs. EN/UV Pin Voltage

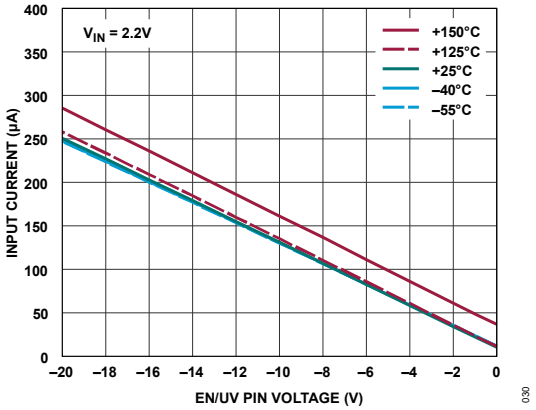


Figure 30. Input Current vs. EN/UV Pin Voltage

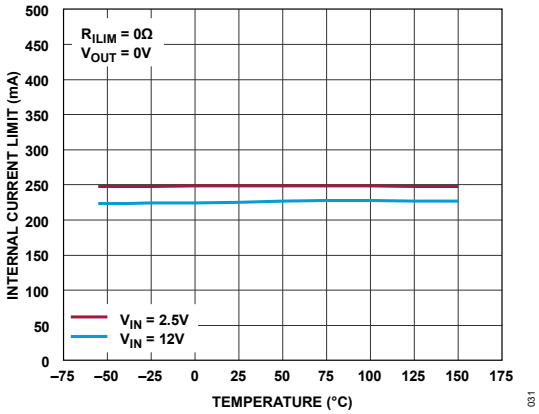


Figure 31. Internal Current Limit vs. Temperature

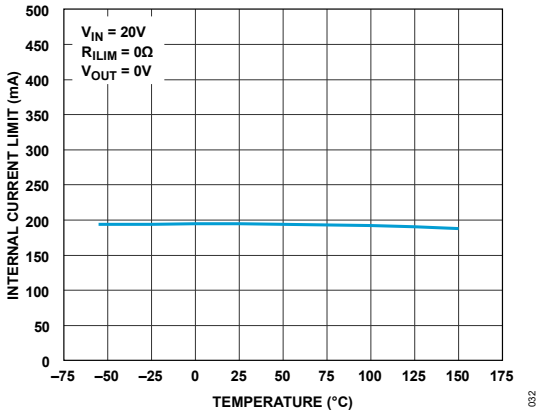


Figure 32. Internal Current Limit vs. Temperature (Foldback)

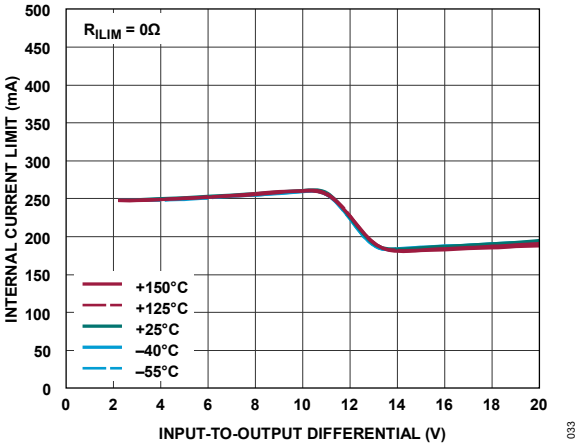


Figure 33. Internal Current Limit vs. Input-to-Output Differential

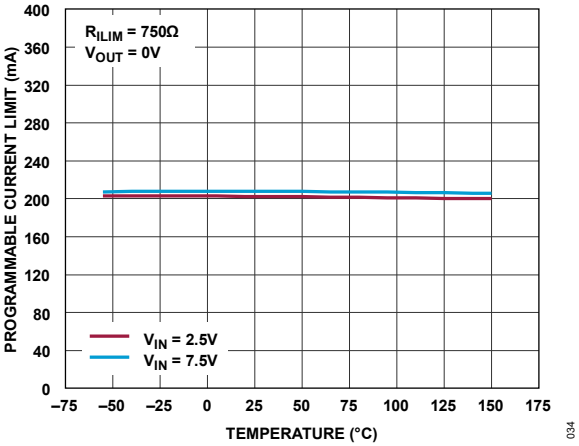


Figure 34. Programmable Current Limit vs. Temperature (200mA)

(T_J = +25°C, unless otherwise noted.)

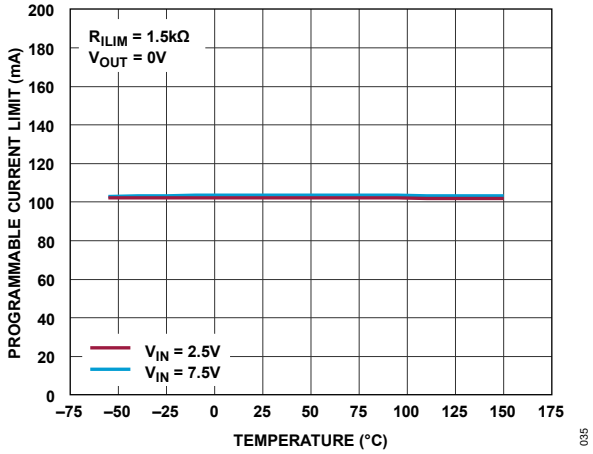


Figure 35. Programmable Current Limit vs. Temperature (100mA)

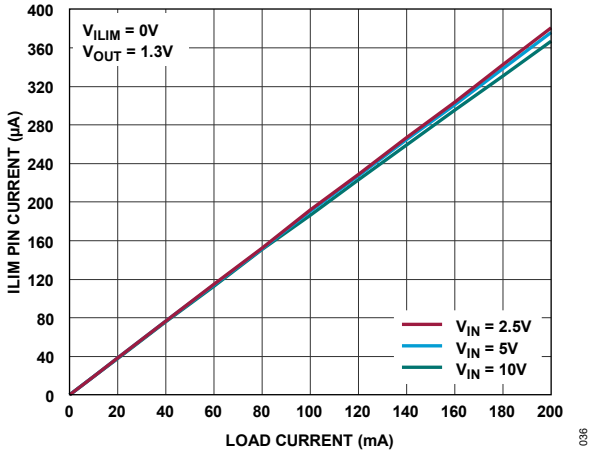


Figure 36. ILIM Pin Current vs. Load Current

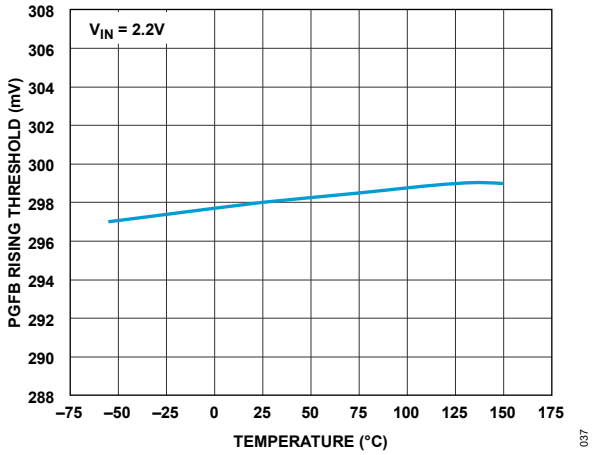


Figure 37. PGFB Rising Threshold vs. Temperature

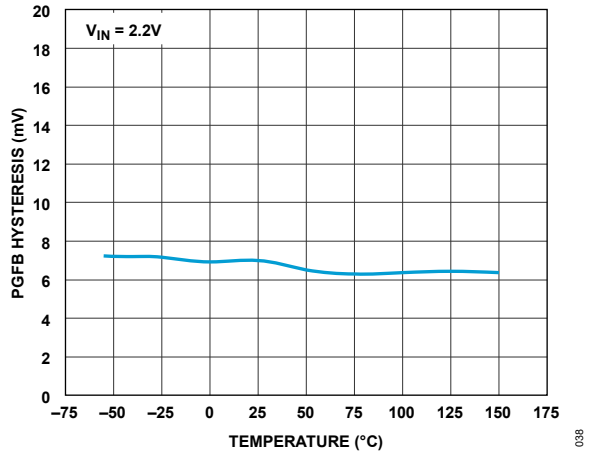


Figure 38. PGFB Hysteresis vs. Temperature

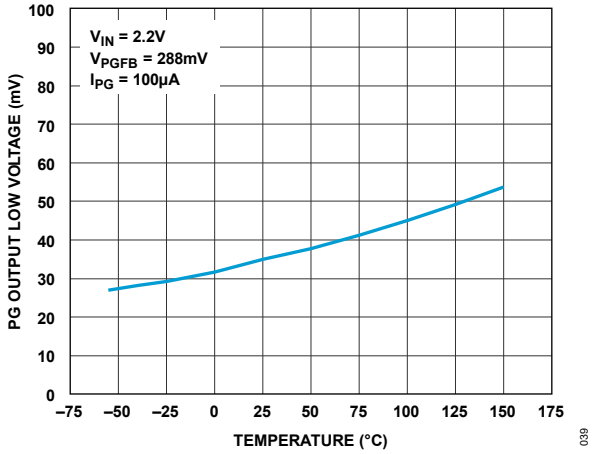


Figure 39. PG Output Low Voltage vs. Temperature

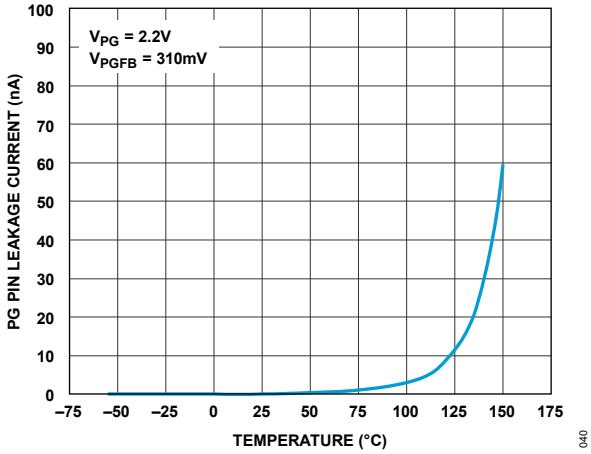


Figure 40. PG Pin Leakage Current vs. Temperature

(T_J = +25°C, unless otherwise noted.)

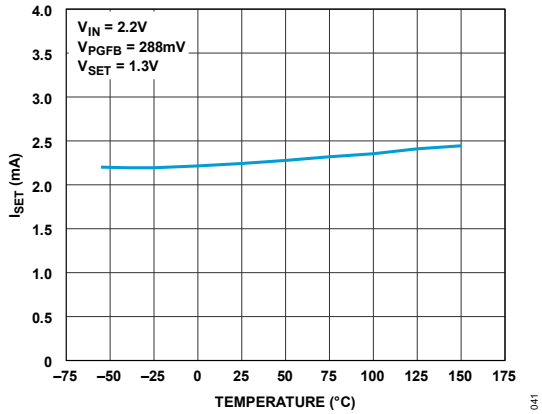


Figure 41. I_{SET} During Start-Up with Fast Start-Up Enabled vs. Temperature

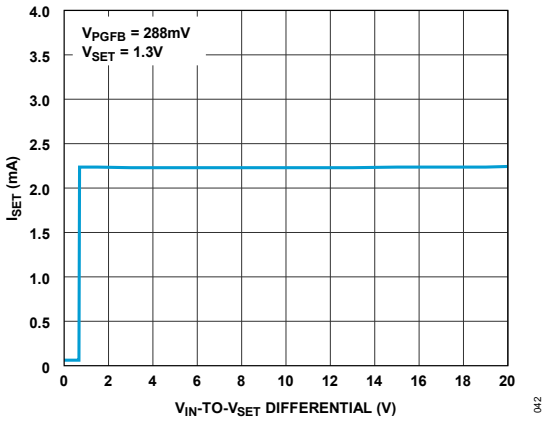


Figure 42. I_{SET} During Start-Up with Fast Start-Up Enabled vs. V_{IN}-to-V_{SET} Differential

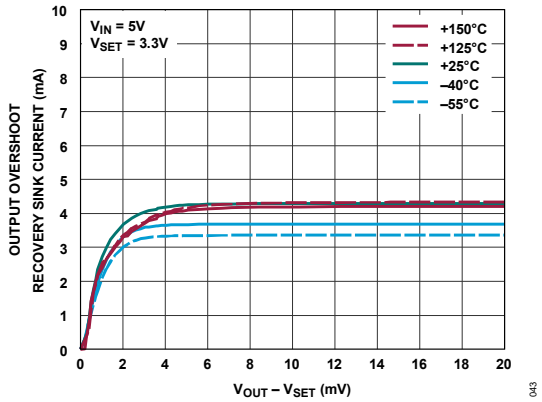


Figure 43.Output Overshoot Recovery Sink Current vs. VOUT - VSET

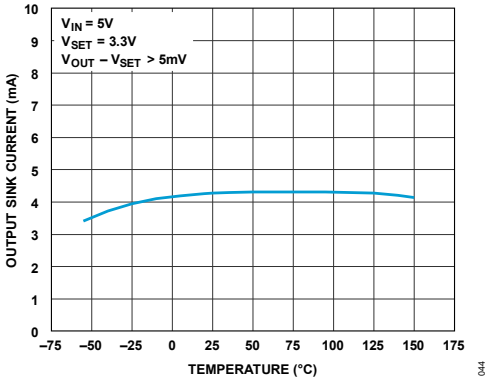


Figure 44. Output Overshoot Recovery Sink Current vs. Temperature

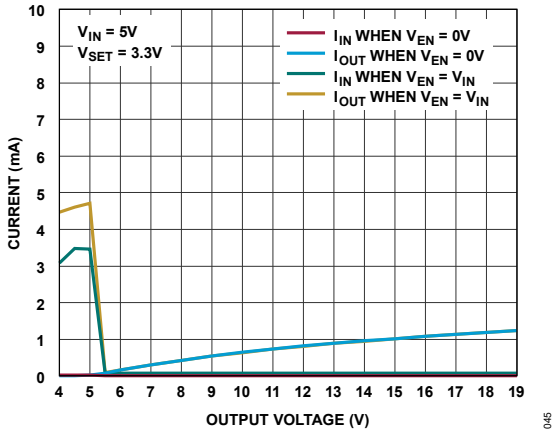


Figure 45. Current when V_{OUT} Forced Above $V_{OUT(NOMINAL)}$ vs. Output Voltage (I_{IN} Is the Input Current, and I_{OUT} Is the Output Current)

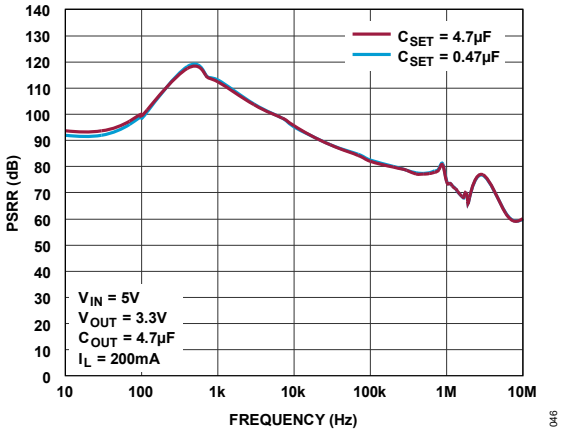


Figure 46. PSRR vs. Frequency (C_{SET} Steps)

(T_J = +25°C, unless otherwise noted.)

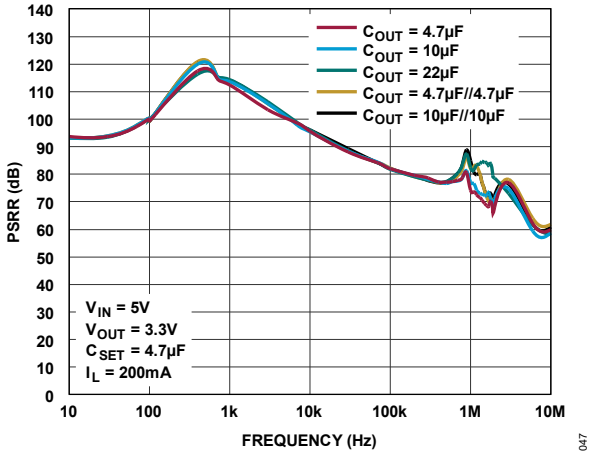


Figure 47. PSRR vs. Frequency (C_{OUT} Steps)

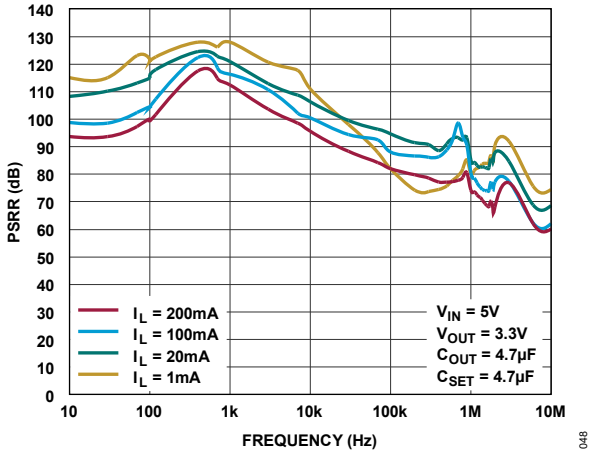


Figure 48. PSRR vs. Frequency (I_L Steps)

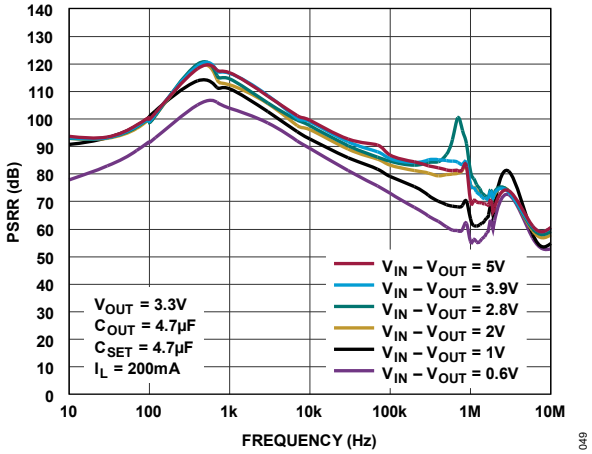


Figure 49. PSRR vs. Frequency (V_{IN} – V_{OUT} Steps)

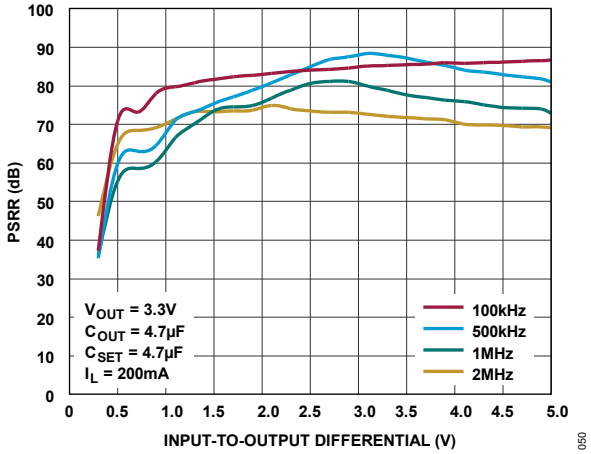


Figure 50. PSRR vs. Input-to-Output Differential

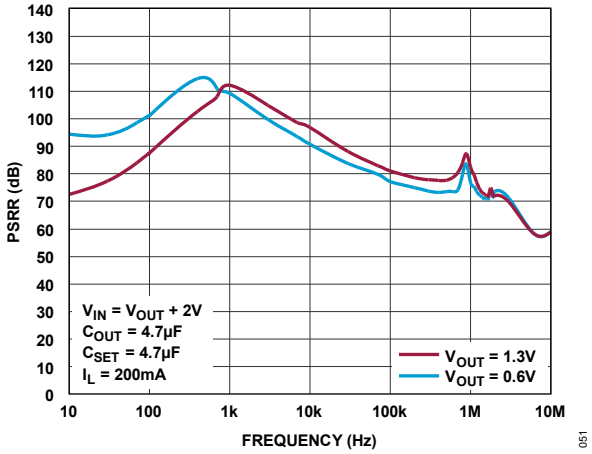


Figure 51. PSRR as a Function of an Error Amplifier Input Pair vs. Frequency

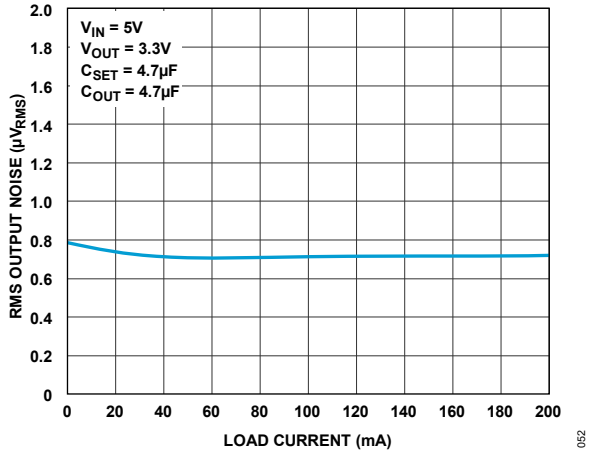


Figure 52. Integrated RMS Output Noise (10Hz to 100kHz) vs. Load Current

(T_J = +25°C, unless otherwise noted.)

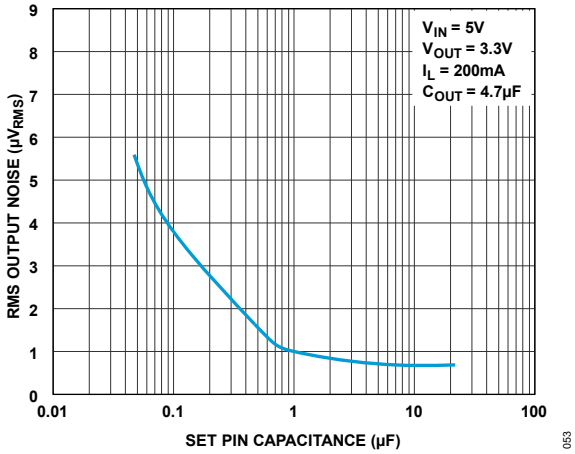


Figure 53. Integrated RMS Output Noise (10Hz to 100kHz) vs. SET Pin Capacitance

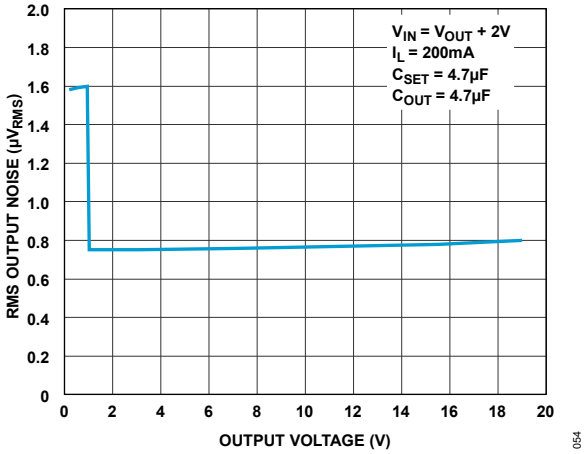


Figure 54. Integrated RMS Output Noise (10Hz to 100kHz) vs. Output Voltage

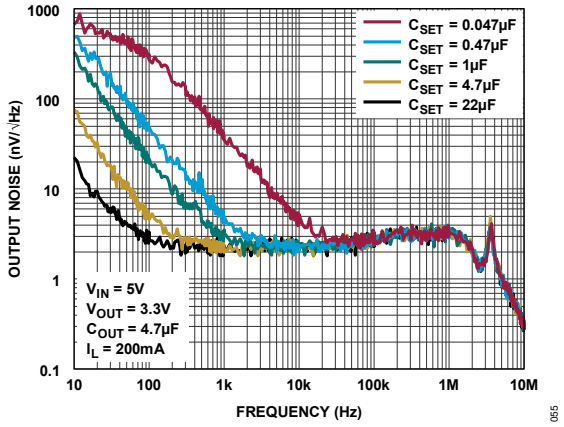


Figure 55. Output Noise vs. Frequency (C_{SET} Steps)

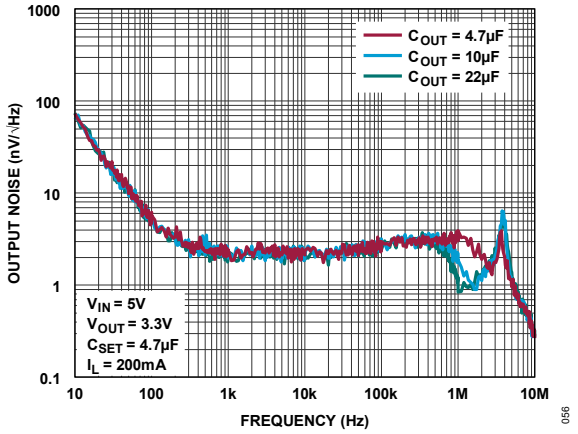


Figure 56. Output Noise vs. Frequency (C_{OUT} Steps)

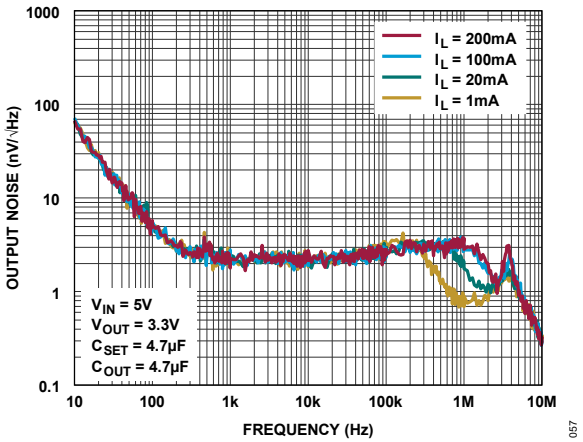


Figure 57. Output Noise vs. Frequency (I_L Steps)

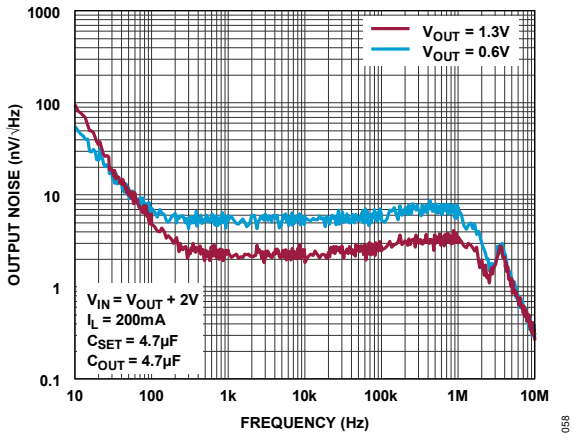


Figure 58. Output Noise as a Function of an Error Amplifier Input Pair vs. Frequency

(T_J = +25°C, unless otherwise noted.)

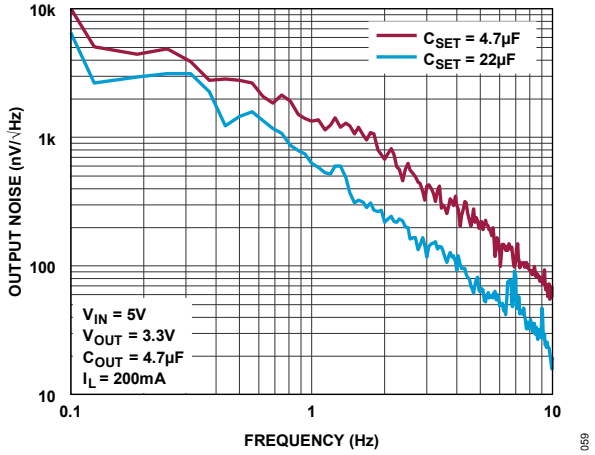


Figure 59. Output Noise (0.1Hz to 10Hz) vs. Frequency

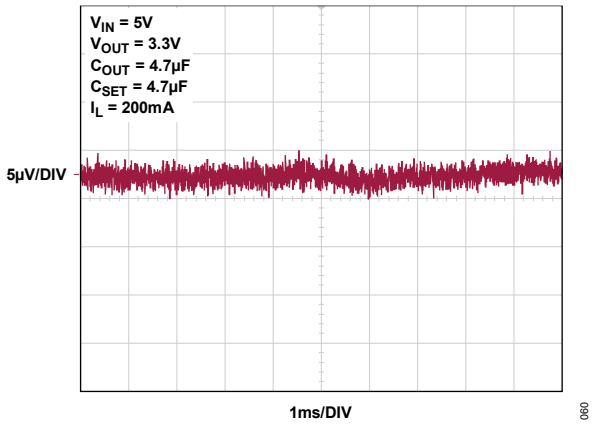


Figure 60. Output Noise: 10Hz to 100kHz

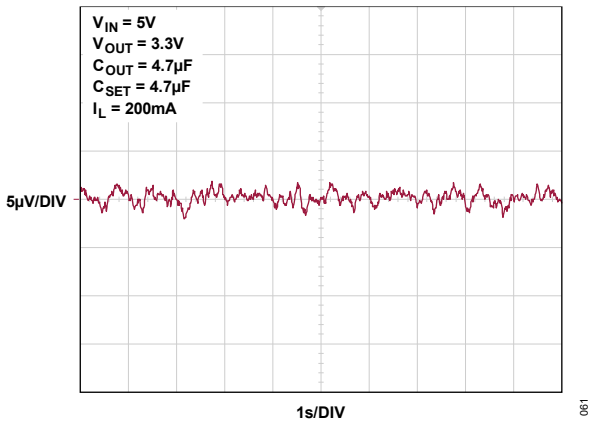


Figure 61. Output Noise: 0.1Hz to 10Hz (C_{SET} = 4.7µF)

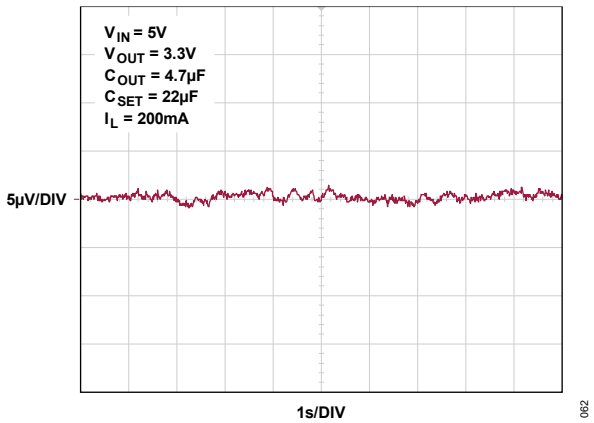


Figure 62. Output Noise: 0.1Hz to 10Hz (C_{SET} = 22µF)

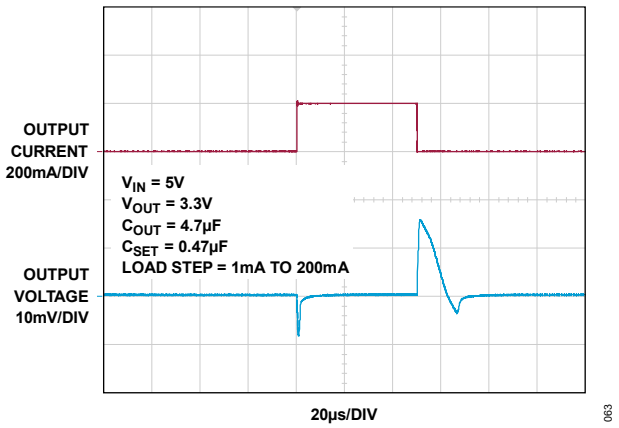


Figure 63. Load-Transient Response

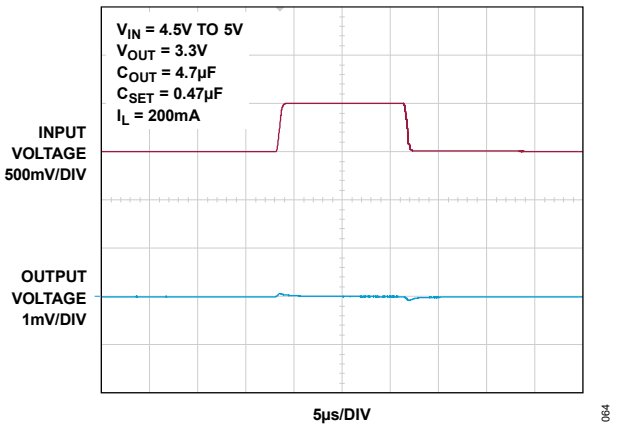


Figure 64. Line-Transient Response

(T_J = +25°C, unless otherwise noted.)

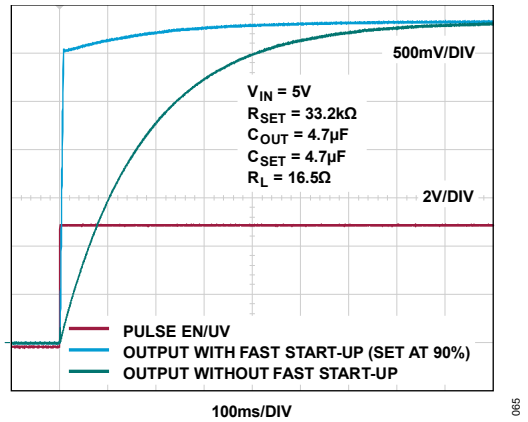


Figure 65. Start-Up Time With and Without Fast Start-Up Circuitry for Large C_{SET}

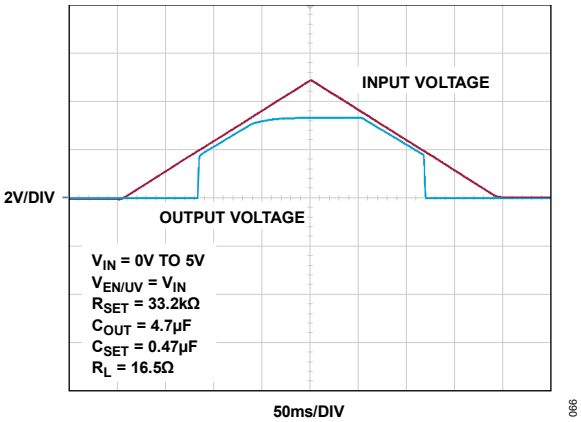


Figure 66. Input Supply Ramp-Up and Ramp-Down

THEORY OF OPERATION

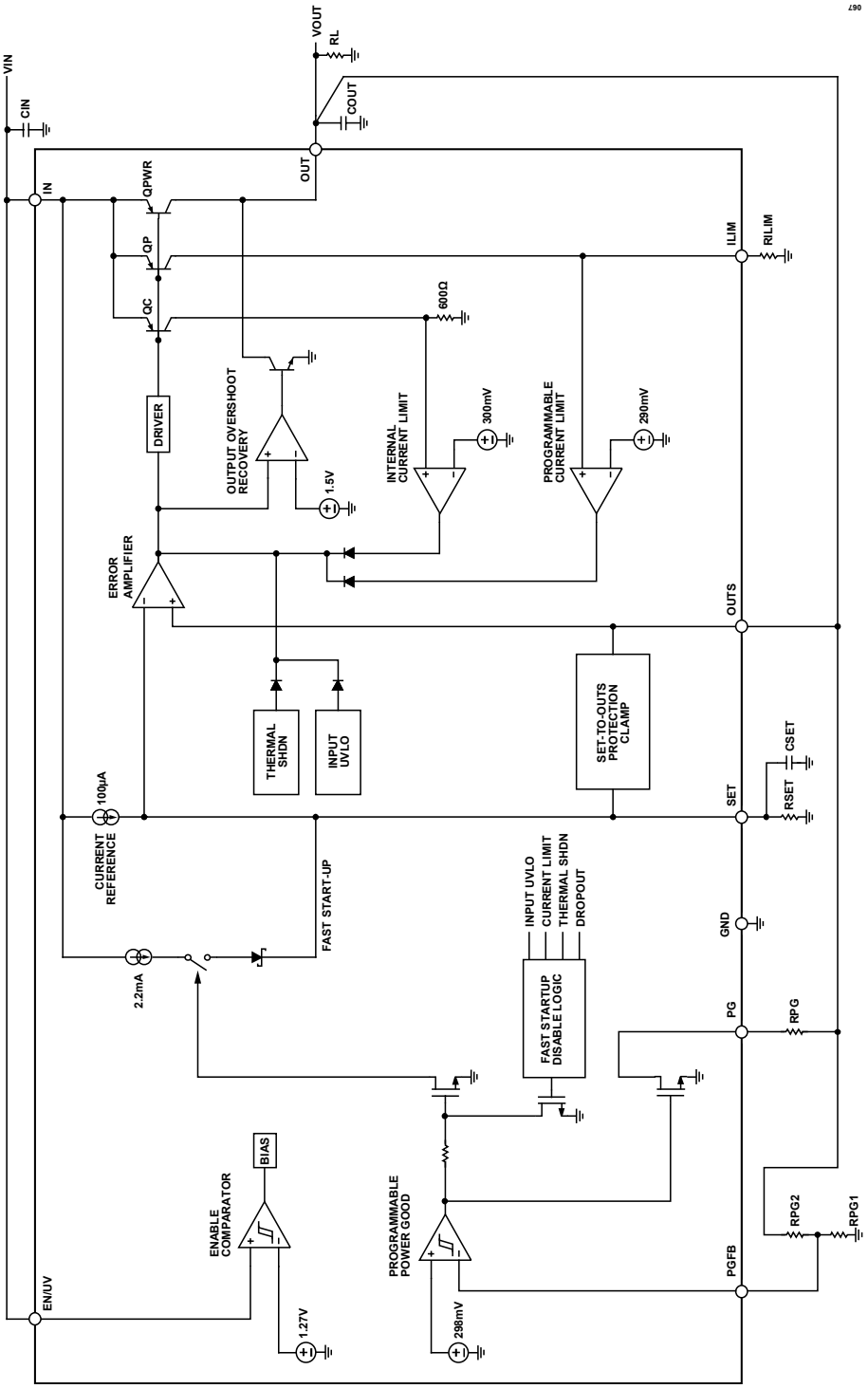


Figure 67. Functional Block Diagram

APPLICATIONS INFORMATION

The LT3046 is a high-performance, low-dropout, linear regulator featuring Analog Devices' ultra-low noise (2.2nV/√Hz at 10kHz) and ultra-high PSRR (82dB at 1MHz) architecture for powering noise-sensitive applications. Designed as a precision current source followed by a high-performance rail-to-rail voltage buffer, the LT3046 can be easily paralleled to further reduce noise, increase output current, and spread heat on the PCB. The device additionally features programmable current limit, fast start-up capability, and programmable power good.

The LT3046 is easy to use and incorporates all of the protection features expected in high-performance regulators. Included are short-circuit protection, safe operating area protection, reverse-battery protection, reverse-current protection, and thermal shutdown with hysteresis.

Output Voltage

The LT3046 incorporates a precision 100µA current source flowing out of the SET pin, which also connects to the inverting input of the error amplifier. *Figure 68* illustrates that connecting a resistor from SET to ground generates a reference voltage for the error amplifier. This reference voltage is the product of the SET pin current and the SET pin resistor. The unity-gain configuration of the error amplifier produces a low-impedance version of this voltage on its noninverting input, that is, the OUTS pin, which is externally connected to the OUT pin.

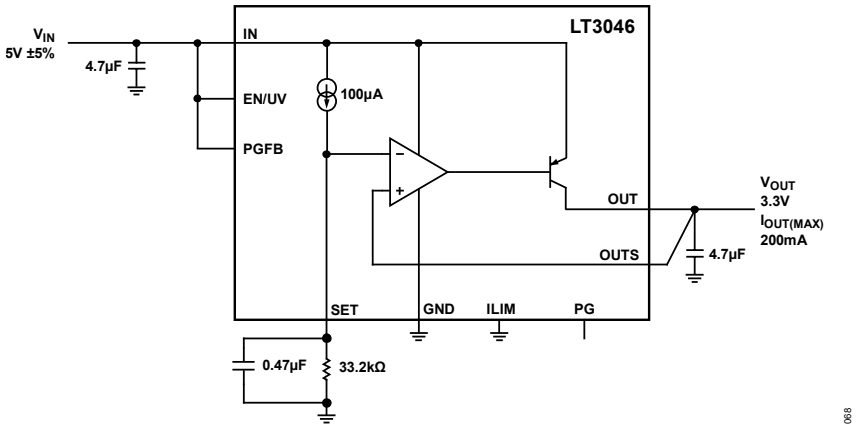


Figure 68. Basic Adjustable Regulator

The rail-to-rail error amplifier and current reference of the LT3046 allows for a wide output-voltage range from 0.2V to V_{IN} minus dropout, up to 19V. A PNP-based input pair is active for a 0.2V to ~0.95V output and an NPN-based input pair is active for output voltages greater than ~0.95V, with an abrupt transition between the two input pairs at ~0.95V output with approximately 28mV of hysteresis. While the NPN-based input pair is designed to offer the best overall performance, see *Table 1* for details on the offset voltage, SET pin current, output noise, and PSRR variation with the error-amplifier input pair. *Table 5* lists many common output voltages and their corresponding 1% R_{SET} resistors.

Table 5. ***1% Resistor for Common Output Voltages***

V_{OUT} (V)	R_{SET} (kΩ)
2.5	24.9
3.3	33.2
5	49.9
12	121
15	150
18	180

The benefit of using a current reference compared to the typical voltage reference used in conventional regulators is that the regulator always operates in a unity-gain configuration, independent of the programmed output voltage. This configuration allows the LT3046 to have loop gain, frequency response, and bandwidth independent of the output voltage. As a result, noise, PSRR, and transient performance do not change with output voltage. Moreover, because none of the error-amplifier gain is needed to amplify the SET pin voltage to a higher output voltage, output load regulation is more tightly specified in the hundreds of microvolts range and not as a fixed percentage of the output voltage.

Because the zero temperature-coefficient current source is highly accurate, the SET pin resistor can become a limiting factor in achieving high accuracy. Therefore, the SET pin resistor must be a precision resistor. Additionally, any leakage paths to or from the SET pin create errors in the output voltage. If necessary, use high-quality insulation (for example, Teflon™ or KEL-F®). Moreover, cleaning of all insulating surfaces to remove fluxes and other residues can be required. High humidity environments can require a surface coating at the SET pin to provide a moisture barrier.

Minimize board leakage by encircling the SET pin with a guard ring that operates at a potential close to itself, ideally connected to the OUT pins. Guarding both sides of the circuit board is recommended. Bulk leakage reduction depends on the guard-ring width. Leakages of 100nA into or out of the SET pin creates a 0.1% error in the reference voltage. Leakages of this magnitude, coupled with other sources of leakage, can cause significant errors in the output voltage, especially over a wide operating temperature range. *Figure 69* illustrates a typical guard-ring layout technique.

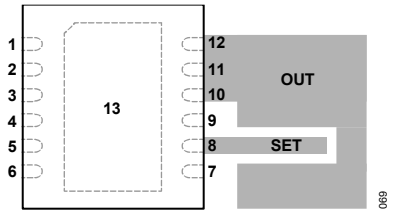


Figure 69. DFN Guard Ring Layout

Because the SET pin is a high-impedance node, unwanted signals can couple into the SET pin and cause erratic behavior, which is most noticeable when operating with a minimum output capacitor at heavy load currents. Bypassing the SET pin with a small capacitance to ground resolves this issue, 10nF is sufficient. For applications requiring higher accuracy or an adjustable output voltage, the SET pin can be actively driven by an external voltage source capable of sinking 100µA. Connecting a precision-voltage reference to the SET pin eliminates any errors present in the output voltage due to the reference current and SET pin resistor tolerances.

Output Sensing and Stability

The OUTS pin of the LT3046 provides a Kelvin-sense connection to the output. The GND side of the SET pin resistor provides a Kelvin-sense connection to the GND side of the load.

Additionally, for ultra-high PSRR, the LT3046 bandwidth is made quite high (~1 MHz), making it close to the self-resonance frequency (~2.3 MHz) of a typical 4.7µF (1206 case size), ceramic, output capacitor. Therefore, it is important to avoid adding extra impedance (ESR and ESL) outside the feedback loop. To that end, as shown in *Figure 70*, minimize the effects of PCB trace and solder inductance by connecting the OUTS pin directly to C_{OUT} and the GND side of C_{SET} directly to the GND side of C_{OUT}. Also keep the GND sides of C_{IN} and C_{OUT} reasonably close. Refer to the LT3046 evaluation board user guide (*LT3046EVK*) for more information on the recommended layout that meets these requirements. While the LT3046 is robust enough not to oscillate if the recommended layout is not followed, depending on the actual layout, phase and gain margin, noise, and PSRR performance can degrade.

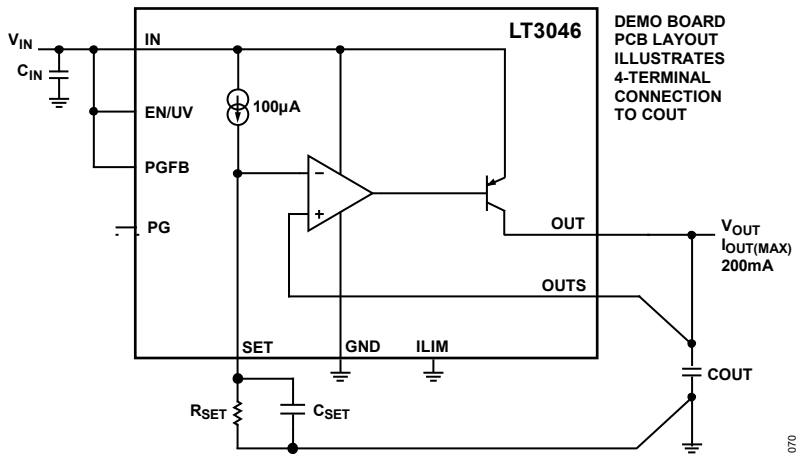


Figure 70. C_{OUT} and C_{SET} Connections for Best Performance

Stability and Output Capacitance

The LT3046 requires an output capacitor for stability. Given its high bandwidth, Analog Devices recommends low ESR and ESL ceramic capacitors. A minimum of 4.7µF effective capacitance with an ESR of less than 20mΩ and an ESL of less than 2nH is required for stability.

Given the high PSRR and low-noise performance attained using a single 4.7µF ceramic-output capacitor, larger values of output capacitors are not necessary. However, these capacitors can still improve the performance. See the *Typical Performance Characteristics* section for additional information. Moreover, larger value output capacitance decreases peak-output deviations during a load transient. Note that bypass capacitors used to decouple individual components powered by the LT3046 increase the effective-output capacitance.

Give extra consideration to the type of ceramic capacitors used. The capacitors are manufactured with a variety of dielectrics, each with different behaviors across temperature and applied voltage. The most common dielectrics used are specified with Electronic Industries Alliance (EIA) temperature characteristic codes of Z5U, Y5V, X5R, and X7R. The Z5U and Y5V dielectrics are good for providing high capacitance in small packages, but these dielectrics tend to have stronger voltage and temperature coefficients as shown in *Figure 71* and *Figure 72*. When used with a 5V regulator, a 16V, 10µF Y5V capacitor can exhibit an effective value as low as 1µF to 3µF for the DC bias voltage applied over the operating temperature range.

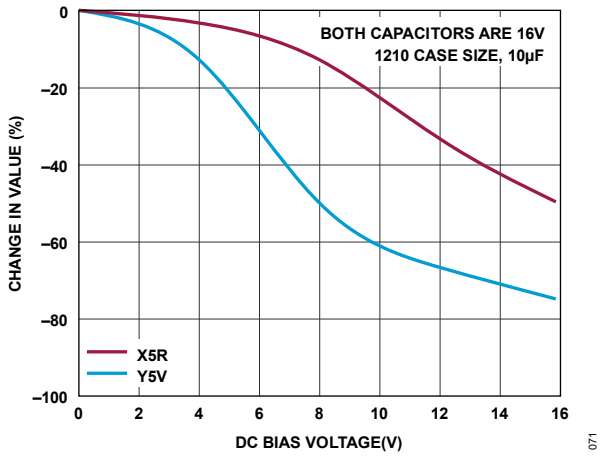


Figure 71. Ceramic Capacitor DC Bias Characteristics

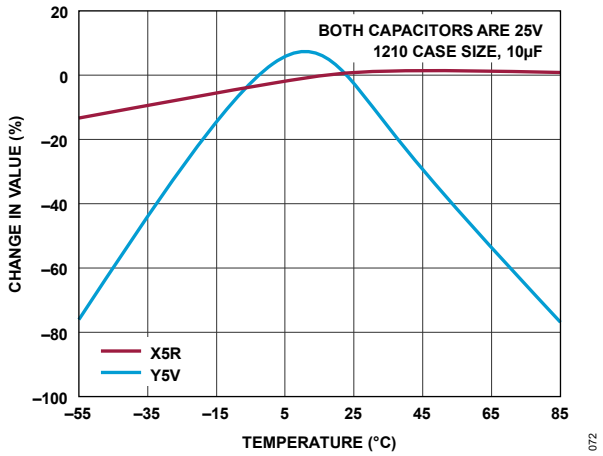


Figure 72. Ceramic Capacitor Temperature Characteristics

X5R and X7R dielectrics result in more stable characteristics and are thus more suitable for the LT3046. The X7R dielectric has better stability across temperature, while the X5R is less expensive and is available in higher values. Nonetheless, care must still be exercised when using X5R and X7R capacitors. The X5R and X7R codes only specify operating temperature range and the maximum capacitance change over temperature. While capacitance changes due to DC bias for X5R and X7R is better than Y5V and Z5U dielectrics, it can still be significant enough to drop capacitance to below sufficient levels. As shown in *Figure 73*, capacitor DC bias characteristics tend to improve as component case size increases. However, verification of expected capacitance at the operating voltage is highly recommended. Due to its good voltage coefficient in small case sizes, Analog Devices recommends using the Murata GCM series ceramic capacitors.

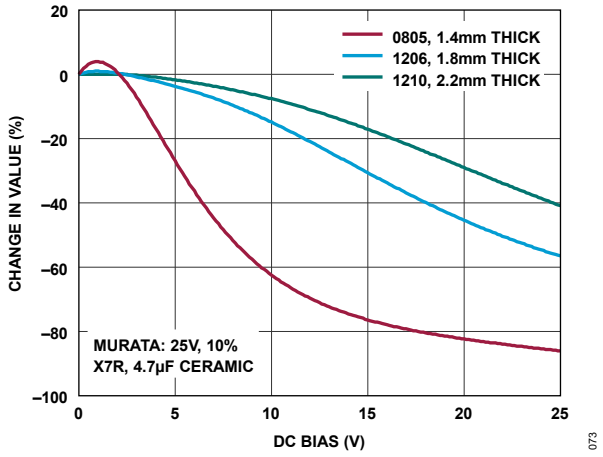


Figure 73. Capacitor Voltage Coefficient for Different Case Sizes

High Vibration Environments

Voltage and temperature coefficients are not the only sources of problems. Some ceramic capacitors have a piezoelectric response. A piezoelectric device generates voltage across its terminals due to mechanical stress, similar to how a piezoelectric microphone works. For a ceramic capacitor, this stress can be induced by mechanical vibrations within the system or due to thermal transients.

LT3046 applications in high-vibration environments have three distinct, piezoelectric noise generators: ceramic output, input, and SET pin capacitors. However, due to the low output impedance over a wide frequency range of the LT3046, negligible output noise is generated using a ceramic-output capacitor. Similarly, due to the ultra-high PSRR of the LT3046, negligible output noise is generated using a ceramic-input capacitor. Nonetheless, given the high SET pin impedance, any piezoelectric response from a ceramic SET pin capacitor generates significant output noise, peak-to-peak excursions of hundreds of mV. However, due to the high ESR and ESL tolerance of the SET pin capacitor, any nonpiezoelectrically responsive (tantalum, electrolytic, or film) capacitor can be used at the SET pin, although electrolytic capacitors tend to have high 1/f noise. In any case, use of a surface-mount capacitor is highly recommended.

Stability and Input Capacitance

The LT3046 is stable with a minimum 4.7µF IN pin capacitor. Analog Devices recommends using low ESR ceramic capacitors. In cases where long wires connect the power supply to the input and ground terminals of the LT3046, the use of low-value input capacitors combined with a large load current can result in instability. The resonant LC tank circuit formed by the wire inductance and the input capacitor is the cause of this instability and not the LT3046.

The self-inductance, or isolated inductance, of a wire is directly proportional to its length. The wire diameter, however, has less influence on its self-inductance. For example, the self-inductance of a 2-AWG isolated wire with a diameter of 0.26in is about half the inductance of a 30-AWG wire with a diameter of 0.01in. One foot of 30-AWG wire has 465nH of self-inductance.

Several methods exist to reduce the self-inductance of a wire. One method divides the current flowing toward the LT3046 between the two parallel conductors. In this case, placing the wires further apart reduces the inductance; up to a 50% reduction when placed only a few inches apart. Splitting the wires connects two equal inductors in parallel. However, when placed close to each other, their mutual inductance adds to the overall self-inductance of the wires; therefore, a 50% reduction is not possible in such cases. The second and more effective technique to reduce the overall inductance is to place the forward and return current conductors (the input and ground wires) close. Two 30-AWG wires separated by 0.02in reduce the overall inductance to about one-fifth of a single wire.

If a battery mounted close powers the LT3046, a 4.7µF input capacitor suffices for stability. However, if a distantly located supply powers the LT3046, use a larger value input capacitor. Use a rough guideline of 1µF (in addition to the 4.7µF minimum) per 6in of wire length. The minimum input capacitance required to stabilize the application also varies with the output capacitance as well as the load current. Place additional capacitance on the output of the LT3046 to help this issue. However, this method requires significantly more output capacitance compared to additional input bypassing. Series resistance between the supply and the input of the LT3046 also helps stabilize the application. As little as 0.1Ω to 0.5Ω suffices. This impedance dampens the LC tank circuit at the expense of the dropout voltage. A better alternative is to use a higher ESR tantalum or electrolytic capacitor at the input of the LT3046 in parallel with a 4.7µF ceramic capacitor.

PSRR and Input Capacitance

For applications using the LT3046 for post-regulating switching converters, placing a capacitor directly at the input of the LT3046 results in AC current (at the switching frequency) to flow near the LT3046. This relatively high-frequency switching current generates a magnetic field that couples to the output of the LT3046, degrading its effective PSRR. While highly dependent on the PCB, the switching preregulator, and the input capacitance, among other factors, the PSRR degradation can be easily more than 30dB at 1 MHz. This degradation is present even if the LT3046 is desoldered from the board because it effectively degrades the PSRR of the PCB itself. While negligible for conventional, low PSRR, LDO regulators, the ultra-high PSRR of the LT3046 requires careful attention to higher order parasitics to extract the full performance offered by the regulator.

To mitigate the flow of the high-frequency switching current near the LT3046, as long as the output capacitor of the switching converter is located more than an inch away from the LT3046, remove the input capacitor of the LT3046. Magnetic coupling rapidly decreases with increasing distance. Nonetheless, if the switching preregulator is placed too far away (conservatively more than a couple inches) from the LT3046, with no input capacitor present, as with any regulator, the input of the LT3046 oscillates at the parasitic LC resonance frequency. In addition, it is generally a common (and a preferred) practice to bypass the regulator input with some capacitance. Therefore, this option is fairly limited in its scope and not the optimal solution.

To that end, Analog Devices recommends using the LT3046 evaluation board layout for achieving the best possible PSRR performance (refer to the *LT3046EVK* evaluation board user guide). The LT3046 evaluation board layout uses magnetic-field cancellation techniques to prevent PSRR degradation caused by this high-frequency current flow, while using the input capacitor.

Filtering High-Frequency Spikes

For applications where the LT3046 is used to post regulate a switching converter, its high PSRR effectively suppresses any noise present at the switching frequency of the switching converter, typically 100kHz to 4MHz. However, the high-frequency (hundreds of MHz) spikes, beyond the bandwidth of the LT3046, associated with the power-switch transition times of the switching converter almost directly pass through the LT3046. While the output capacitor is intended partly to absorb these spikes, its ESL limits its ability at these frequencies. A ferrite bead or even the inductance associated with a short (for example, 0.5in) PCB trace between the output of the switching converter and the input of the LT3046 can serve as an LC filter to suppress these high-frequency spikes.

Output Noise

The LT3046 offers many advantages with respect to noise performance. Traditional linear regulators have several sources of noise. The most critical noise sources for a traditional regulator are its voltage reference, error amplifier, noise from the resistor-divider network used for setting the output voltage, and the noise gain created by this resistor-divider. Many low-noise regulators pin out their voltage reference to allow for noise reduction by bypassing the reference voltage.

Unlike most linear regulators, the LT3046 does not use a voltage reference. Instead, the LT3046 uses a 100µA current reference. The current reference operates with a typical noise-current level of 20pA/√Hz ($6nA_{RMS}$ over a 10Hz to 100kHz bandwidth). The resultant voltage noise equals the current noise multiplied by the resistor value, which, in turn, is RMS summed with the noise of the error amplifier and the thermal noise of the resistor, √4kTR, where k = Boltzmann constant (1.380649×10^{-23}J/K), and T is the absolute temperature.

One problem that conventional linear regulators face is that the resistor-divider setting the output voltage gains up the reference noise. In contrast, the unity-gain follower architecture of the LT3046 presents no gain from the SET pin to the output. Therefore, if a capacitor bypasses the SET pin resistor, the output noise is independent of the programmed output voltage. The resultant output noise is then set only by the noise of the error amplifier, typically 2.2nV/√Hz from a 10kHz to 1MHz bandwidth and 0.8μV_{RMS} from a 10Hz to 100kHz bandwidth using a 4.7µF SET pin capacitor. Paralleling multiple LT3046 devices further reduces noise by √N, for N parallel regulators.

See *Figure 52*, *Figure 53*, *Figure 55*, *Figure 57*, and *Figure 59* for the noise spectral density (for the 10Hz to 10MHz frequency range and for the 0.1Hz to 10Hz 1/f noise frequency range) and RMS integrated noise over various load currents and SET pin capacitance information.

SET Pin (Bypass) Capacitance: Noise, PSRR, Transient Response, and Soft-Start

In addition to reducing output noise, using a SET pin bypass capacitor also improves PSRR and transient performance. Note that any bypass-capacitor leakage deteriorates the DC regulation of the LT3046. Capacitor leakage of even 100nA is a 0.1% DC error. Therefore, Analog Devices recommends the use of a good quality, low-leakage ceramic capacitor.

Using a SET pin bypass capacitor also soft starts the output and limits inrush current. The RC time constant, formed by the SET pin resistor and capacitor, controls the soft-start time. The ramp-up rate from 0% to 90% of nominal V_{OUT} is the following:

$$t_{SS} \approx 2.3 \times R_{SET} \times C_{SET} \ (Fast\ Startup\ Disabled)$$

Fast Startup

For ultra-low noise applications that require low 1/f noise (that is, at frequencies below 100Hz), a larger value, SET pin capacitor of up to 22µF is required. Typically, this larger value significantly increases the start-up time of the regulator. However, the LT3046 incorporates fast start-up circuitry that increases the SET pin current to approximately 2.2mA during startup.

As shown in *Figure 67*, the 2.2mA current source remains engaged while PGFB is less than 298mV, unless the regulator is in current limit, dropout, thermal shutdown, or the input voltage is less than the minimum V_{IN}.

If the fast start-up capability is not used, connect PGFB to IN or to OUT for output voltages more than 298mV and note that this also disables the power-good functionality.

EN/UV

The EN/UV pin is used to put the regulator into a micropower shutdown state. The LT3046 has an accurate 1.27V turn-on threshold on the EN/UV pin with 110mV of hysteresis. This threshold can be used with a resistor-divider from the input supply to define an accurate UVLO threshold for the regulator. The EN/UV pin current ($I_{EN/UV}$) at the threshold from *Table 1* must be considered when calculating the resistor-divider network as follows:

$$V_{IN(UVLO)} = 1.27V \times \left(1 + \frac{R_{EN2}}{R_{EN1}}\right) + I_{EN/UV} \times R_{EN2}$$

where:

R_{EN1} and R_{EN2} are the resistors from the EN/UV pin to GND and the EN/UV pin to IN, respectively.

$I_{EN/UV}$ can be ignored if R_{EN1} is less than 100kΩ. If unused, connect the EN/UV pin to IN.

Programmable Power Good

As illustrated in *Figure 67*, the power-good threshold is user programmable using the ratio of two external resistors, R_{PG2} and R_{PG1}:

$$V_{OUT(PG\_THRESHOLD)} = 0.298V \times \left(1 + \frac{R_{PG2}}{R_{PG1}}\right) + I_{PGFB} \times R_{PG2}$$

If the PGFB pin increases to more than 298mV, the open-drain PG pin deasserts and becomes high impedance. The power-good comparator has 7mV hysteresis and 20µs of deglitching. The I_{PGFB} from *Table 1* must be considered when determining the resistor-divider network. The I_{PGFB} can be ignored if R_{PG1} is less than 30kΩ. If the power-good functionality is not used, float the PG pin. Note that programmable power good and fast start-up capabilities are disabled for output voltages less than 298mV. Connect FGFB to IN if the power good and fast start-up functions are not needed.

Externally Programmable Current Limit

The current-limit threshold of the ILIM pin is 290mV. Connecting a resistor from ILIM to GND sets the maximum current flowing out of the ILIM pin, which, in turn, programs the current limit of the LT3046. With a 150mA × kΩ programming scale factor, calculate the current limit as follows:

$$Current\ Limit = \frac{150mA \times k\Omega}{R_{ILIM}}$$

For example, a 750Ω resistor programs the current limit to 200mA and a 1.5kΩ resistor programs the current limit to 100mA. For accuracy, Kelvin connect this resistor to the GND pin of the LT3046.

When the IN-to-OUT differential is greater than 11V, the foldback circuitry of the LT3046 decreases the internal current limit. As a result, the internal current limit can override the externally programmed current-limit level to keep the LT3046 within its safe-operating area (SOA). See *Figure 33*.

As shown in *Figure 67*, the ILIM pin sources current proportional (1:520) to the output current; therefore, it also serves as a current-monitoring pin with a 0V to 290mV range. If external current limit or current monitoring is not used, connect ILIM to GND.

Output Overshoot Recovery

During a load-step change from full load to no load (or light load), the output voltage overshoots before the regulator responds to turn the power transistor off. Given that there is no load (or a light load) present at the output, it takes a long time to discharge the output capacitor.

As shown in *Figure 67*, the LT3046 incorporates overshoot recovery circuitry that turns on a current sink to discharge the output capacitor in the event OUTS is higher than SET. This current is typically approximately 4mA. No load recovery is disabled for input voltages less than 2.5V or output voltages less than 1.5V.

If OUTS is externally held more than SET, the current sink turns on in an attempt to restore OUTS to its programmed voltage. The current sink remains on until the external circuitry releases OUTS.

Direct Paralleling for Higher Current

Higher output current is obtained by paralleling multiple LT3046 devices. Connect all SET pins together and all IN pins together. Connect the OUT pins together using small pieces of PCB trace (used as a ballast resistor) to equalize currents in the LT3046 devices. PCB trace resistance in milliohms per inch is shown in *Table 6*.

Table 6. PCB Trace Resistance (Measured in mΩ per Inch)

WEIGHT (oz)	10mil WIDTH	20mil WIDTH
1	54.3	27.1
2	27.1	13.6

The small worst-case offset of 2mV for each paralleled LT3046 minimizes the required ballast resistor value. *Figure 74* illustrates that two LT3046 devices, each using a 50mΩ PCB trace ballast resistor, providing better than 20% accurate output current sharing at full load. The two 50mΩ external resistors only add 10mV of output regulation drop with a 400mA maximum current. With a 3.3V output, this voltage drop only adds 0.3% to the regulation accuracy. As mentioned previously, connect the OUTS pin directly to the output capacitor.

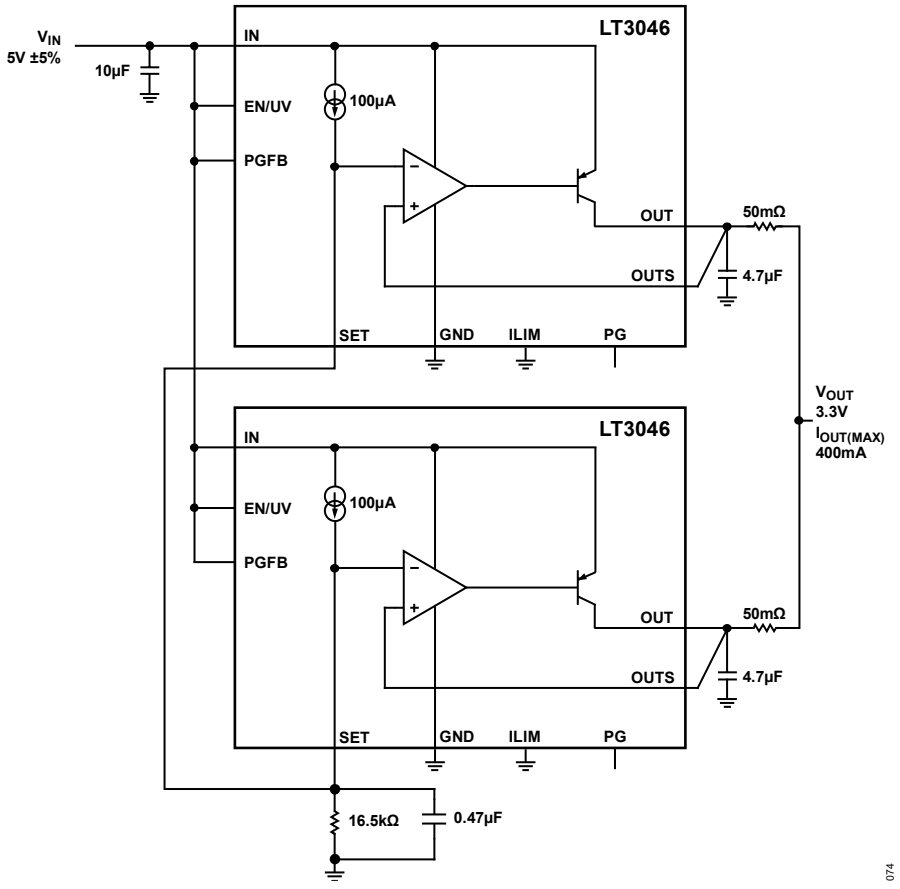


Figure 74. Parallel Devices

In addition, more than two LT3046 devices can be paralleled for even higher output current and lower output noise. Paralleling multiple LT3046 devices is also useful for distributing heat on the PCB. For applications with high input-to-output voltage differential, an input series resistor or resistor in parallel with the LT3046 can also be used to spread heat.

PCB Layout Considerations

Given the high bandwidth and ultra-high PSRR of the LT3046, careful PCB layout must be employed to achieve full device performance. *Figure 75* shows the *LT3046EVK* evaluation board for the DFN package with a layout that delivers the full performance of the regulator. *Figure 76* shows the *LT3046EVK* evaluation board for the WLCSP package with a layout that delivers the full performance of the regulator. Refer to the LT3046 evaluation board user guide (*LT3046EVK*) for further details.

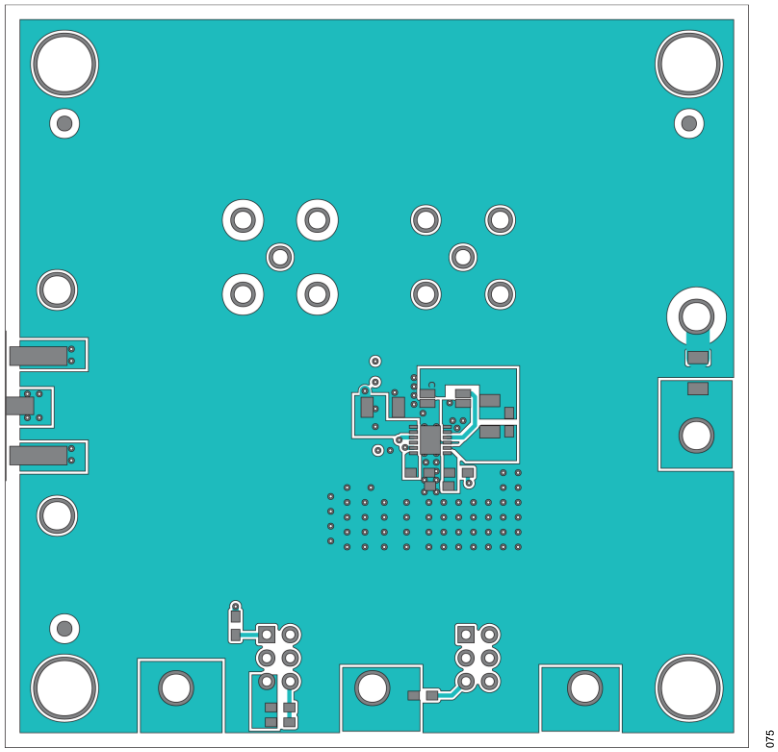


Figure 75. LT3046EVK#DFN Evaluation Board

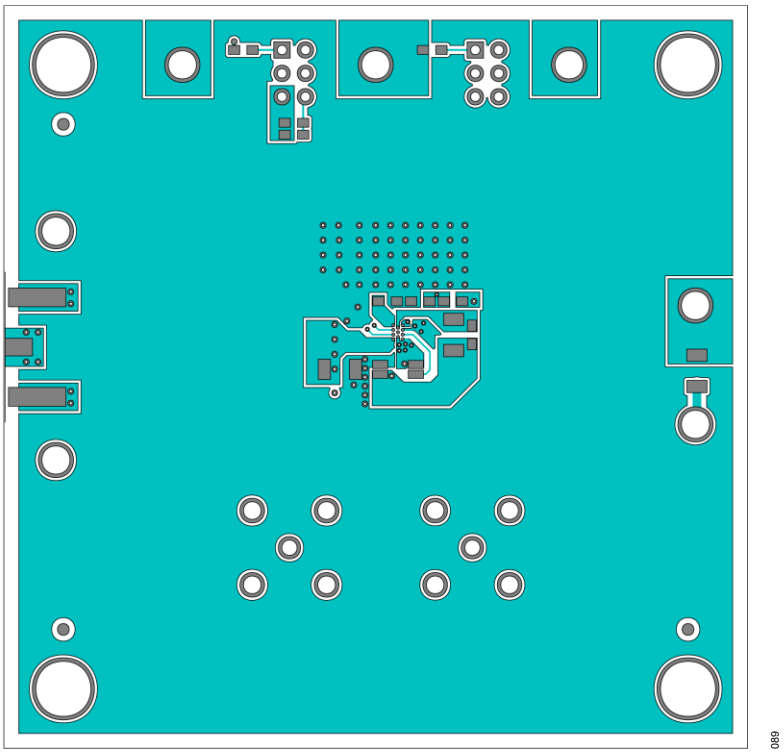


Figure 76. LT3046EVK#WLCSP Evaluation Board

Thermal Considerations

The LT3046 has internal power and thermal limiting circuits that protect the device under overload conditions. The thermal shutdown temperature is nominally +165°C with about 6°C of hysteresis. For continuous normal load conditions, do not exceed the maximum junction temperature, +125°C. It is important to consider all sources of thermal resistance from junction to ambient, which includes junction to case, case to heatsink interface, heatsink resistance, or circuit board to ambient as the application dictates. Additionally, consider all heat sources close to the LT3046.

The underside of the DFN package has exposed metal from the lead frame to the die attachment. This package allows heat to directly transfer from the die junction to the PCB metal to limit maximum operating junction temperature. The dual, inline pin arrangement allows metal to extend beyond the ends of the package on the top side (component side) of the PCB.

For surface-mount devices, heat sinking is accomplished by using the heat-spreading capabilities of the PCB and its copper traces. Copper board stiffeners and plated throughholes can also be used to spread the heat generated by the LDO regulator.

Table 7 lists the thermal resistance as a function of the copper area on a fixed board size. All measurements were taken in still air on a 4-layer FR4 board with 1oz solid internal planes and 2oz top and bottom planes with a total board thickness of 1.6mm. The four layers were electrically isolated with no thermal vias present. PCB layers, copper weight, board layout, and thermal vias affect the resultant thermal resistance. For more information on thermal resistance and high thermal conductivity test boards, refer to JEDEC standard JESD-51, JESD51-7, and JESD51-12. Achieving low thermal resistance necessitates careful PCB layout.

Table 7. Measured Thermal Resistance for DFN and WLCSP Packages

COPPER AREA		BOARD AREA (mm²)	THERMAL RESISTANCE (θ_{JA})	
TOP SIDE[1] (mm²)	BOTTOM SIDE (mm²)		DFN	WLCSP
2500	2500	2500	34°C/W	73°C/W
1000	2500	2500	34°C/W	73°C/W
225	2500	2500	35°C/W	74°C/W
100	2500	2500	36°C/W	75°C/W

[1]Device is mounted on the top side.

Calculating Junction Temperature

For example, given an output voltage of 3.3V, an input voltage of 5V ± 5%, an output current range from 1mA to 200mA, and a maximum ambient temperature of +105°C, what is the maximum junction temperature?

The power dissipation of the LT3046 is the following:

$$I_{OUT(MAX)} \times \left(V_{IN(MAX)} - V_{OUT}\right) + I_{GND} \times V_{IN(MAX)}$$

where:

$I_{OUT(MAX)}$ = 200mA.

$V_{IN(MAX)}$ = 5.25V.

I_{GND} (at I_{OUT} = 200mA and V_{IN} = 5.25V) = 7.2mA.

Therefore,

$$P_{DISS} = 0.2A \times (5.25V - 3.3V) + 7.2mA \times 5.25V = 0.43W$$

Using a DFN package, the thermal resistance is in the range of 34°C/W to 36°C/W depending on the copper area. Therefore, the junction temperature rise above ambient approximately equals 0.43W × 35°C/W = 15°C.

The maximum junction temperature equals the maximum ambient temperature plus the maximum junction temperature rise above ambient, which calculates as follows:

$$T_{JMAX} = 105°C + 15°C = 120°C$$

Overload Recovery

Like many IC power regulators, the LT3046 incorporates SOA protection. The SOA protection activates at input-to-output differential voltages greater than 11V. The SOA protection decreases the current limit because the input-to-output differential increases and keeps the power transistor inside a safe operating region for all values of input-to-output voltages up to the *Absolute Maximum Ratings* of the LT3046. The LT3046 provides some level of output current for all values of input-to-output differentials. See *Figure 33*. When power is first applied and the input voltage rises, the output follows the input and keeps the input-to-output differential low to allow the LDO regulator to supply the large output current and startup into high-current loads.

Due to current-limit foldback, however, at high-input voltages, a problem can occur if the output voltage is low, and the load current is high. Such situations occur after the removal of a short-circuit or if the EN/UV pin is pulled high after the input voltage is already turned on. The load-line in such cases intersects the output-current profile at two points. The regulator now has two stable operating points. With this double intersection, the input-power supply may need to be cycled down to zero and brought back up again to allow the output to recover. Other LDO regulators with foldback current-limit protection (such as the **LT1965** and **LT1963A**) also exhibit this phenomenon; therefore, it is not unique to the LT3046.

Protection Features

The LT3046 incorporates several protection features for battery-powered applications. Precision current-limit and thermal-overload protection protect the LT3046 against overload and fault conditions at the output of the device. For normal operation, do not allow the junction temperature to exceed +125°C.

To protect the low-noise error amplifier of the LT3046, the SET-to-OUTS protection clamp limits the maximum voltage between SET and OUTS with a maximum DC current of 20mA through the clamp. Therefore, for applications where SET is actively driven by a voltage source, the voltage source must be current limited to 20mA or less. Moreover, to limit the transient current flowing through these clamps during a transient fault condition, limit the maximum value of the SET pin capacitor (C_{SET}) to 22µF.

The LT3046 also incorporates reverse-input protection whereby the IN pin withstands reverse voltages of up to -20V without causing any input-current flow and without developing negative voltages at the OUT pin. The regulator protects both itself and the load against batteries that are plugged in backwards.

In circuits where a backup battery is required, several different input and output conditions can occur. The output voltage can be held up while the input is either pulled to GND, pulled to some intermediate voltage, or left open-circuit. In all cases, the reverse-current protection circuitry prevents current flow from the output to the input. Nonetheless, due to the OUTS-to-SET clamp, unless the SET pin is floating, current can flow to GND through the SET pin resistor as well as up to 15mA to GND through the output overshoot recovery circuitry. This current flow through the output overshoot recovery circuitry can be significantly reduced by placing a Schottky diode between the OUTS and SET pins, with its anode at the OUTS pin.

TYPICAL APPLICATIONS

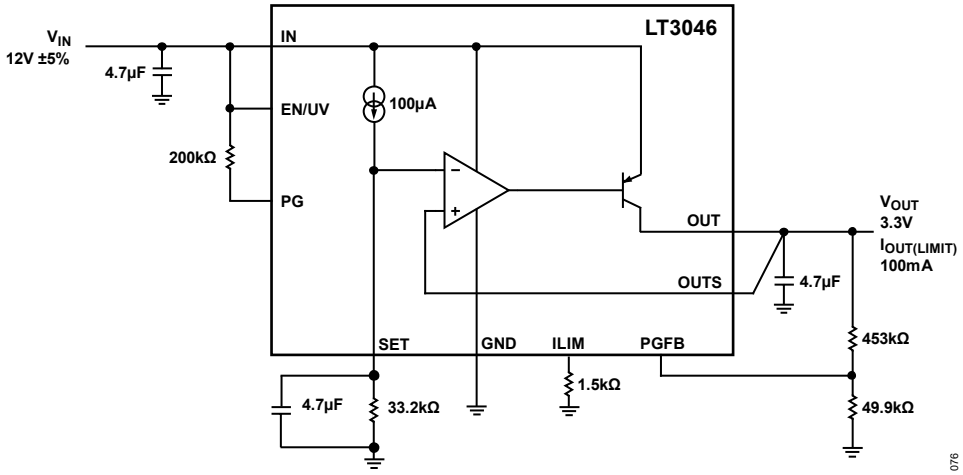


Figure 77. 12V$_{IN}$ to 3.3V$_{OUT}$ with 0.8µV$_{RMS}$ Integrated Noise

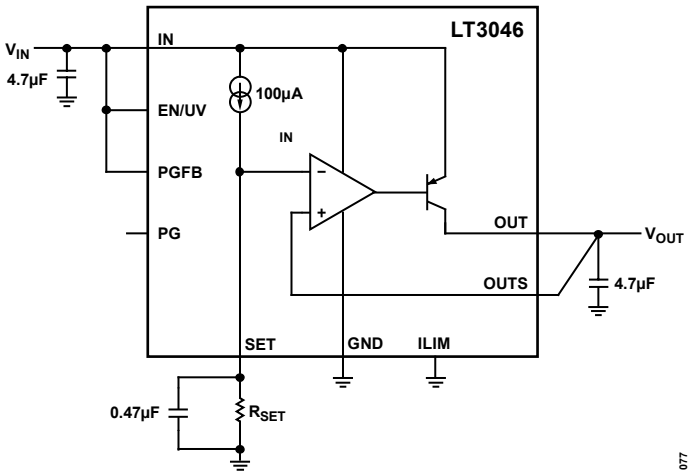


Figure 78. PGFB Disabled without Reverse Input Protection

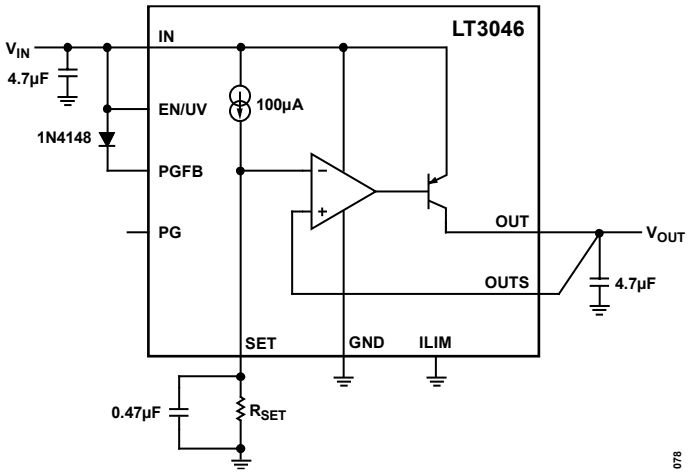


Figure 79. PGFB Disabled with Reverse Input Protection

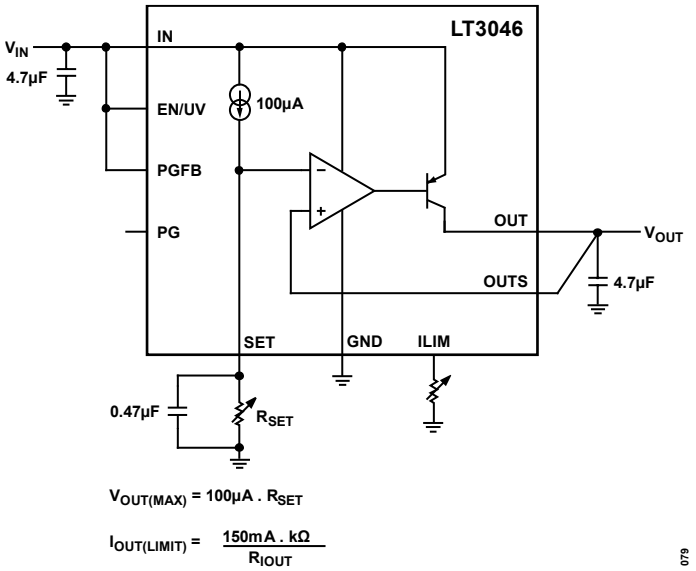


Figure 80. Low Noise Constant-Current/Constant-Voltage Lab Power Supply

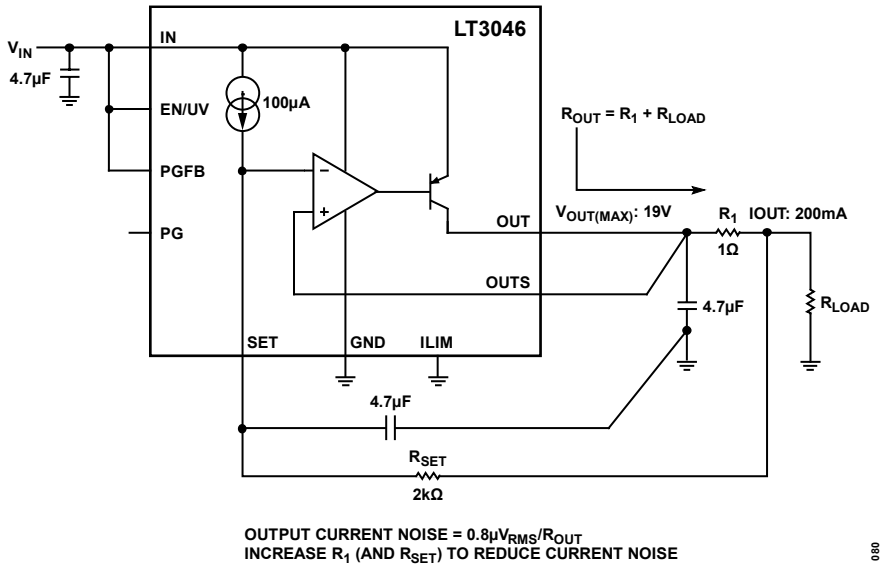


Figure 81. Ultra-Low Noise Current Source for RF Biasing Applications (R_{OUT} is the Output Resistance)

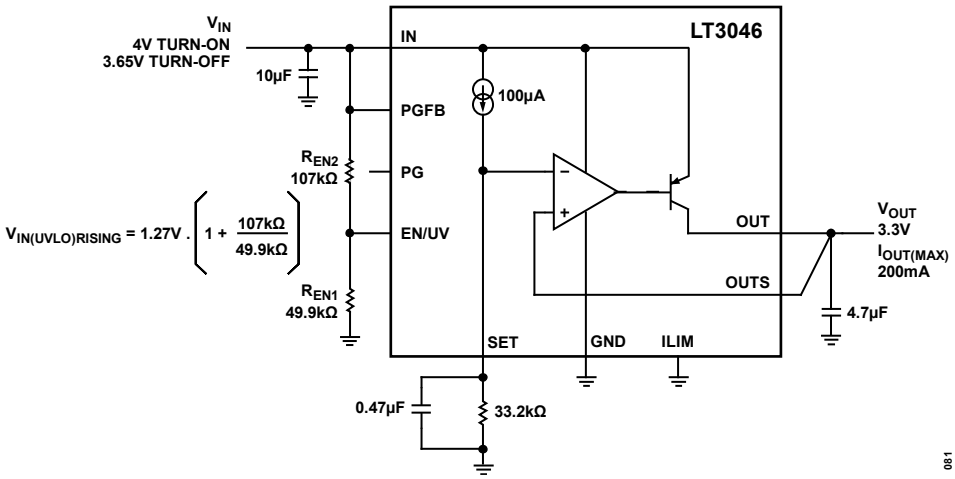


Figure 82. Programming UVLO

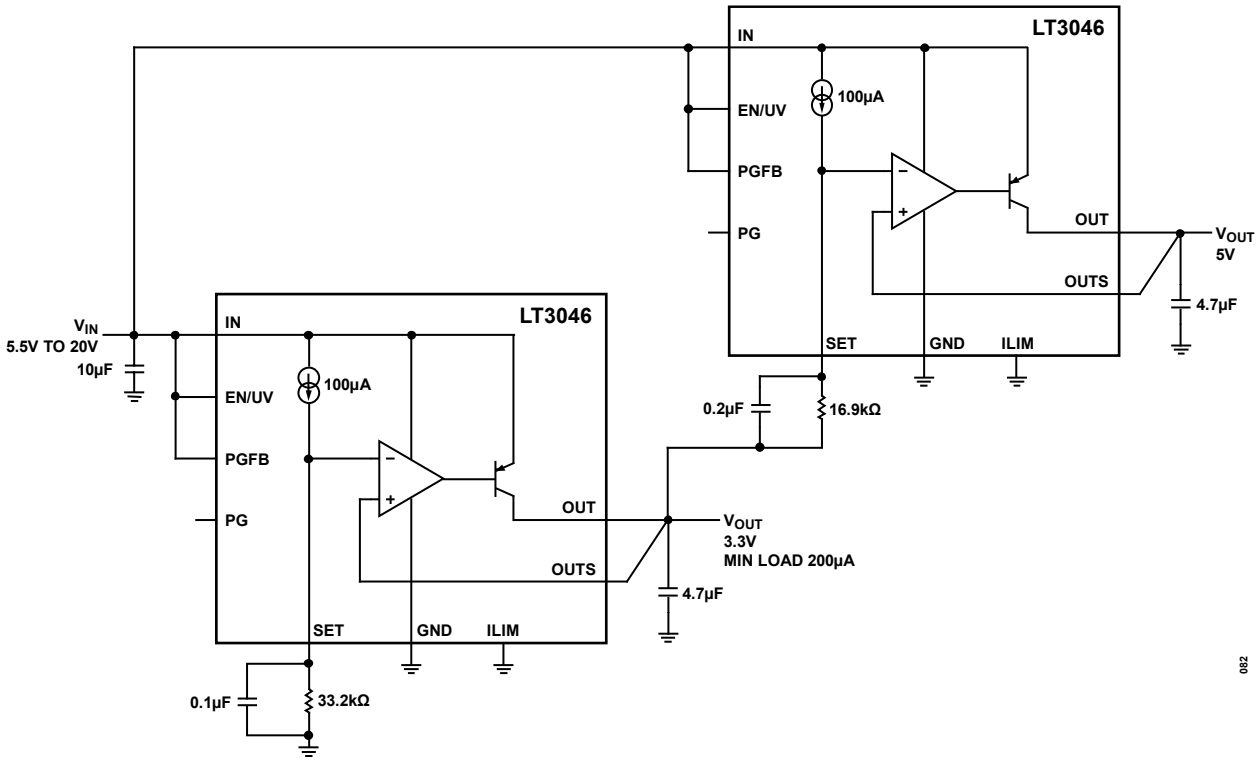


Figure 83. Ratiometric Tracking

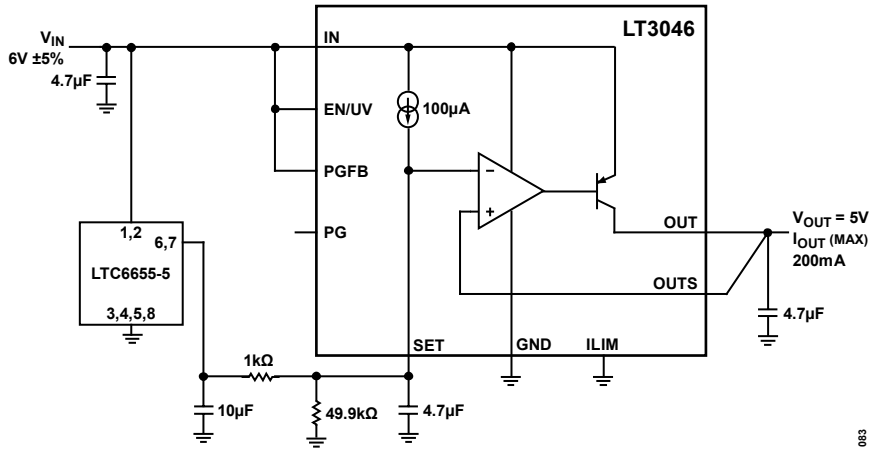


Figure 84. Ultra-Low 1/f Noise Reference Buffer

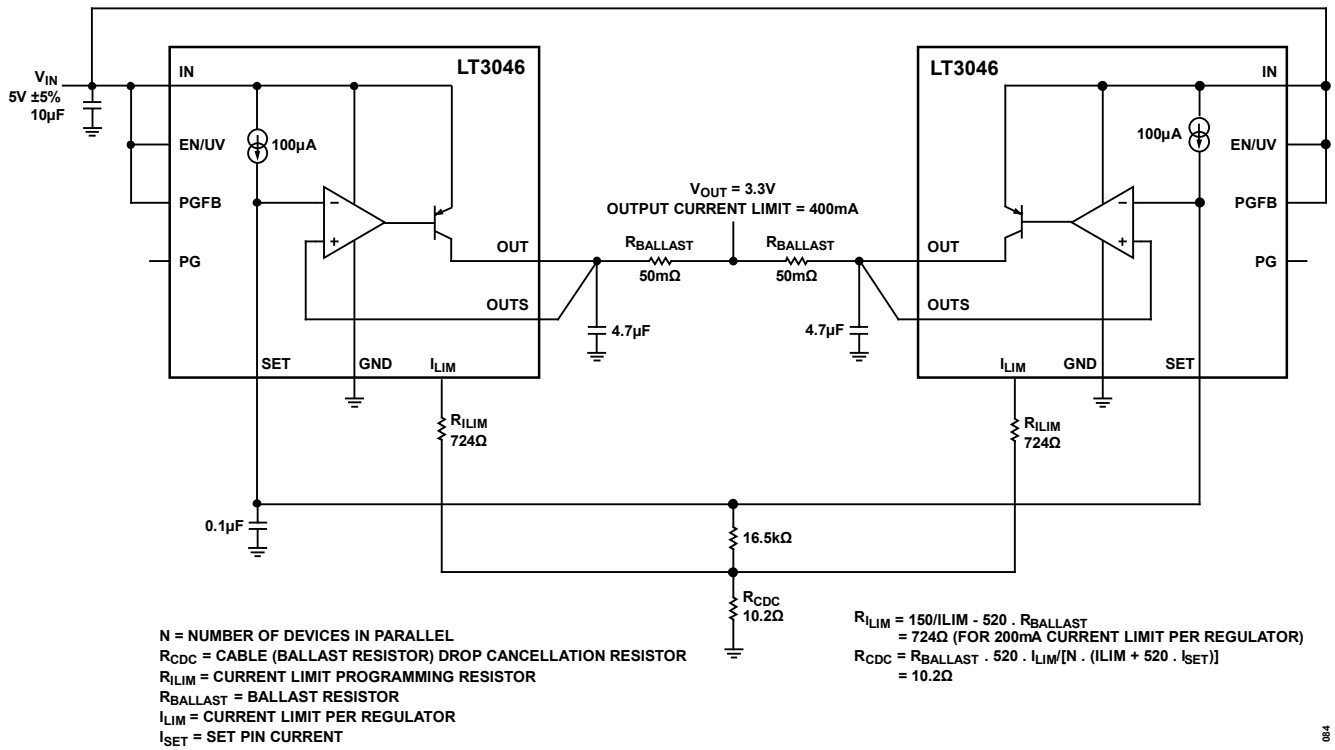


Figure 85. Paralleling Multiple Devices Using ILIM

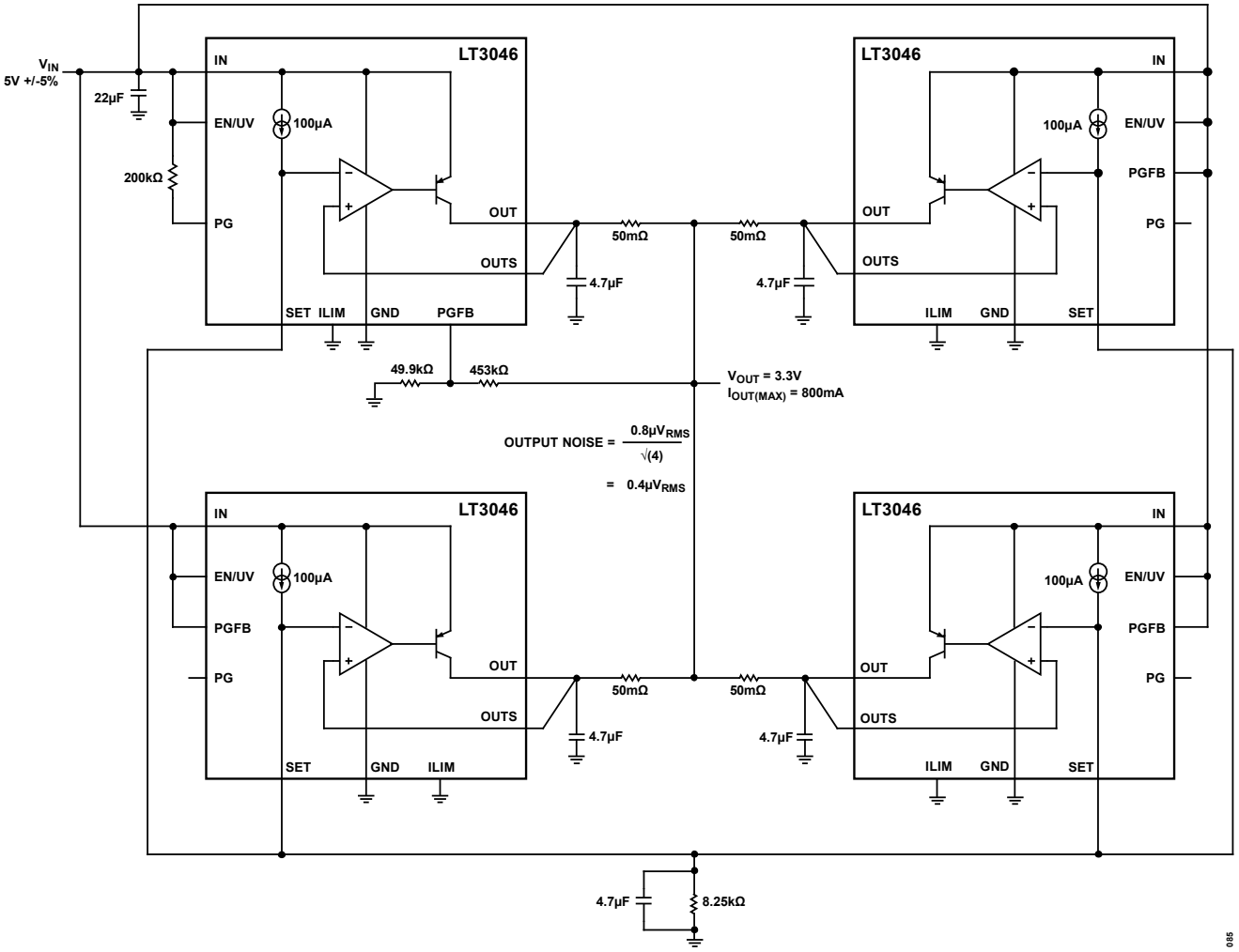


Figure 86. Paralleling Multiple LT3046 Devices for 800mA Output Current

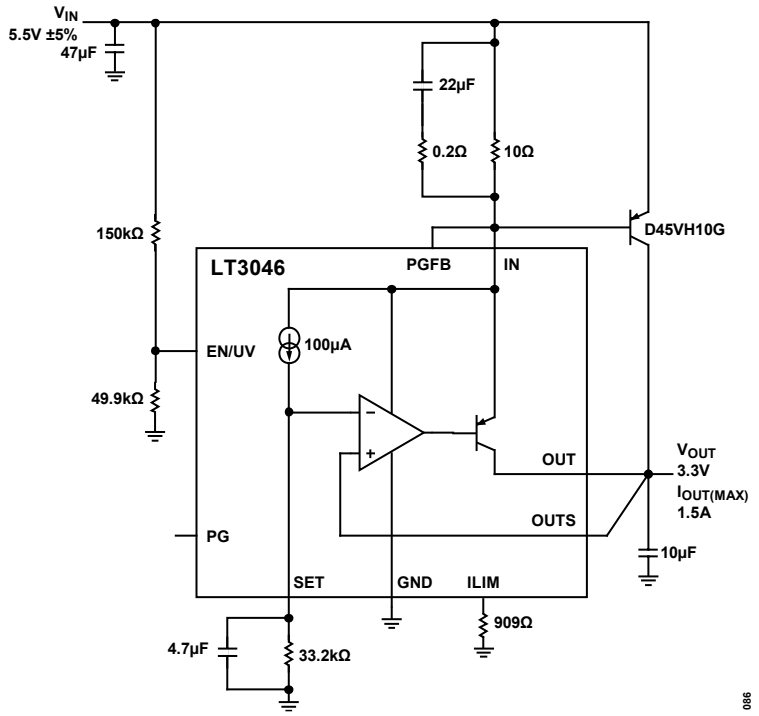


Figure 87. Ultra-Low Noise Higher Current Regulator with External PNP

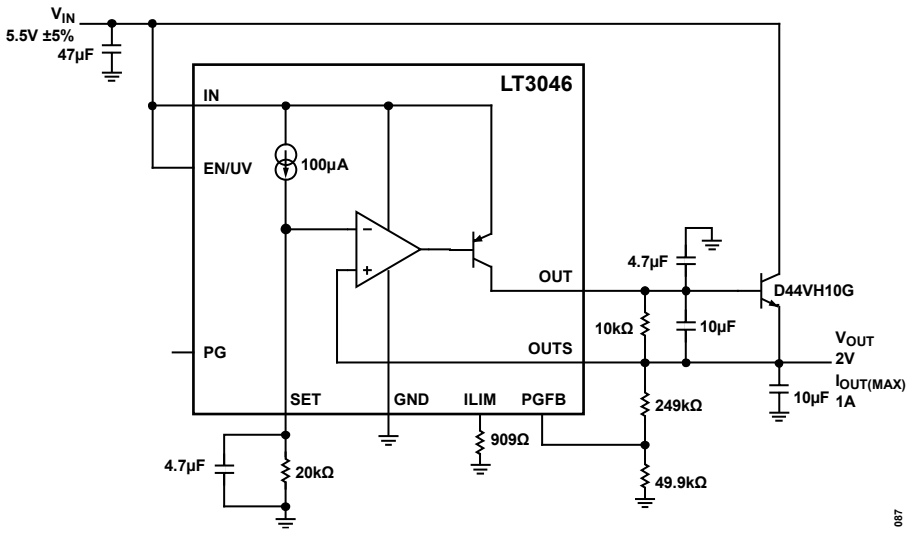
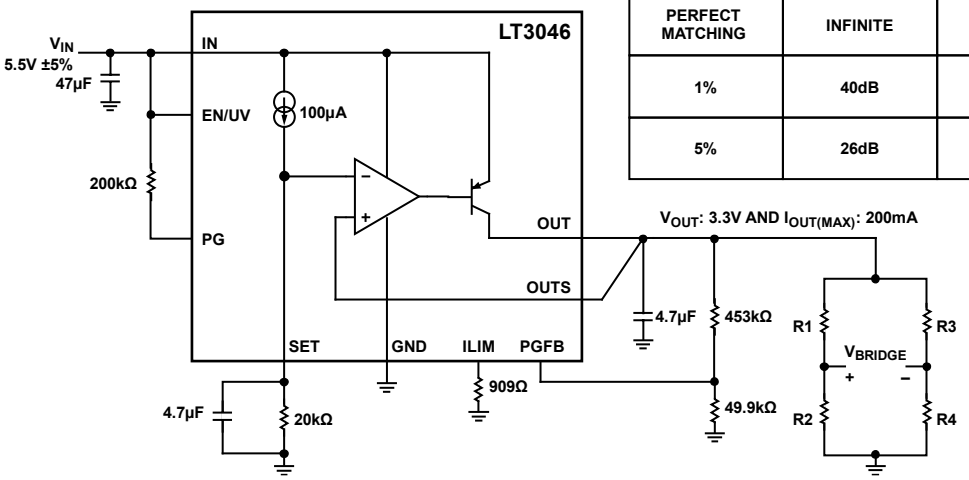


Figure 88. Ultra-Low Noise Higher Current Regulator with External NPN



LT1763 NOISE: $20\mu V_{RMS}$ (10Hz TO 100kHz)
LT3046 NOISE: $0.8\mu V_{RMS}$ (10Hz TO 100kHz)

RESISTOR TOLERANCE	BRIDGE PSRR	NOISE AT V_{BRIDGE} USING LT1763	NOISE AT V_{BRIDGE} USING LT3046
PERFECT MATCHING	INFINITE	-	-
1%	40dB	$200nV_{RMS}$	$8nV_{RMS}$
5%	26dB	$1000nV_{RMS}$	$42.5nV_{RMS}$

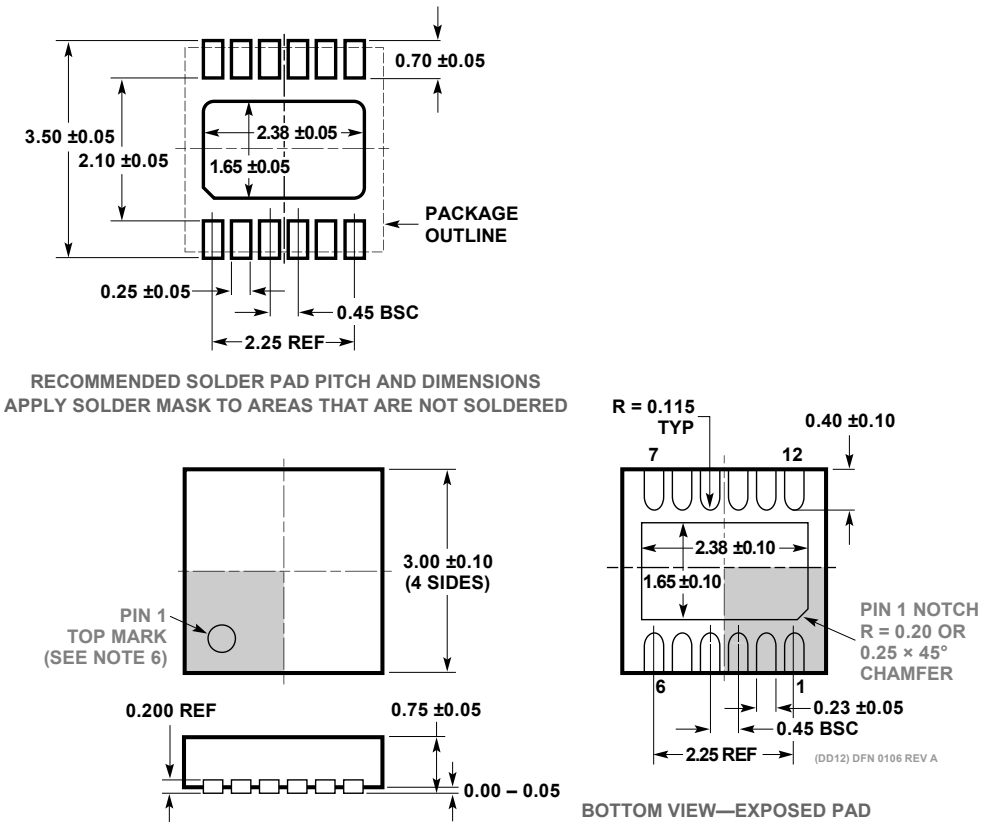
Figure 89. Low Noise Wheatstone Bridge Power Supply

RELATED PRODUCTS

Table 8. Related Products

PART NUMBER	DESCRIPTION	COMMENTS
LT3042	20V, 200mA, ultra-low noise, ultra-high PSRR RF linear regulator	0.8μV_{RMS} noise and 79dB PSRR at 1 MHz, V_{IN} = 1.8V to 20V, 350mV dropout voltage, programmable current limit and power good, 3mm × 3mm DFN and MSOP packages
LT3045	20V, 500mA, ultra-low noise, ultra-high PSRR linear regulator	0.8μV_{RMS} noise and 75dB PSRR at 1MHz, V_{IN} = 1.8V to 20V, 260mV dropout voltage, 3mm × 3mm DFN and MSOP packages
LT3045-1	20V, 500mA, ultra-low noise, ultra-high PSRR linear regulator with VIOC control	0.8μV_{RMS} noise and 75dB PSRR at 1MHz, V_{IN} = 1.8V to 20V, 260mV dropout voltage, 3mm × 3mm DFN and MSOP packages
LT3041	20V, 1A, ultra-low noise, ultra-high PSRR linear regulator with VIOC control	1μV_{RMS} noise and 80dB PSRR at 1MHz, V_{IN} = 2.2V to 20V, 310mV dropout voltage, programmable current limit and power good, 4mm × 3mm DFN package
LT3040	20V, 200mA, ultra-low noise, ultra-high PSRR precision DAC/ reference buffer	1.2μV_{RMS} noise and 73dB PSRR at 1MHz, V_{IN} = 1.8V to 20V, 350mV dropout voltage, 3mm × 3mm DFN and MSOP packages
LT3093	-20V, 200mA, ultra-low noise, ultra-high PSRR negative linear regulator	0.8μV_{RMS} noise and 73dB PSRR at 1MHz, V_{IN} = -1.8V to -20V, 190mV dropout voltage, programmable current limit and power good, 3mm × 3mm DFN and MSOP packages
LT3094	-20V, 500mA, ultra-low noise, ultra-high PSRR negative linear regulator	0.8μV_{RMS} noise and 74dB PSRR at 1MHz, V_{IN} = -1.8 V to -20V, 235mV dropout voltage, programmable current limit and power good, 3mm × 3mm DFN and MSOP packages
ADP7112	20V, 200mA, low-noise, CMOS LDO linear regulator	11μV_{RMS} noise and 68dB PSRR at 100kHz, V_{IN} = 2.7V to 20V, 200mV dropout voltage, user-programmable soft start, 1mm × 1.2mm WLCSP package
ADP7118	20V, 200mA, low-noise, CMOS LDO linear regulator	11μV_{RMS} noise and 68dB PSRR at 100kHz, V_{IN} = 2.7V to 20V, 200mV dropout voltage, user-programmable soft start, 2mm × 2mm LFCSP, SOIC, and TSOT packages
ADM7160	Ultra-low noise, 200mA linear regulator	9μV_{RMS} noise and 54dB PSRR at 100kHz, V_{IN} = 2.2V to 5V, 150mV dropout voltage, low quiescent current, 2mm × 2mm LFCSP and TSOT packages
ADP151	Ultra-low noise, 200mA, CMOS linear regulator	9μV_{RMS} noise and 70dB PSRR at 10kHz, V_{IN} = 2.2V to 5V, 135mV dropout voltage, low quiescent current, 2mm × 2mm LFCSP, 0.76mm x 0.76mm WLCSP, and TSOT packages

OUTLINE DIMENSIONS



NOTE:
1. DRAWING IS NOT A JEDEC PACKAGE OUTLINE
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD AND TIE BARS SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

Figure 90. DFN Package

12-Lead Plastic DFN (3mm x 3mm)
Reference LTC Drawing No. 05-08-1725 Rev A

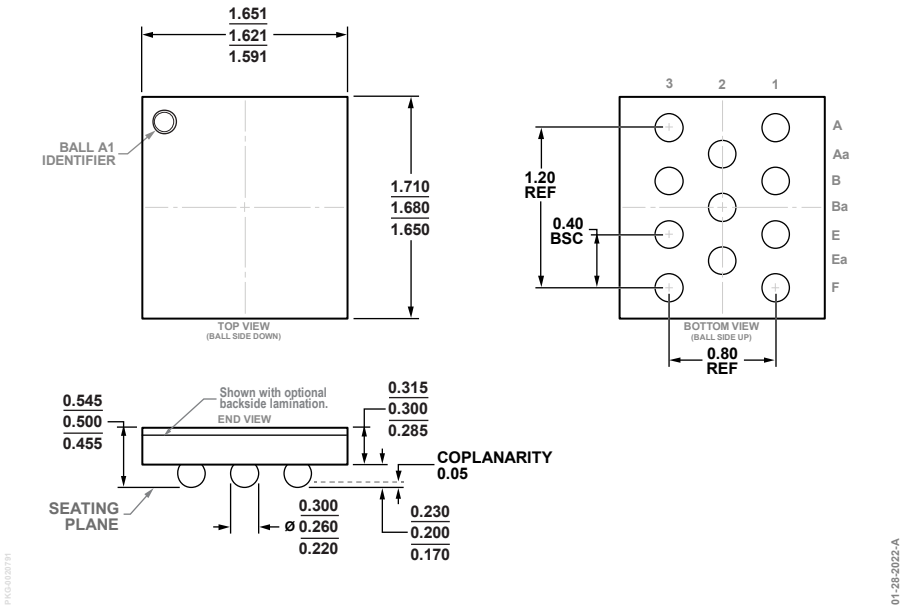


Figure 91. WLCSP Package (21-100706)

11-Ball WLCSP (1.621mm x 1.680mm)

ORDERING GUIDE

Table 9. Ordering Guide

MODEL	TEMPERATURE RANGE	PACKAGE DESCRIPTION	PACKAGE OPTION
LT3046ATC+	-40°C to +125°C	12-Lead Plastic DFN (3mm x 3mm)	05-08-1725
LT3046ATC+ T	-40°C to +125°C	12-Lead Plastic DFN (3mm x 3mm)	05-08-1725
LT3046ANQ+	-40°C to +125°C	11-Ball WLCSP (1.621mm x 1.680mm)	21-100706
LT3046ANQ+ T	-40°C to +125°C	11-Ball WLCSP (1.621mm x 1.680mm)	21-100706

+ Denotes a lead (Pb)-free/RoHS-compliant package.
T = Tape and reel.

SELECTOR GUIDE

Table 10. Evaluation Kit

MODEL[1]	DESCRIPTION
LT3046EVK#DFN	DFN Evaluation Kit
LT3046EVK#WLP	WLCSP Evaluation Kit

[1] The LT3046EVK#DFN and LT3046EVK#WLP are RoHS-compliant parts.