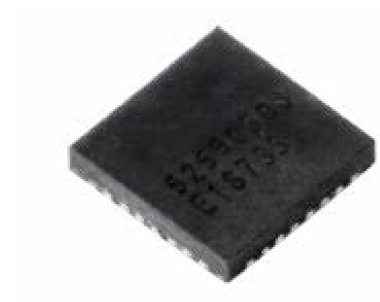
CMPA5259050S

50 W, 5.0 - 5.9 GHz, GaN MMIC, Power Amplifier



Package Type: 5 x 5 QFN
PN: CMPA5259050S

Description

The CMPA5259050S is a gallium nitride (GaN) High Electron Mobility Transistor (HEMT) based monolithic microwave integrated circuit (MMIC). This MMIC contains a two-stage reactively matched amplifier design approach enabling high power and power added efficiency to be achieved in a 5 mm x 5 mm surface mount (QFN package).

Typical Performance Over 5.0 - 5.9 GHz (T_C = 25°C)

Parameter	5.2 GHz	5.5 GHz	5.9 GHz	Units
Small Signal Gain[1,2]	27.0	26.0	27.1	dB
Output Power[1,3]	48.2	48.1	48.6	dBm
Power Gain[1,3]	23.2	23.1	23.6	dB
Power Added Efficiency[1,3]	56	51	49	%

Note:
[1] V_{DD} = 28 V, I_{DQ} = 500 mA
[2] Measured at P_{IN} = -20 dBm
[3] Measured at P_{IN} = 25 dBm and 150µs; Duty Cycle = 20%

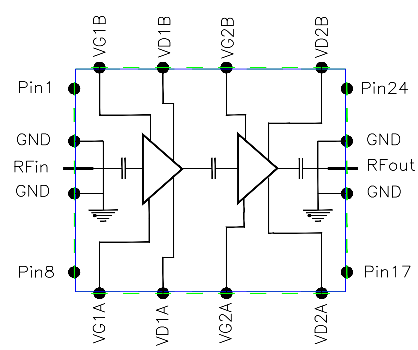
Features

- >50% Typical Power Added Efficiency
- 27 dB Small Signal Gain
- 65 W Typical P_{SAT}
- Operation up to 28 V
- High Breakdown Voltage
- High Temperature Operation

Note: Features are typical performance across frequency under 25°C operation. Please reference performance charts for additional details.

Applications

- Civil and Military Pulsed Radar Amplifiers



RoHS compliant

Absolute Maximum Ratings (not simultaneous) at 25°C

Parameter	Symbol	Rating	Units	Conditions
Drain-source Voltage	V_{DSS}	84	V_{DC}	25˚C
Gate-source Voltage	V_{GS}	-10, +2		
Storage Temperature	T_{STG}	-55, +150	°C	
Maximum Forward Gate Current	I_{GMAX}	18.96	mA	25˚C
Maximum Drain Current	I_{DMAX}	4.5	A	
Soldering Temperature	T_S	260	°C	

Electrical Characteristics (Frequency = 5.0 GHz to 5.9 GHz unless otherwise stated; T_C = 25°C)

Characteristics	Symbol	Min.	Typ.	Max.	Units	Conditions
DC Characteristics						
Gate Threshold Voltage	$V_{GS(th)}$	-2.6	-2.0	-1.6	V	V_{DS} = 10 V, I_D = 18.96 mA
Gate Quiescent Voltage	$V_{GS(Q)}$	–	-1.8	–	V_{DC}	V_{DD} = 28 V, I_{DQ} = 500 mA
Saturated Drain Current[1]	I_{DS}	18.96	22.75	–	A	V_{DS} = 6.0 V, V_{GS} = 2.0 V
Drain-Source Breakdown Voltage	V_{BD}	84	–	–	V	V_{GS} = -8 V, I_D = 18.96 mA
RF Characteristics[2,3]						
Small Signal Gain at 5.2 GHz	$S21_1$	–	27	–	dB	V_{DD} = 28 V, I_{DQ} = 500 mA, P_{IN} = 5 dBm
Small Signal Gain at 5.55 GHz	$S21_2$	–	26.6	–		
Small Signal Gain at 5.9 GHz	$S21_3$	–	27.2	–		
Output Power at 5.2 GHz	P_{OUT1}	–	47.8	–	dBm	V_{DD} = 28 V, I_{DQ} = 500 mA, P_{IN} = 25 dBm
Output Power at 5.55 GHz	P_{OUT2}	–		–		
Output Power at 5.9 GHz	P_{OUT3}	–	48.1	–		
Power Added Efficiency at 5.2 GHz	PAE_1	–	54	–	%	
Power Added Efficiency at 5.55 GHz	PAE_2	–	53	–		
Power Added Efficiency at 5.9 GHz	PAE_3	–	50	–		
Output Mismatch Stress	VSWR	–	–	3:1	Ψ	No damage at all phase angles

Notes:
[1] Scaled from PCM data
[2] Measured in CMPA5259050S high volume test fixture at 5.2, 5.55 and 5.9 GHz and may not show the full capability of the device due to source inductance and thermal performance.
[3] Unless otherwise noted: Pulse Width = 25µs, Duty Cycle = 1%

Thermal Characteristics

Parameter	Symbol	Rating	Units	Conditions
Operating Junction Temperature	T_J	225	°C	
Thermal Resistance, Junction to Case (packaged)[1]	$R_{\theta JC}$	1.13	°C/W	Pulse Width = 150µs, Duty Cycle =20%

Notes:
[1] Measured for the CMPA5259050S at P_{DISS} = 64 W

Typical Performance of the CMPA5259050S

Test conditions unless otherwise noted: V_D = 28 V, I_{DQ} = 500 mA, Pulse Width = 150µs, Duty Cycle = 20%, P_{IN} = 25 dBm, T_{BASE} = +25°C

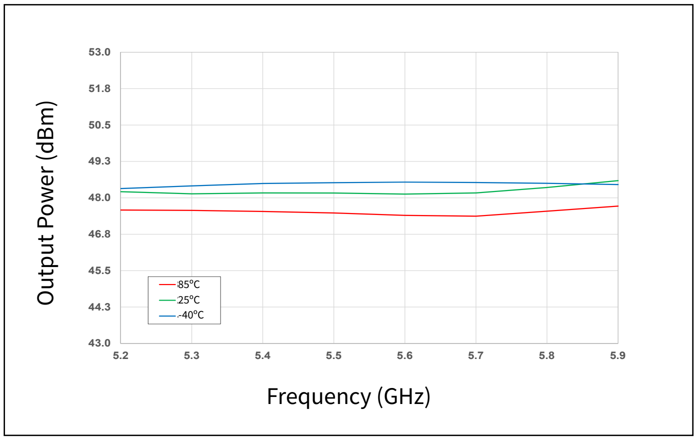


Figure 1. Output Power vs Frequency as a Function of Temperature

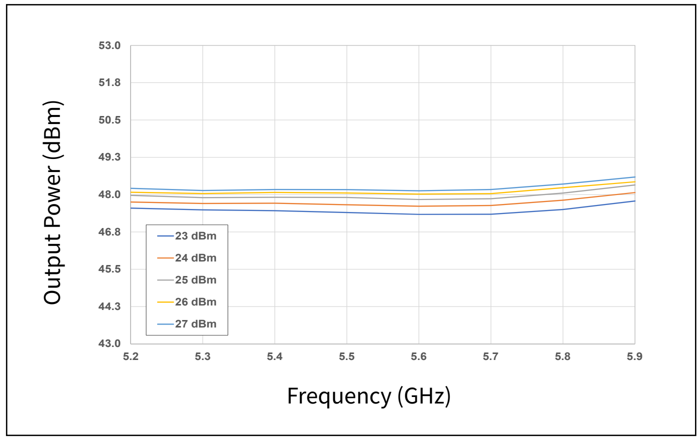


Figure 2. Output Power vs Frequency as a Function of Input Power

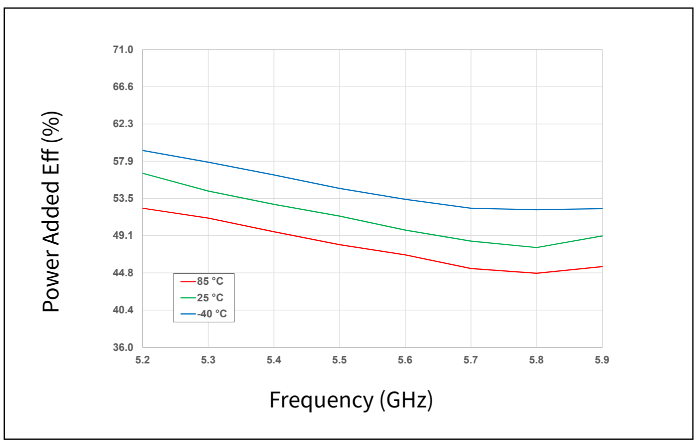


Figure 3. Power Added Eff. vs Frequency as a Function of Temperature

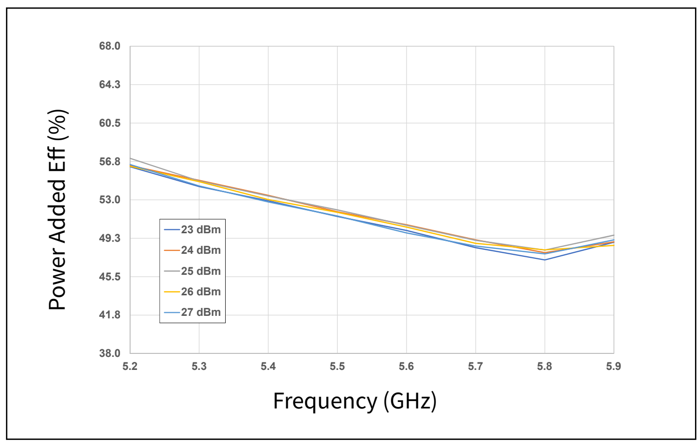


Figure 4. Power Added Eff. vs Frequency as a Function of Input Power

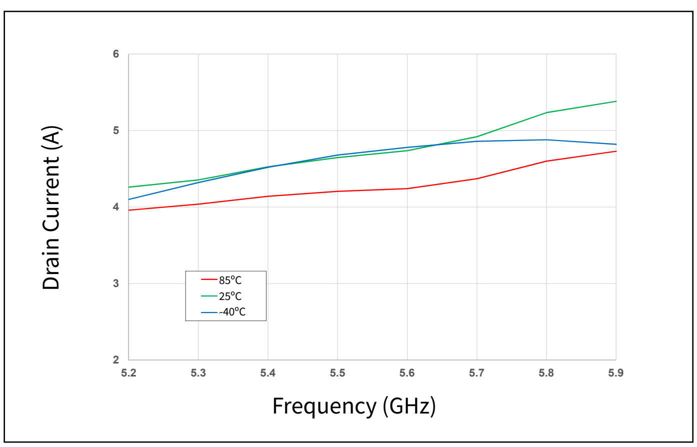


Figure 5. Drain Current vs Frequency as a Function of Temperature

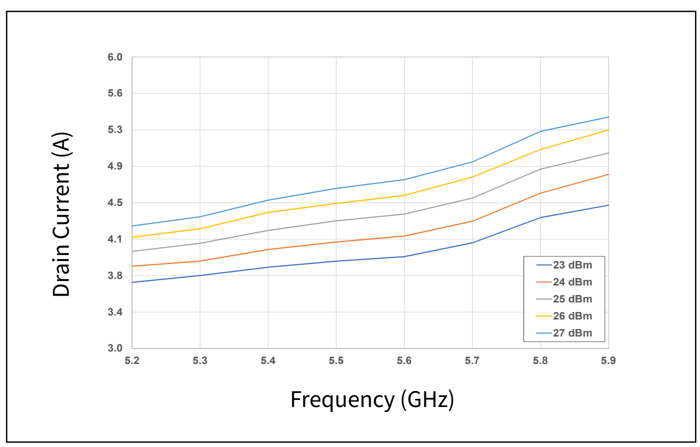


Figure 6. Drain Current vs Frequency as a Function of Input Power

Typical Performance of the CMPA5259050S

Test conditions unless otherwise noted: V_D = 28 V, I_{DQ} = 500 mA, Pulse Width = 150µs, Duty Cycle = 20%, P_{IN} = 25 dBm, T_{BASE} = +25°C

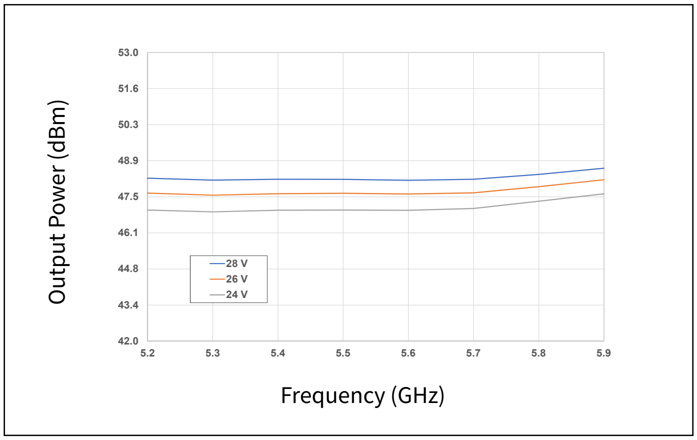


Figure 7. Output Power vs Frequency as a Function of V_D

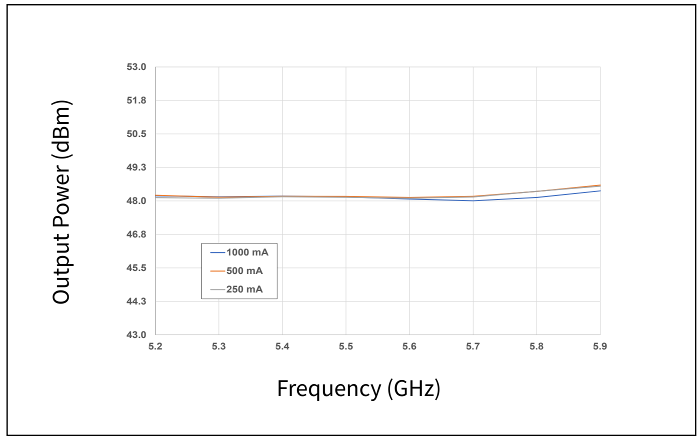


Figure 8. Output Power vs Frequency as a Function of I_{DQ}

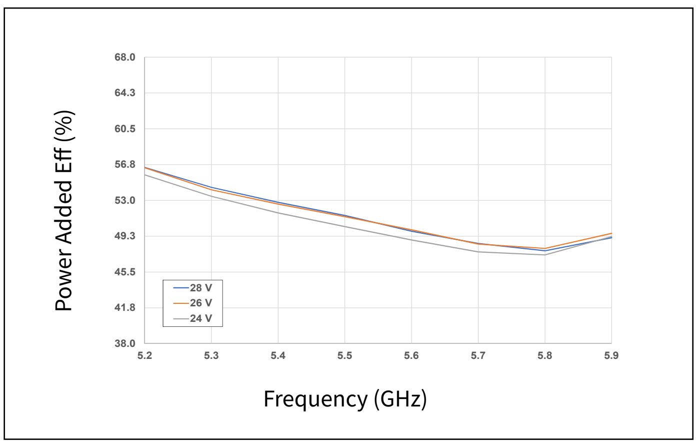


Figure 9. Power Added Eff. vs Frequency as a Function of V_D

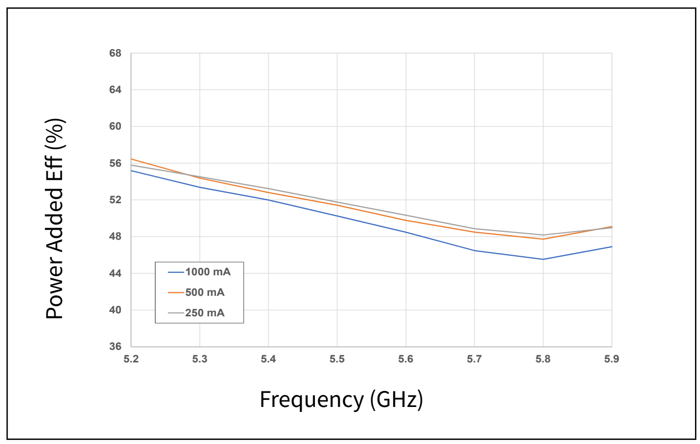


Figure 10. Power Added Eff. vs Frequency as a Function of I_{DQ}

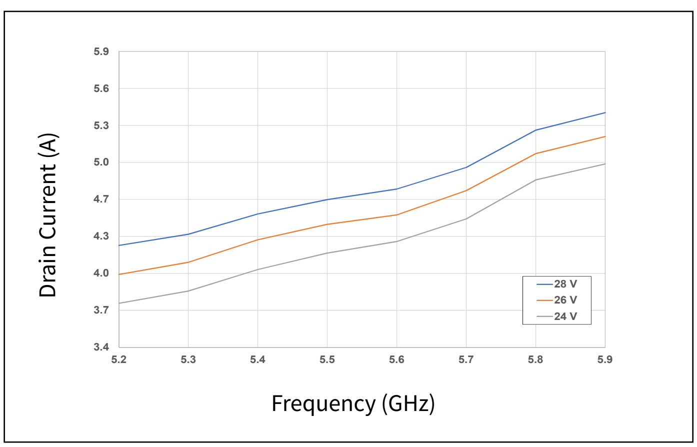


Figure 11. Drain Current vs Frequency as a Function of V_D

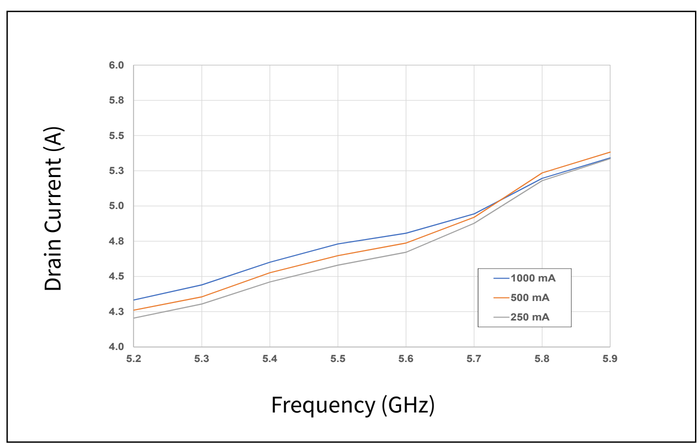


Figure 12. Drain Current vs Frequency as a Function of I_{DQ}

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Typical Performance of the CMPA5259050S

Test conditions unless otherwise noted: V_D = 28 V, I_{DQ} = 500 mA, Pulse Width = 150µs, Duty Cycle = 20%, P_{IN} = 25 dBm, T_{BASE} = +25°C

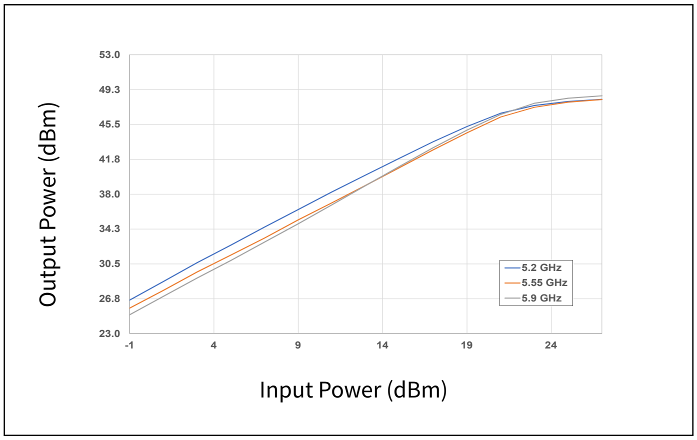

Figure 13. Output Power vs Input Power as a Function of Frequency

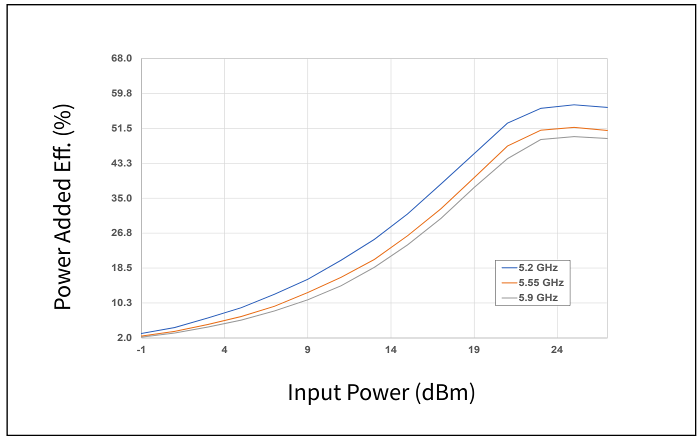

Figure 14. Power Added Eff. vs Input Power as a Function of Frequency

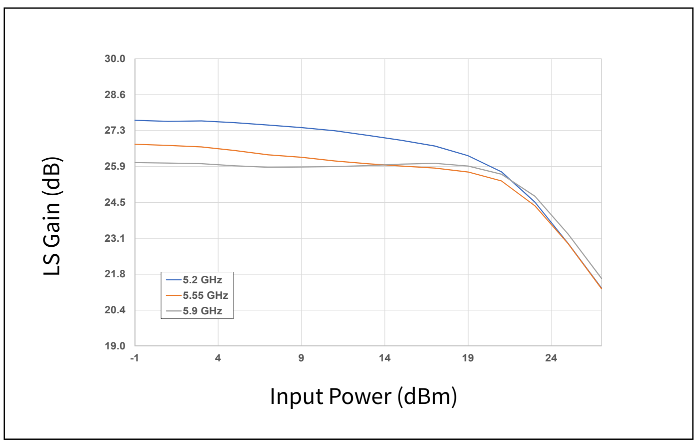

Figure 15. Large Signal Gain vs Input Power as a Function of Frequency

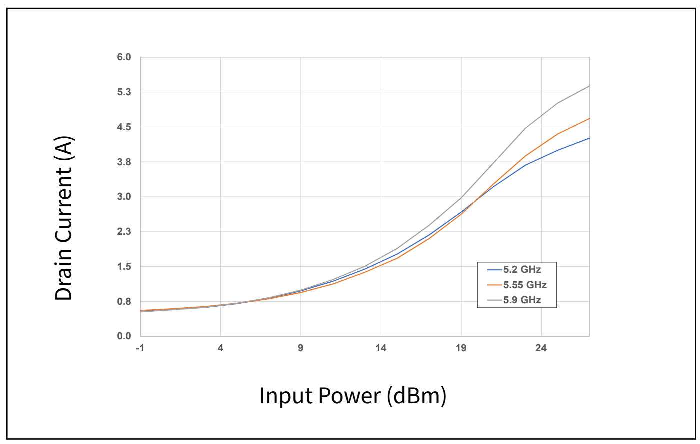

Figure 16. Drain Current vs Input Power as a Function of Frequency

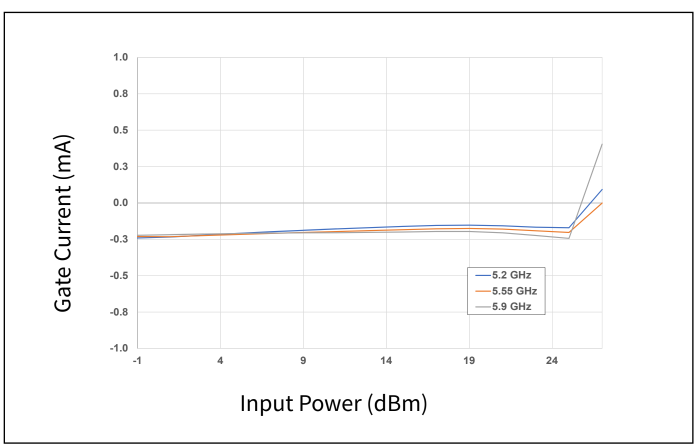

Figure 17. Gate Current vs Input Power as a Function of Frequency

Typical Performance of the CMPA5259050S

Test conditions unless otherwise noted: V_D = 28 V, I_{DQ} = 500 mA, Pulse Width = 150µs, Duty Cycle = 20%, P_{IN} = 25 dBm, T_{BASE} = +25°C

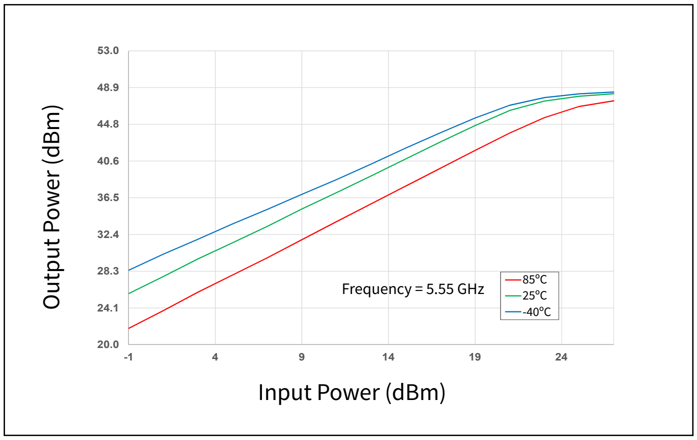

Figure 18. Output Power vs Input Power as a Function of Temperature

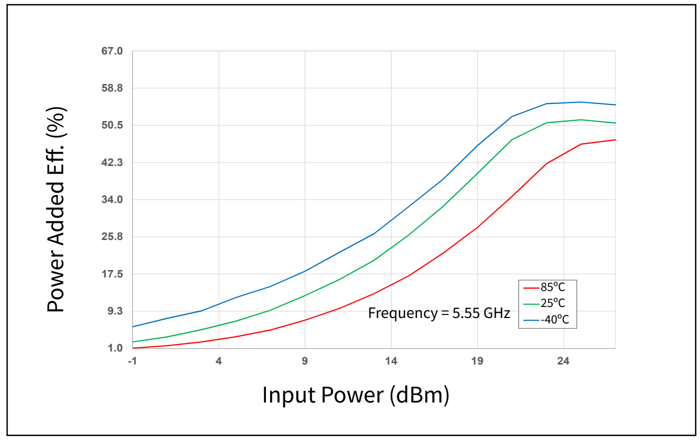

Figure 19. Power Added Eff. vs Input Power as a Function of Temperature

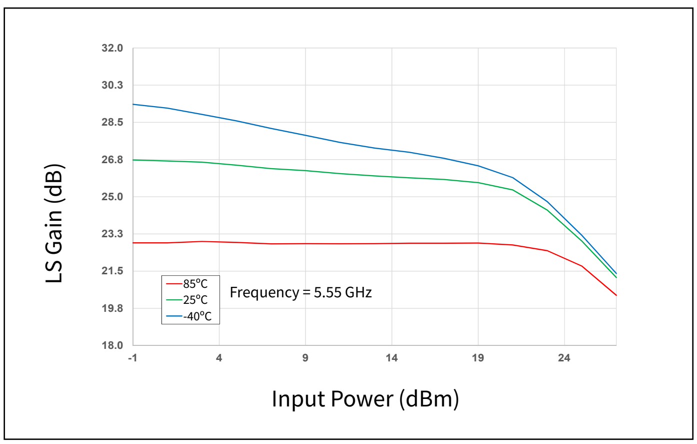

Figure 20. Large Signal Gain vs Input Power as a Function of Temperature

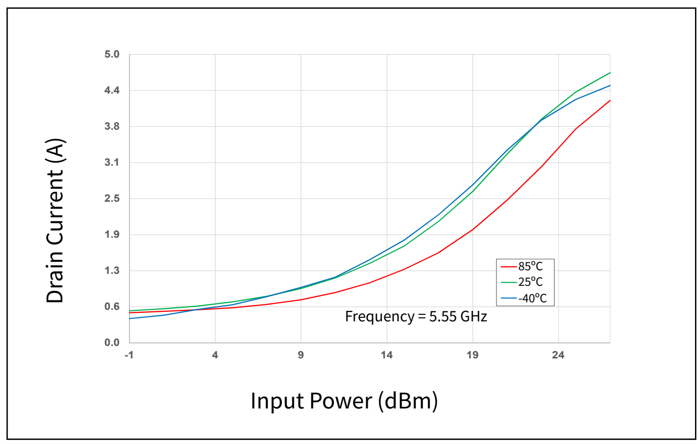

Figure 21. Drain Current vs Input Power as a Function of Temperature

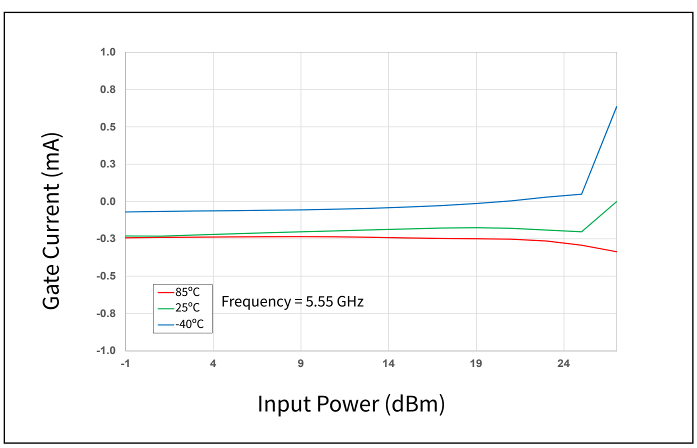

Figure 22. Gate Current vs Input Power as a Function of Temperature

Typical Performance of the CMPA5259050S

Test conditions unless otherwise noted: V_D = 28 V, I_{DQ} = 500 mA, Pulse Width = 150µs, Duty Cycle = 20%, P_{IN} = 25 dBm, T_{BASE} = +25°C

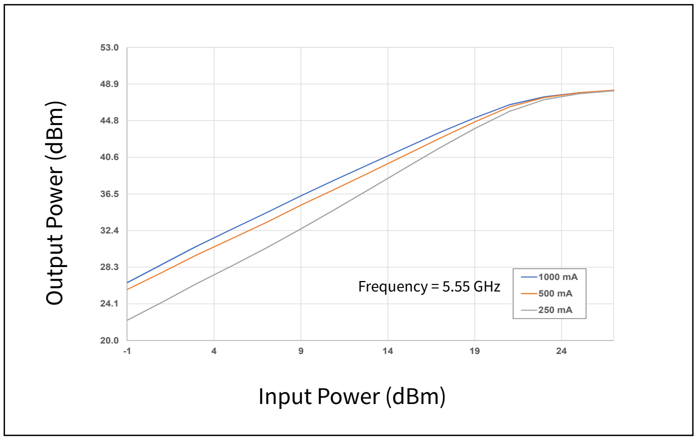

Figure 23. Output Power vs Input Power as a Function of I_{DQ}

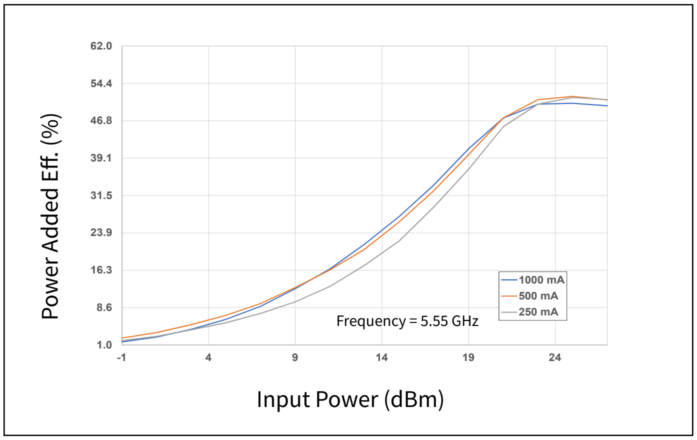

Figure 24. Power Added Eff. vs Input Power as a Function of I_{DQ}

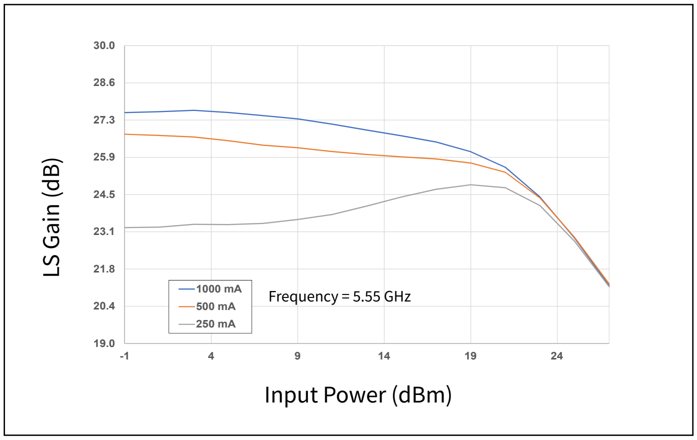

Figure 25. Large Signal Gain vs Input Power as a Function of I_{DQ}

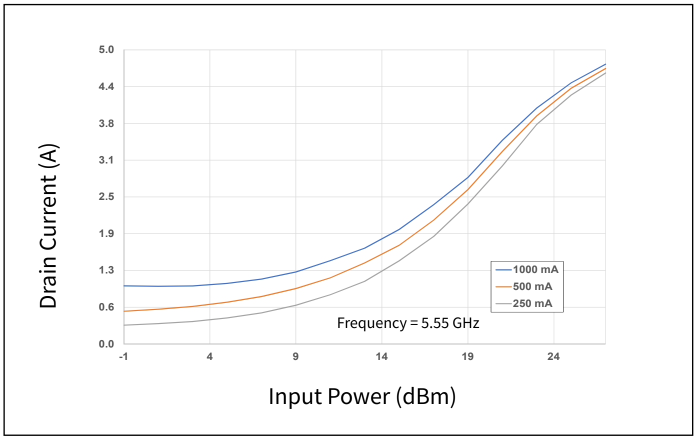

Figure 26. Drain Current vs Input Power as a Function of I_{DQ}

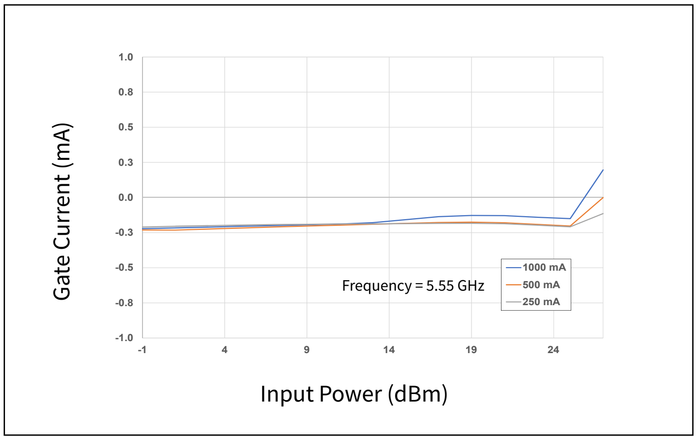

Figure 27. Gate Current vs Input Power as a Function of I_{DQ}

Typical Performance of the CMPA5259050S

Test conditions unless otherwise noted: V_D = 28 V, I_{DQ} = 500 mA, Pulse Width = 150µs, Duty Cycle = 20%, P_{IN} = 25 dBm, T_{BASE} = +25°C

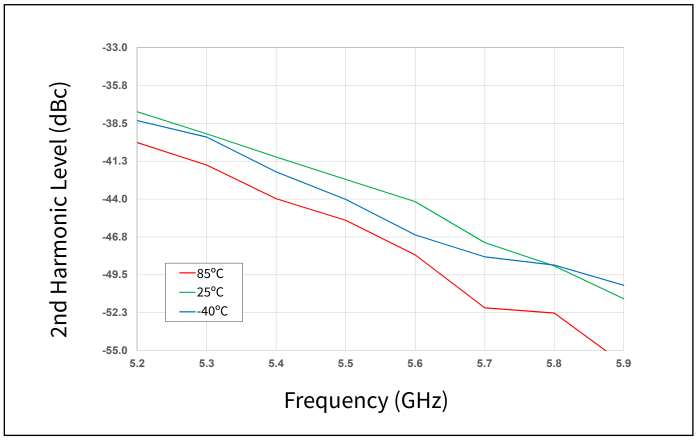

Figure 28. 2nd Harmonic vs Frequency as a Function of Temperature

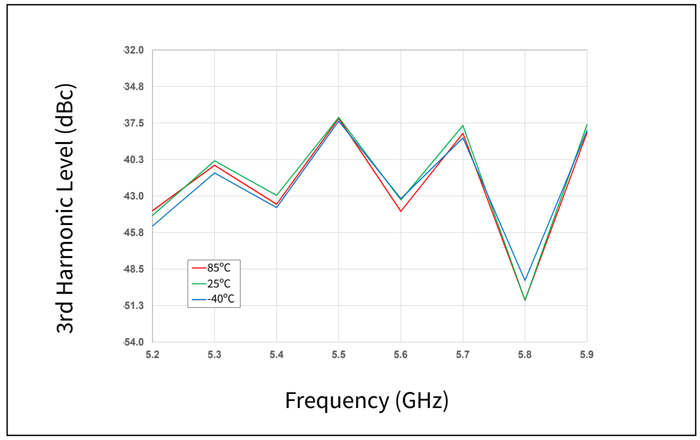

Figure 29. 3rd Harmonic vs Frequency as a Function of Temperature

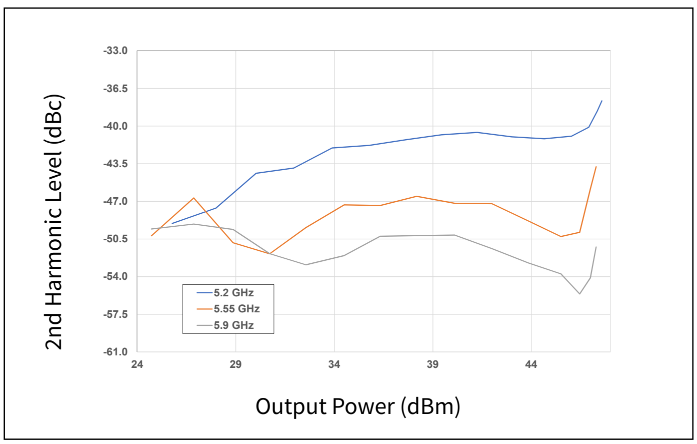

Figure 30. 2nd Harmonic vs Output Power as a Function of Frequency

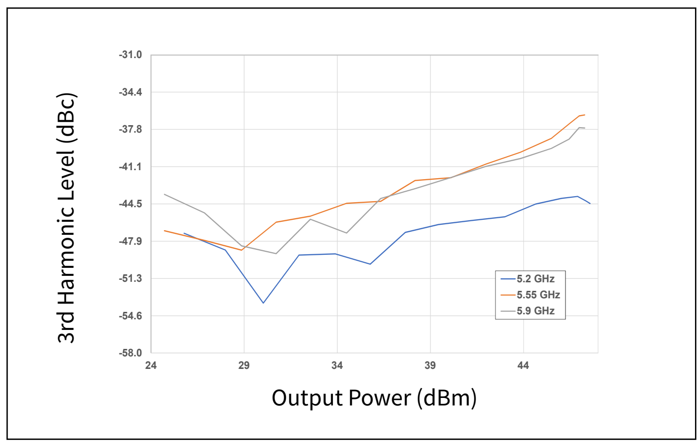

Figure 31. 3rd Harmonic vs Output Power as a Function of Frequency

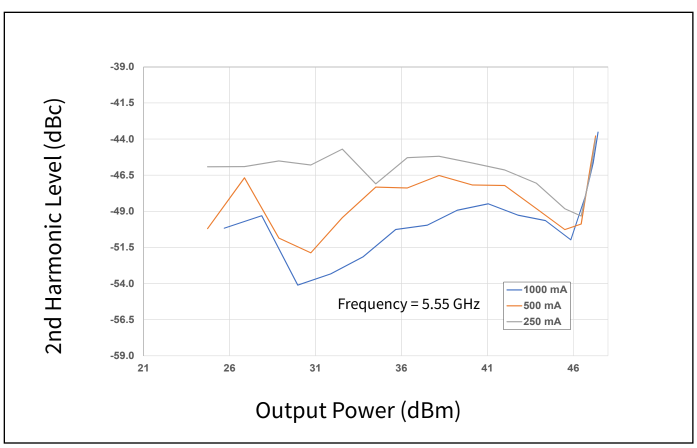

Figure 32. 2nd Harmonic vs Output Power as a Function of I_{DQ}

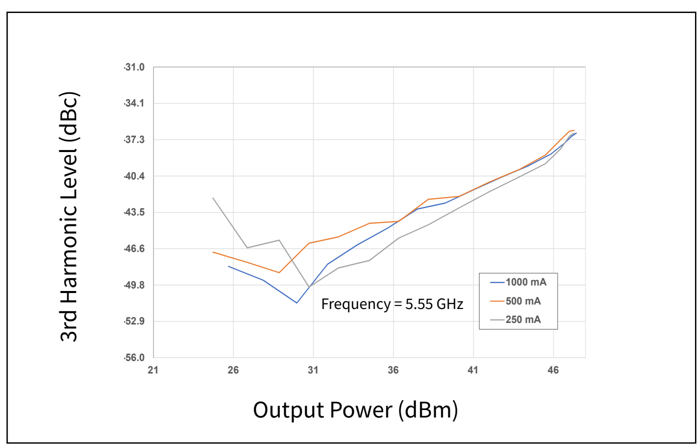

Figure 33. 3rd Harmonic vs Output Power as a Function of I_{DQ}

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Typical Performance of the CMPA5259050S

Test conditions unless otherwise noted: V_D = 28 V, I_{DQ} = 500 mA, P_{IN} = -20 dBm, T_{BASE} = +25°C

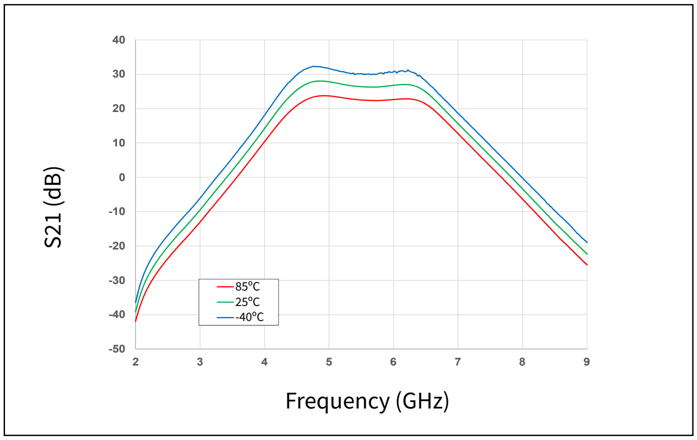


Figure 34. Gain vs Frequency as a Function of Temperature

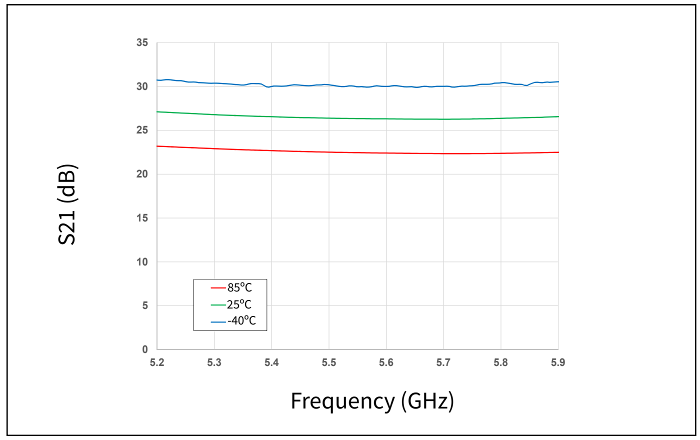


Figure 35. Gain vs Frequency as a Function of Temperature

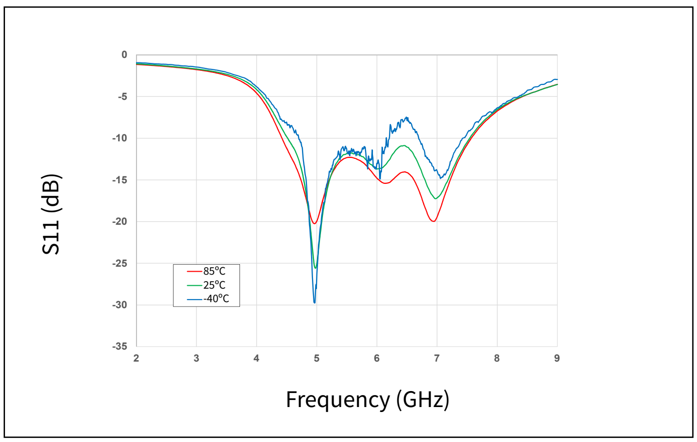


Figure 36. Input RL vs Frequency as a Function of Temperature

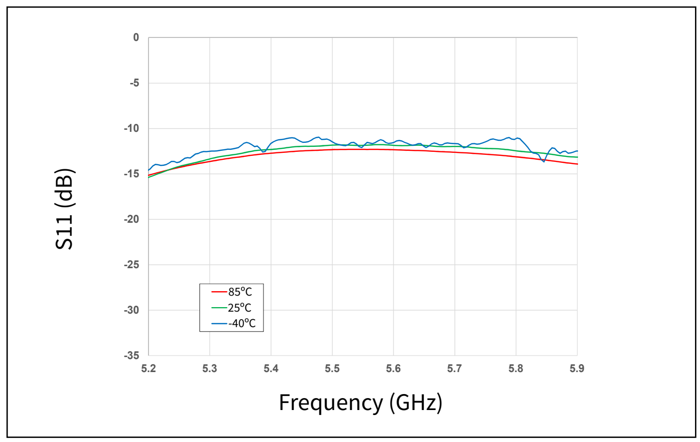


Figure 37. Input RL vs Frequency as a Function of Temperature

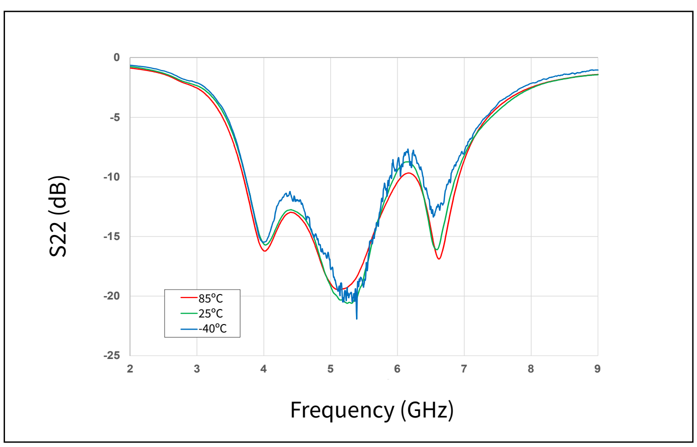


Figure 38. Output RL vs Frequency as a Function of Temperature

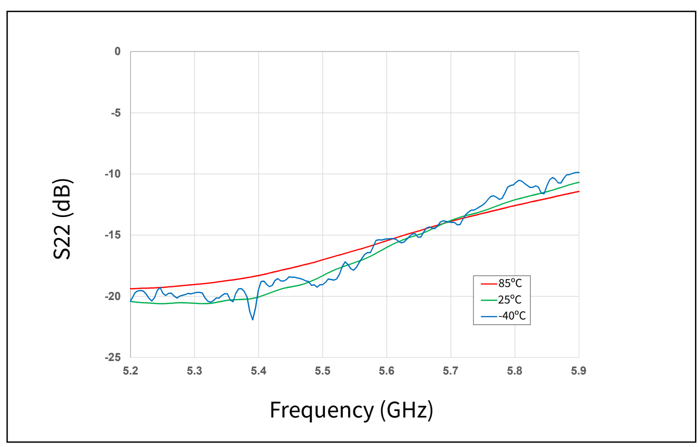


Figure 39. Output RL vs Frequency as a Function of Temperature

Typical Performance of the CMPA5259050S

Test conditions unless otherwise noted: V_D = 28 V, I_{DQ} = 500 mA, P_{IN} = -20 dBm, T_{BASE} = +25°C

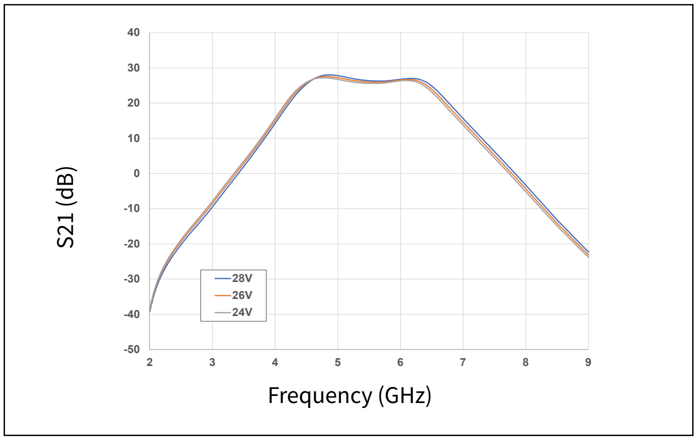


Figure 40. Gain vs Frequency as a Function of Voltage

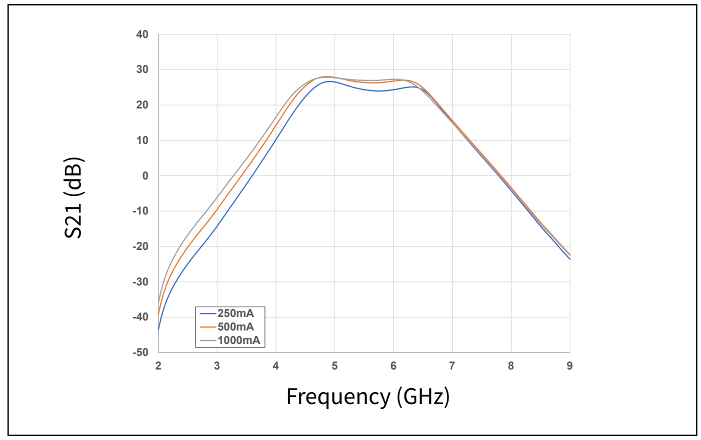


Figure 41. Gain vs Frequency as a Function of I_{DQ}

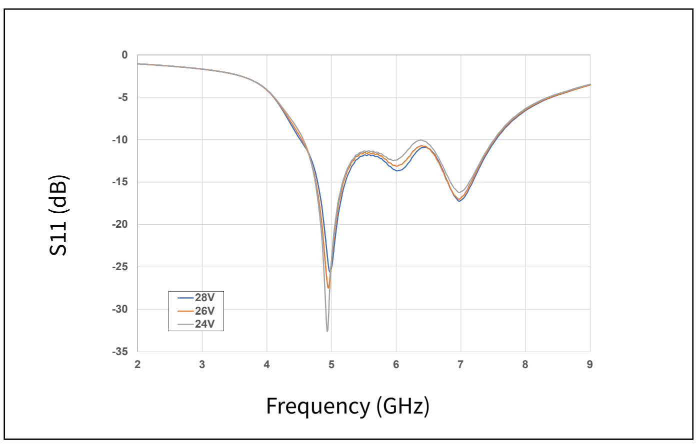


Figure 42. Input RL vs Frequency as a Function Voltage

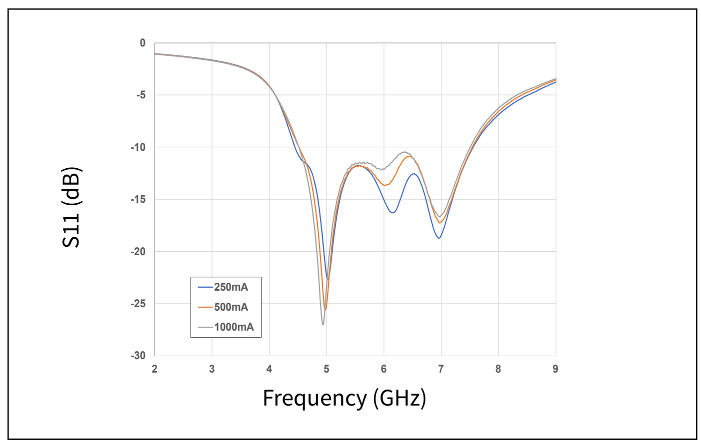


Figure 43. Input RL vs Frequency as a Function of I_{DQ}

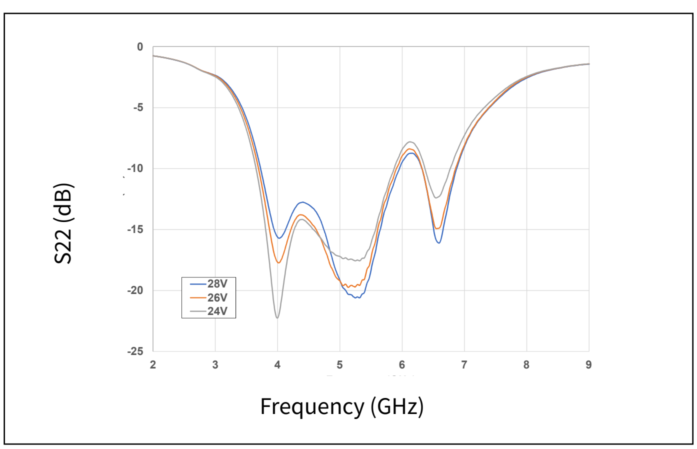


Figure 44. Output RL vs Frequency as a Function of Voltage

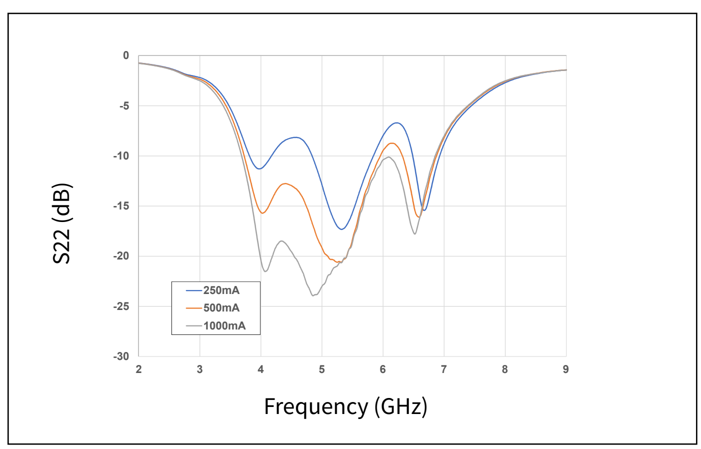
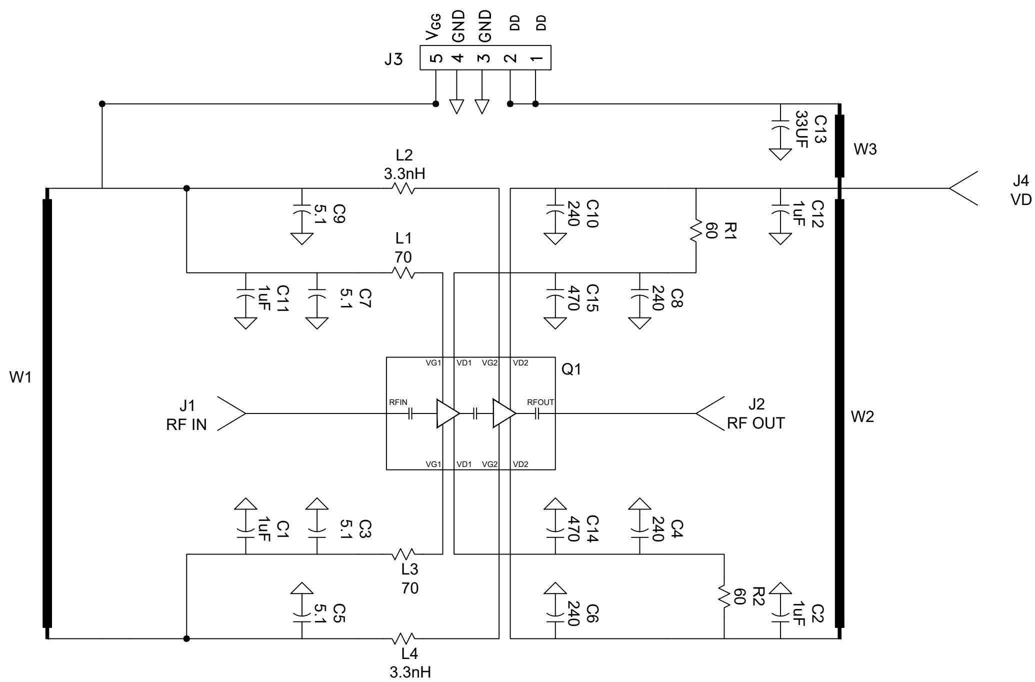
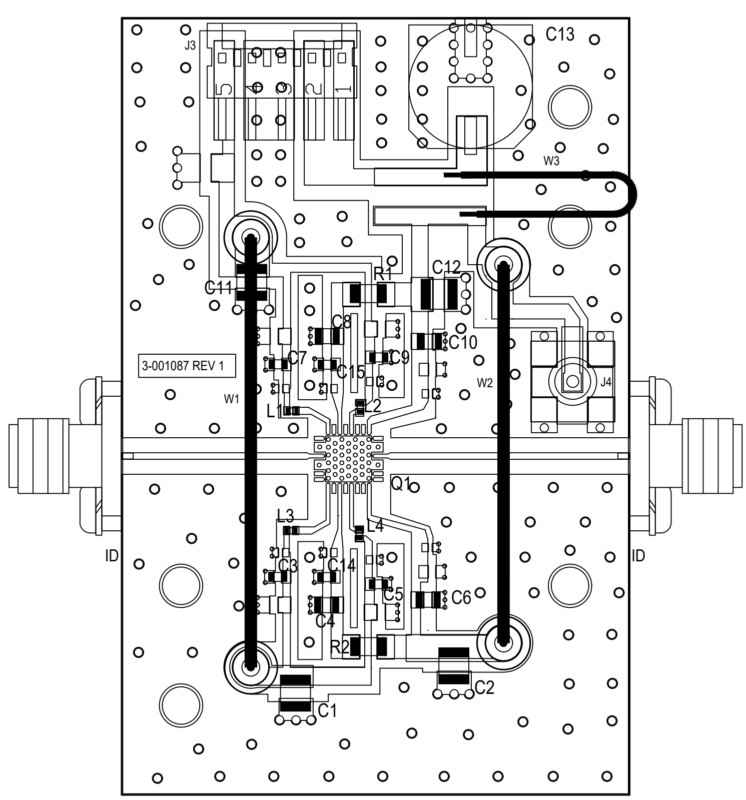


Figure 45. Output RL vs Frequency as a Function of I_{DQ}

CMPA5259050S-AMP1 Demonstration Amplifier Schematic



CMPA5259050S-AMP1 Demonstration Amplifier Circuit Outline



CMPA5259050S-AMP1 Demonstration Amplifier Circuit Bill of Materials

Designator	Description	Qty
C13	CAP, 33µF, 20%, G CASE	1
C1, C2, C11, C12	CAP, 1.0µF, 100V, 10%, X7R, 1210	4
C3, C5, C7, C9	CAP, 5.1pF, +/-0.05pF, 0603, ATC, 600S	4
C4, C6, C8, C10	CAP, 240pF +/-5%, 0805, ATC, 600F	4
C14, C15	470pF, NPO/COG 0603	2
L2, L4	INDUCTOR, SMT, 0402, 3.3nH, 5%	2
L1, L3	Ferrite bead, 70 ohm, 780mA, 0402	2
R1, R2	Ferrite bead, 60 ohm, 3.7A, 18806	2
J1, J2	CONN, SMA, PANEL MOUNT JACK, FLANGE, 4-HOLE, BLUNT POST, 20MIL	2
J3	HEADER RT>PLZ .1CEN LK 5POS	1
J4	CONN, SMB, STRAIGHT JACK RECEPTACLE, SMT, 50 OHM, Au PLATED	1
W1	WIRE, BLACK, 20 AWG ~ 1.5”	1
W2	WIRE, BLACK, 20 AWG ~ 1.3”	3
W3	WIRE, BLACK, 20 AWG ~ 1.5”	3
	PCB, TEST FIXTURE, RF35, 0.010", 5X5 2-STAGE, QFN	1
	HEATSINK, 6X6 QFN, 3-STAGE 2.600 X 1.700 X 0.250	1
	2-56 SOC HD SCREW 3/16 SS	4
	#2 SPLIT LOCKWASHER SS	4
Q1	CMPA5259050S	1

Electrostatic Discharge (ESD) Classifications

Parameter	Symbol	Class	Classification Level	Test Methodology
Human Body Model	HBM	1B	ANSI/ESDA/JEDEC JS-001 Table 3	JEDEC JESD22 A114-D
Charge Device Model	CDM	C3	ANSI/ESDA/JEDEC JS-002 Table 3	JEDEC JESD22 C101-C

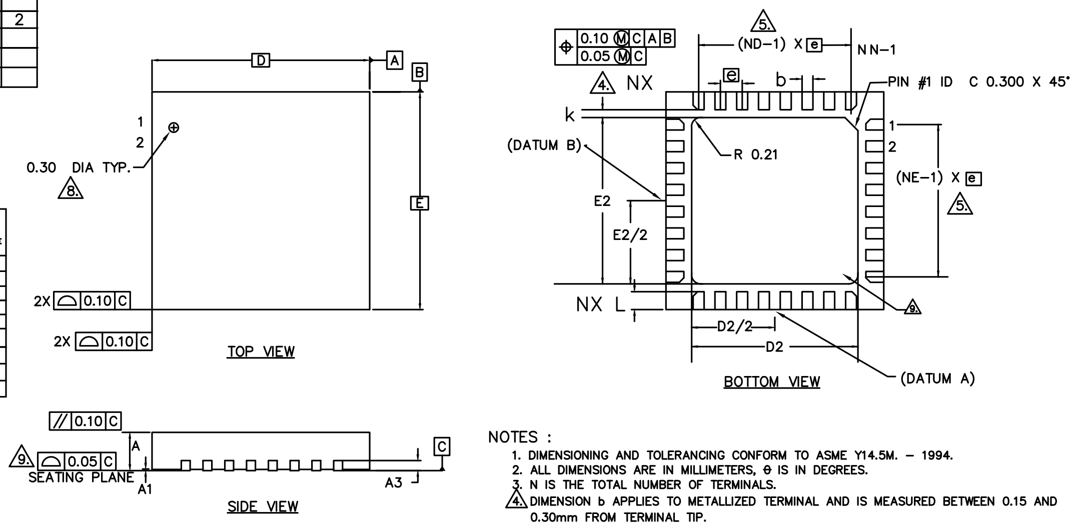
Moisture Sensitivity Level (MSL) Classification

Parameter	Symbol	Level	Test Methodology
Moisture Sensitivity Level	MSL	3 (168 hours)	IPC/JEDEC J-STD-20

Product Dimensions CMPA5259050S (Package 5 x 5 QFN)

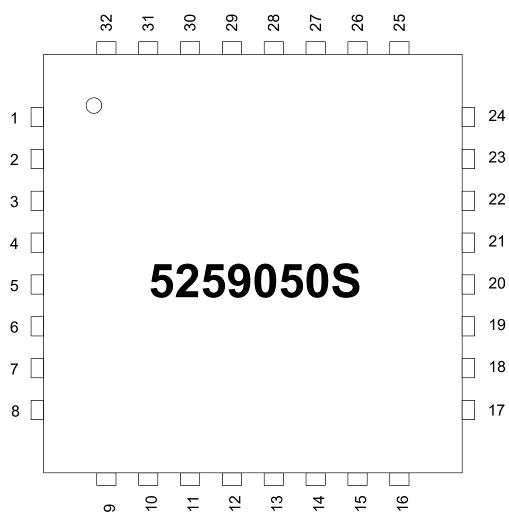
SYMBOL	MIN.	NOM.	MAX.	NOTE
A	0.80	0.90	1.00	
A1	0.00	0.03	0.06	
A3		0.203 REF.		
θ	0	——	12	2
K		0.17 MIN.		
D		5.0 BSC		
E		5.0 BSC		

SYMBOL	0.50mm LEAD PITCH			NOTE
	MIN.	NOM.	MAX.	
e		0.50 BSC.		
N		32		3
ND		8		5
NE		8		5
L	0.35	0.41	0.46	
b	0.21	0.25	0.29	4
D2	3.76	3.82	3.88	
E2	3.76	3.82	3.88	



NOTES :

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M. – 1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS, θ IS IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP.
5. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
6. MAX. PACKAGE WARPAGE IS 0.05 mm.
7. MAXIMUM ALLOWABLE BURRS IS 0.076 mm IN ALL DIRECTIONS.
8. PIN #1 ID ON TOP WILL BE LASER MARKED.
9. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
10. THIS DRAWING CONFORMS TO JEDEC REGISTERED OUTLINE MO–220
11. ALL PLATED SURFACES ARE 100% TIN MATTE 0.010 mm +/– 0.005 mm.



PIN	DESC.	PIN	DESC.	PIN	DESC.
1	NC	15	NC	29	NC
2	NC	16	VD2A	30	VD1B
3	RFGND	17	NC	31	NC
4	RFIN	18	NC	32	VG1B
5	RFGND	19	NC		
6	NC	20	RFGND		
7	NC	21	RFOUT		
8	NC	22	RFGND		
9	VG1A	23	NC		
10	NC	24	NC		
11	VD1A	25	VD2B		
12	NC	26	NC		
13	VG2A	27	NC		
14	NC	28	VG2B		

Part Number System

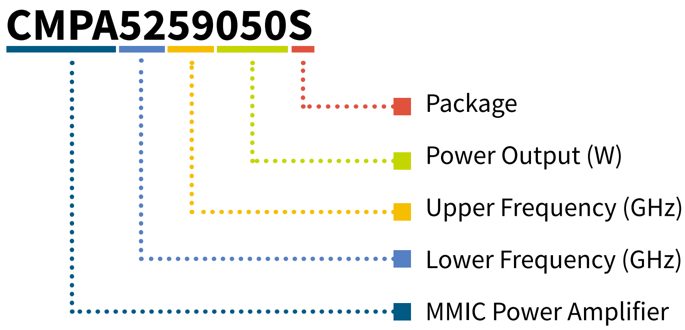


Table 1.

Parameter	Value	Units
Lower Frequency	5.0	GHz
Upper Frequency	5.9	
Power Output	50	W
Package	Surface Mount	—

Note:
[1] Alpha characters used in frequency code indicate a value greater than 9.9 GHz. See Table 2 for value.

Table 2.

Character Code	Code Value
A	0
B	1
C	2
D	3
E	4
F	5
G	6
H	7
J	8
K	9
Examples	1A = 10.0 GHz 2H = 27.0 GHz

Product Ordering Information

Order Number	Description	Unit of Measure	Image
CMPA5259050S	GaN HEMT	Each	
CMPA5259050S-AMP1	Test board with GaN MMIC installed	Each	

Notes & Disclaimer

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