# BLP25RFE001

## Signal generator for RF energy solutions

AMPLEON

Rev. 2 — 26 January 2018

Product data sheet

## 1. General description

The product provides an all-in-one solution for the small signal generation in the RF energy solutions such as cooking and lighting markets.

The product facilitates RF energy design by:

- Allowing on-board integration
- Providing flexibility in system solution development

## 2. Features and benefits

- Support from 2400 MHz to 2483.5 MHz, from 902 MHz to 928 MHz and from 433 MHz to 434.8 MHz ISM bands
- Single 3.3 V supply voltage
- SPI-bus interface up to 20 MHz
- Fully integrated LC-VCO operating in the range from 6.6 GHz to 10 GHz and used with a ΣΔ PLL to generate the frequency
- Very fast tuning and hopping time PLL
- High frequency daisy chaining allowing coherent excitation of multiple RF amplifier chains
- 360° phase shifter with 1.4° steps
- Medium Power Amplifier (MPA) delivering an output up to +27 dBm peak power (max. +24 dBm for continuous use)
- Low Power Amplifier (PPA) delivering an output up to +7 dBm
- Integrated 20 dB gain control
- Integrated RF switch allowing PWM control
- Temperature sensor indicates the junction temperature of the die
- RoHS compliant

## 3. Applications

- Solid-state cooking
- Solid-state lighting

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# 4. Ordering information

**Table 1. Ordering information**

| Type number | Package | | |
|---|---|---|---|
| | Name | Description | Version |
| BLP25RFE001 | HVQFN28 | plastic thermal enhanced very thin quad flat package; no leads; 28 terminals; body 5 × 5 × 0.85 mm | SOT993-3 |

# 5. Marking

**Table 2. Marking codes**

| Type number | Marking code |
|---|---|
| BLP25RFE001 | E2501 |


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**Table 3. BLP25RFE001 pin description** *…continued*

| Symbol | Pin | Description |
|---|---|---|
| $V_{DD(RF)}$ | 17 | RF power supply; 3.3 V |
| PPA_OUT_P | 18 | RF low-power positive output |
| PPA_OUT_N | 19 | RF low-power negative output |
| MPA_LP_OUT_P | 20 | RF Intermediate supply for high-power first stage MPA positive path |
| MPA_LP_OUT_N | 21 | RF Intermediate supply for high-power first stage MPA negative path |
| MPA_HP_OUT_P | 22 | medium-power RF amplifier positive output |
| MPA_HP_OUT_N | 23 | medium-power RF amplifier negative output |
| SWITCH | 24 | RF switch control |
| GND(DIG) | 25 | digital ground |
| MISO | 26 | SPI-bus: Master Input Slave Output |
| MOSI | 27 | SPI-bus: Master Output Slave Input |
| SCLK | 28 | SPI-bus: Serial Clock (from master) |
| Exposed die pad | - | connect to RF ground |

# 8. Functional description

General purpose 4 wires SPI-bus with a dedicated integrated oscillator for the digital clock, enabling high-speed SPI-bus.

Very high frequency LC oscillator running at 4 × Fout for lowest pulling sensitivity.

Fractional-N PLL enabling 10 kHz steps at Fout with a very low PLL settling time.

ADC on Vtune for an easy estimation via SPI-bus of the PLL locking point.

High frequency daisy chaining operation enabling coherent frequencies to all the circuits in the application.

360° phase shifter with small and accurately controlled steps (1.4° typical).

Medium RF power output: up to +27 dBm peak power (max. +24 dBm for continuous use).

Low RF power output up to 7 dBm adjustable.

Integrated RF switch (dedicated control pin SWITCH) allowing PWM control of the RF outputs (MPA/PPA).

## 8.1 Medium Power Amplifier (MPA)

The medium power amplifier (MPA) consists of 3 cascaded gain stages. The last 2 stages have open collector which must be DC supplied through adequate reactive circuitry to optimize power and efficiency. The third stage is able to drive up to +27 dBm peak power (max. +24 dBm for continuous use) into 50 Ω. The output matching network is for impedance transformation (from 40 Ω to 50 Ω) and also acts as a low pass filter that attenuates harmonics.


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## 8.2 Low-Power Amplifier (PPA)

The low power amplifier (PPA) consists of 2 cascaded gain stages. The last stage have open collector which must be DC supplied through adequate reactive circuitry to optimize power and efficiency. The third stage is able to drive up to 7 dBm into 50 Ω. The output matching network is for impedance transformation (from 200 Ω to 50 Ω) and also acts as a low pass filter that attenuates harmonics.

## 8.3 SPI-bus interface

- The SPI-bus protocol used on BLP25RFE001 IC is composed of:
  - 2 operand code bits (00: write, 01: read, 1x: reserved)
  - 6 address bits
  - 8 data bits
- A burst mode, in write and read mode, is implemented (an auto-increment of the address is used to manage this mode)
- The SPI-bus frequency up to 20 MHz
- MISO output pin is not tri-state and cannot be connected with an other BLP25RFE001 IC


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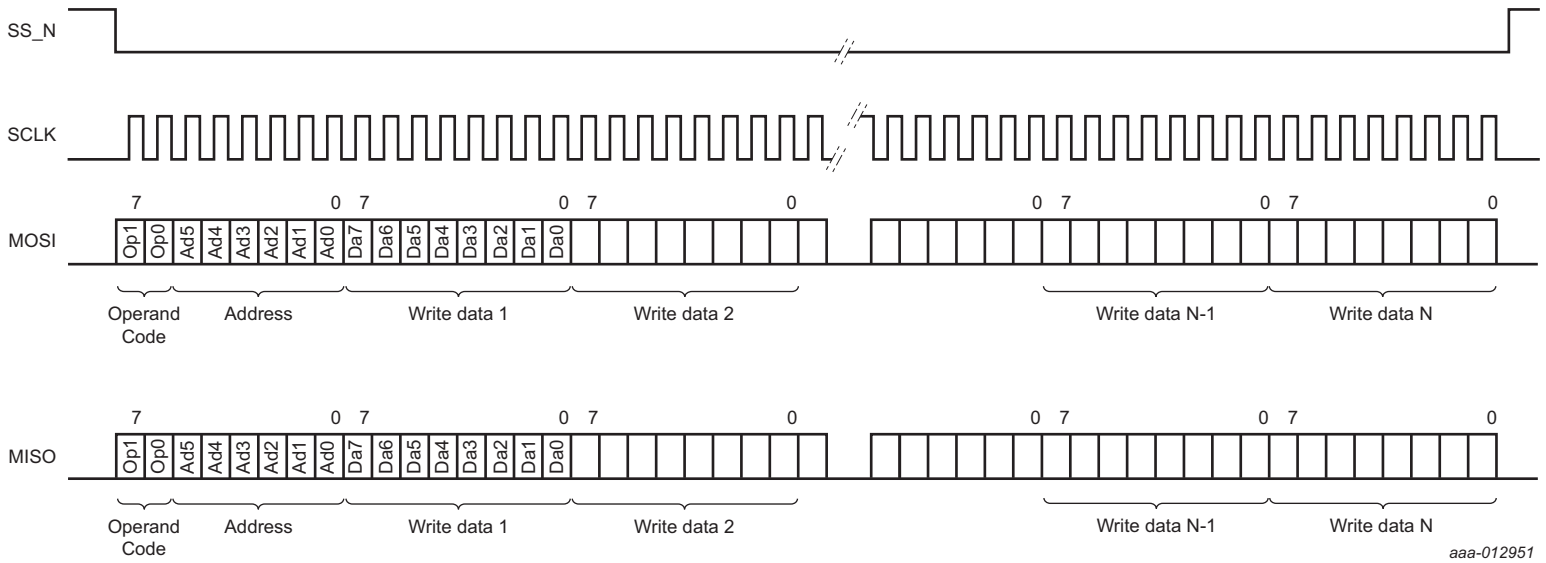
### 8.3.1 SPI-bus write protocol burst mode




Operand Code Op[1:0] = 00.

**Fig 3. SPI-bus write protocol burst mode**



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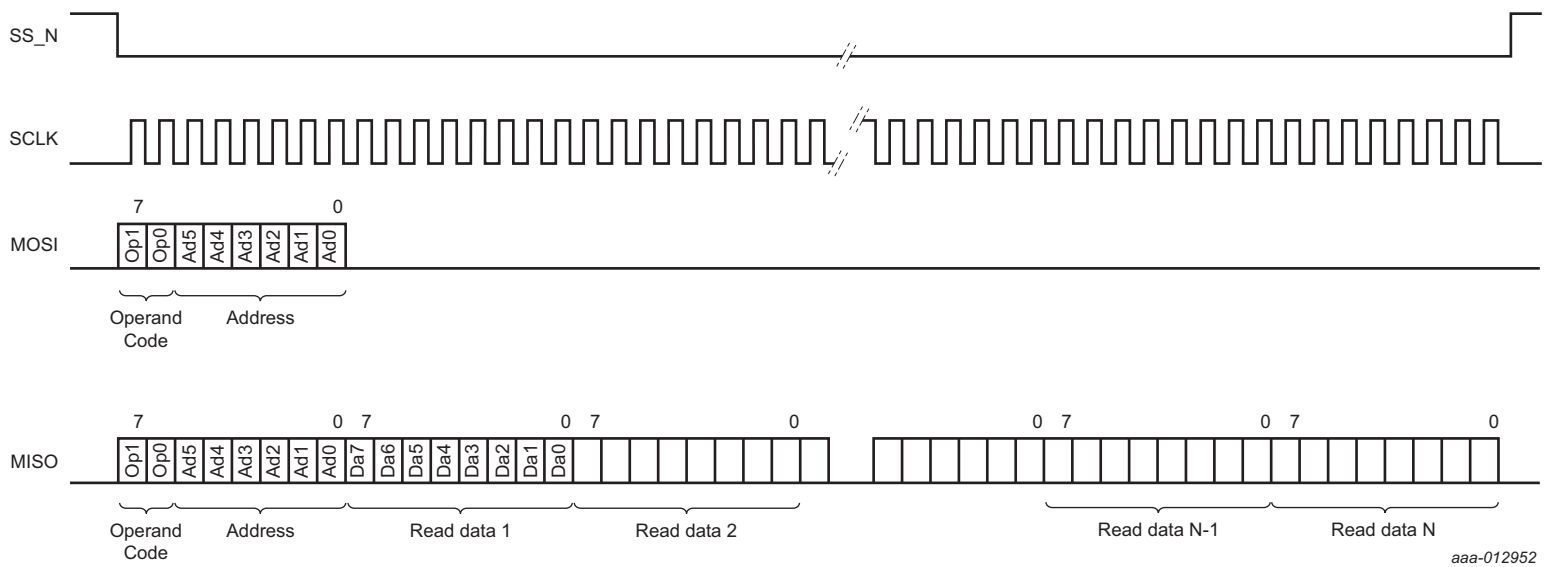
### 8.3.2 SPI-bus read protocol burst mode




Operand Code Op[1:0] = 01.

**Fig 4. SPI-bus read protocol burst mode**



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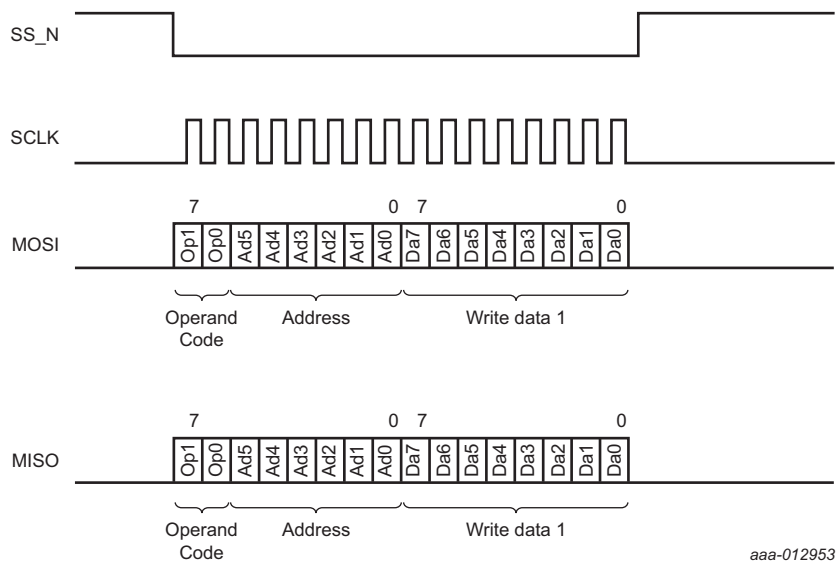
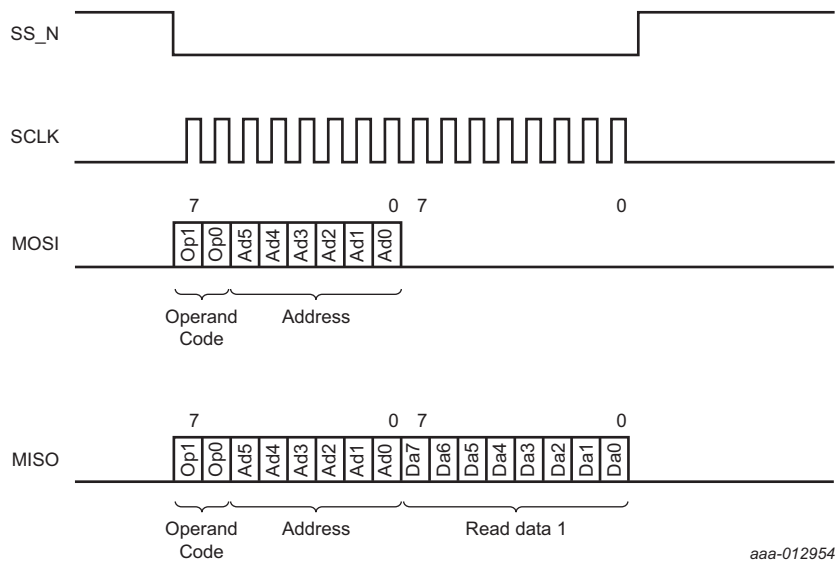
### 8.3.3 SPI-bus write protocol 16 bits frame




Operand Code Op[1:0] = 00;

**Fig 5. SPI-bus write protocol 16 bits frame**

### 8.3.4 SPI-bus read protocol 16 bits mode




Operand Code Op[1:0] = 01.

**Fig 6. SPI-bus read protocol 16 bits mode**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### 8.3.5 SPI-bus timings

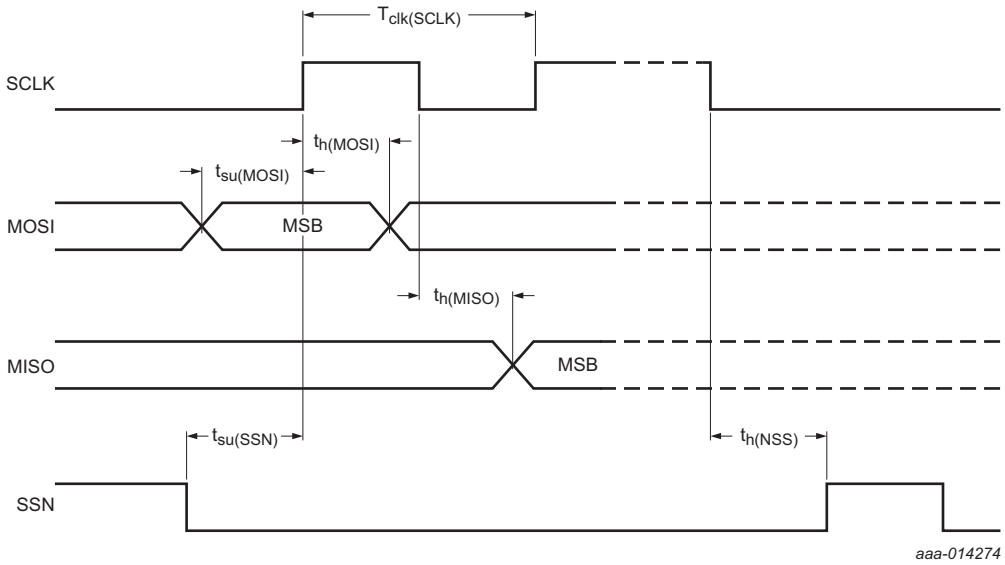


**Fig 7. SPI-bus timing diagram**

**Table 4. SPI-bus timings specification**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $T_{clk(SCLK)}$ | clock period on pin SCLK | | 50 | - | ns |
| $t_{su(MOSI)}$ | MOSI set-up time | | 12 | - | ns |
| $t_{h(MOSI)}$ | MOSI hold time | | 0 | - | ns |
| $t_{h(MISO)}$ | MISO hold time | | - | 0 | ns |
| $t_{h(SSN)}$ | SSN hold time | | 0 | - | ns |
| $t_{su(SSN)}$ | SSN set-up time | | 12 | - | ns |

## 8.4 Temperature sensor

The temperature sensor indicates the junction temperature of the die via SPI-bus interface. This feature has been implemented to provide an indicator for the soldering process. If the exposed die pad is not properly soldered, the thermal dissipation is affected, leading to a junction temperature increase.

The sensor provides the junction temperature in the range from 22 °C to 127 °C.


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# 9. Control interface

## 9.1 Register table description

**Table 5. Register table description**

| Address (h) | Name | Bit | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 00 | ID_1 | MAJOR_REV[3:0] | | | | MINOR_REV[3:0] | | | |
| 01 | POWER_STATUS_1 | LO_Lock | LO_forced_lock | - | | | | | POR |
| 02 | VCO_LOG | - | adc_vtune[2:0] | | | - | | | |
| 04 | LO_CALIB_1 | - | | LO_calib_counter_1[5:0] | | | | | |
| 05 | LO_CALIB_2 | LO_calib_counter_2[7:0] | | | | | | | |
| 07 | THERMO_1 | - | TM_D [6:0] | | | | | | |
| 08 | IRQ_status | - | | | | | | VCO_Freq_End | - |
| 09 | IRQ_enable | - | | | | | | VCO_Freq_Enable | - |
| 0A | IRQ_clear | - | | | | | | VCO_Freq_Clear | - |
| 0B | IRQ_set | - | | | | | | VCO_Freq_Set | - |
| 0C | THERMO_2 | - | | | | | | | TM_ON |
| 0D | XT_OUT | - | | | | | 0 | | |
| 0E | XT_CAL_2 | XT_In_Force | XT_Cal_Bypass | XT_cal_timer [1:0] | | XT_Dac_Force [3:0] | | | |
| 0F | POWER_DOWN_1 | pd_lotest | pd_Synthe | pd_adc_vtune | pd_rf_mpa | pd_rf_ppa | 1 | pd_rf_tx | pd_lochain |
| 10 | POWER_DOWN_2 | - | | | | | 0 | pd_daisy_out | pd_daisy_in |
| 11 | POWER_SAVING_MODE_1 | - | | | | | | 1 | 0 |
| 12 | RF_LO_DRIVER | - | | | | | | 0 | 1 |
| 13 | DAISY_CHAIN_1 | - | | | lomux_to_daisy | 0 | 1 | 1 | 0 |
| 14 | RF_PHASE_SHIFTER_1 | rf_load_capa[3:0] | | | | 0 | 1 | 1 | 0 |
| 15 | RF_PHASE_SHIFTER_2 | rf_phase_selector[7:0] | | | | | | | |
| 16 | RF_PHASE_SHIFTER_3 | - | | | | | | 0 | 1 |
| 19 | RF_PPA_MPA_1 | - | | rf_mpa_power[5:0] | | | | | |
| 1A | RF_PPA_MPA_2 | - | 0 | | | rf_mpa_bias_ctrl[1:0] | | 1 | 0 |
| 1B | LO_CHAIN | ckdiv2_reset | ckdiv2_start | ckdiv2_invert | PLL_Div2_Highfreq | LoChain_ratio[3:0] | | | |


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**Table 5. Register table description** *…continued*

| Address (h) | Name | Bit | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 1C | SD_1 | LO_Int [7:0] | | | | | | | |
| 1D | SD_2 | - | LO_Frac_2[6:0] | | | | | | |
| 1E | SD_3 | LO_Frac_1[7:0] | | | | | | | |
| 1F | CP | - | 0 | | | 1 | 1 | 1 | 1 |
| 20 | SD_TEST | - | 1 | 0 | | | | 1 | 0 |
| 21 | VCO | - | 1 | 0 | 1 | 0 | 1 | VCO_Select[1:0] | |
| 23 | REG | - | | 0 | 1 | 0 | 1 | 0 | 1 |
| 28 | POWERDOWN | - | | | | | | force_soft_reset | Soft_reset |
| 2B | PROGR_REG | - | | | | | | | Update_prg |
| 2C | LAUNCH | - | | | | | | fvco_max_Launch | - |
| 3E | RESERVED_0 | | | | reserved_0 [4:0] | | | | |
| 3F | RESERVED_1 | | | | | | | reserved_1 [1:0] | |


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**Table 6. ID_1 bit descriptions**

| Address | Register | Bit | Symbol | Access | Value (b) | Description |
|---|---|---|---|---|---|---|
| 00 | ID_1 | 7 to 4 | MAJOR_REV[3:0] | R | 0001 | major revision of the IC |
| | | 3 to 0 | MINOR_REV[3:0] | R | 0000 | minor revision of the IC |

**Table 7. POWER_STATUS_1 bit descriptions**

| Address | Register | Bit | Symbol | Access | Value | Description |
|---|---|---|---|---|---|---|
| 01 | POWER_STATUS_1 | 7 | LO_Lock | R | | PLL lock status indicator |
| | | | | | 0 | PLL unlocked |
| | | | | | 1 | PLL locked |
| | | 6 | LO_forced_lock | R | | forces PLL Lock bit if not present after 5 ms |
| | | | | | 0 | LO_lock_force not triggered (LO_lock was present before 5 ms) |
| | | | | | 1 | LO_lock_force triggered (LO_lock was not present before 5 ms) |
| | | 0 | POR | R | | Power-On Reset |
| | | | | | 0 | the chip supply voltage did not fall below the POR threshold voltage since the previous read operation of this bit |
| | | | | | 1 | the chip supply voltage felt below the POR threshold voltage (an HW reset has occurred). So the IC must be initialized before any further action. Reading this bit resets it |

**Table 8. VCO_LOG bit descriptions**

| Address | Register | Bit | Symbol | Access | Value | Description |
|---|---|---|---|---|---|---|
| 02 | VCO_LOG | 6 to 4 | adc_vtune[2:0] | R | | output value of ADC connected to Vtune |
| | | | | | 0 | 0 V to 0.33 V |
| | | | | | 1 | 0.33 V to 0.45 V |
| | | | | | 2 | 0.45 V to 0.58 V |
| | | | | | 3 | 0.58 V to 1.05 V |
| | | | | | 4 | 1.05 V to 1.62 V |
| | | | | | 5 | 1.62 V to 1.84 V |
| | | | | | 6 | 1.84 V to 2.1 V |
| | | | | | 7 | > 2.1 V |

**Table 9. LO_CALIB_1 bit descriptions**

| Address | Register | Bit | Symbol | Access | Value | Description |
|---|---|---|---|---|---|---|
| 04 | LO_CALIB_1 | 5 to 0 | LO_calib_counter_1[5:0] | R | [1] | current VCO frequency measurement result (MSB) |

[1] VCO frequency measurement result (kHz) = 125 / 16 × decimal(LO_calib_counter[13:0]), with LO_calib_counter[13:0] = $2^8$ × LO_calib_counter_1[5:0] + LO_calib_counter_2[7:0].


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**Table 10. LO_CALIB_2 bit descriptions**

| Address | Register | Bit | Symbol | Access | Value | Description |
|---|---|---|---|---|---|---|
| 05 | LO_CALIB_2 | 7 to 0 | LO_calib_counter_2[7:0] | R | [1] | current VCO frequency measurement result (LSB) |

[1] VCO frequency measurement result (kHz) = 125 / 16 × decimal(LO_calib_counter[13:0]), with LO_calib_counter[13:0] = $2^8$ × LO_calib_counter_1[5:0] + LO_calib_counter_2[7:0].

**Table 11. THERMO_1 bit descriptions**

| Address | Register | Bit | Symbol | Access | Value | Description |
|---|---|---|---|---|---|---|
| 07 | THERMO_1 | 6 to 0 | TM_D[6:0] | R | | junction temperature measurement |
| | | | | | [000 0000: 001 0101] | junction temperature < 22 °C |
| | | | | | [001 0110: 111 1110] | 22 °C ≤ junction temperature = decimal(TM_DA[6:0]) < 127 °C |
| | | | | | 111 1111 | junction temperature ≥ 127 °C |

**Table 12. IRQ_status bit descriptions**

| Address | Register | Bit | Symbol | Access | Value | Description |
|---|---|---|---|---|---|---|
| 08 | IRQ_status | 1 | VCO_Freq_End | R | | VCO frequency measurement end IRQ |

**Table 13. IRQ_enable bit descriptions**

| Address | Register | Bit | Symbol | Access | Value | Description |
|---|---|---|---|---|---|---|
| 09 | IRQ_enable | 1 | VCO_Freq_Enable | RW | | VCO frequency measurement IRQ enable |

**Table 14. IRQ_clear bit descriptions**

| Address | Register | Bit | Symbol | Access | Value | Description |
|---|---|---|---|---|---|---|
| 0A | IRQ_clear | 1 | VCO_Freq_Clear | RW | | VCO frequency measurement IRQ clear |

**Table 15. IRQ_set bit descriptions**

| Address | Register | Bit | Symbol | Access | Value | Description |
|---|---|---|---|---|---|---|
| 0B | IRQ_set | 1 | VCO_Freq_Set | RW | | VCO frequency measurement IRQ set |

**Table 16. THERMO_2 bit descriptions**

| Address | Register | Bit | Symbol | Access | Value | Description |
|---|---|---|---|---|---|---|
| 0C | THERMO_2 | 0 | TM_ON | RW | | temperature sensor ON or OFF |
| | | | | | 0 | disable the temperature sensor |
| | | | | | 1 | enable the temperature sensor |


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**Table 17. XT_CAL_2 bit descriptions**

| Address | Register | Bit | Symbol | Access | Value | Description |
|---|---|---|---|---|---|---|
| 0E | XT_CAL_2 | 7 | XT_In_Force | RW | | Xtal oscillator Master/Slave mode |
| | | | | | 0 | Xtal Osc Master mode (forbidden) |
| | | | | | 1 | Xtal Osc Slave mode (External 16MHz signal to be provided) |
| | | 6 | XT_Cal_Bypass | RW | | allow bypass of the Xtal calibration value with XT_Dac_Force[3:0] from SPI-bus |
| | | | | | 0 | XT_Cal_Bypass OFF |
| | | | | | 1 | XT_Cal bypassed with XT_Dac_Force value |
| | | 5 to 4 | XT_cal_timer[1:0] | RW | | Xtal oscillator calibration timer selection |
| | | | | | 0 | 5.12 ms |
| | | | | | 1 | 10.24 ms |
| | | | | | 2 | 20.48 ms |
| | | | | | 3 | 40.96 ms |
| | | 3 to 0 | XT_Dac_Force[3:0] | RW | [0:15] | Xtal Osc Amplitude Control value |

**Table 18. POWER_DOWN_1 bit descriptions**

| Address | Register | Bit | Symbol | Access | Value | Description |
|---|---|---|---|---|---|---|
| 0F | POWER_DOWN_1 | 7 | pd_lotest | RW | | LO test input buffer enable/disable |
| | | | | | 0 | LO test buffer disabled |
| | | | | | 1 | LO test buffer enabled |
| | | 6 | pd_Synthe | RW | | PLL enable/disable (excluding LO Chain) |
| | | | | | 0 | PLL disabled |
| | | | | | 1 | PLL enabled |
| | | 5 | pd_adc_vtune | RW | | enables/disables the ADC connected on Vtune |
| | | | | | 0 | ADC Vtune disabled |
| | | | | | 1 | ADC Vtune enabled |
| | | 4 | pd_rf_mpa | RW | | MPA ON/OFF |
| | | | | | 0 | MPA disabled |
| | | | | | 1 | MPA enabled |
| | | 3 | pd_rf_ppa | RW | | Pre PA ON/OFF |
| | | | | | 0 | Pre PA disabled |
| | | | | | 1 | Pre PA enabled |
| | | 1 | pd_rf_tx | RW | | phase shifter ON/OFF |
| | | | | | 0 | phase shifter disabled |
| | | | | | 1 | phase shifter enabled |
| | | 0 | pd_lochain | RW | | LOCHAIN ON/OFF |
| | | | | | 0 | LO Chain disabled |
| | | | | | 1 | LO Chain enabled |


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**Table 19. POWER_DOWN_2 bit descriptions**

| Address | Register | Bit | Symbol | Access | Value | Description |
|---|---|---|---|---|---|---|
| 10 | POWER_DOWN_2 | 1 | pd_daisy_out | RW | | daisy chaining output buffer enable/disable |
| | | | | | 0 | daisy output buffer disabled |
| | | | | | 1 | daisy output buffer enabled |
| | | 0 | pd_daisy_in | RW | | daisy chaining input buffer enable/disable |
| | | | | | 0 | daisy input buffer disabled |
| | | | | | 1 | daisy input buffer enabled |

**Table 20. DAISY_CHAIN_1 bit descriptions**

| Address | Register | Bit | Symbol | Access | Value | Description |
|---|---|---|---|---|---|---|
| 13 | DAISY_CHAIN_1 | 4 | lomux_to_daisy | RW | | allow LO signal to Daisy output buffer |
| | | | | | 0 | no signal to daisy output buffer |
| | | | | | 1 | allow LO to daisy output buffer |

**Table 21. RF_PHASE_SHIFTER_1 bit descriptions**

| Address | Register | Bit | Symbol | Access | Value | Description |
|---|---|---|---|---|---|---|
| 14 | RF_PHASE_SHIFTER_1 | 7 to 4 | rf_load_capa[7:4] | RW | | RF phase shifter filtering capacitor |
| | | | | | 1 | ISM band from 2.4 GHz to 2.483 GHz |
| | | | | | 5 | ISM band from 902 MHz to 928 MHz |
| | | | | | 10 | ISM band from 433 MHz to 435 MHz |

**Table 22. RF_PHASE_SHIFTER_2 bit descriptions**

| Address | Register | Bit | Symbol | Access | Value | Description |
|---|---|---|---|---|---|---|
| 15 | RF_PHASE_SHIFTER_2 | 7 to 0 | rf_phase_selector[7:0] | RW | [0:255][1] | RF phase shifter control; from 0° to 360° with 1.4° step |

[1] Do not set the values 0, 64, 128 and 192.

**Table 23. RF_PPA_MPA_1 bit descriptions**

| Address | Register | Bit | Symbol | Access | Value | Description |
|---|---|---|---|---|---|---|
| 19 | RF_PPA_MPA_1 | 5 to 0 | rf_mpa_power[5:0] | RW | | MPA/PPA output power control |
| | | | | | 0 | do not use |
| | | | | | from 1 to 62 | [1] |
| | | | | | 63 | [2]/[3] |

[1] See Figure 8.

[2] See Table 37 for $P_{o(max)}$ in MPA.

[3] See Table 37 for $P_{o(max)}$ in PPA.


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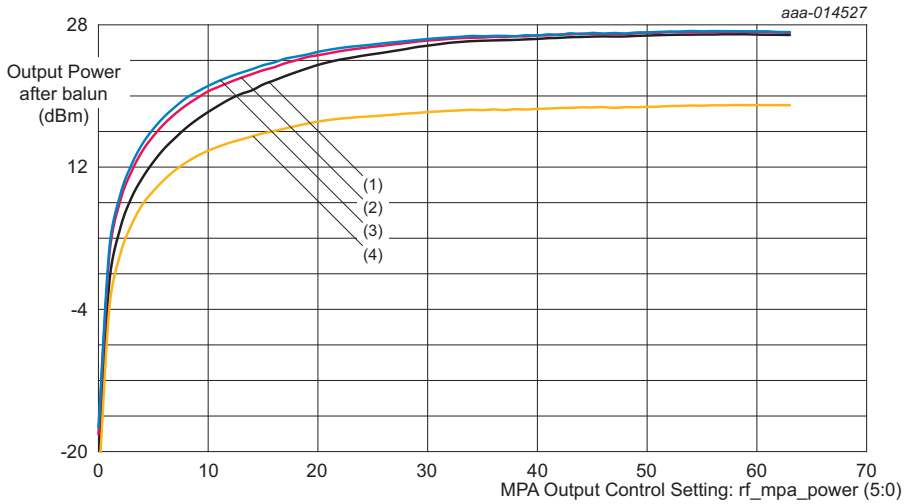
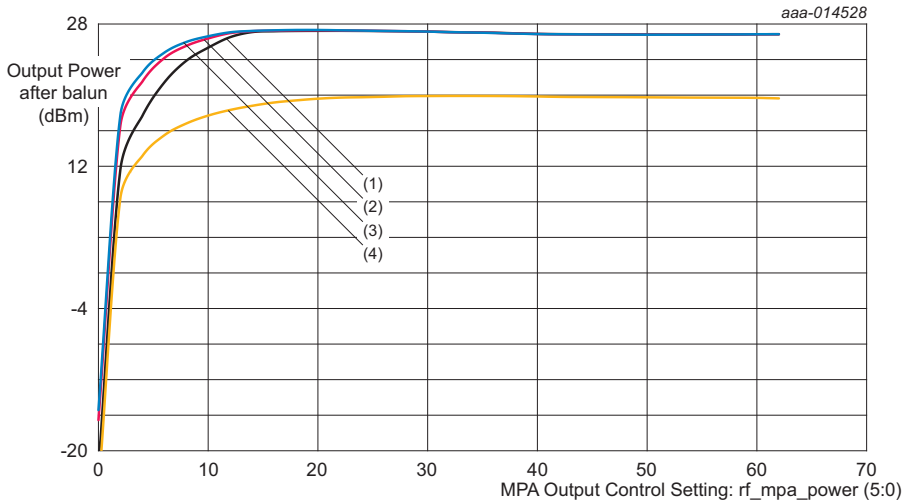



(1) MPA_bias_ctrl = 0.
(2) MPA_bias_ctrl = 1.
(3) MPA_bias_ctrl = 2.
(4) MPA_bias_ctrl = 3.
$V_{DD}$ = 3.3 V.
$t_{amb}$ = 25 °C.

**Fig 8. MPA output power at 2.4 GHz (typical)**




(1) MPA_bias_ctrl = 0.
(2) MPA_bias_ctrl = 1.
(3) MPA_bias_ctrl = 2.
(4) MPA_bias_ctrl = 3.
$V_{DD}$ = 3.3 V.
$t_{amb}$ = 25 °C.

**Fig 9. MPA output power at 915 MHz (typical)**


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**Table 24. RF_PPA_MPA_2 bit descriptions**

| Address | Register | Bit | Symbol | Access | Value | Description |
|---|---|---|---|---|---|---|
| 1A | RF_PPA_MPA_2 | 3 to 2 | rf_mpa_bias_ctrl[1:0] | RW | | MPA first and second stage bias current control |
| | | | | | 0 | +27 dBm / 150 μA / 300 μA |
| | | | | | 1 | +27 dBm / 200 μA / 400 μA |
| | | | | | 2 | +27 dBm / 250 μA / 500 μA |
| | | | | | 3 | +21 dBm / 150 μA / 300 μA |


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**Table 25. LO_CHAIN bit descriptions**

| Address | Register | Bit | Symbol | Access | Value | Description |
|---|---|---|---|---|---|---|
| 1B | LO_CHAIN | 7 | ckdiv2_reset | RW | | force reset of phase shifter div2 (used to synchronize Generator and Daisy) |
| | | | | | 0 | div2 running |
| | | | | | 1 | div2 output frozen |
| | | 6 | ckdiv2_start | RW | | allow clock to IQ div2. Used to synchronize Generator and Daisy |
| | | | | | 0 | no clock to IQ div2 |
| | | | | | 1 | clock to IQ div2 allowed |
| | | 5 | ckdiv2_invert | RW | | phase selection of clock to IQ div2 (0°/180°). Used to synchronize Generator and Daisy. |
| | | | | | 0 | clock phase = 0° |
| | | | | | 1 | clock phase = 180° |
| | | 4 | PLL_Div2_Highfreq | RW | | PLL Div 2 HIGH frequency biasing current |
| | | | | | 0 | biasing to be used for ISM bands 433 MHz and 915 MHz |
| | | | | | 1 | biasing to be used for ISM band 2450 MHz |
| | | 3 to 0 | LoChain_ratio[3:0] | RW | | Lo divider ratio |
| | | | | | 0 | 2 used for ISM band 2450 MHz |
| | | | | | 1 | do not use |
| | | | | | 2 | 4 used for ISM band 915 MHz |
| | | | | | 3 | do not use |
| | | | | | 4 | do not use |
| | | | | | 5 | do not use |
| | | | | | 6 | do not use |
| | | | | | 7 | do not use |
| | | | | | 8 | 8 used for ISM band 433 MHz |
| | | | | | 9 | do not use |
| | | | | | 10 | do not use |
| | | | | | 11 | do not use |
| | | | | | 12 | do not use |
| | | | | | 13 | do not use |
| | | | | | 14 | do not use |
| | | | | | 15 | daisy in |

**Table 26. SD_1 bit descriptions**

| Address | Register | Bit | Symbol | Access | Value | Description |
|---|---|---|---|---|---|---|
| 1C | SD_1 | 6 to 0 | LO_Int[7:0] | RW | [0:255] | PLL integer part N |


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**Table 27. SD_2 bit descriptions**

| Address | Register | Bit | Symbol | Access | Value | Description |
|---|---|---|---|---|---|---|
| 1D | SD_2 | 7 to 0 | LO_Frac_2[7:0] | RW | [0:127] | PLL ΣΔ modulator byte 2 corresponds to K[15:8] |

**Table 28. SD_3 bit descriptions**

| Address | Register | Bit | Symbol | Access | Value | Description |
|---|---|---|---|---|---|---|
| 1E | SD_3 | 7 to 0 | LO_Frac_1[7:0] | RW | [0:255] | PLL ΣΔ modulator byte 1 corresponds to K[22:9] |

**Table 29. CP bit descriptions**

| Address | Register | Bit | Symbol | Access | Value | Description |
|---|---|---|---|---|---|---|
| 1F | CP | 6 | ICP_Force_Sink | RW | | enable/disable charge-pump forced sinking current |
| | | | | | 0 | no action |
| | | | | | 1 | charge pump forced to sink current |
| | | 5 | ICP_Force_Src | RW | | enable/disable charge-pump forced sourcing current |
| | | | | | 0 | no action |
| | | | | | 1 | charge pump forced to source current |
| | | 4 | cpleak0 | RW | | charge-pump offset current ON/OFF |
| | | | | | 0 | charge-pump offset current enabled |
| | | | | | 1 | charge-pump offset current disabled |
| | | 3 | cpleak05 | RW | | proportional CP offset current |
| | | | | | 0 | 10 % offset current |
| | | | | | 1 | 5 % offset current |

**Table 30. VCO bit descriptions**

| Address | Register | Bit | Symbol | Access | Value | Description |
|---|---|---|---|---|---|---|
| 21 | VCO | 1 to 0 | VCO_Select[1:0] | RW | | VCO selection |
| | | | | | 0 | all OFF |
| | | | | | 1 | forbidden |
| | | | | | 2 | VCO MID |
| | | | | | 3 | VCO HIGH |

**Table 31. RESERVED_0 bit descriptions**

| Address | Register | Bit | Symbol | Access | Value | Description |
|---|---|---|---|---|---|---|
| 3E | RESERVED_0 | 4 to 0 | reserved_0[4:0] | RW | - | POR bit control |

**Table 32. RESERVED_1 bit descriptions**

| Address | Register | Bit | Symbol | Access | Value | Description |
|---|---|---|---|---|---|---|
| 3E | RESERVED_1 | 4 to 0 | reserved_1[1:0] | RW | - | page selection; default page = 0; page 1 used only for debug |


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# 10. Limiting values

**Table 33. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | supply voltage | | –0.3 | +3.6 | V |
| $V_I$ | input voltage | $V_{CC}$ < 3.3 V | –0.3 | $V_{CC}$ + 0.3 | V |
| | | $V_{CC}$ > 3.3 V | –0.3 | +3.6 | V |
| $T_{stg}$ | storage temperature | | –40 | +150 | °C |
| $T_j$ | junction temperature | | - | 105 | °C |
| $T_{amb}$ | ambient temperature | | –20 | +85[1] | °C |
| $V_{ESD}$ | electrostatic discharge voltage | EIA/JESD22-A114 (HBM) | –2 | +2 | kV |
| | | EIA/JESD22-C101-C (FCDM) class III[2] | 500 | - | V |

[1] The maximum allowed ambient temperature $T_{amb(max)}$ depends on the assembly conditions of the package and especially on the design of the Printed-Circuit Board (PCB) and die connection. The application mounting must be done in such a way that the maximum junction temperature is never exceeded. The junction temperature can be obtained by reading the temperature sensor bit via SPI-bus. The junction temperature: $T_j = T_{amb} + \Delta T_{j-c}$. where $\Delta T_{j-c}$ = power × $R_{th}$.

[2] Class III: > 500 V to 1000 V.

# 11. Thermal characteristics

**Table 34. Thermal characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | | - | - | 32.6 | K/W |

# 12. Characteristics

**Table 35. General characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ | supply voltage | | 3.13 | 3.30 | 3.47 | V |
| $I_{CC}$ | supply current | at 27 dBm output power; daisy chaining output buffer ON | - | 450 | - | mA |
| | | with power amplifier OFF; $V_{SWITCH}$ = 0 V | - | 120 | - | mA |
| | | in Standby mode | - | 2.5 | - | mA |

**Table 36. Characteristics**

*$T_{amb}$ = 25 °C; $V_{dd}$ = 3.3 V; for ISM bands: 433 MHz, 915 MHz and 2450 MHz; unless otherwise specified.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Digital levels (SPI-bus)** | | | | | | |
| $f_{SPI_CLK(SCLK)}$ | SPI_CLK frequency on pin SCLK | | - | - | 20 | MHz |
| $V_{IL}$ | LOW-level input voltage | | - | - | 0.3$V_{CC}$ | V |
| $V_{IH}$ | HIGH-level input voltage | | 0.7$V_{CC}$ | - | - | V |


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**Table 36. Characteristics** *...continued*

*$T_{amb}$ = 25 °C; $V_{dd}$ = 3.3 V; for ISM bands: 433 MHz, 915 MHz and 2450 MHz; unless otherwise specified.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{OL}$ | LOW-level output voltage | | - | - | $0.3V_{CC}$ | V |
| $V_{OH}$ | HIGH-level output voltage | | $0.7V_{CC}$ | - | - | V |
| **PLL** | | | | | | |
| $f_{step}$ | step frequency | | 10 | - | - | kHz |
| $f_{clk(ref)}$ | reference clock frequency | external reference clock | - | 16 | - | MHz |
| $V_{clk(ref)}$ | reference clock voltage | external reference clock | $0.7V_{CC}$ | - | $V_{CC}$ | V |

**Table 37. Characteristics**

*$T_{amb}$ = 25 °C; $V_{dd}$ = 3.3 V; for ISM bands: 2450 MHz; unless otherwise specified.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **PLL** | | | | | | |
| $f_{range}$ | frequency range | | 2400 | - | 2483.5 | MHz |
| $t_{set}$ | setting time | | - | - | 50 | µs |
| $t_{s(f)}$ | frequency settling time | from one frequency to another | - | 5 | 10 | µs |
| $\varphi_n$ | phase noise | at 2483.5 MHz; at 100 kHz frequency offset | - | –87 | - | dBc/Hz |
| **Phase shifter** | | | | | | |
| $\Delta\varphi_{step}$ | phase shift step | | - | 1.4 | - | ° |
| $\varphi_{RF}$ | RF phase | [1] | 0 | - | 360 | ° |
| $E\varphi$ | phase error | absolute value step size error | 0 | 0.5 | 1 | ° |
| | | cumulative phase error [2] | - | 5 | - | ° |
| **MPA** | | | | | | |
| $P_{o(max)}$ | maximum output power | | - | 24 | 27 | dBm |
| $\alpha_{sp(ob)}$ | out-band spurious attenuation | consider second and third harmonics only | - | –30 | - | dBc |
| $P_{ob}$ | out-band power | integrated power outside the band of interest; $f_{VCO(max)} = f_{range}$ max – 1 MHz; $f_{VCO(min)} = f_{range}$ min + 1 MHz; rf_mpa_power[5:0] = 42 | - | –45 | - | dBc |
| $P_{o(range)}$ | output power range | | - | 20 | - | dB |
| $\alpha_{isol}$ | isolation | ON/OFF switch isolation | - | 40 | - | dB |
| $t_{sw}$ | switching time | OFF/ON ramping transition [3] | - | 700 | - | ns |
| $Z_o$ | output impedance | | - | 40 | - | Ω |
| **PPA** | | | | | | |
| $P_{o(max)}$ | maximum output power | rf_mpa_power[5:0] = 63 | - | 7 | - | dBm |
| $P_o$ | output power | rf_mpa_power[5:0] = 42 | - | 5 | - | dBm |
| $P_{o(range)}$ | output power range | | - | 30 | - | dB |
| $Z_o$ | output impedance | | - | 200 | - | Ω |

[1] Phase range = 360° (maximum phase $\varphi_{RF}$ = 360° minus minimum phase $\varphi_{RF}$ = 0°).

[2] See Figure 10.

[3] See Figure 11.


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**Table 38. Characteristics**

*$T_{amb}$ = 25 °C; $V_{dd}$ = 3.3 V; for ISM bands: 915 MHz; unless otherwise specified.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **PLL** | | | | | | |
| $f_{range}$ | frequency range | | 902 | - | 928 | MHz |
| $t_{set}$ | setting time | | - | - | 50 | µs |
| $t_{s(f)}$ | frequency settling time | from one frequency to another | - | 5 | 10 | µs |
| **Phase shifter** | | | | | | |
| $\Delta\varphi_{step}$ | phase shift step | | - | 1.4 | - | ° |
| $\varphi_{RF}$ | RF phase | [1] | 0 | - | 360 | ° |
| $E\varphi$ | phase error | absolute value step size error | 0 | 0.5 | 1 | ° |
| | | cumulative phase error [2] | - | 5 | - | ° |
| **MPA** | | | | | | |
| $P_{o(max)}$ | maximum output power | | - | 24 | 27 | dBm |
| $P_{o(range)}$ | output power range | | - | 20 | - | dB |
| $\alpha_{isol}$ | isolation | ON/OFF switch isolation | - | 40 | - | dB |
| $t_{sw}$ | switching time | OFF/ON ramping transition [3] | - | 700 | - | ns |
| $Z_o$ | output impedance | | - | 40 | - | Ω |
| **PPA** | | | | | | |
| $P_{o(max)}$ | maximum output power | rf_mpa_power[5:0] = 63 | - | 7 | - | dBm |
| $P_o$ | output power | rf_mpa_power[5:0] = 42 | - | 5 | - | dBm |
| $P_{o(range)}$ | output power range | | - | 30 | - | dB |
| $Z_o$ | output impedance | | - | 200 | - | Ω |

[1] Phase range = 360° (maximum phase $\varphi_{RF}$ = 360° minus minimum phase $\varphi_{RF}$ = 0°).

[2] See Figure 10.

[3] See Figure 11.

**Table 39. Characteristics**

*$T_{amb}$ = 25 °C; $V_{dd}$ = 3.3 V; for ISM bands: 433 MHz; unless otherwise specified.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **PLL** | | | | | | |
| $f_{range}$ | frequency range | | 433.0 | - | 434.8 | MHz |
| $t_{set}$ | setting time | | - | - | 50 | µs |
| $t_{s(f)}$ | frequency settling time | from one frequency to another | - | 5 | 10 | µs |
| **MPA** | | | | | | |
| $P_{o(max)}$ | maximum output power | | - | 24 | 27 | dBm |
| $P_{o(range)}$ | output power range | | - | 20 | - | dB |
| $\alpha_{isol}$ | isolation | ON/OFF switch isolation | - | 40 | - | dB |
| $t_{sw}$ | switching time | OFF/ON ramping transition [1] | - | 700 | - | ns |


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**Table 39. Characteristics** *…continued*

*$T_{amb}$ = 25 °C; $V_{dd}$ = 3.3 V; for ISM bands: 433 MHz; unless otherwise specified.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $Z_o$ | output impedance | | - | 40 | - | Ω |
| **PPA** | | | | | | |
| $P_{o(max)}$ | maximum output power | rf_mpa_power[5:0] = 63 | - | 7 | - | dBm |
| $P_o$ | output power | rf_mpa_power[5:0] = 42 | - | 5 | - | dBm |
| $P_{o(range)}$ | output power range | | - | 30 | - | dB |
| $Z_o$ | output impedance | | - | 200 | - | Ω |

[1] See Figure 11.

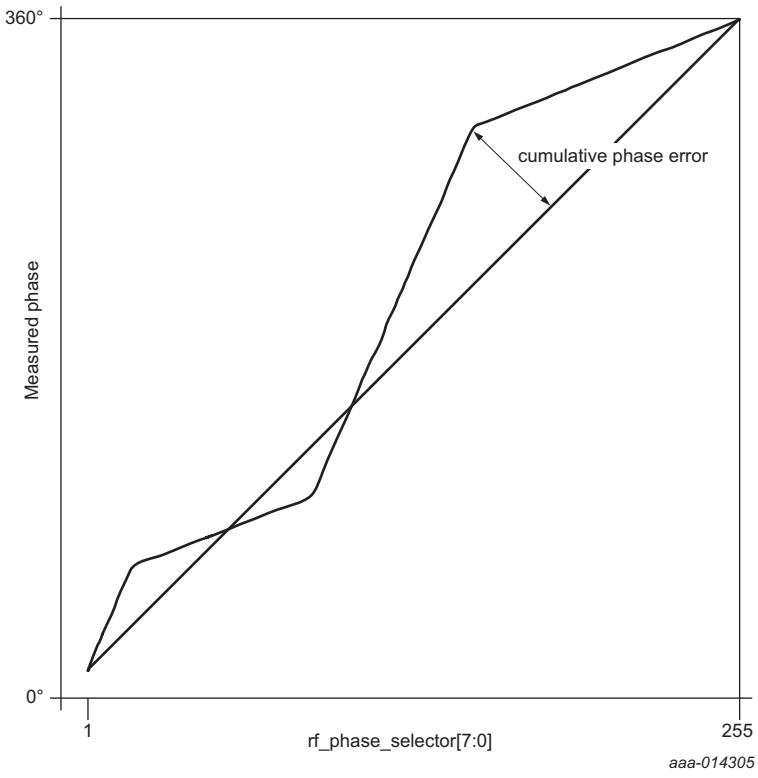


**Fig 10. Phase error definition**


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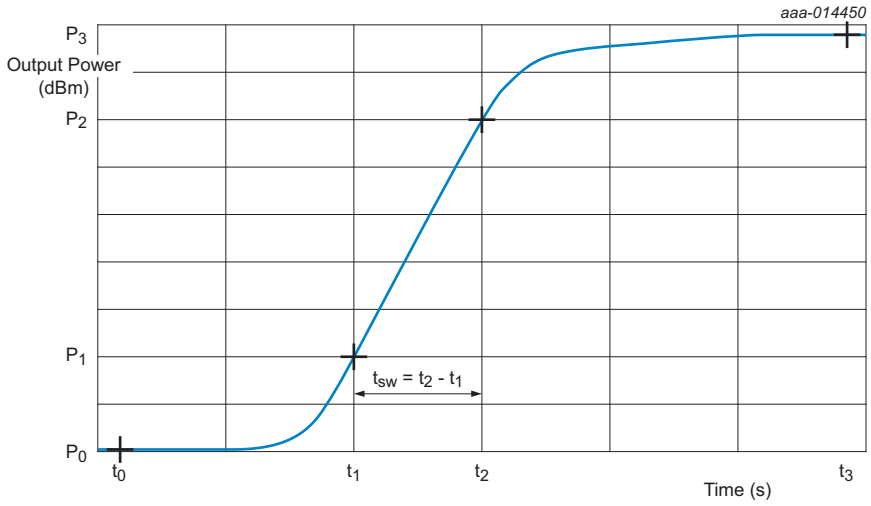


$t_0$ = MPA off, steady state.

$t_1$ = When MPA output power crosses $P_1$.

$t_2$ = When MPA output power crosses $P_2$.

$t_3$ = MPA on, steady state.

$P_0$ = MPA off, steady state.

$P_1 = P_3 - 11$ dB.

$P_2 = P_3 - 1$ dB.

$P_3$ = MPA on, steady state.

**Fig 11. MPA power on settling**


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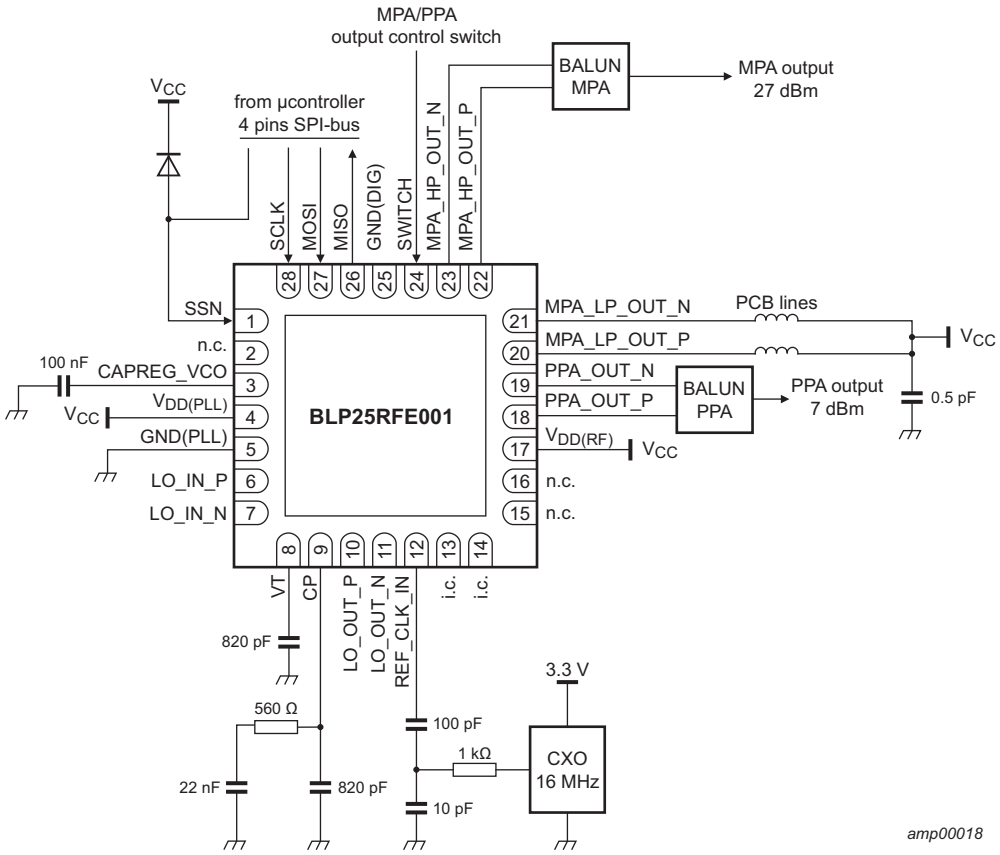
# 13. Application information

## 13.1 Application




**Remark:** decoupling capacitors are not depicted

**Fig 12. Application**

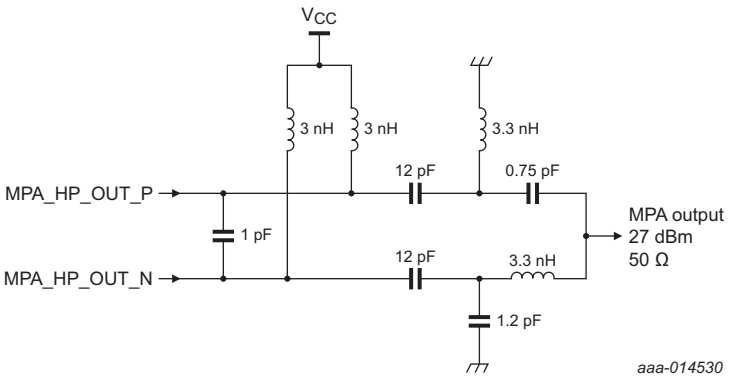



**Fig 13. Balun MPA 2.4 GHz ISM band**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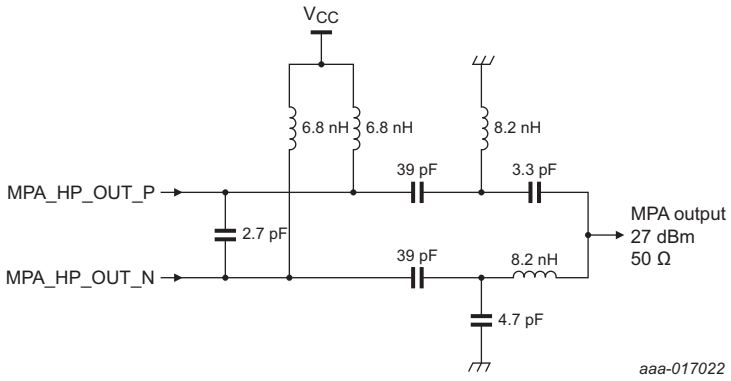


**Fig 14. Balun MPA 915 MHz ISM band**

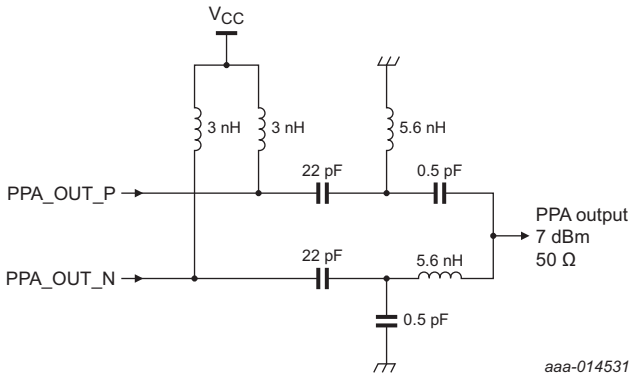


**Fig 15. Balun PPA 2.4 GHz ISM band**

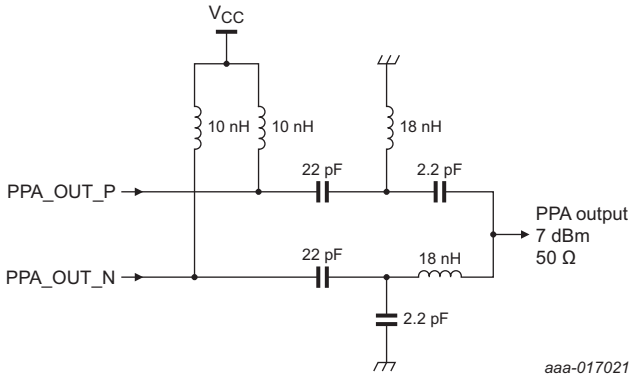


**Fig 16. Balun PPA 915 MHz ISM band**


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## 13.2 Typical cooking application

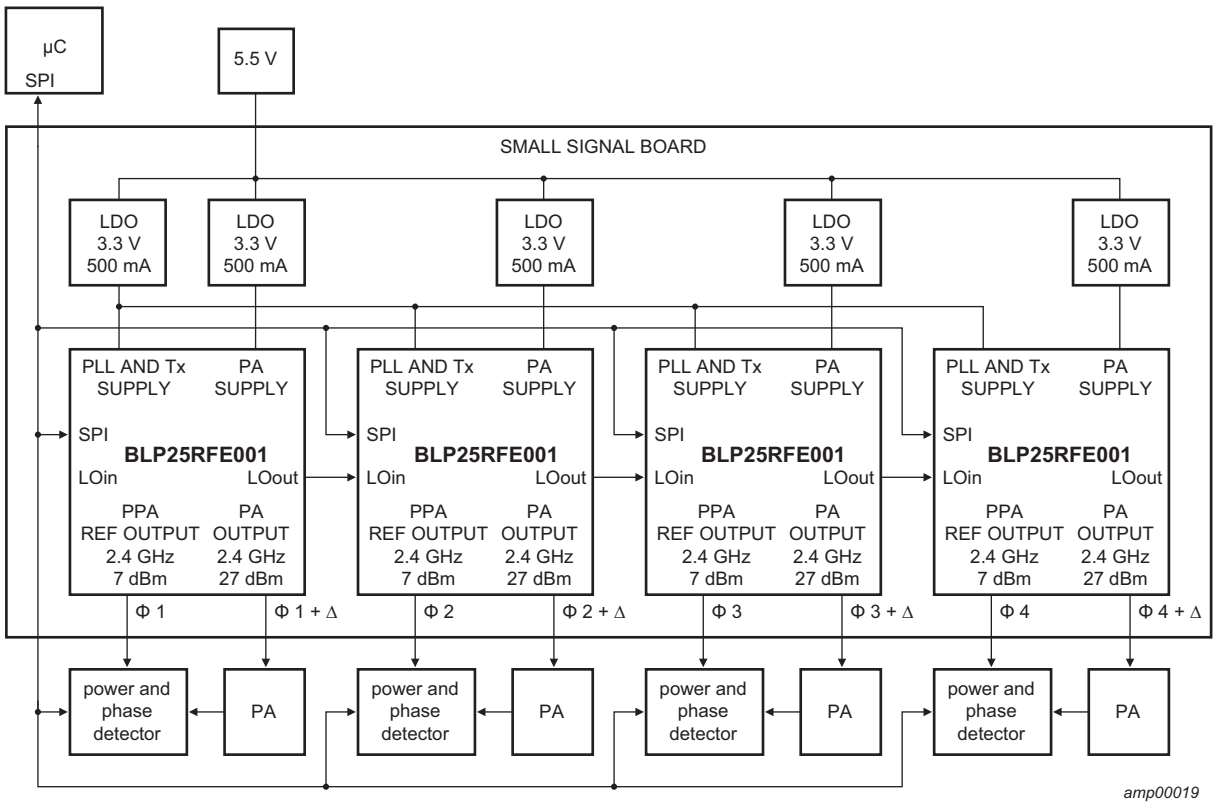


**Fig 17. Typical cooking application**


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## 13.3 Typical lighting application

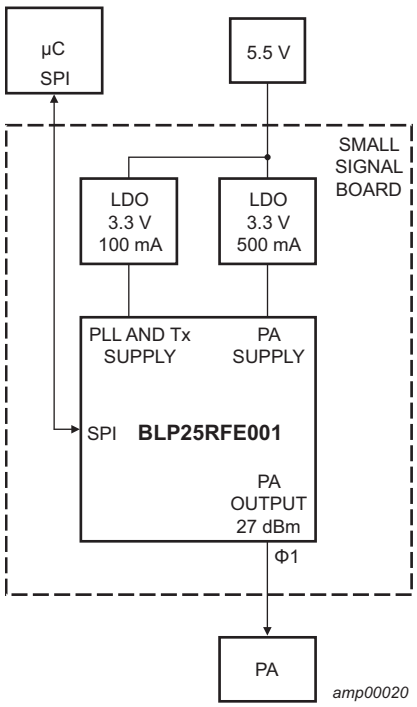


**Fig 18. Typical lighting application**


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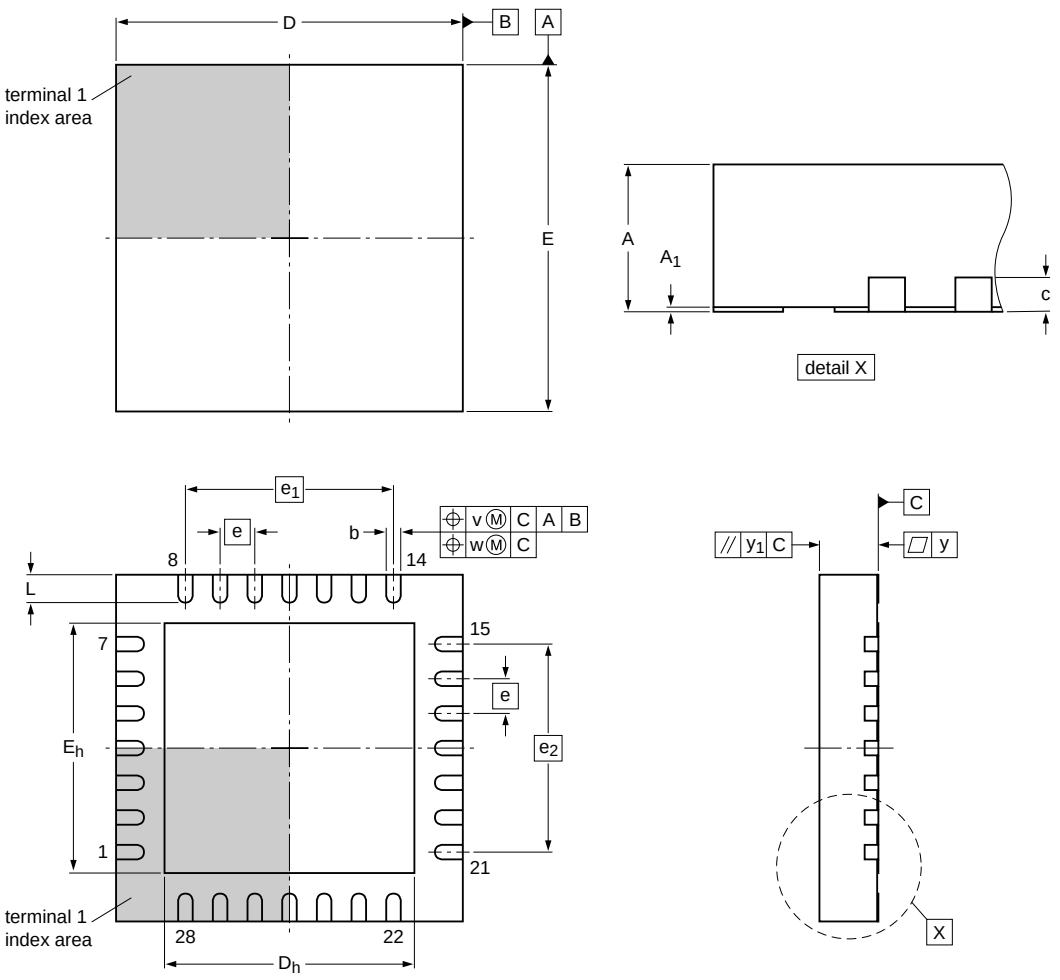
# 14. Package outline

**HVQFN28: plastic thermal enhanced very thin quad flat package; no leads; 28 terminals; body 5 x 5 x 0.85 mm** **SOT993-3**




Dimensions

| Unit(1) | | A | $A_1$ | b | c | D | $D_h$ | E | $E_h$ | e | $e_1$ | $e_2$ | L | v | w | y | $y_1$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | max | 1.00 | 0.05 | 0.30 | | 5.1 | 3.7 | 5.1 | 3.7 | | | | 0.5 | | | | |
| mm | nom | 0.85 | 0.02 | 0.21 | 0.2 | 5.0 | 3.6 | 5.0 | 3.6 | 0.5 | 3 | 3 | 0.4 | 0.1 | 0.05 | 0.05 | 0.1 |
| | min | 0.80 | 0.00 | 0.18 | | 4.9 | 3.5 | 4.9 | 3.5 | | | | 0.3 | | | | |

Note
1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

*sot993-3_po*

| Outline version | References | | | | European projection | Issue date |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT993-3 | | MO-220 | - - - | | | ~~10-01-14~~ 10-03-02 |

**Fig 19. Package outline SOT993-3 (HVQFN28)**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# 15. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

## 15.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

## 15.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

## 15.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities


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## 15.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 20) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 40 and 41

**Table 40. SnPb eutectic process (from J-STD-020D)**

| Package thickness (mm) | Package reflow temperature (°C) | |
|---|---|---|
| | Volume ($mm^3$) | |
| | < 350 | ≥ 350 |
| < 2.5 | 235 | 220 |
| ≥ 2.5 | 220 | 220 |

**Table 41. Lead-free process (from J-STD-020D)**

| Package thickness (mm) | Package reflow temperature (°C) | | |
|---|---|---|---|
| | Volume ($mm^3$) | | |
| | < 350 | 350 to 2000 | > 2000 |
| < 1.6 | 260 | 260 | 260 |
| 1.6 to 2.5 | 260 | 250 | 245 |
| > 2.5 | 250 | 245 | 245 |

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 20.


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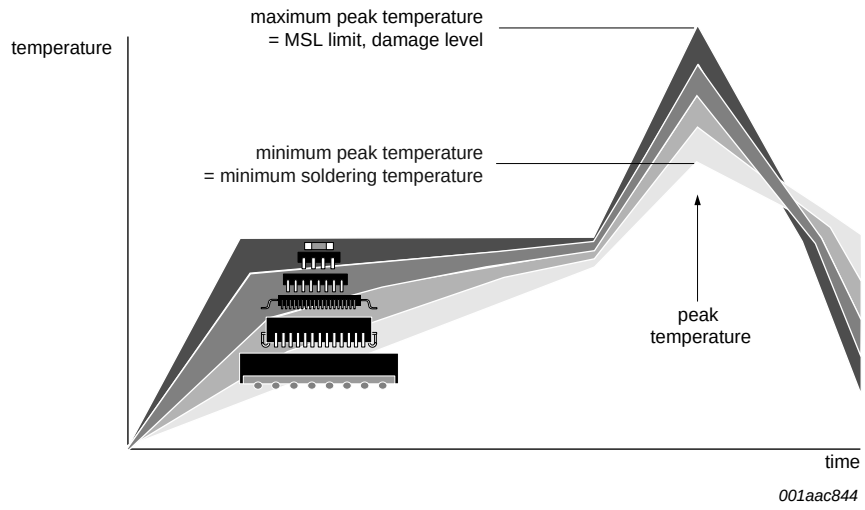


MSL: Moisture Sensitivity Level

**Fig 20. Temperature profiles for large and small components**

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

## 16. Abbreviations

**Table 42. Abbreviations**

| Acronym | Description |
|---|---|
| BOM | Bill Of Material |
| FCDM | Field-induced Charge Device Model |
| IC | Integrated Circuit |
| ISM | Industrial Scientific Medical |
| LC-VCO | Inductors and Capacitors - Voltage Controlled Oscillator |
| LO | Local Oscillator |
| LSB | Least Significant Bit |
| MainDiv | Main Divider |
| MPA | Medium Power Amplifier |
| MSB | Most Significant Bit |
| MSL | Moisture Sensibility Level |
| PA | Power Amplifier |
| PCB | Printed-Circuit Board |
| PFD | Phase Frequency Detector |
| PLL | Phase-Locked Loop |
| PPA | Pre-Power Amplifier |
| PWM | Pulse Width Modulation |
| RoHS | Restriction of Hazardous Substances |


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# 17. Revision history

**Table 43. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| BLP25RFE001 v.2 | 20180126 | Product data sheet | - | BLP25RFE001 v.1.0 |
| Modifications: | • Section 2 on page 1: changed text of list item 8<br>• Section 8 on page 5: changed text of paragraph 7<br>• Section 8.1 on page 5: changed text of third sentence<br>• Table 37 on page 22: changed values of maximum output power MPA<br>• Table 38 on page 23: changed values of maximum output power MPA<br>• Table 39 on page 23: changed values of maximum output power MPA | | | |
| BLP25RFE001 v.1.0 | 20180109 | Product data sheet | - | - |


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## 18.1 Data sheet status

| Document status[1][2] | Product status[3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.ampleon.com.

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