

Datasheet

BL54H20 Series

Version 1.0

Revision History

Version	Date	Notes	Contributor(s)	Approver
0.1	02 Oct 2024	Initial PRELIMINARY release.	Raj Khatri	Jonathan Kaye
0.2	16 Oct 2024	Added External Antenna Integration with BL54H20 RF trace pin variant (453-00198)	Raj Khatri	Jonathan Kaye
0.3	25 Oct 2024	Added Ignion NN02-101 chip antenna part number into section PCB Layout on Host PCB for the 453-0019x	Raj Khatri	Jonathan Kaye
0.4	22 Nov 2024	Add Chip Antenna Performance Modify Maximum Transmit Power Setting in Specification Summary to 7dBm	Louis Chang	Jonathan Kaye
0.5	5 Dec 2024	Modify some incorrect comment in 3.2 Pin Definition Add partial sensitivity value	Louis Chang	
1.0	5 Dec 2024	Initial release.	Dave Drogowski	Jonathan Kaye

Contents

1	Overview and Key Features	5
1.1	Features and Benefits	5
1.2	Application Areas	5
2	Specification	6
2.1	Specification Summary	6
3	Hardware Specifications	10
3.1	Block Diagram and Pin-out	10
3.2	Pin Definitions	11
3.3	Electrical Specifications	14
3.3.1	Absolute Maximum Ratings	14
3.3.2	Recommended Operating Parameters	16
3.4	Clocks	16
3.4.1	HFXO - 32MHz crystal oscillator and nRF54H20 internal load capacitor TBDpF mandatory setting	16
3.4.2	LFCLK - Low Frequency clock source	16
3.4.3	Other Internal Clocks	17
3.5	BL54H20 Power Supply Options	18
3.5.1	High Voltage mode (option1) or Normal Voltage mode (option2)	18
3.5.2	VBUS pin and 10uF Mandatory Capacitor	20
4	Programmability	21
4.1	BL54H20 Default Firmware	21
4.2	BL54H20 Firmware Options	21
5	Mandatory SW requirements related to hardware	22
5.1	32MHz crystal internal load capacitor setting of TBD pF	22
6	Hardware Integration Suggestions	23
6.1	Circuit	23
6.2	PCB Layout on Host PCB - General	24
6.3	PCB Layout on Host PCB for the 453-0019x	25
6.3.1	Antenna Keep-out on Host PCB	25
6.3.2	Antenna Keep-out and Proximity to Metal or Plastic	25
6.4	External Antenna Integration with BL54H20 RF trace pin variant (453-00198)	26
7	Mechanical Details	27
7.1	BL54H20 Mechanical Details	27
7.2	Host PCB Land Pattern and Antenna Keep-out for the 453-00197	28
8	Chip Antenna Performance	29
8.1	Summary of Antenna Performance	29
8.2	2.4GHz Radiated Performance	29
8.3	Antenna S11 measuring data	30
9	Ordering Information	31

10 Additional Information 32

1 Overview and Key Features



The newest entry in our Nordic Semiconductor based Bluetooth LE portfolio is by far the most advanced, most secure, and highest performing multi core MCU architecture wireless solution available anywhere.

The BL54H20 series of robust, tiny modules feature the **Nordic nRF54H20 SoC**. It directly targets the highest-performance processing capabilities with double the application processing (vs. prior BL5340). **2x Cortex-M33 AND 2x RISC-V coprocessors** each are optimized for particular workloads. We've also scaled up memory to 2MB non-volatile and 1MB RAM.

Featuring BT 5.4, capabilities include support for Bluetooth LE, LE Audio, Bluetooth Mesh, and 802.15.4 protocols including Thread and Matter. It's further enhanced with state-of-the-art security, designed for PSA Certified level 3, and supports Secure Boot, Secure Firmware Update, Secure Storage, and integrated tamper sensors for physical security.

The BL54H20 series brings out all nRF54H20 hardware features and capabilities including high speed **USB access**, **CAN FD** controller, 2 x **I3C** and **14bit ADC**, up to +10 dBm transmit power, from **1.9V to 5.5V** supply considerations, and a true industrial operating range of **-40 to 105°C**.

Complete regulatory certifications enable faster time to market and reduced development risk, simplifying your next wireless design.

Note: BL54H20 hardware provides all functionality of the nRF54H20 chipset used in the module design. This is a hardware datasheet only – it does not cover the software aspects of the BL54H20. This is to acknowledge that information in this datasheet is referenced from the nRF54H20 datasheet.

1.1 Features and Benefits

- **Nordic nRF54H20** – 4.7x4.3 mm WSLCP with 64 GPIOs available.
- **Multi-protocol support:** Bluetooth 5.4 LE, 802.15.4 (Thread/Matter)
- Bluetooth LE: Peripheral/Central, 2 Mbps (high throughput), LE Coded (long range), AoA/AoD, LE Audio/Isochronous Channels, Mesh
- **Dual Cortex M33 processor cores:** Application processor (up to 320MHz Cortex M33), Radio processor (256MHz Cortex M33)
- Dual RISC-V co-processor cores: 320 MHz VPR, 16 MHz VPR
- **Memory:** 2MB non-volatile memory, 768 KB RAM, and External interfaces – XIP, QSPI, xSPI, HyperBus
- Extended Industrial Temperature Rating (-40° to +105°C)
- **Small form factor:** 13.5 x 10 x 1.8 mm
- **Most configurable interfaces:** - NFC A-Tag, USB, CAN FD, I3C, UART, QSPI, SPI, High Speed SPI, SMIF, I2S, I2C, PDM, PWM, ADC, GPIO, QDEC, Comparator, Low Power Comparator
- **Additional SoC Hardware Features** like RNG, WDT, temperature sensor, floating point unit, inter-processor communication, debug trace, NFC
- **Antenna choice** –external antenna support via MHF4 connector OR integrated pre-certified Chip antenna - **Ignion NANO NN02**
- **Development choice:** Zephyr RTOS, Nordic nRF Connect SDK, Canvas Software Suite
- Firmware Over the Air (FOTA) via MCUboot and Zephyr
- Hostless operation – Multi Core MCU reduces BOM
- Fully featured development kits to jump start Bluetooth LE development

1.2 Application Areas

- Smart Building
- Asset Tracking
- Secure Medical Peripherals
- Industrial Automation

2 Specification

2.1 Specification Summary

Categories/Feature	Implementation						
Wireless Specification							
Bluetooth®	Bluetooth 5.4 – Single mode <ul style="list-style-type: none"> • GATT client/server – Any adopted/custom services • Central/Peripheral roles • Bluetooth LE mesh • 2M PHY • LE Coded PHY • LE Audio w/ Isochronous streams • AoA / AoD • LE Advertising Extensions • LE secure connections • Data packet length extensions • LE privacy v1.2 • DTM Firmware (Test Modes) 						
IEEE 802.15.4-2006 PHY	2405–2480 MHz IEEE 802.15.5-2006 radio transceiver, implementing IEEE 802.15.5-2006 compliant <ul style="list-style-type: none"> • 250kbps,2450MHz, O-QPSK PHY • Channels 11-26. Channel 11 2405MHz and CH26 2480MHz. • Clear channel assessment (CCA) • Energy detection (ED) scan • CRC generation 						
Nordic proprietary 1Mbps and 2Mbps modes radio (<i>not currently certified by Ezurio</i>)	2402–2480 MHz Nordic proprietary 1Mbps and 2Mbps modes radio transceiver <ul style="list-style-type: none"> • 1Mbps nRF proprietary mode (ideal transmitter) • 2Mbps nRF proprietary mode (ideal transmitter) • 4Mbps nRF proprietary mode (ideal transmitter) 						
Frequency	2.402 - 2.480 GHz for BLE (CH0 to CH39) 2.405 - 2.480 GHz for IEEE 802.15.4-2006 PHY (CH11 to CH26)						
Raw Data Rates	1 Mbps BLE (over-the-air) 2 Mbps BLE (over-the-air) 125 kbps BLE (over-the-air) 500 kbps BLE (over-the-air) 250 kbps IEEE 802.15.4 802.15.4-2006 (over-the-air) Nordic proprietary 1Mbps, 2Mbps and 4Mbps modes (over-the-air)						
Maximum Transmit Power Setting	<table border="1"> <tr> <td>+7 dBm</td> <td>Conducted 453-000197 (Integrated antenna), (Exclude antenna gain)</td> </tr> <tr> <td>+7 dBm</td> <td>Conducted 453-000198 (External antenna), (Test at MHF4 connector)</td> </tr> </table>	+7 dBm	Conducted 453-000197 (Integrated antenna), (Exclude antenna gain)	+7 dBm	Conducted 453-000198 (External antenna), (Test at MHF4 connector)		
+7 dBm	Conducted 453-000197 (Integrated antenna), (Exclude antenna gain)						
+7 dBm	Conducted 453-000198 (External antenna), (Test at MHF4 connector)						
Minimum Transmit Power Setting	TBD						
Receive Sensitivity (≤ 37 byte packet for BLE) ¹	<table border="1"> <tr> <td>BLE 1 Mbps (BER=1E-3)</td> <td>-97 dBm typical</td> </tr> <tr> <td>BLE 2 Mbps</td> <td>-94 dBm typical</td> </tr> <tr> <td>BLE 125 kbps</td> <td>-105 dBm typical</td> </tr> </table>	BLE 1 Mbps (BER=1E-3)	-97 dBm typical	BLE 2 Mbps	-94 dBm typical	BLE 125 kbps	-105 dBm typical
BLE 1 Mbps (BER=1E-3)	-97 dBm typical						
BLE 2 Mbps	-94 dBm typical						
BLE 125 kbps	-105 dBm typical						

Note¹ Known Noise on channels 2432MHz and 2464MHz degrades receiver sensitivity, in which sensitivity are not within the typical value

	BLE 500 kbps	-100 dBm typical
	IEEE 802.15.4-2006 250kbps	-TBD dBm typical
Link Budget (conducted)	TBD dB	@ BLE 1 Mbps
	TBD dB	@ BLE 125 kbps
NFC		
NFC-Tag A Listen mode compliant	Based on NFC forum specification: 13.56 MHz, Data rate 106 kbps, NFC Type2 and Type 4 emulation Modes of Operation: Disable, Sense, Activated Use Cases: Touch-to-Pair with NFC, NFC enabled Out-of-Band Pairing System Wake-On-Field function: Proximity Detection	

Peripherals Domain	Co-processor High Speed Core	Co-processor Low Leakage Core	Application Core	Radio Core	Security Core
Global Domain					
Two co-processors	FLPR "Flipper" Viper Risc-V 320MHz 64KB RAM 2048KB MRAM	PPR "Pepper" Viper Risc-V 16MHz 64KB RAM	Arm Cortex M33 320MHz Max 32KB RAM, DVFS L1 I-cache L1 D-cache TrustZone, FPU, DSP.	Arm Cortex M33 256MHz Max Fast Start-Stop. 192KB RAM L1 I-cache L1 D-cache TrustZone, FPU, DSP	Arm Cortex M33 DVFS. 32kB RAM. Designed for PSA Level 3. Secure boot, secure FW
Total	64 x multifunction I/O lines				
GPIO	14x 1.8V 200MHz GPIO's. 8x 1.8V 100MHz GPIO's.	6x 1.8-3.6V 16MHz GPIO's. 36x 1.2-1.8V 16MHz GPIO's.			
EXMIF (External Memory Interface)	1x EXMIF interface XiP capable, supports SPI, QPSI, xSPI, Hyperbus upto 400MB/s. Max clock 200MHz				
HS-USB 2.0	1x 480Mbps				
I3C	2x I3C (33.4Mbps) Master, slave or Multimaster				
CAN	1x				
Global RTC	1x System Timer 1us resolution 52bits wide				
HS-SPIM	1x (64MHz)				
HS-SPIS	1x (64MHz)				
HS-SPIM-UART	1x				
HS-PWM	1x 8 channel PWM (160MHz)				
PWM	2x runs 320MHz	4x 4 channel PWM (16MHz). 8channel			
Timer	2x runs 320MHz	6x runs 16MHz			
SMIF	1x works with external ISO7816 standard				
I2S, TDM	1x				
PDM	1x				

Peripherals Domain	Co-processor High Speed Core	Co-processor Low Leakage Core	Application Core	Radio Core	Security Core
Global Domain					
Audio PLL		1x Optional clock source for PDM, I2S, TDM audio interfaces. Incoming BLE audio.			
QDEC (Quadrature decoder)		2x			
SPI, I2C, UART		8x			
ADC (200kbps)		1xSAADC on GPIO port P1 or P9. P9 can use voltage division. 3 modes: 10-bit 4MS/s 12-bit 125kS/s 14-bit 31.25kS/s Upto 8channels AIN0-AIN7			
COMP		1 x COMP (comparator)			
LPCOMP		1 x LPCOMP (low power comparator) can wake from System OFF			
NFC A-Tag		1x NFC A-Tag			
External optional 32.768 kHz crystal		Not needed for normal radio operation. Optionally, connect +/-20ppm accuracy crystal for more accurate protocol timing. Fit associated load capacitor for crystal or use nRF54L15 internal load capacitor, which is configurable as TBD pF to TBD pF in TBDpF steps on pins XL1, XL2.			
Security					Designed for PSA Certified Level 3 with Secure Boot, Secure Firmware Update, and Secure Storage. Integrated tamper sensors detect attacks and take action, and cryptographic accelerators are hardened against side-channel attacks.

Programmability	
Programming Options	Nordic nRF Connect SDK: Software/Support available from Nordic directly: https://devzone.nordicsemi.com/ Zephyr RTOS: Software/Support available from Nordic directly: https://www.zephyrproject.org/ Canvas SW Suite: Software/ Support available from https://www.ezurio.com/canvas/software-suite
FW upgrade	Via UART, SWD, or Bluetooth LE – via nRF Connect SDK or Zephyr
Supply Voltage	
Supply Voltage	High Voltage Mode (VDD_HV): 1.9 - 5.5V (Internal DCDC convertor or LDO) Normal Voltage Mode (VDD_VDD_HV): 1.8V

Power Consumption		
Active Modes Peak Current (for maximum Tx power +10 dBm) – Radio only	TBD mA peak Tx (with DCDC)	
Active Modes Peak Current (for Tx power -TBD dBm) – Radio only	TBD mA peak Tx (with DCDC)	
Active Modes Average Current	Depends on many factors (e.g. BLE Advertising interval BLE connection interval etc..)	
Ultra-low Power Modes	System ON Idle	TBD uA (wake on any event)
	System OFF	0.6 uA (with GPIO wake up on 12pins)
Antenna Options		
Internal	Chip antenna – on-board (453-00197 variant)	
External	Connection via <i>on module</i> IPEX MHF4 – 453-00198 variant	
Physical		
Dimensions	13.5mm x 10mm x 1.8mm	
	Pad Pitch – 0.65 mm	
	Pad Type – Three rows of pads (LGA - Land Grid Array).	
Weight	< 1 gram	
Environmental		
Operating	-40 °C to +105 °C	
Storage	-40 °C to +105 °C	
Miscellaneous		
Lead Free	Lead-free and RoHS compliant	
Warranty	One-Year Warranty	
Development Tools		
Development Kit	Development kit per module SKU (453-00197-K1 and 453-00198-K1 respectively)	
Development Tools	Nordic nRF Connect - Android and iOS applications XBit Tools & Utilities	
Bluetooth®	Full Bluetooth SIG Declaration ID	
FCC/ISED/CE/MIC/RCM/UKCA	All BL54H20 Series	

3 Hardware Specifications

3.1 Block Diagram and Pin-out

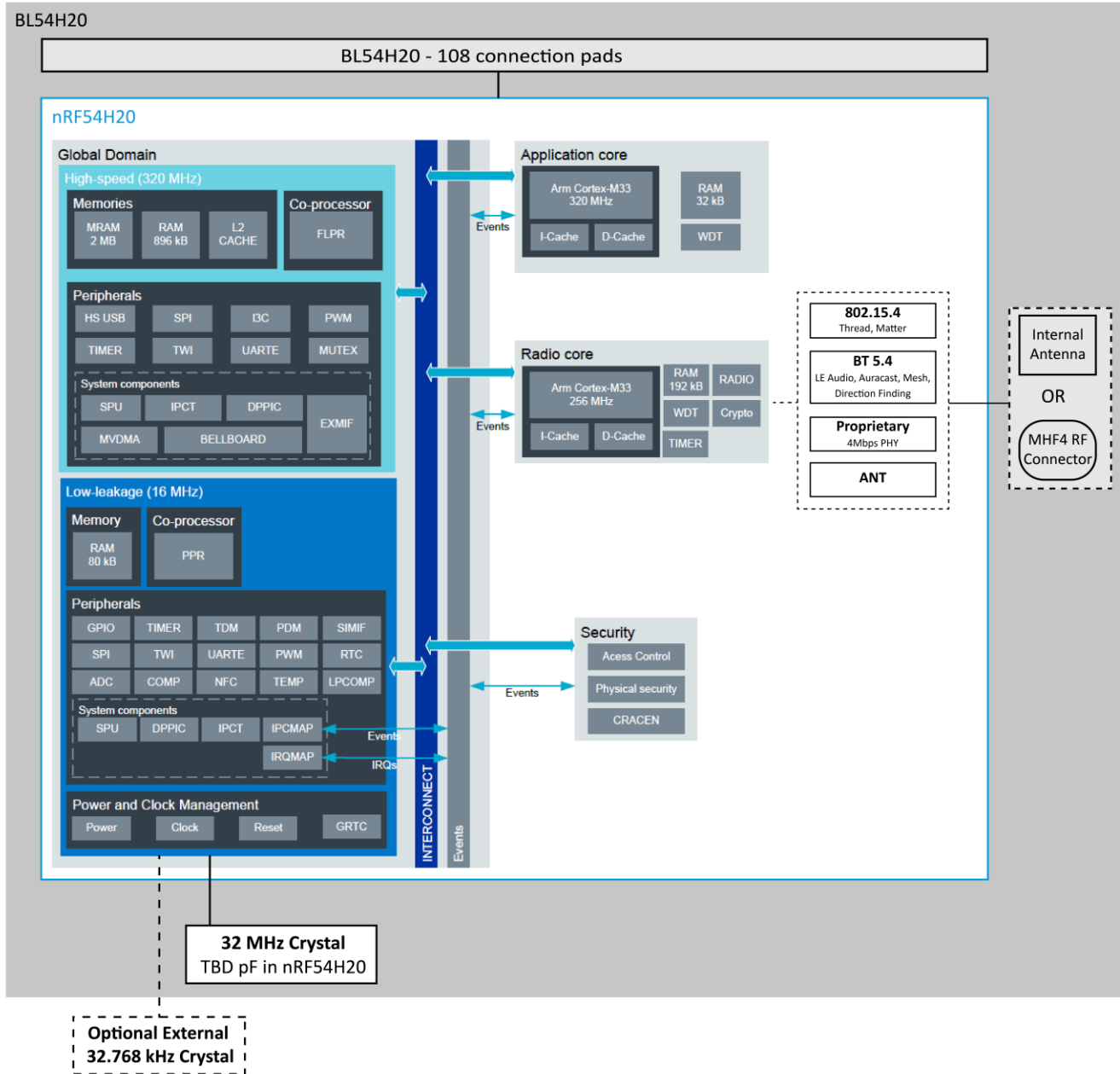


Figure 1: BL54H20 HW block diagram

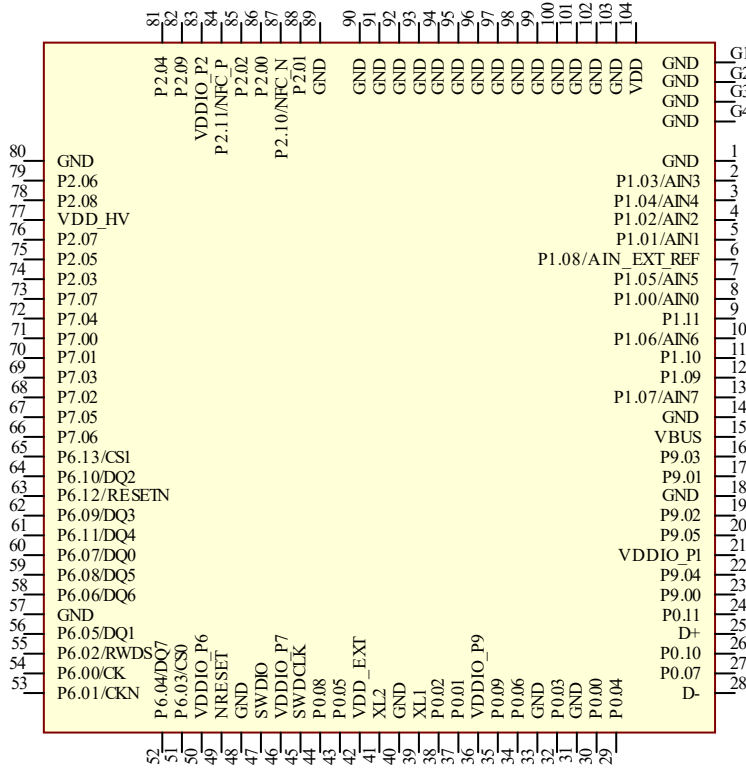


Figure 2: Top view - Schematic symbol for 453-00197 BL54H20 Multi-Core/Protocol -Bluetooth +802.15.4+NFC Module (Nordic nRF54H20) - Integrated Antenna (Ignion chip antenna) or MHF4 RF connector variant 453-00198

3.2 Pin Definitions

Table 1: Pin definitions

Pin #	Pin Name	nRF54H20 WLCSP Pin	nRF54H20 WLCSP Name	Comment	If Not Used
1	GND	-	VSS		
2	P1.03/AIN3	E5	P1.03/AIN3	Ezurio Devkit: MikroE I2C SCL and PMIC I2C SCL	
3	P1.04/AIN4	D5	P1.04/AIN4	Ezurio Devkit: MikroE I2C SDA and PMIC I2C SDA	
4	P1.02/AIN2	E4	P1.02/AIN2		
5	P1.01/AIN1	D4	P1.01/AIN1	Ezurio Devkit: MikroE Reset	
6	P1.08/AIN_EXT_REF	D6	P1.08/AIN_EXT_REF		
7	P1.05/AIN5	C5	P1.05/AIN5		
8	P1.00/AIN0	B4	P1.00/AIN0	Ezurio Devkit: MikroE Analog	
9	P1.11	C6	P1.11	Ezurio Devkit: UART1_TXD (output)	
10	P1.06/AIN6	B5	P1.06/AIN6		
11	P1.10	B6	P1.10	Ezurio Devkit: UART1_RXD (input)	
12	P1.09	A6	P1.09	Ezurio Devkit: UART1_RTS (output)	
13	P1.07/AIN7	A5	P1.07/AIN7	Ezurio Devkit: UART1_CTS (input)	
14	GND		VSS		
15	VBUS	A9	VBUS	VBUS USB supply voltage 4.4V-5.5V. MUST fit 10uF to GND.	
16	P9.03	B10	P9.03	Ezurio Devkit: LED5	
17	P9.01	A10	P9.01	Ezurio Devkit: LED3	
18	GND				

Pin #	Pin Name	nRF54H20 WLCSP Pin	nRF54H20 WLCSP Name	Comment	If Not Used
19	P9.02	B11	P9.02	Ezurio Devkit: LED4	
20	P9.05	C10	P9.05		
21	VDDIO_P1	A4	VDDIO_P1	External supply for GPIO port P1. 1.8V typical (1.62V-1.98V).	
22	P9.04	C11	P9.04	-	
23	P9.00	A11	P9.00	Ezurio Devkit: LED2	
24	P0.11	G9	P0.11	Ezurio Devkit: BUTTON4	
25	D+	B7	D+		
26	P0.10	F9	P0.10	Ezurio Devkit: BUTTON3	
27	P0.07	E9	P0.07	-	
28	D-	B8	D-		
29	P0.04	D8	P0.04	-	
30	P0.00	C9	P0.00	-	
31	GND		VSS		
32	P0.03	D9	P0.03	-	
33	GND		VSS		
34	P0.06	E10	P0.06	-	
35	P0.09	F10	P0.09	Ezurio Devkit: BUTTON2	
36	VDDIO_P9	A12	VDDIO_P9	External supply for 3V GPIO port P9. 3.3V typical (1.62-3.6V).	
37	P0.01	D11	P0.01	-	
38	P0.02	D10	P0.02	-	
39	XL1	B12	XL1	Ezurio Devkit: Optional 32.768kHz crystal pad XL2 and associated 9pF load capacitor inside nRF54H20 chipset	
40	GND		VSS		
41	XL2	C12	XL2	Ezurio Devkit: Optional 32.768kHz crystal pad XL2 and associated 9pF load capacitor inside nRF54H20 chipset	
42	VDD_EXT	D12	VDD_EXT	Power output	
43	P0.05	E11	P0.05	-	
44	P0.08	F11	P0.08	Ezurio Devkit: BUTTON1	
45	SWDCLK	F12	SWDCLK	Serial Wire Debug clock input for debug and programming	
46	VDDIO_P7	J12	VDDIO_P7	External supply for GPIO port P7. 1.8V typical (1.62V-1.98V).	
47	SWDIO	G12	SWDIO	Serial Wire Debug IO for debug and programming	
48	GND		VSS	-	
49	NRESET	H12	NRESET	Pin RESET with internal pull-up resistor (13k Ohms). System Reset (Active Low).	
50	VDDIO_P6	K8, K9, K19, K11	VDDIO_P6	External supply for GPIO port P6. 1.8V typical (1.62V-1.98V).	
51	P6.03/CS0	K12	P6.03/CS0	Recommended usage EXMIF CS0.	
52	P6.04/DQ7	L11	P6.04/DQ7	Recommended usage EXMIF DQ7.	
53	P6.01/CKN	L12	P6.01/CKN		
54	P6.00/CK	M12	P6.00/CK	Recommended usage EXMIF CK.	
55	P6.02/RWDS	M11	P6.02/RWDS	Recommended usage EXMIF DQS.	
56	P6.05/DQ1	M10	P6.05/DQ1	Recommended usage EXMIF DQ1.	
57	GND		VSS		
58	P6.06/DQ6	L10	P6.06/DQ6	Recommended usage EXMIF DQ6.	
59	P6.08/DQ5	L9	P6.08/DQ5	Recommended usage EXMIF DQ5.	

Pin #	Pin Name	nRF54H20 WLCSP Pin	nRF54H20 WLCSP Name	Comment	If Not Used
60	P6.07/DQ0	M9	P6.07/DQ0	Recommended usage EXMIF DQ0.	
61	P6.11/DQ4	M7	P6.11/DQ4	Recommended usage EXMIF DQ4.	
62	P6.09/DQ3	M8	P6.09/DQ3	Recommended usage EXMIF DQ3.	
63	P6.12/RESETN	L7	P6.12/RESETN	Recommended usage EXMIF RESETN.	
64	P6.10/DQ2	L8	P6.10/DQ2	Recommended usage EXMIF DQ2.	
65	P6.13/CS1	K7	P6.13/CS1	.	
66	P7.06	J10	P7.06	Ezurio Devkit: MikroE SPI PWM (default no connection) and TRACE DATA2	
67	P7.05	J11	P7.05	Ezurio Devkit: MikroE SPI PWM (default connection) and TRACE DATA1	
68	P7.02	H11	P7.02	Ezurio Devkit: MikroE SPI CLK	
69	P7.03	H10	P7.03	Ezurio Devkit: TRACE CLK	
70	P7.01	G10	P7.01	Ezurio Devkit: MikroE SPI MOSI	
71	P7.00	G11	P7.00	Ezurio Devkit: MikroE SPI MISO	
72	P7.04	H9	P7.04	Ezurio Devkit: TRACE DATA0 and MikroE SPI CS	
73	P7.07	J9	P7.07	Ezurio Devkit: TRACE DATA3	
74	P2.03	H3	P2.03	Ezurio Devkit: MikroE INT	
75	P2.05	J3	P2.05	Ezurio Devkit: UART0_CTS (input)	
76	P2.07	K3	P2.07	Ezurio Devkit: UART0_RTS (output)	
77	VDD_HV	L1	VDD_HV	Main Supply input 1.9V-5.5V for High Voltage Mode where connect external supply to VDD_HV and pin104(VDD_1V8) becomes an output supply (1.8V). MUST fit 10uF to GND.	
78	P2.08	K2	P2.08	Ezurio Devkit: MikroE UART RX	
79	P2.06	J2	P2.06	Ezurio Devkit: UART0_TXD	
80	GND		VSS		
81	P2.04	H2	P2.04	Ezurio Devkit: UART0_RXD	
82	P2.09	K1	P2.09	Ezurio Devkit: MikroE UART TX	
83	VDDIO_P2	G1	VDDIO_P2	External supply for GPIO port P2. 1.8V typical (1.62V-1.98V).	
84	P2.11/NFC_P	J1	P2.11/NFC_P	For NFC or GPIO	
85	P2.02	G2	P2.02		
86	P2.00	F3	P2.00		
87	P2.10/NFC_N	H1	P2.10/NFC_N	For NFC or GPIO	
88	P2.01	G3	P2.01		
89	GND		VSS	-	
90	GND		VSS	-	
91	GND		VSS	-	
92	GND		VSS	-	
93	GND		VSS	-	
94	GND		VSS	-	
95	GND		VSS	-	
96	GND		VSS	-	
97	GND			Extra GND for chip antenna	
98	GND			Extra GND for chip antenna	
99	GND			Extra GND for chip antenna	
100	GND			Extra GND for chip antenna	
101	GND			Extra GND for chip antenna	

Pin #	Pin Name	nRF54H20 WLCSP Pin	nRF54H20 WLCSP Name	Comment	If Not Used
102	GND			Extra GND for chip antenna	
103	GND			Extra GND for chip antenna	
104	VDD_1V8			For Normal voltage mode connect external supply of 1.8V only to BOTH pin104(VDD_1V8) and pin77(VDD_HV).	
G1	GND			GND for the nRF54H20 GND paddle	
G2	GND			GND for the nRF54H20 GND paddle	
G3	GND			GND for the nRF54H20 GND paddle	
G4	GND			GND for the nRF54H20 GND paddle	

Pin Definition Notes:

Note 1 GPIO	GPIO = General Input or Output (GPIO level voltage tracks VDD pin) . AIN = Analog input. If GPIO is selected as an input, ensure the input is not floating (which can cause current consumption to drive with time in low power modes (such as System ON Idle), by selecting the internal pull up or pull down. Must connect all GND pads to host board PCB GND plane.
Note 2 SPI/TWI/Trace	TBD
Note 3 USB	If using the USB interface, then the BL54H20 VBUS pin (pin15) must be connected to external supply within the range 4.4V to 5.5V and MUST externally fit a 10uF to ground.
Note 4 SWDIO / SWCLK / nRESET / VDD / GND	Customer MUST bring out SWDIO, SWCLK, nRESET, VDD, GND for programming purposes.

GPIO ports information

GPIO ports per port number GOIO pins, pad type and description

Port number	Available pins	Pad type	Description
P0	11:0	1V8 - Slow	Always-on port
P1	11:0	1V8 - Slow	Analog peripherals
P2	11:0	1V8 - Slow	Slow peripherals
P6	13:0	1V8 - Fast	EXMIF and Fast peripherals
P7	7:0	1V8 - Fast	Fast peripherals
P9	5:0	3V3 - Slow	Analog peripherals

3.3 Electrical Specifications

3.3.1 Absolute Maximum Ratings

Absolute maximum ratings are the extreme limits for supply voltage and voltages on digital and analogue pins of the module are listed below; exceeding these values causes permanent damage.

Table 2: Absolute maximum ratings

Parameter	Min	Max	Unit
Supply Voltages			
VDD_HV pin	-0.3	+5.8	V
VDD pin	-0.3	+2	V
VBUS	-0.3	+5.8	V
VDDIO_P1	-0.3	+2	V
VDDIO_P2	-0.3	+2	V
VDDIO_P6	-0.3	+2	V
VDDIO_P7	-0.3	+2	V
VDDIO_P9	-0.3	+3.9	V
Voltage at GND pin	-0.3	0	V
I/O pin voltage			

Parameter	Min	Max	Unit
Voltage at GPIO pin (at VDD≤3.6V)	-0.3	VDD +0.3	V
Voltage at GPIO pin (at VDD≥3.6V)	-0.3	+3.9	V
NFC antenna pin current (NFC1/2)	-	TBD	mA
Radio RF input level	-	TBD	dBm
Environmental			
Storage temperature	-40	+105	°C
MSL (Moisture Sensitivity Level)	-	4	-
ESD (as per EN301-489)			
Conductive		4	kV
Air Coupling		8	kV
Flash Memory (Endurance)	-	TBD	Write/erase cycles
Flash Memory (Retention)	-	TBD	-

Note 1 Wear levelling can be implemented by customer.

3.3.2 Recommended Operating Parameters

Table 3: Power supply operating parameters

Parameter	Min	Typ	Max	Unit
VDD_HV (independent of DCDC) supply range	1.9	3.0	5.5	V
VDD supply voltage		1.8		V
VBUS USB supply range	4.4	5	5.5	V
VDDIO_P1 External supply for GPIO port P1	1.62	1.8	1.98	V
VDDIO_P2 External supply for GPIO port P2	1.62	1.8	1.98	V
VDDIO_P6 External supply for GPIO port P6	1.62	1.8	1.98	V
VDDIO_P7 External supply for GPIO port P7	1.62	1.8	1.98	V
VDDIO_P9 External supply for 3V GPIO port P9	1.62	3.3	3.6	V
VDD Maximum ripple or noise (See Note 1)	-	-	10	mV
Time in Power-on reset after supply reaches minimum operating voltage, depend on supply rise time.				
VDD supply rise time (0V to 1.7V) ² 10uS	-	TBD	TBD	mS
VDD supply rise time (0V to 1.7V) ² >10mS	-	TBD	TBD	mS
Operating Temperature Range	-40	+25	+105	°C

Note 1 This is the maximum VDD or VDD_HV ripple or noise (at any frequency) that does not disturb the radio.

Note 2 The on-board power-on reset circuitry may not function properly for rise times longer than the specified maximum.

Note 3 BL54H20 power supply options:

- **Option 1 High Voltage Mode** - Connect external supply voltage (within range 1.9V-5.5V) to VDDH pin. Customer MUST externally fit a 10uF (0603 body size) to ground. Ensure capacitor value reduction due to DC bias, AC bias, temperature is minimized so the Effective Specification for this 10uF capacitor is 3uF to 12uF over all conditions (DCbias=5.5V, ACbias=0.01V and temperature range -40°C to +105°C).
- **Option 2 Normal Voltage Mode** - Connect external supply voltage (within range 1.8V) to both VDDH and VDD pin.

If using USB interface then the BL54H20 VBUS pin must be connected to external supply within the range 4.4V to 5.5V.

When using the BL54H20 VBUS pin, customer MUST externally fit a 10uF (0603 body size) to ground. Ensure capacitor value reduction due to DC bias, AC bias, temperature is minimized so the Effective Specification for this 10uF capacitor is 3uF to 12uF over all conditions (DCbias=5.5V, ACbias=0.01V and temperature range -40°C to +105°C).

Note 4 VDDH/VDD (either High voltage mode or Normal voltage mode) must be powered before VDDIO_Px.

3.4 Clocks

3.4.1 HFXO - 32MHz crystal oscillator and nRF54H20 internal load capacitor TBDpF mandatory setting

The BL54H20 module contains the 32 MHz crystal, but the load capacitors to create 32MHz crystal oscillator circuit are inside the nRF54H20 chipset. Customer MUST set the internal nRF54H20 capacitors to TBDpF (for proper operation of the 32 MHz crystal circuit).

The 32 MHz crystal inside the BL54H20 module is a high accuracy crystal (± 15 ppm at room temperature) that helps with radio operation and reducing power consumption in the active modes.

3.4.2 LFCLK - Low Frequency clock source

There are four possibilities (see figure 5) for the low frequency clock (LFCLK) and options are:

LFRC (32.768kHz RC oscillator): The Internal 32.768 kHz RC oscillator (LFRC) is fully embedded in nRF54H20 (and does not require additional external components) with an accuracy ± 250 ppm (after calibration of LFRC at least every eight seconds using the HFXO as a reference oscillator). See section **Error! Reference source not found..**

LFXO (32.768kHz crystal oscillator): For higher LFCLK accuracy (greater than ± 250 ppm accuracy is required), the low frequency crystal oscillator (LFXO) must be used. To use LFXO, a 32.768kHz crystal must be connected between the XL1 and XL2 pins and the load capacitance between each crystal terminal and ground. Optionally internal (to nRF54H20) capacitor of maximum TBDpF in TBDpF steps are provided on pins XL1 and XL2.

Low frequency (32.768 kHz) external source: The 32.768 kHz oscillator (LFXO) is designed to work with external sources. Following external sources are supported:

LFSYNTH (32.768kHz Synthesised clock) from HFCLK (LFSYNTH): The LFCLK can be synthesised from the HFCLK source. LFSYNTH depends on the HFCLK to run. The accuracy of the LFCLK clock with LFSYNTH as a source assumes the accuracy of the HFCLK. If high accuracy is required, the HFCLK must be generated from the HFXO. Using the LFSYNTH clock removes the requirement for an external 32.768kHz crystal but increases the average power consumption as the HFCLK will be turned on in the system.

3.4.3 Other Internal Clocks

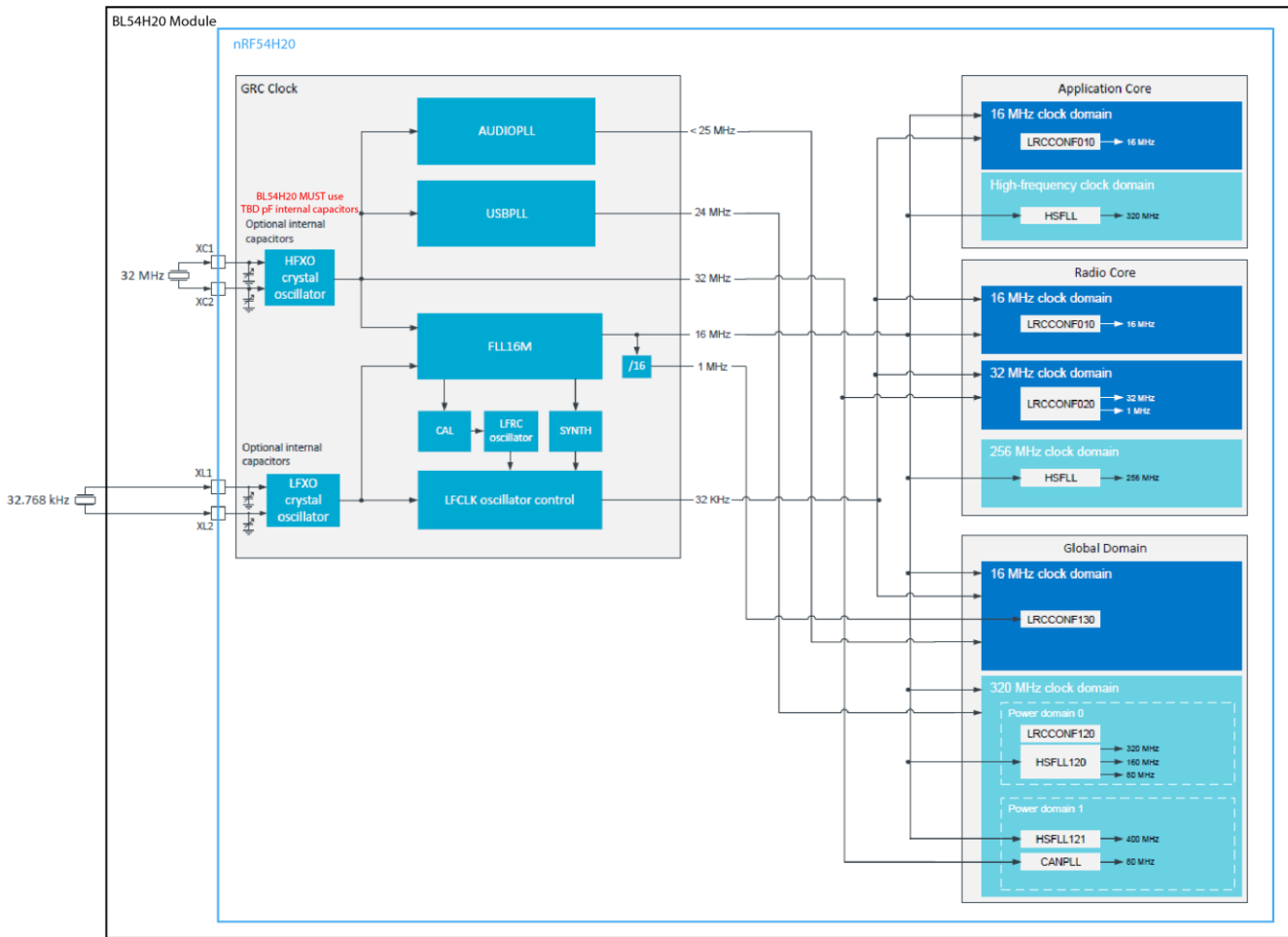


Figure 3: nRF54H20 Clock System Overview (adapted from Nordic)

3.5 BL54H20 Power Supply Options

The BL54H20 module power supply internally contains the following two main supply regulator stages (Figure 4):

- VDD_HV pin
- VDD pin

The USB peripheral is powered separately (connected to the VBUS pin).

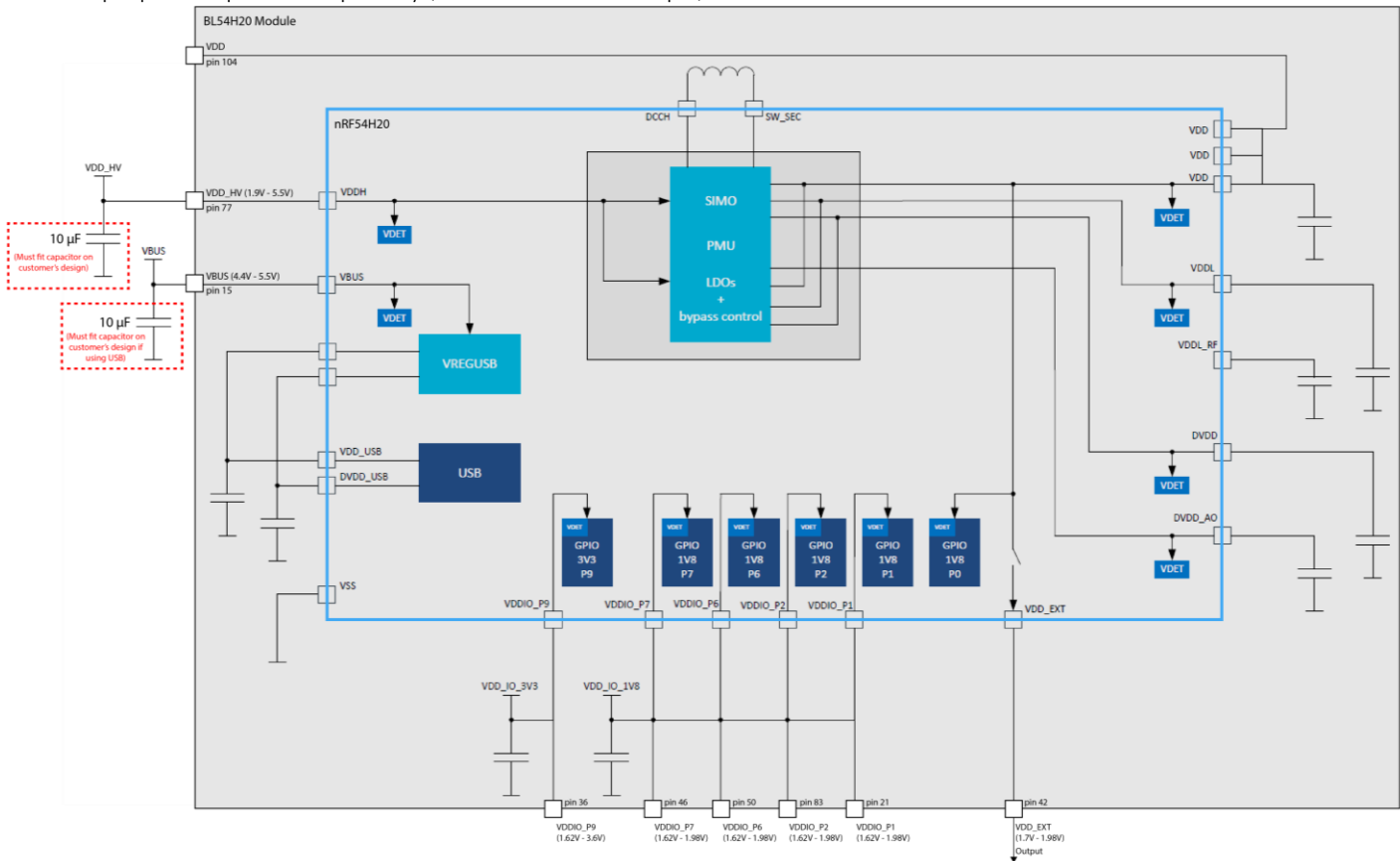


Figure 4: BL54H20 power supply block diagram (adapted from Nordic)

3.5.1 High Voltage mode (option1) or Normal Voltage mode (option2)

The BL54H20 power supply system enters one of two supply voltage modes, High voltage mode or Normal voltage mode, depending on how the external supply voltage is connected to these pins.

BL54H20 power supply options:

- **Option 1 High Voltage Mode** - Connect external supply voltage (within range 1.9V-5.5V) to VDDH pin.
Customer MUST externally fit a 10uF (0603 body size) to ground. Ensure capacitor value reduction due to DC bias, AC bias, temperature is minimized so the Effective Specification for this 10uF capacitor is 3uF to 12uF over all conditions (DCbias=5.5V, ACbias=0.01V and temperature range -40°C to +105°C).

OR

- **Option 2 Normal Voltage Mode** - Connect external supply voltage (1.8V) to both VDDH and VDD pin.

For either option, If using USB interface then the BL54H20 VBUS pin must be connected to external supply within the range 4.4V to 5.5V.

When using the BL54H20 VBUS pin, customer MUST externally fit a 10uF (0603 body size) to ground. Ensure capacitor value reduction due to DC bias, AC bias, temperature is minimized so the Effective Specification for this 10uF capacitor is 3uF to 12uF over all conditions (DCbias=5.5V, ACbias=0.01V and temperature range -40°C to +105°C).

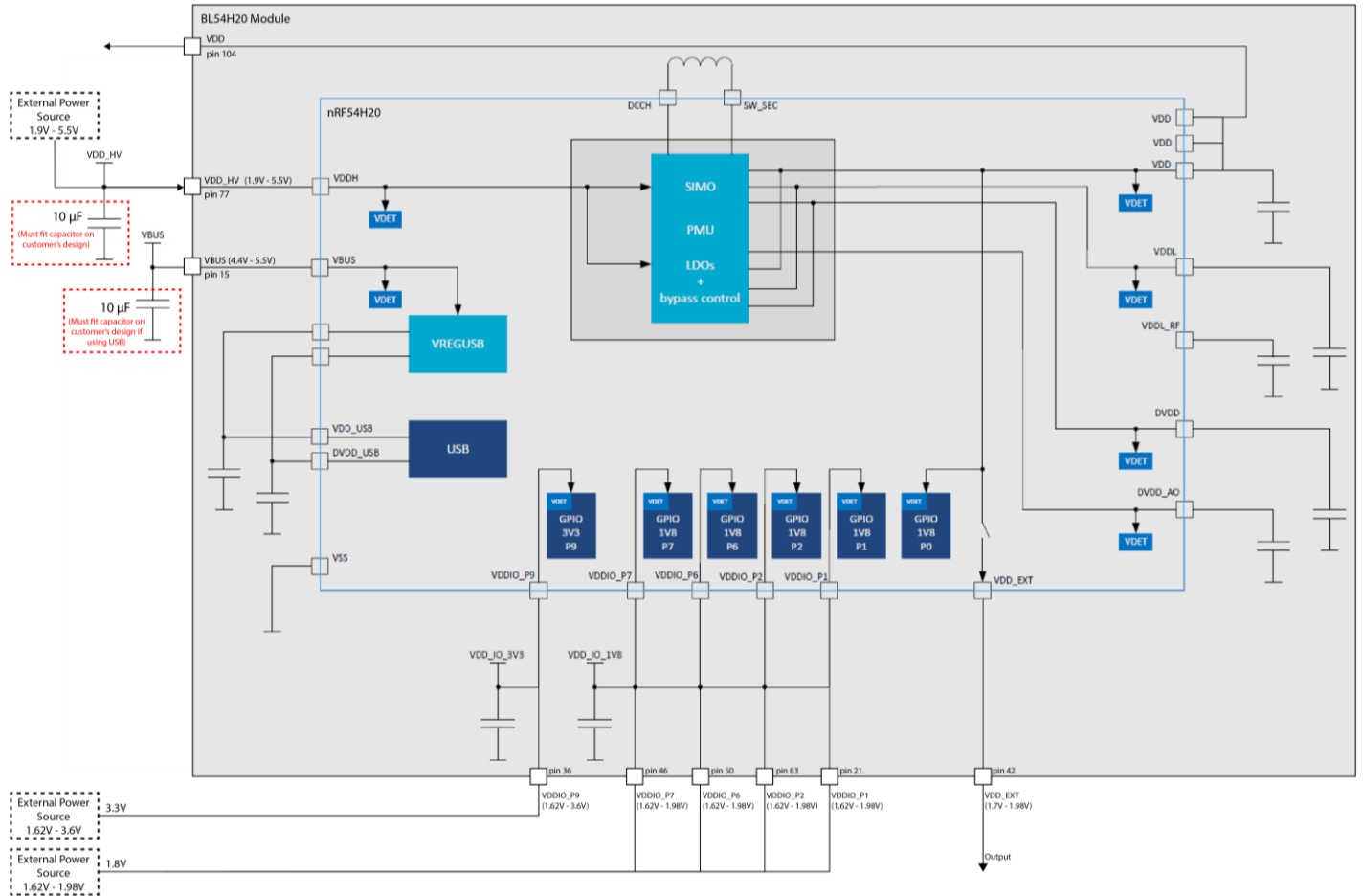


Figure 5: High Voltage mode (option1)

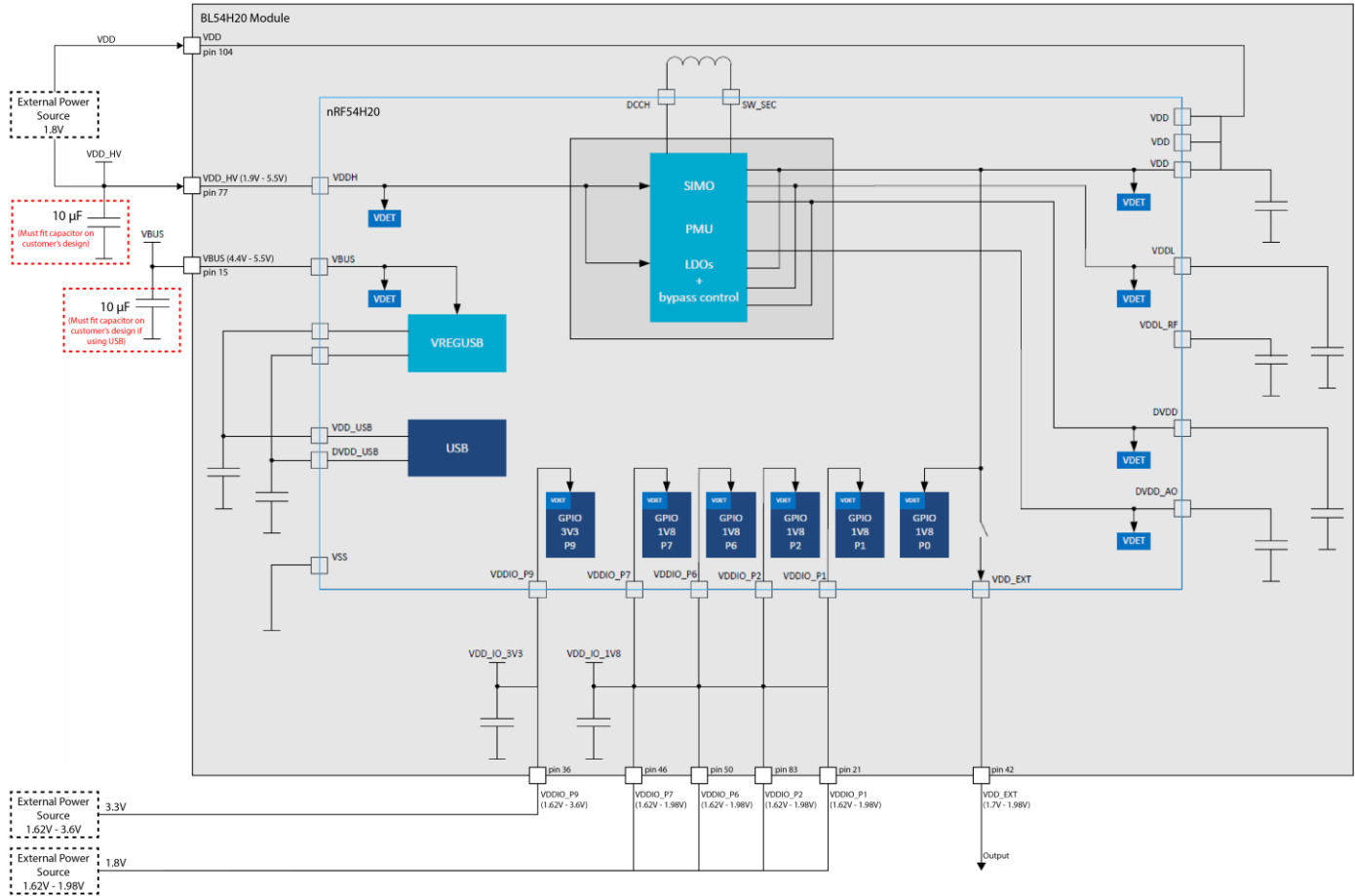


Figure 6: Normal Voltage Mode (option2)

3.5.2 VBUS pin and 10uF Mandatory Capacitor

To use the BL54H20 USB peripheral:

1. Connect the BL54H20 VBUS pin to the external supply within the range 4.4V to 5.5V. When using the BL54H20 VBUS pin, you **MUST** externally fit a 10uF (0603 body size) to ground. Ensure capacitor value reduction due to DC bias, AC bias, temperature is minimized (the Effective Specification for this 10uF capacitor is 3uF to 12uF over all conditions DCbias=5.5V, ACbias=0.01V and temperature range -40°C to +105°C).
2. When using the BL54H20 USB peripheral, the VBUS pin can be supplied from same source as VDD_HV (within the operating voltage range of the VBUS pin and VDD_HV pin).
3. An optional series 2.2ohms resistor on the USB supply (VBUS) can be fitted for improved immunity to transient over-voltage VBUS connection.

If not using USB peripheral, the VBUS pin can be left unconnected.

4 Programmability

4.1 BL54H20 Default Firmware

The BL54H20 module is shipped from Ezurio manufacturing facilities with no firmware programmed.

4.2 BL54H20 Firmware Options

Firmware for use with the BL54H20 can be divided into the following types.

- Bootloader** – This is the application that resides on the Application core used for perform firmware updates on the Application, Radio, FLPR and PPR cores.
 The MCU Boot or Trusted Firmware M Bootloaders are recommended to be used as the basis for the BL54H20 Bootloader functionality.
- Application** – This is the main application code that resides on the Application core. It interfaces with the Radio core and PPR/FLPR cores and provides supplementary functionality to that of the time critical activities being performed on the Radio, PPR and FLPR cores.
- Radio Stack** – This is the protocol stack(s) that reside on the Radio Core. These control the radio and perform time critical radio operations, the results of which are provided to the Application core for high level processing.
- Software Defined Peripheral** – These are the applications running on the FLPR and PPR RISC-V cores intended to offload activities from the Application core.

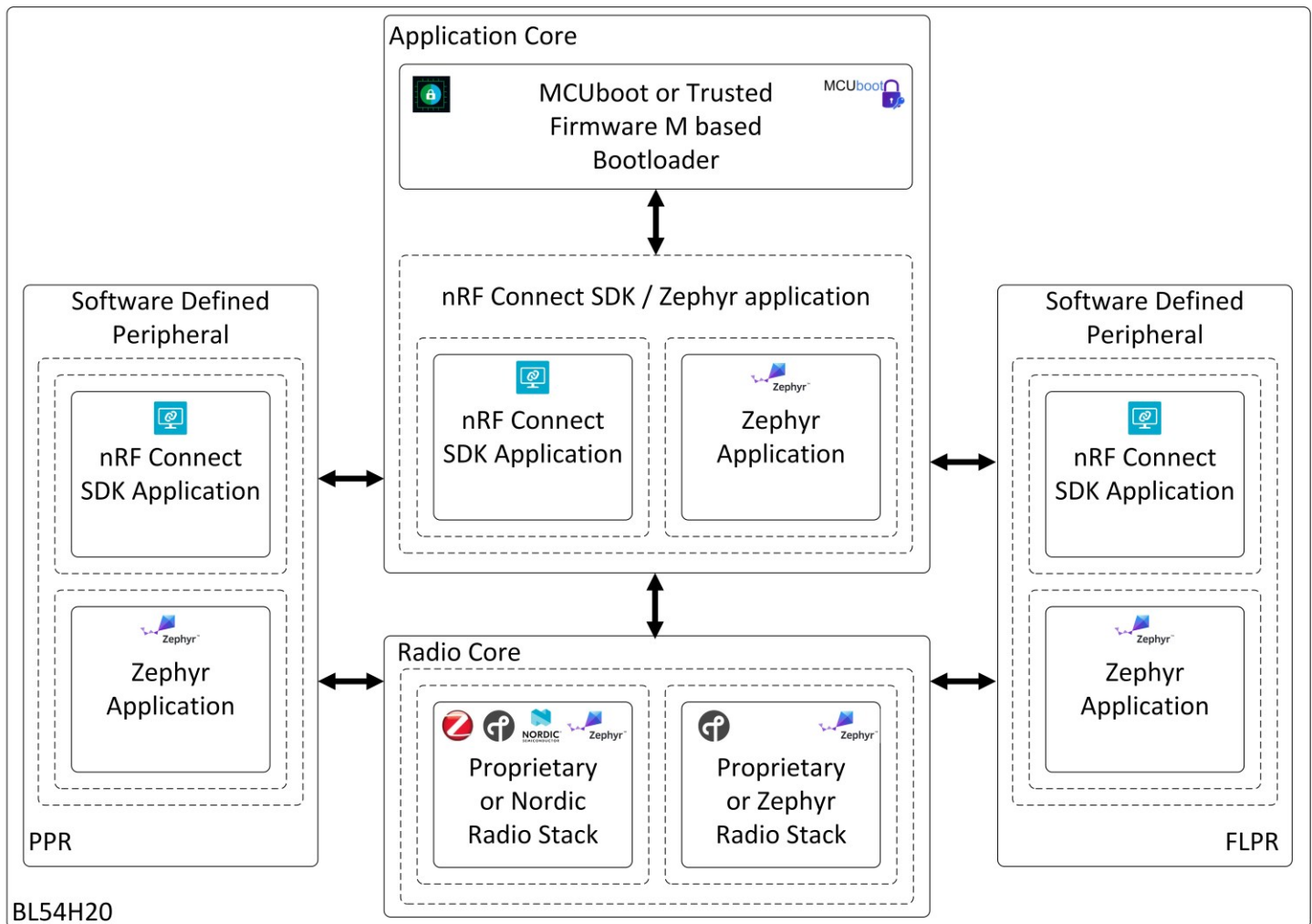


Figure 7: Functional SW block diagram for BL54H20 series module

5 Mandatory SW requirements related to hardware

5.1 32MHz crystal internal load capacitor setting of TBD pF

MANDATORY. BL54H20 module contains the 32 MHz crystal but the load capacitors to create 32 MHz crystal oscillator circuit are inside the nRF54H20 chipset. Customer MUST set the internal nRF54H20 capacitors to TBD pF (for proper operation of the 32 MHz crystal circuit in the BL54H20 module).

6 Hardware Integration Suggestions

6.1 Circuit

The BL54H20 is easy to integrate, requiring no external components on your board apart from those which you require for development and in your end application.

The following are suggestions for your design for the best performance and functionality.

Checklist (for Schematic):

- **BL54H20 power supply options:**

Option1 High Voltage Mode – Main voltage input (using BL54H20 VDD_HV pin) the external supply voltage (within range 1.9V-5.5V) is ONLY connected to the VDD_HV pin.

Option 2 Normal Voltage Mode - Connect external supply voltage (within range 1.8V) to both VDD_HV and VDD pin.

- **BL54H20 GPIO ports power:**

VDDIO_P1, VDDIO_P2, VDDIO_P6, VDDIO_7 GPIO power supply pins: Connect external supply (within range 1.62V to 1.98V range) to power BL54H20 GPIO these GPIO ports P1, P2, P6, P7 ports power pins

VDDIO_P9 GPIO power supply pins: Connect external supply (within range 1.62V to 3.6V range) to power BL54H20 GPIO 3V port power pin VDDIO_P9.

External power source should be within the operating range, rise time and noise/ripple specification of the BL54H20. Add decoupling capacitors for filtering the external source. Power-on reset circuitry within BL54H20 series module incorporates brown-out detector, thus simplifying your power supply design. Upon application of power, the internal power-on reset ensures that the module starts correctly.

- **BL54H20 USB peripheral:**

To use the BL54H20 USB peripheral:

1. Connect the BL54H20 VBUS pin to the external supply within the range 4.4V to 5.5V. When using the BL54H20 VBUS pin, you **MUST** externally fit a 10uF to ground. Ensure capacitor value reduction due to DC bias, AC bias, temperature is minimized so the Effective Specification for this 10uF capacitor is 3uF to 12uF over all conditions (DCbias=5.5V, ACbias=0.01V and temperature range -40°C to +105°C).
2. Connect the external supply to VDD_HV pin to operate the rest of BL54H20 module.
3. When using the BL54H20 USB peripheral, the VBUS pin can be supplied from same source as VDD_HV (within the operating voltage range of the VBUS pin and VDD_HV pin).
4. An optional series 2.2Ohms resistor on the USB supply (VBUS) can be fitted for improved immunity to transient over-voltage VBUS connection.

If not using USB peripheral, the VBUS pin can be left unconnected.

- **AIN (ADC) and GPIO pin IO voltage levels**

BL54H20 GPIO voltage levels are at VDD. Ensure input voltage levels into GPIO pins are at VDD also (if VDD source is a battery whose voltage drops). Ensure ADC pin maximum input voltage for damage is not violated.

- **AIN (ADC) impedance and external voltage divider setup**

If you need to measure with ADC a voltage higher than 3.6V, you can connect a high impedance voltage divider to lower the voltage to the ADC input pin.

- **SWD**

This is REQUIRED for loading firmware. MUST wire out the SWD two wire interface on host design. Five lines should be wired out, namely SWDIO, SWDCLK, nRESET, GND and VDD.

- **UART and flow control (CTS, RTS)**

Required if customer requires UART.

- **TWI (I2C)**

It is essential to remember that pull-up resistors on both SCL and SDA lines are required, the value as per I2C standard. nRF54H20 can provide 13K Ohms typical pull up values internally. For other values, fit external pull-up resistor on both SCL and SDA as per I2C specification to set speed. The I2C specification allows a line capacitance of 400pF.

- **EXMIF, QSPI, High Speed SPI (32Mbps), High speed TWI (I2C, 1Mbps), QSPI and Trace**

EXMIF, QSPI, High-Speed SPI (32Mbps), TWI 1Mbps and Trace come on dedicated GPIO pins only. Other lower speed SPI and TWI can come out on any GPIO pins.

For all high-speed signal, the printed circuit board (PCB) layout must ensure that connections are made using short PCB traces.

- **GPIO pins**

If GPIO is selected as an input, ensure the input is not floating (which can cause current consumption to drive with time in low power modes (such as System ON Idle), by selecting the internal pull up or pull down.

- **NFC antenna connector**

To make use of the Ezurio flexi-PCB NFC antenna (part # 0600-00061), fit connector:

- Description – FFC/FPC Connector, Right Angle, SMD/90d, Dual Contact, 1.2 mm Mated Height
- Manufacturer – Molex
- Manufacturers Part number – 512810594

Add tuning capacitors of 300 pF on NFC1 pin to GND and 300 pF on NFC2 pins to GND if the PCB track length is similar as development board.

- **nRESET pin (active low)**

Hardware reset. Wire out to push button or drive by host.

By default module is out of reset when power applied to VDD pins (13K pull-up inside nRF54H20).

- **Optional External 32.768kHz crystal**

If the optional external 32.768kHz crystal is needed, then use a crystal that meets specification and add load capacitors (either inside nRF54H20 or discrete capacitors outside nRF55) whose values should be tuned to meet all specification for frequency and oscillation margin.

6.2 PCB Layout on Host PCB - General

Checklist (for PCB):

- MUST locate BL54H20 module close to the edge of PCB (mandatory for the 453-00197 for on-board chip antenna to radiate properly).
- Use solid GND plane on inner layer (for best EMC and RF performance).
- All module GND pins MUST be connected to host PCB GND.
- Place GND vias close to module GND pads as possible.
- Unused PCB area on surface layer can flooded with copper but place GND vias regularly to connect the copper flood to the inner GND plane. If GND flood copper is on the bottom of the module, then connect it with GND vias to the inner GND plane.
- Route traces to avoid noise being picked up on VDD, VDD_HV, VBUS supply and AIN (analogue), GPIO (digital) traces and high-speed traces.
- Ensure no exposed copper is on the underside of the module (refer to land pattern of BL54H20 development board).

6.3 PCB Layout on Host PCB for the 453-0019x

6.3.1 Antenna Keep-out on Host PCB

The 453-00197 has an integrated chip antenna (Ignion NN02-101) and its performance is sensitive to host PCB. It is critical to locate the 453-00197 on the edge of the host PCB (or corner) to allow the antenna to radiate properly. Refer to guidelines in section *PCB land pattern and antenna keep-out area for the 453-00197*. Some of those guidelines repeated below.

- Ensure there is no copper in the antenna keep-out area on any layers of the host PCB. Keep all mounting hardware and metal clear of the area to allow proper antenna radiation.
- For best antenna performance, place the 453-00197 module on the edge of the host PCB, preferably in the edge center.
- The BL54H20 development board (453-00197-K1) has the 453-00197 module on the edge of the board (not in the corner). The antenna keep-out area is defined by the BL54H20 development board which was used for module development and antenna performance evaluation is shown in [Figure 8](#), where the antenna keep-out area is 5mm wide, 5mm long; with PCB dielectric (no copper) height 1.6mm sitting under the 453-00197 chip antenna. There is an extra copper cutout of 3.631mm x 1.046mm under 453-00197 chip antenna RF matching circuit.
- The 453-00197 chip antenna is tuned when the 453-00197 is sitting on development board (host PCB) with size of 141.6mm x 63.5mm x 1.6mm.
- A different host PCB thickness dielectric will have small effect on antenna.
- The antenna-keep-out defined in the [7.2 Host PCB Land Pattern and Antenna Keep-out for the 453-00197](#) section.
- Host PCB land pattern and antenna keep-out for the BL54H20 applies when the 453-00197 is placed in the edge of the host PCB preferably in the edge center. [Figure 8](#) shows an example.

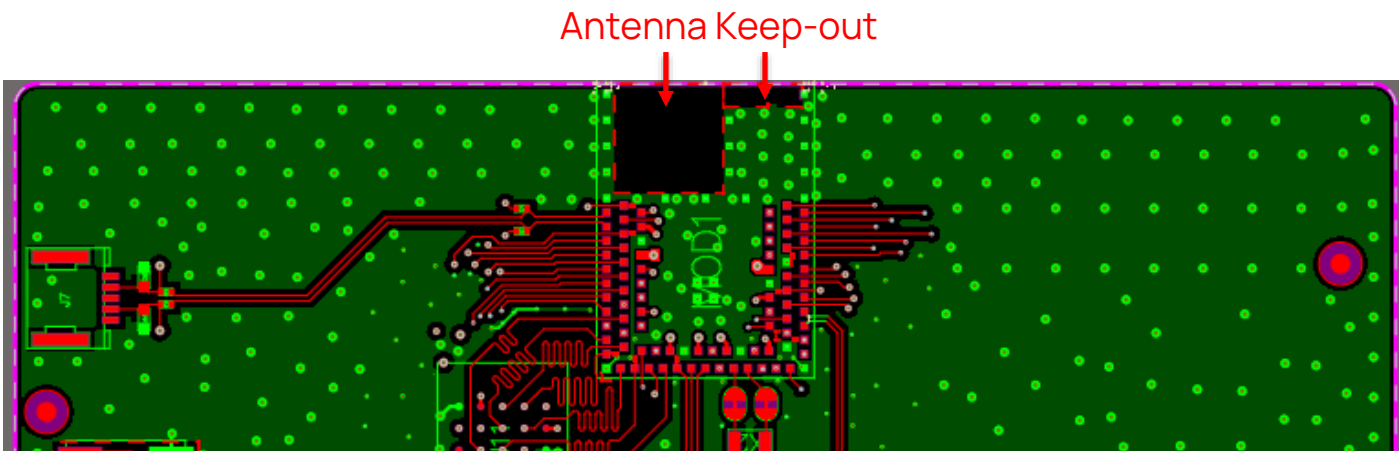


Figure 8: Chip Antenna keep-out area (shown in red), corner of the BL54H20 development board for the 453-00197 module.

Antenna Keep-out Notes:

Note 1 The BL54H20 module is placed on the edge, preferably edge centre of the host PCB.

Note 2 Copper cut-away on all layers in the *Antenna Keep-out* area under the 453-00197 on host PCB.

6.3.2 Antenna Keep-out and Proximity to Metal or Plastic

Checklist (for metal /plastic enclosure):

- Minimum safe distance for metals without seriously compromising the antenna (tuning) is 40 mm top/bottom and 30 mm left or right.
- Metal close to the 453-00197 chip antenna (bottom, top, left, right, any direction) will have degradation on the antenna performance. The amount of that degradation is entirely system dependent, meaning you will need to perform some testing with your host application.
- Any metal closer than 20 mm will begin to significantly degrade performance (S11, gain, radiation efficiency).
- It is best that you test the range with a mock-up (or actual prototype) of the product to assess effects of enclosure height (and materials, whether metal or plastic) and host PCB ground (GND plane size).

6.4 External Antenna Integration with BL54H20 RF trace pin variant (453-00198)

Please refer to the regulatory sections for FCC, ISED, CE, MIC, UKCA and RCM details of use of BL54H20 with external antennas in each regulatory region.

The BL54LH20 family has been designed to operate with the below external antennas (with a maximum gain of 2.32 dBi). The required antenna impedance is 50 ohms. See [Table 4](#). External antennas improve radiation efficiency.

Table 4: External antennas for the BL54H20 RF trace pin variant module (453-00044)

Manufacturer	Model	Ezurio Part Number	Type	Connector	Peak Gain	
					2400-2500 MHz	2400-2480 MHz
Ezurio (Laird Connectivity)	NanoBlue	EBL2400A1-10MH4L	PCB Dipole	IPEX MHF4	2 dBi	-
Ezurio (Laird Connectivity)	FlexPIFA	001-0022	PIFA	IPEX MHF4	-	2 dBi
Mag.Layers	EDA-8709-2G4C1-B27-CY	0600-00057	Dipole	IPEX MHF4	2.32 dBi	-
Ezurio (Laird Connectivity)	mFlexPIFA	EFA2400A3S-10MH4L	PIFA	IPEX MHF4	-	2 dBi
Ezurio (Laird Connectivity)	iFlexPIFA Mini	EFG2401A3S-10MH4L	PIFA	IPEX MHF4	-	2 dBi
Ezurio (Laird Connectivity)	Ezurio NFC	0600-00061	NFC	N/A	-	-

7 Mechanical Details

7.1 BL54H20 Mechanical Details

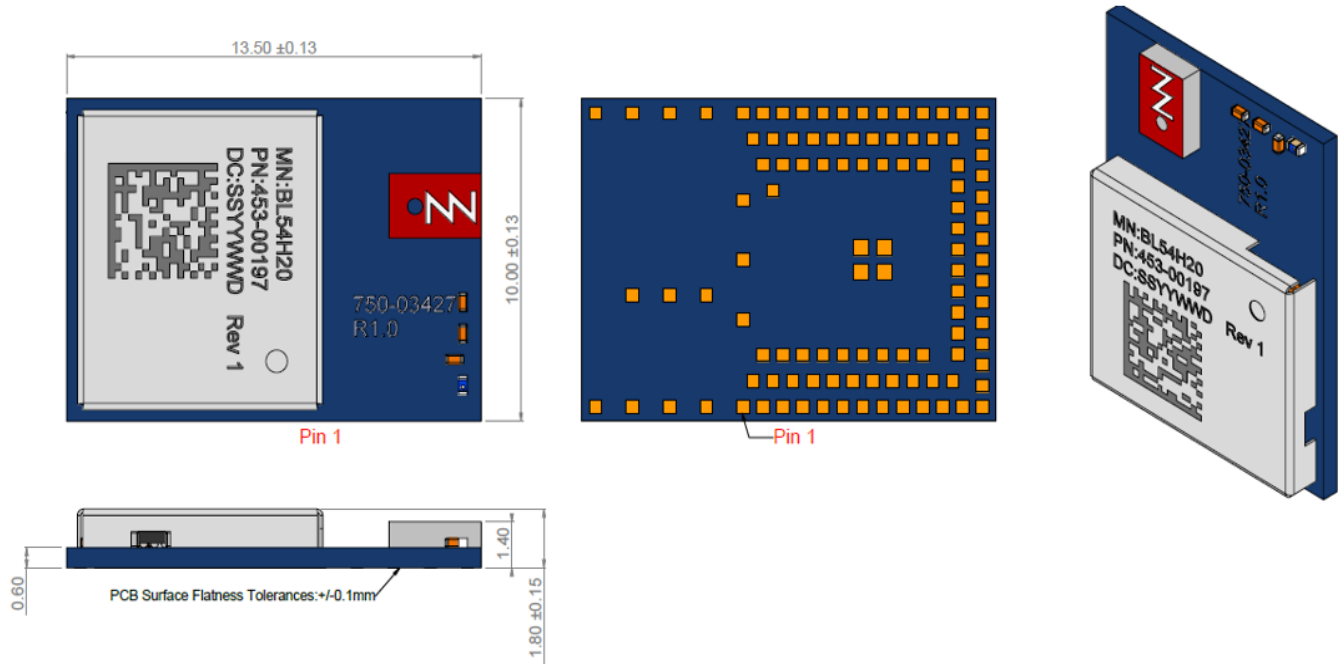


Figure 9: Mechanical Details - Internal Antenna variant

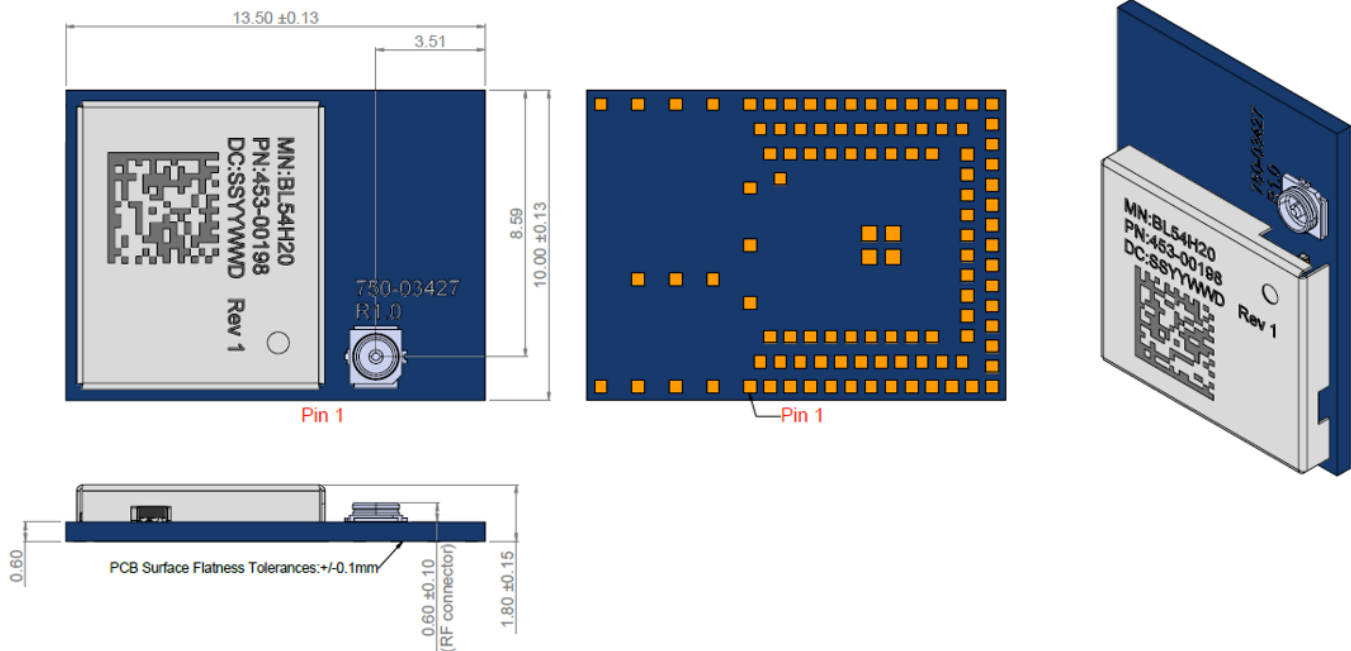
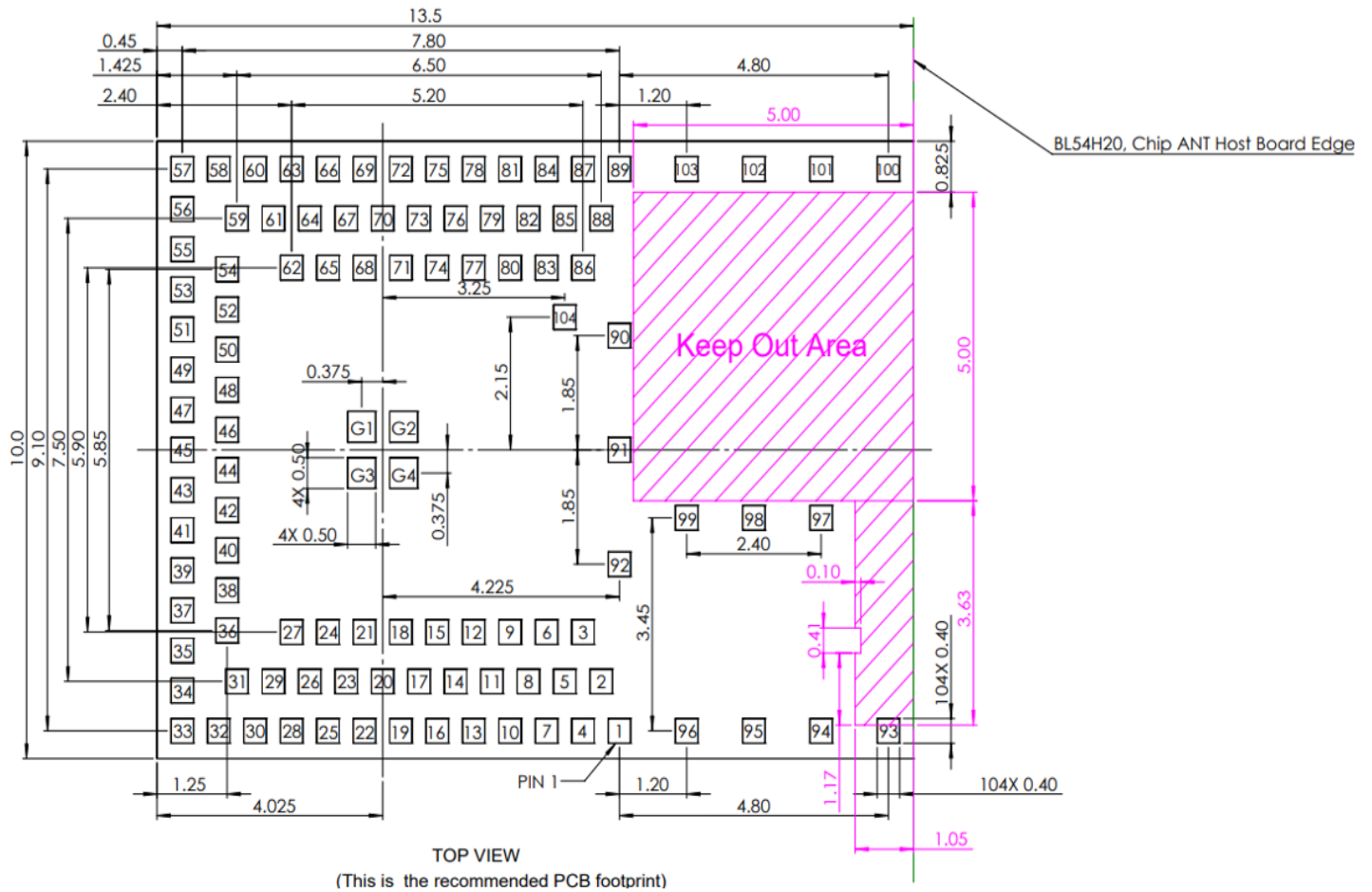


Figure 10: Mechanical Details - MHF4 RF connector variant

3D models for BL54H20 Module, Chip Antenna (453-00197) and BL54H20 Module, MHF4 (453-00198) can be found on the BL54H20 product page <https://www.ezurio.com/product/bl54h20-series-multi-core-bluetooth-le-80215-4-nfc>

7.2 Host PCB Land Pattern and Antenna Keep-out for the 453-00197

PCB footprint - BL54H20, Chip ANT (DXF and Altium format) and SCH Symbol - BL54H20, Chip ANT (Altium format) can be found on the BL54H20 product page - <https://www.ezurio.com/product/bl54h20-series-multi-core-bluetooth-le-80215-4-nfc>



All dimensions are in mm.

Figure 11: Land pattern 453-00xxx and Keep-out for the 453-00197

Host PCB Land Pattern and Antenna Keep-out for the 453-000xx Notes:

- Note 1** Ensure there is no copper in the antenna 'keep out area' on any layers of the host PCB. Also keep all mounting hardware or any metal clear of the area (Refer to 6.3.2) to reduce effects of proximity detuning the antenna and to help antenna radiate properly.
- Note 2** For the best on-board chip antenna performance, the module 453-00197 MUST be placed on the edge of the host PCB and preferably in the edge centre and host PCB (see Note 4).
- Note 3** BL54H20 development board has the 453-00197 placed on the edge of the PCB board (and not in corner), see section 7.2 Host PCB Land Pattern and Antenna Keep-out for the 453-00197.
- Note 4** Ensure that there is no exposed copper under the module on the host PCB.
- Note 5** You may modify the PCB land pattern dimensions based on their experience and/or process capability.

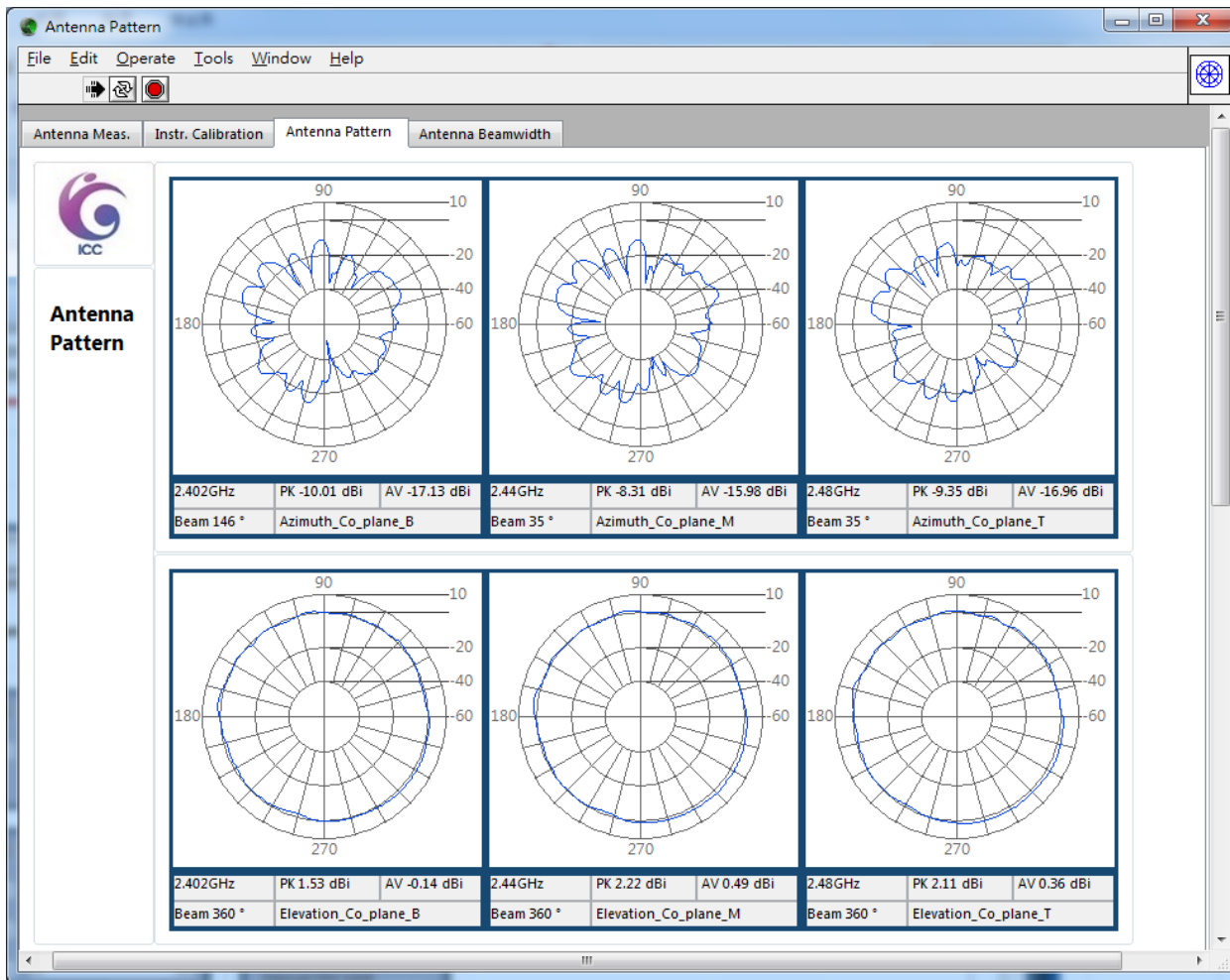
8 Chip Antenna Performance

8.1 Summary of Antenna Performance

Note : The result is measured with 453-00197-K1

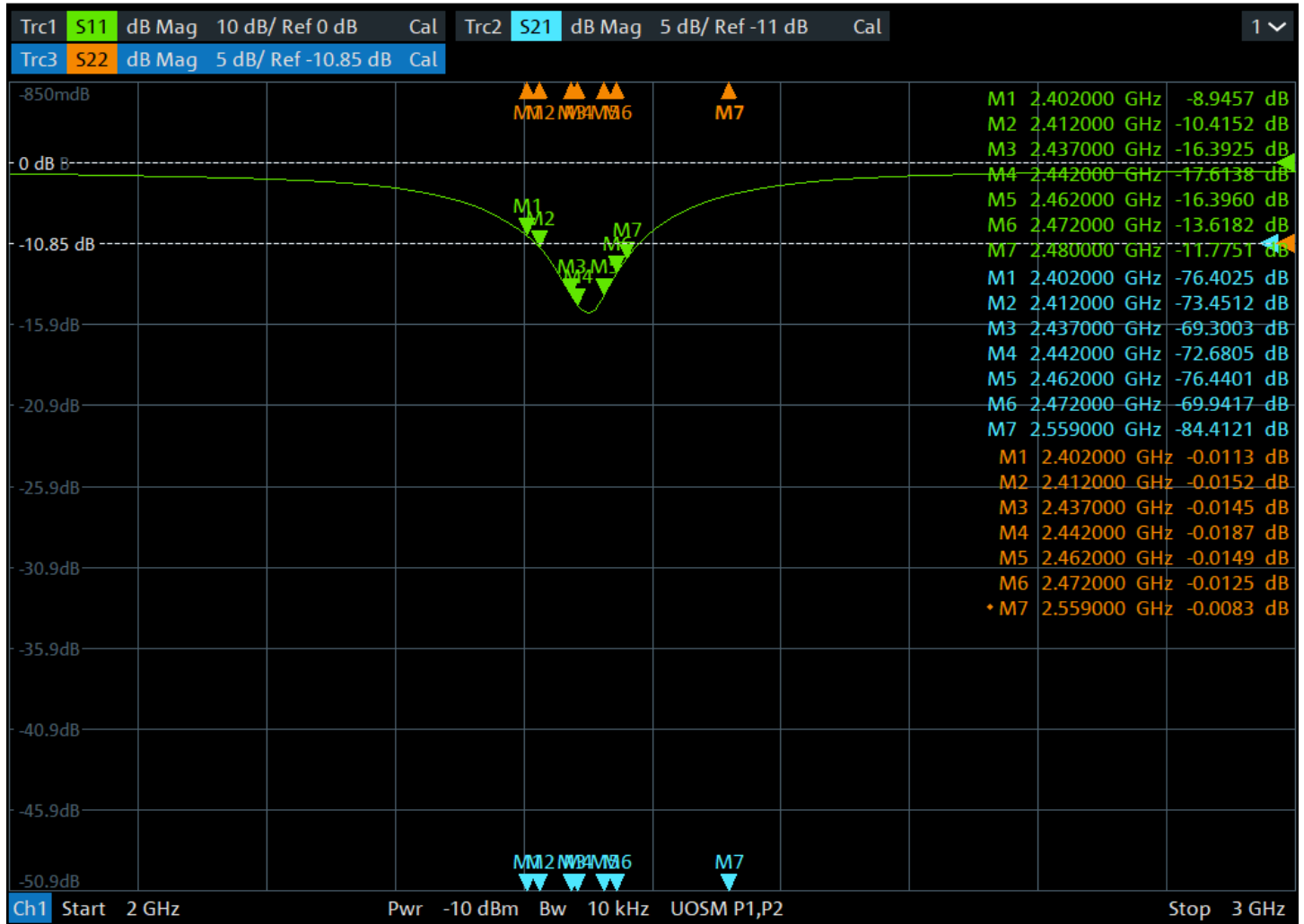
	2402MHz	2440MHz	2480MHz
Peak Antenna Gain dBi	1.53dBi	2.22dBi	2.11dBi
Average Antenna Gain dBi	-0.14dBi	0.49dBi	0.36dBi

8.2 2.4GHz Radiated Performance



8.3 Antenna S11 measuring data

11/14/2024 2:27:18 PM
1334.3330K63-100953-EU



9 Ordering Information

Part Number	Product Description
453-00197R	Module, BL54H20 (Nordic nRF54H20), Chip antenna, Tape/Reel
453-00198R	Module, BL54H20 (Nordic nRF54H20), MHF4 Connector, Tape/Reel
453-00197C	Module, BL54H20 (Nordic nRF54H20), Chip antenna, Cut Tape
453-00198C	Module, BL54H20 (Nordic nRF54H20), MHF4 Connector, Cut Tape
453-00197-K1	Development kit, Module BL54H20 (Nordic nRF54H20), Chip antenna
453-00198-K1	Development kit, Module BL54H20 (Nordic nRF54H20) - MHF4 Connector

10 Additional Information

Please contact your local sales representative or our support team for further assistance:

Headquarters	Ezurio 50 S. Main St. Suite 1100 Akron, OH 44308 USA
Website	http://www.ezurio.com
Technical Support	http://www.ezurio.com/resources/support
Sales Contact	http://www.ezurio.com/contact

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