Datasheet

INNOVATOR IN ELECTRONICS

Type 2BP UWB Module

NXP SR150 Chipset – Rev. J

- Design Name: Type 2BP
- P/N: LBUA0VG2BP-741



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About This Document

The Murata Type 2BP is an ultra-small Ultra-Wide Band (UWB) module that includes NXP's SR150 UWB chipset, clock, filters, and peripheral components. This document is a specification of the Murata 2BP module.

Please be aware that an important notice concerning availability, standard warranty and use in critical applications of Murata products and disclaimers thereto appears at the end of this specification sheet.

Audience & Purpose

This document is intended audience includes any customer looking to integrate this module into their product. In particular, RF, hardware, software, and systems engineers.

Document Conventions

Table 1 describes the document conventions.

Table 1: Document Conventions

Conventions	Description
	Warning Note Indicates very important note. Users are strongly recommended to review.
	Info Note Intended for informational purposes. Users should review.
	Menu Reference Indicates menu navigation instructions. **Example**: Insert➔Tables➔Quick Tables➔Save Selection to Gallery
	External Hyperlink This symbol indicates a hyperlink to an external document or website. **Example**: Murata Click on the text to open the external link.
	Internal Hyperlink This symbol indicates a hyperlink within the document. **Example**: Scope Click on the text to open the link.
`Console input/output or code snippet`	**Console I/O or Code Snippet** This text **Style** denotes console input/output or a code snippet.
`# Console I/O comment` `// Code snippet comment`	**Console I/O or Code Snippet Comment** This text **Style** denotes a console input/output or code snippet comment. • Console I/O comment (preceded by "#") is for informational purposes only and does not denote actual console input/output. • Code Snippet comment (preceded by "//") may exist in the original code.

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1 Scope

This specification is applied to the NXP SR150 UWB module.

2 Key Features

- Main IC : NXP / SR150
- Compliant with IEEE 802.15.4z HRP PHY
- Supports SHF UWB bands, Ch 5 and 9.
- Supports 62.4 MHz,124.8 MHz and 249.6 MHz PRF mode.
- Data rates of 6.81 Mbps, 7.8 Mbps, 27.24 Mbps and 31.2 Mbps.
- Complies with FCC & ETSI UWB spectral masks.
- Supports 2-way ranging (DS-TWR) and one way ranging (TDoA)
- Supports 2D and 3D Angle of Arrival (AoA) measurement
- Surface mount type 6.6 x 5.8 mm (Typical), H = 1.2 mm (Maximum)
- Weight : 107 mg
- MSL : 3
- RoHS compliant

3 Ordering Information

Table 2 describes the ordering information.

Table 2: Ordering Information

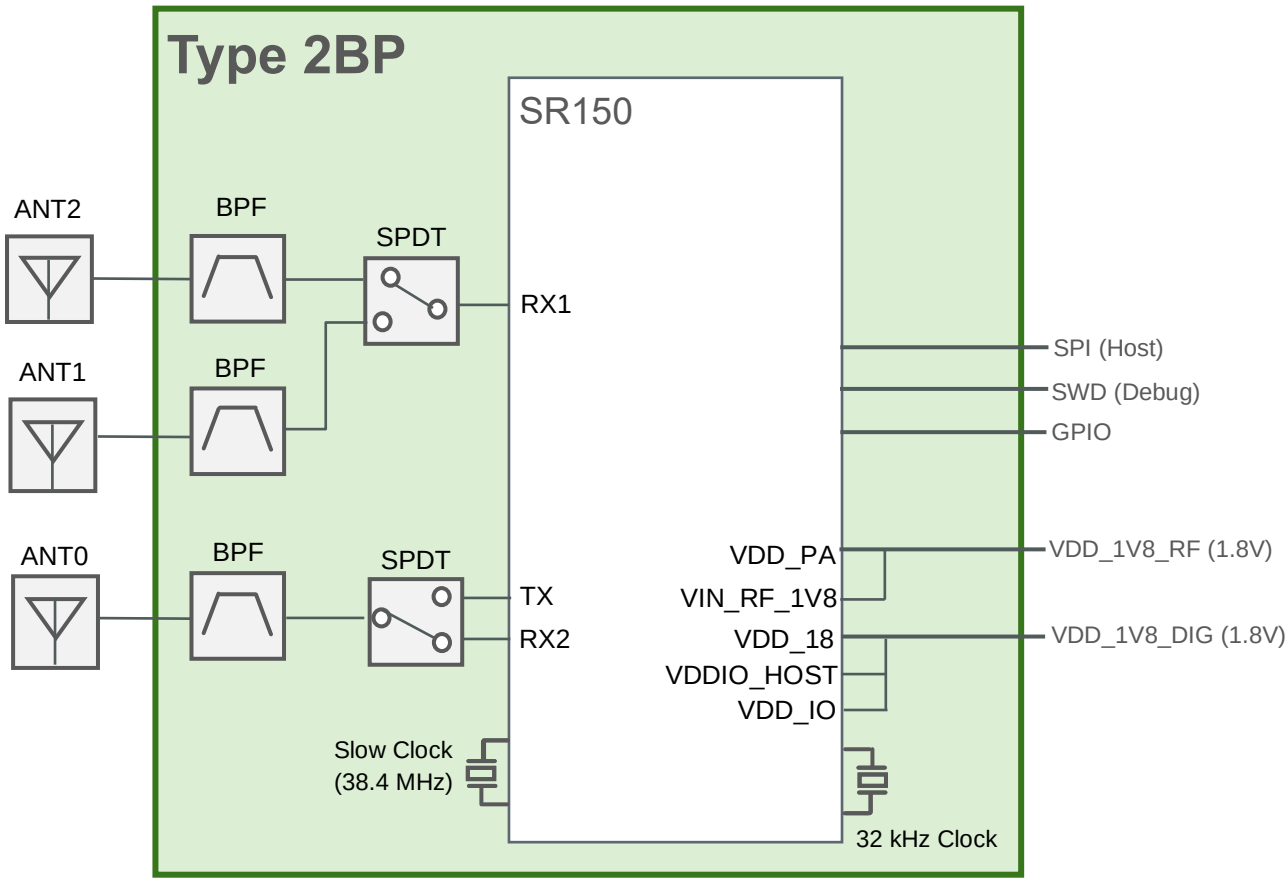
Ordering Part Number	Description
LBUA0VG2BP-741	MP order
LBUA0VG2BP-SMP	In case of sample order
LBUA0VG2BP-EVK-P	Evaluation Kit

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4 Block Diagram

Figure 1 shows the block diagram.

Figure 1: Block Diagram



5 Certification Information

5.1 Radio Certification

Table 3: Radio Certification

Country	ID	Country Code	Notes
USA (FCC)	VPYLB2BP	US	Certified diversion is allowed only if the final product is the Hand-held system (PART 15 Subpart F §15.519) and is an exact copy of the antenna used. Please see Section 16 for the antenna registered by Murata.
Canada (IC)	772C-LB2BP	CA	Certified diversion is allowed only if the final product is the Hand-held system (RSS-220 Section 5.3) and is an exact copy of the antenna used. Please see Section 16 for the antenna registered by Murata.

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Country	ID	Country Code	Notes
Europe	EN302065	DE	Conducted test report is prepared. This test report is for reference only and not applicable to the customer's final product.
Japan	R 003-220111	JP	Japanese type certification is prepared. **Note**: Certified diversion is allowed only when the antenna applied for by Murata is used.

6 Dimensions, Marking, and Terminal Configurations

Figure 2 shows the dimensions of the module from top.

Figure 2: Dimensions, Marking, and Terminal Configurations

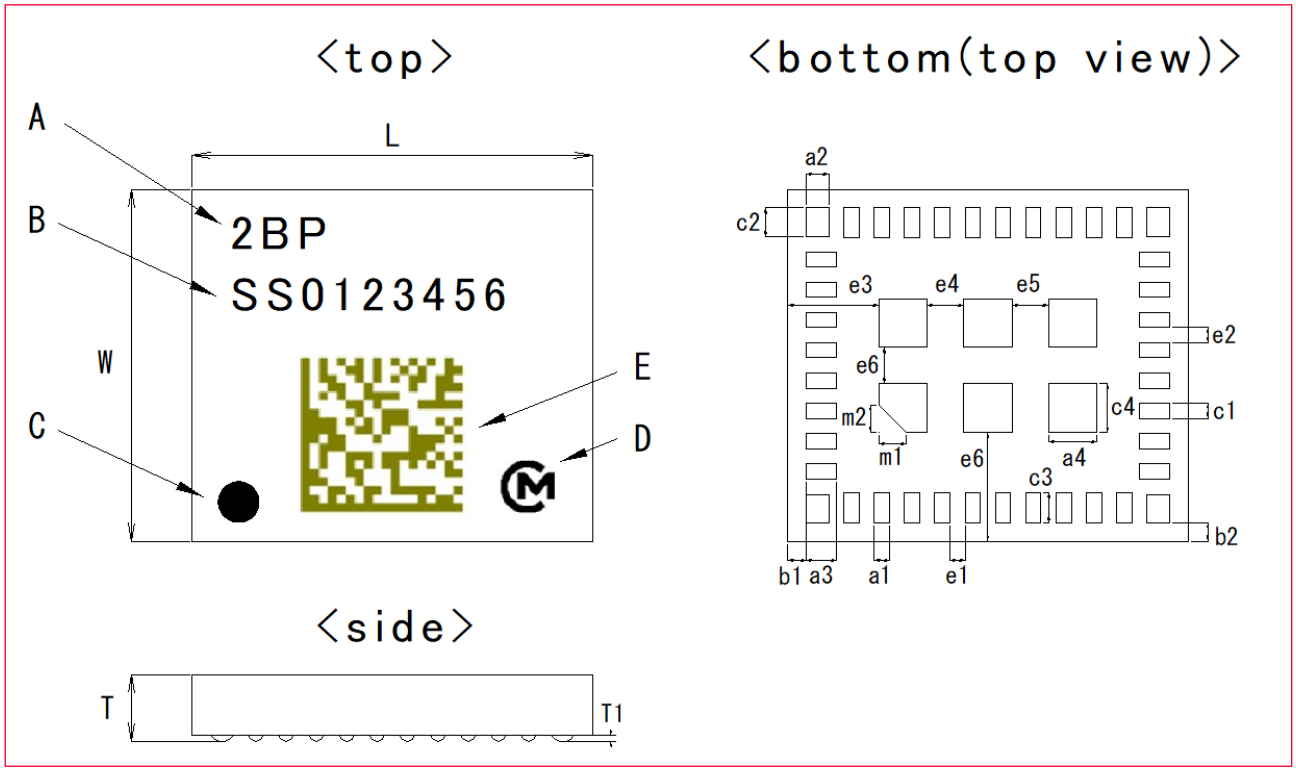


Table 4 describes the markings and meaning.

Table 4: Marking and Meaning

Marking	Meaning
A	Module Type
B	Inspection Number
C	Pin 1 Marking
D	Murata Logo
E	2D Code

Table 5 describes the markings and dimensions in millimeters.

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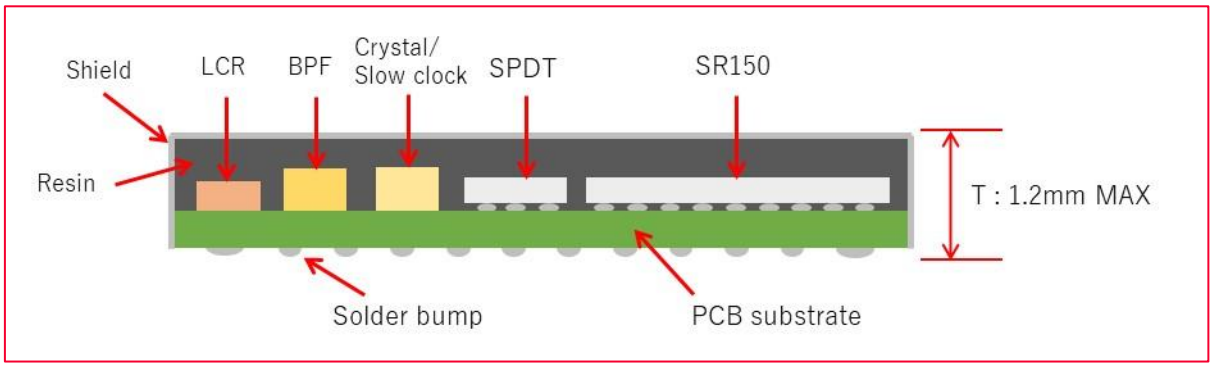
Table 5: Markings and Dimensions

Mark	Dimensions (mm)	Mark	Dimensions (mm)	Mark	Dimensions (mm)
L	6.6 +/- 0.2	W	5.8 +/- 0.2		
T	1.20 maximum	T1	0.045 typical		
a1	0.25 +/- 0.1	a2	0.375 +/- 0.1	a3	0.5 +/- 0.1
a4	0.8 +/- 0.1	b1	0.3 +/- 0.2	b2	0.3 +/- 0.2
c1	0.25 +/- 0.1	c2	0.475 +/- 0.1	c3	0.5 +/- 0.1
c4	0.8 +/- 0.1	e1	0.25 +/- 0.1	e2	0.25 +/- 0.1
e3	1.5 +/- 0.2	e4	0.6 +/- 0.1	e5	0.6 +/- 0.1
e6	1.8 +/- 0.2	m1	0.45 +/- 0.1	m2	0.45 +/- 0.1

6.1 Structure

Figure 3 shows the side view of the module structure.

Figure 3: Structure



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7 Module Pin Descriptions

This section describes the module pins.

7.1 Pin Assignments

Figure 4 shows the pin mapping (top view).

Figure 4: Pin Assignments (Top View)

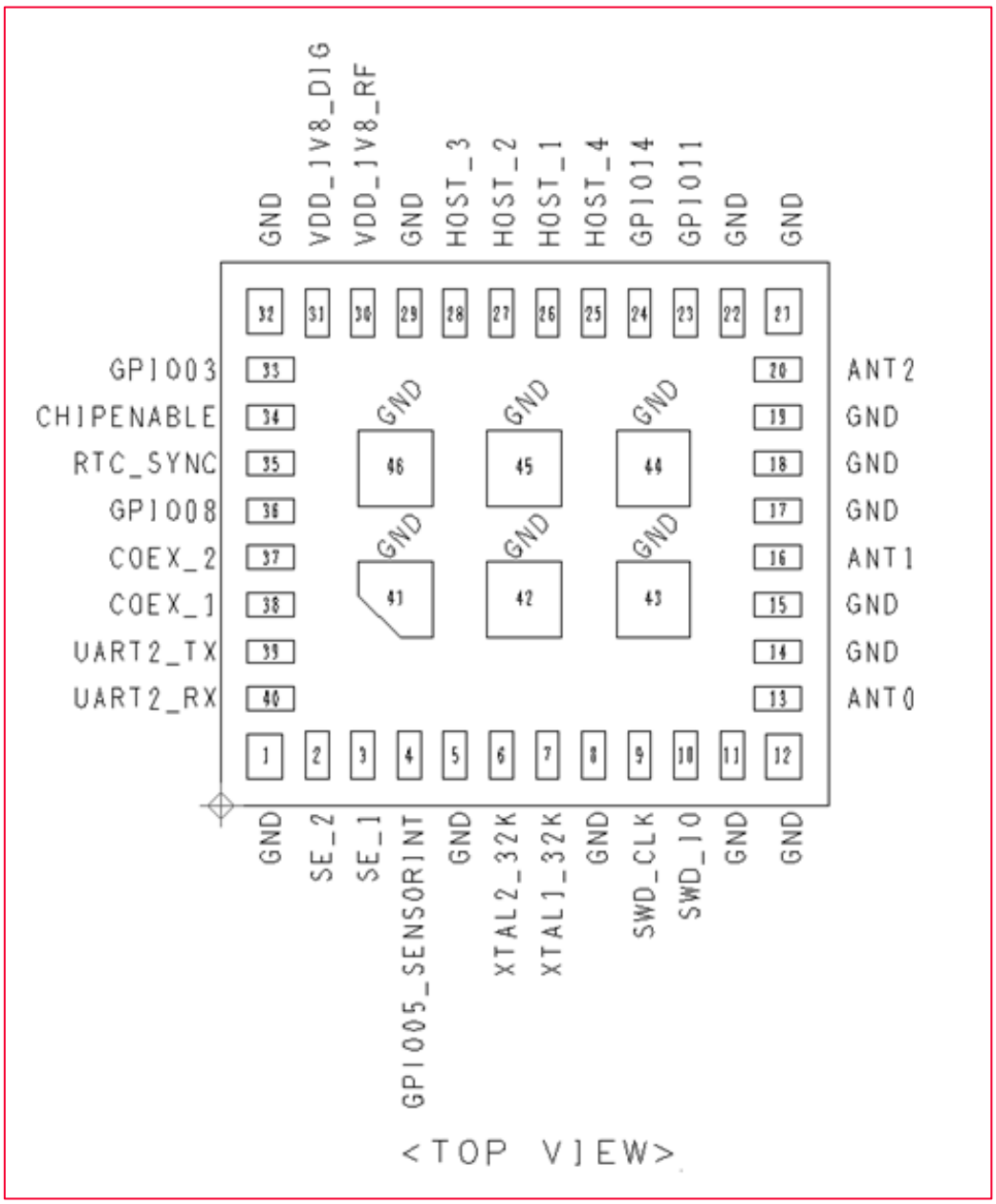


Table 6 lists the pin names.

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Table 6: Pins

No.	Terminal Name	No.	Terminal Name	No.	Terminal Name	No.	Terminal Name
1	GND	13	ANT0	25	HOST_4	37	COEX_2
2	SE_2	14	GND	26	HOST_1	38	COEX_1
3	SE_1	15	GND	27	HOST_2	39	UART2_TX
4	GPIO05_SENSORINT	16	ANT1	28	HOST_3	40	UART2_RX
5	GND	17	GND	29	GND	41	GND
6	XTAL2_32K	18	GND	30	VDD_1V8_RF	42	GND
7	XTAL1_32K	19	GND	31	VDD_1V8_DIG	43	GND
8	GND	20	ANT2	32	GND	44	GND
9	SWD_CLK	21	GND	33	GPIO03_SYNC	45	GND
10	SWD_IO	22	GND	34	CHIPENABLE	46	GND
11	GND	23	GPIO11	35	RTC_SYNC		
12	GND	24	GPIO14	36	GPIO08		

7.2 Pin Descriptions

Table 7 describes the pins.

Table 7: Pin Descriptions

No.	Pin Name	Type	Connection to IC	Supply	Description
			Pin Name		
1	GND				
2	SE_2	I/O	SE_2	VDD_IO	NA Kept open.
3	SE_1	I/O	SE_1	VDD_IO	NA Kept open.
4	GPIO05_SENSORINT	I/O	GPIO05_HOST_INT	VDD_IO	IRQ to host for indicating data ready, switching time is 125 ns.
5	GND				
6	XTAL2_32K	I	XTAL2_32K		Reserved pin for external X'tal option, please leave this pin as NC.
7	XTAL1_32K	I	XTAL1_32K		Reserved pin for external X'tal option, please leave this pin as NC.
8	GND				
9	SWD_CLK	I/O	SWD_CLK		Serial Wire Debug interface clock input. Default configuration is secondary SPI bus clock interface connection SPI_SCK, switching time is 125 ns.
10	SWD_IO	I/O	SWD_IO		Serial Wire Debug interface input/output. Default configuration is secondary SPI bus MISO connection, switching time is 125 ns.
11	GND				
12	GND				
13	ANT0	RF	TX_OUT / RX2_IN		RF Antenna port, Tx / Rx switched by internal SPDT.
14	GND				

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No.	Pin Name	Type	Connection to IC	Supply	Description
			Pin Name		
15	GND				
16	ANT1	RF	RX1_IN		RF Antenna port. ANT1 / ANT2 switched by internal SPDT.
17	GND				
18	GND				
19	GND				
20	ANT2	RF	RX1_IN		RF Antenna port. ANT1 / ANT2 switched by internal SPDT.
21	GND				
22	GND				
23	GPIO11	I/O	GPIO11_ANT_CTRL1	VDD_IO	General purpose IO, switching time is dependent on the end control point, 125 ns when controlled by ARM, 33 ns when controlled by the DSP.
24	GPIO14	I/O	GPIO14_ANT_CTRL2	VDDIO_HOST	General purpose IO, switching time is dependent on the end control point, 125 ns when controlled by ARM, 33 ns when controlled by the DSP.
25	HOST_4	I/O	HOST_4	VDDIO_HOST	Host Interface line 4, SPI MISO connection, switching time is 125 ns.
26	HOST_1	I/O	HOST_1	VDDIO_HOST	Host Interface line 1, SPI clock line, switching time is 125 ns.
27	HOST_2	I/O	HOST_2	VDDIO_HOST	Host Interface line 2, SPI slave connection, switching time is 125 ns
28	HOST_3	I/O	HOST_3	VDDIO_HOST	Host Interface line 3, SPI MOSI connection, switching time is 125 ns.
29	GND				
30	VDD_1V8_RF	Power	VDD_PA / VIN_RF_1V8		VDD supply for PA and Vin input to 1.8V RF
31	VDD_1V8_DIG	Power	VDD_1V8 / VDD_IO / VDDIO_HOST		VDD for all Digital LDOs, Host interface and IO pins.
32	GND				
33	GPIO03_SYNC	I	GPIO03_SYNC	VDDIO_HOST	SPI Rx handshake from Host Interface, General purpose IO, switching time is 125 ns
34	CHIPENABLE	I	CHIPENABLE	VDD_IO	Connection for disabling/enabling the chip
35	RTC_SYNC	I	RTC_SYNC	VDD_IO	Not used. Kept open
36	GPIO08_eSE	I/O	GPIO08_SE_IRQ	VDD_IO	NA Kept open
37	COEX_2	I/O	COEX_2		NA Kept open
38	COEX_1	I/O	COEX_1		NA Kept open
39	UART2_TX		UART2_TX		NA Kept open
40	UART2_RX		UART2_RX		NA Kept open
41	GND				
42	GND				
43	GND				
44	GND				
45	GND				
46	GND				

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8 Absolute Maximum Ratings

Table 9 describes the absolute maximum ratings.

Table 8: Absolute Maximum Ratings

Parameter		Minimum	Maximum	Unit
Storage Temperature		-40	+85	°C
Supply Voltage	VDD_1V8_DIG		2.5	V
	VDD_1V8_RF		2.5	V

Stresses in excess of the absolute ratings may cause permanent damage. Functional operation is not implied under these conditions. Exposure to absolute ratings for extended periods of time may adversely affect reliability. No damage assuming only one parameter is set at limit at a time with all other parameters are set within operating condition.

9 Operating Conditions

9.1 Operating Conditions

Table 9 describes the operating conditions.

Table 9: Operating Conditions

Parameter		Minimum	Typical	Maximum	Unit
Operating Temperature Range		-30	+25	+85	°C
Supply Voltage	VDD_1V8_DIG	1.71	1.8	1.98	V
	VDD_1V8_RF	1.71	1.8	1.98	V

9.2 Digital I/O Requirements

Table 10 describes the Pin Characteristics for GPIO's. SPI_SCK, SPI_SS.

Table 10: Pin Characteristics for GPIO 's. SPI_SCK, SPI_SS

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{IH}	High level input voltage	VDDIO=1.8V	0.85		VDDIO+0.5	V
V_{IL}	Low level input voltage	VDDIO=1.8V	-0.5		0.82	V
I_{OH}	Output high current	VOH=VDDIO 1.8V-0.4V	10		19.4	mA
I_{OL}	Output low current	VOL=0.4V, VDDIO@1.8V	39		58	mA
trise	Rise time at IO	20% to 80%, VDDIO=1.8V	0.97		2.15	ns
t_{fall}	Fall time at IO	80% to 20%, VDDIO=1.8V	1.03		2	ns
R_{PU}	Weak Pull-up resistor	VDDIO=0V	40	50	60	kΩ
R_{PD}	Weak Pull-down resistor	VDDIO=1.8V	40	50	60	kΩ
C_{IN}	IO pin capacitance				7	pF

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Table 11 describes the Pin Characteristics for SPI_MISO, SPI_MOSI.

Table 11: Pin Characteristics for SPI_MISO, SPI_MOSI

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{IH}	High level input voltage	VDDIO=1.8V	0.85		VDDIO+0.5	V
V_{IL}	Low level input voltage	VDDIO=1.8V	-0.5		0.78	V
I_{OH}	Output high current	VOH=VDDIO 1.8V-0.4V	17		33	mA
I_{OL}	Output low current	VOL=0.4V, VDDIO@1.8V	38		56	mA
trise	Rise time at IO	20% to 80%, VDDIO=1.8V	0.4		0.6	ns
t_{fall}	Fall time at IO	80% to 20%, VDDIO=1.8V	0.4		0.55	ns
R_{PU}	Weak Pull-up resistor	VDDIO=0V	40	48.8	58	kΩ
R_{PD}	Weak Pull-down resistor	VDDIO=1.8V	40	48.8	58	kΩ
C_{IN}	IO pin capacitance				6	pF

10 System Power Status and Power Sequence

This section describes the system power status and sequences.

10.1 System Modes

This module has 6 power modes : HPD (Hard Power Down) mode, DPD (Deep Power Down) mode, Deep power down retention mode, Sleep, Active mode, and Hardware configuration Autoload. Description of these modes are presented in **Table 12**.

Table 12: System Modes

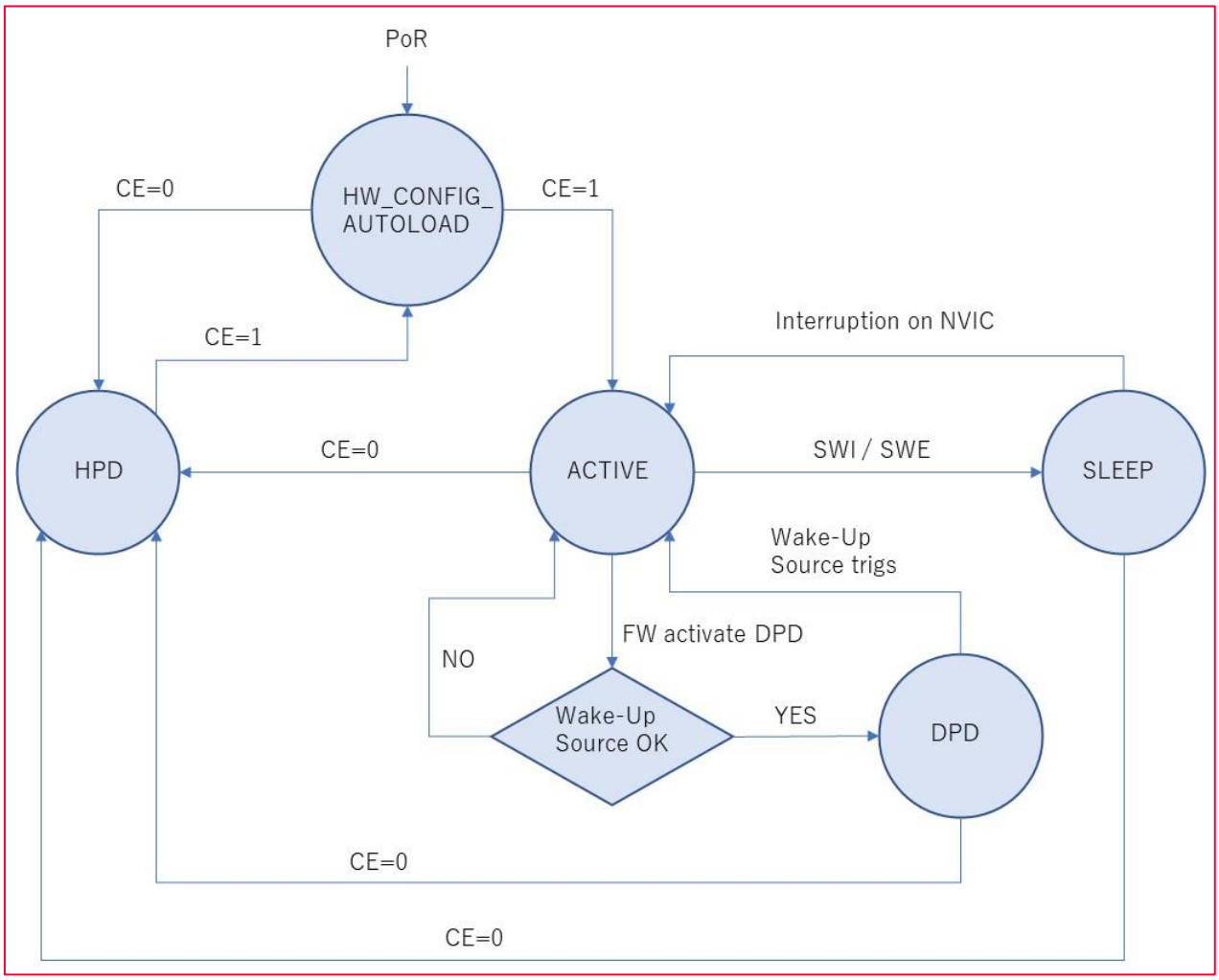
System Power State	Description
Active mode	The device is running and supplied by Platform PMU, in this mode several active states are available : Idle, TX, RX and Dual RX.
Deep power down (DPD) retention mode	The device is in low power mode and supplied by the Platform PMU, the memory is supplied, a configured wake up can bring the device back to the Active mode, no RF communication is possible.
Sleep	Specific parts can be active or inactive, this sleep mode can be configured by firmware which enables several power states, no RF communication is possible.
Hard power down (HPD) mode	The device is powered down and supplied by the PMU, it can be activated by the CE (CHIPENABLE) signal.
Hardware configuration Autoload	The device is supplied by the platform PMU and is loading the Hardware configuration and firmware into the memory.

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10.2 State Diagram and Power Modes

The state diagram and power modes are shown in **Figure 5**.

Figure 5: Power State Diagram and Power Modes



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10.3 Power Mode Entry and Exit Conditions

This section describes the power mode entry and exit conditions.

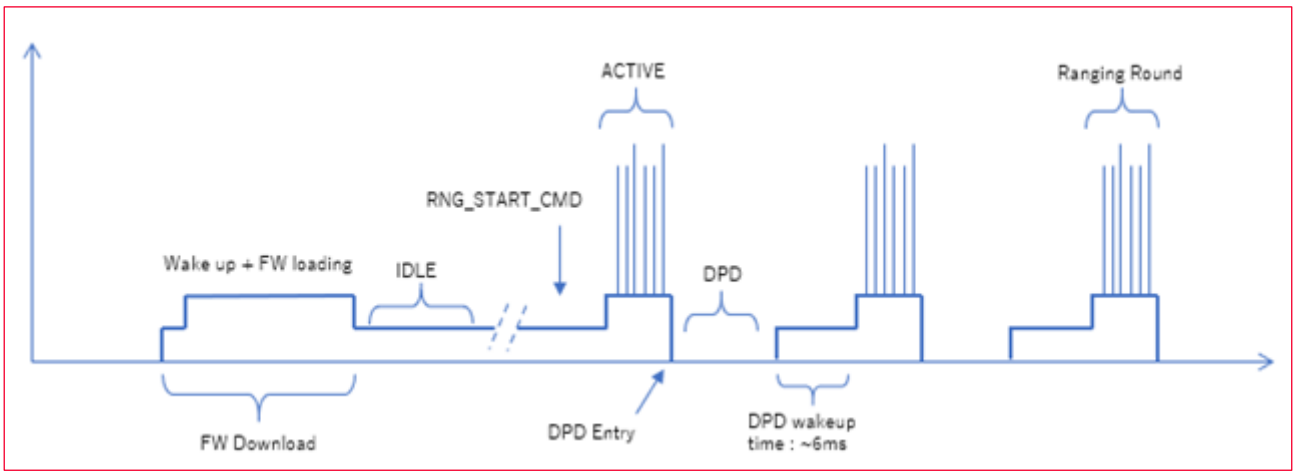
Table 13: Power Mode Entry and Exit Conditions

Power State	Entry Condition	Exit Condition
HPD	Two possible methods • Software command • Assert CE low for > 80 us	Assert CE to High
DPD with memory retention mode	• Software Command	Exit to HPD state: • Assert CE low for > 80us Exit to Active state: • Wake up timer expired • Temperature sensor event • SPI NSS Negative Edge, GPIO(3,5) event.
ACTIVE	• End of system boot after wake up • Wake up timer expired • Temperature sensor event • SPI NSS Negative Edge, GPIO (3,5) event.	• Software command • Assert CE low for > 80 µs

The time required for the module to go into DPD state is < 100 µs controlled by the firmware. The required time for the module to enter HPD state is less then 100 µs starting for the instance that CE is de-asserted, in both modes VDD_1V8_DIG is turned off. The Wakeup timing from DPD state is around 370 µs, the wakeup from HPD state is triggered once CE is asserted and takes around 380 µs.

A typical system power cycle image is shown in **Figure 6**.

Figure 6: Power Cycle Image



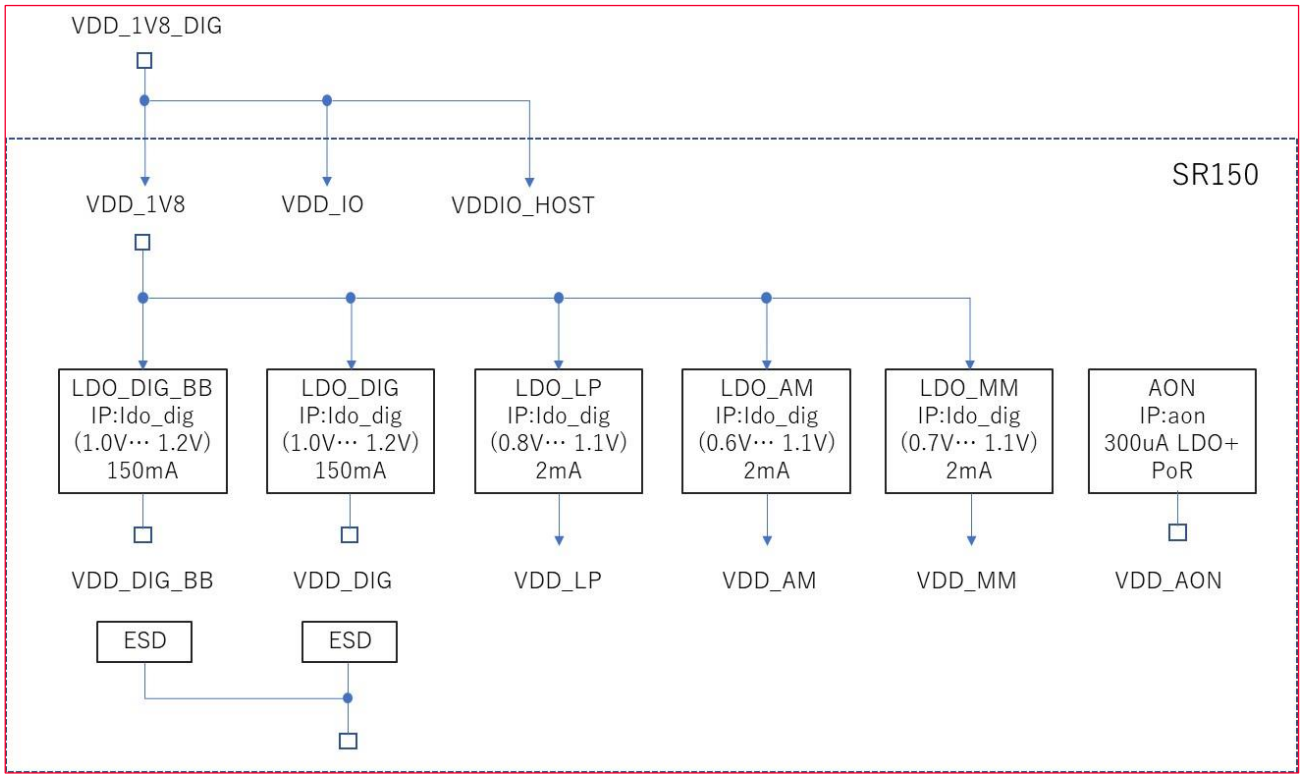
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10.4 Power Management Block

The Power management unit of SR150 in this module generates the following internal supplies required by SR150 system out of VDD_1V8 input supply voltage (VDD_1V8 supplied by VDD_1V8_DIG pin of this module):

- **VDD_AON**: Digital output supply voltage for Always ON logic.
- **VDD_LP**: Digital output supply voltage for LP Logic.
- **VDD_AM**: Digital output supply voltage for retaining ARM Subsystem memories.
- **VDD_MM**: Digital output supply voltage for retaining BB Subsystem memories.
- **VDD_DIG**: Digital output supply voltage for powering BB Subsystem.
- **VDD_DIG_BB**: Digital output supply voltage for powering BB Subsystem.

Figure 7: Power Management Block



10.5 Power Timing Diagrams

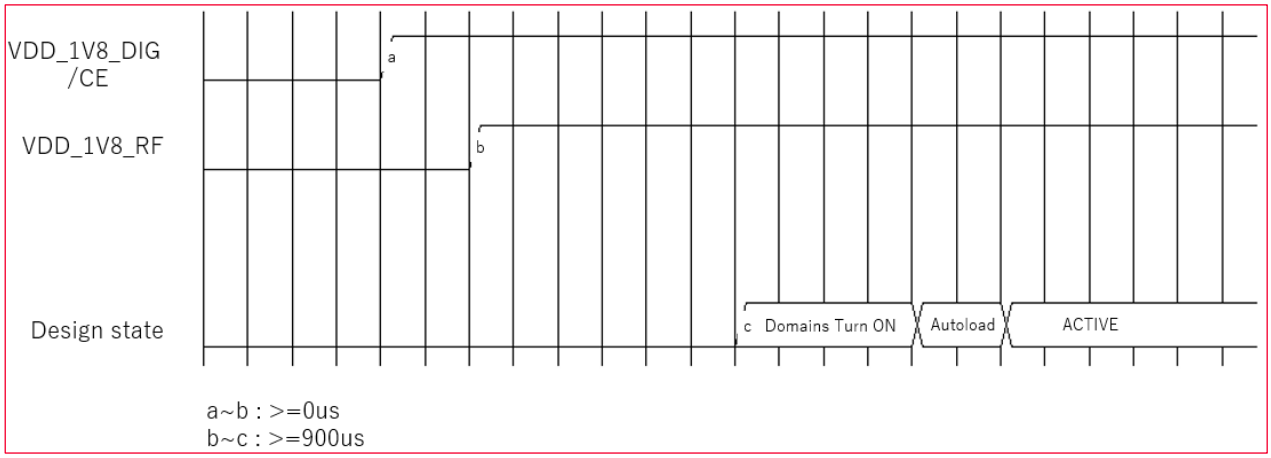
PMU of SR150 subsystem has a main power up sequence that requires VDD_1V8_DIG, VDD_1V8_RF and CE (CHIPENABLE) to be orderly powered to boot-up.

In all cases, host communication with SR150 will only be possible after one defined amount of time from the different supply sequence setup and CE at rising edge.

High level boot sequence is indicated below, power supply start-up time should be followed. CE pin must be set to high only when VDD_IO and VDDIO_HOST are high. Then the CE pin level will be taken into account from autoload phase.

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Figure 8: Power Timing Diagram

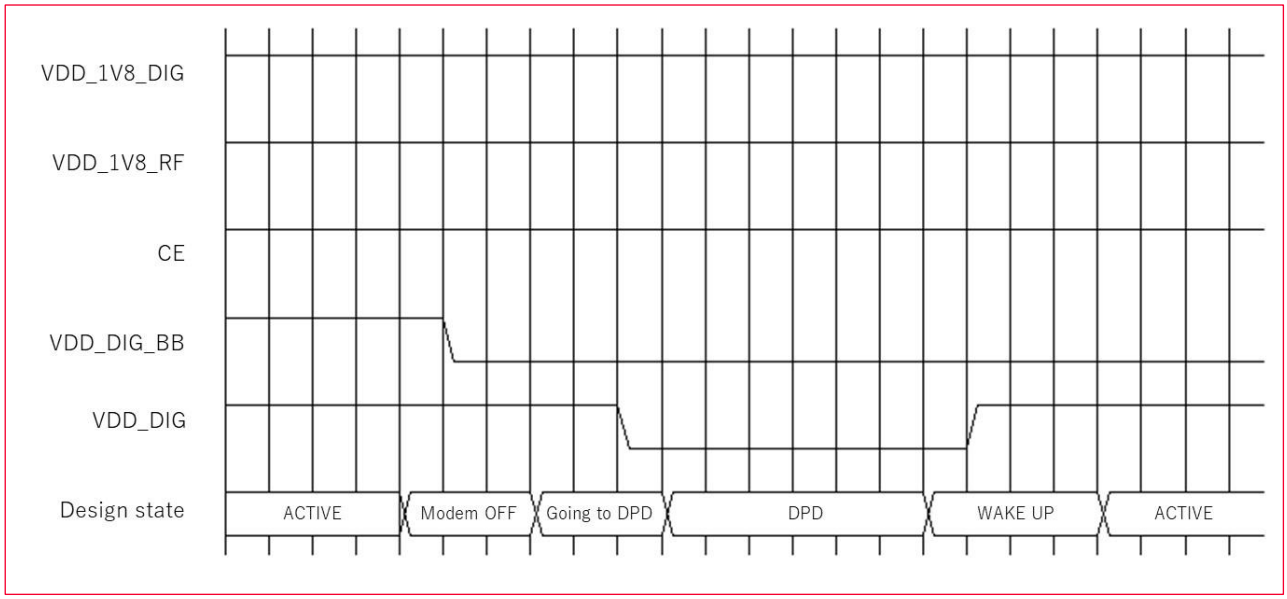


CE pin must be set to high only VDD_1V8_DIG is high.

10.5.1 Deep Power-Down (DPD) Sequence

In DPD Lowe power mode, CE needs to be High all the time, Modem domain needs to be turned OFF before decided to go to DPD. All IOs are retained to same state before going to DPD. All high frequency clocks.

Figure 9: Deep Power-Down (DPD) Sequence

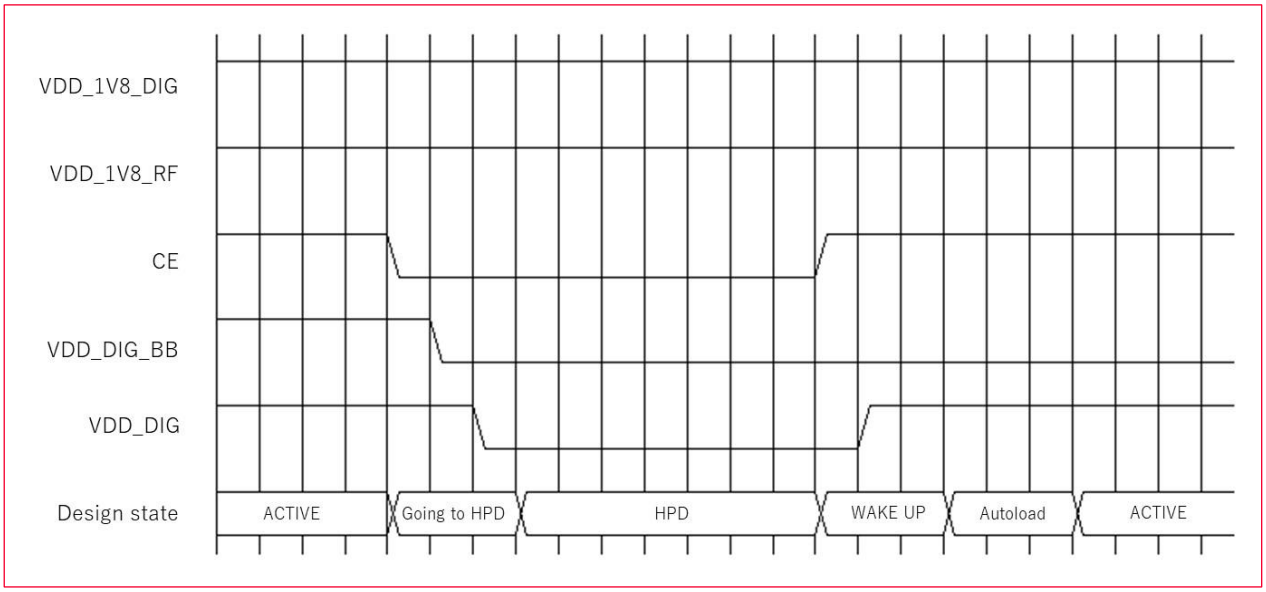


10.5.2 Hard Power-Down (HPD) Sequence

HPD is the lowest Power mode where only SR150 AON domain is ON and rest of the power domains of SR150s are in OFF state. (Note : note the VDD_1V8_RF supplies connected to internal RF switch and it also causing leak current. The dominant current consumption factors in HPD mode are current consumption of SR150 HPD state and leakage current of RF switch). HPD state can be entered or exited only by CE pin.

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Figure 10: Hard Power-Down (HPD) Sequence



11 Host Interface (SPI)

The SR150 supports SPI-bus Master/Slave interface, up to 16.66 Mbits/s.

11.1 SPI-Bus Configuration Options

The operation mode of the SPI-bus is shown in **Table 14**, CPHA refers to the Clock Phase option and CPOL refers to the Clock Polarity. Default setting of CHPA/CPOL settings are CHPA = 0, CPOL = 0.

Table 14: Operation Mode of SPI Bus

Connection
CPHA switch: Clock Phase: defines the sampling edge of MOSI data • CPHA = 1: data are sampled on MOSI on the even clock edges of SCK after NSS goes low • CPHA = 0: data are sampled on MOSI on the odd clock edges of SCK after NSS goes low
CPOL switch: Clock Polarity • CPOL = 0: the clock is idle low and the first valid edge of SCK will be a rising one • CPOL = 1: the clock is idle high and the first valid edge of SCK will be a falling one

The SPI-bus interface shares the pins with the other host interfaces that are supported by SR150. When SPI-bus is configured the functionality of the interface pins is as described in **Table 15**.

Table 15: Functionality of SPI Interface Pins For SPI-Bus Configuration

Pin name	Functionality
Host_1	SCK (Serial input Clock)
Host_2	NSS (Not Slave Select)
Host_3	MOSI (Master Out Slave In)
Host_4	MISO (Master In Slave Out)

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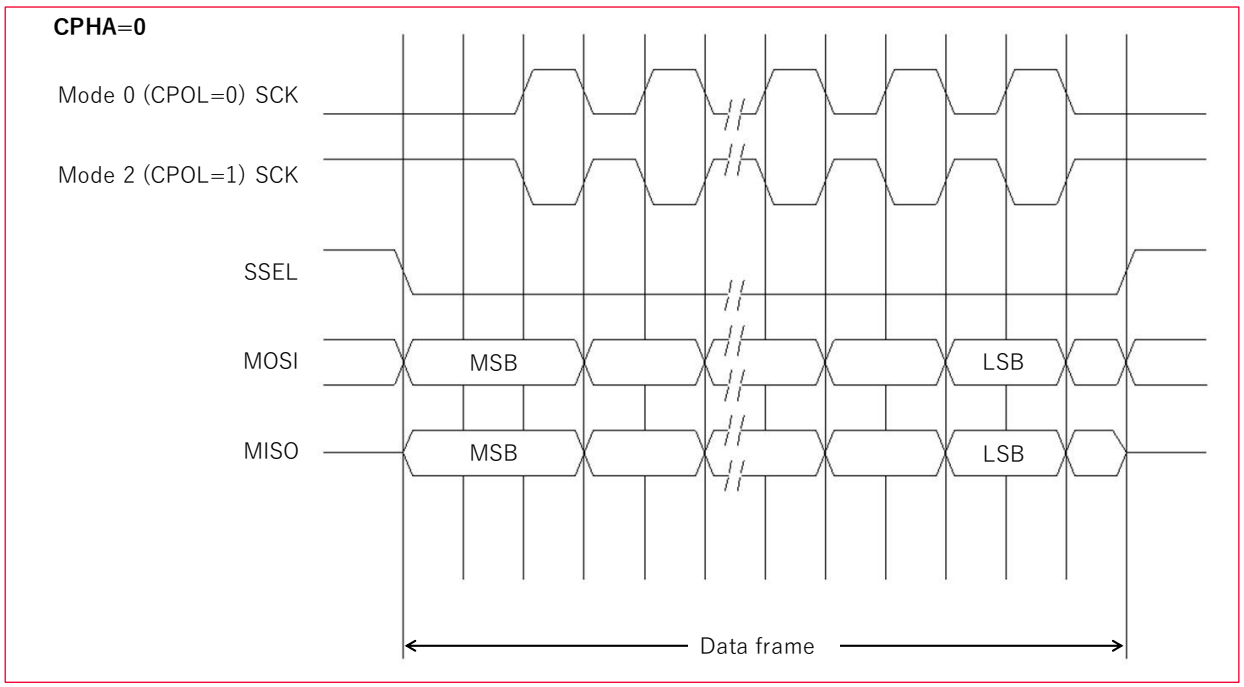
11.1.1 SPI-Bus Functional Description

When a master device transmits data to the SR150 via the MOSI line, the SR150 responds by sending data to the master device via the MISO line. This implies full-duplex transmission with both, data out and data in synchronized with the same clock signal.

SR150 starts sampling when receiving a logic low at pins NSS Host_2 pin and the clock at input pin SHOST_1. Thus, SR150 is synchronized with the master. Data from the master is received serially at the slave MOSI line and loaded in the 8-bit shift register. After the 8bit shrift register is loaded, its data is transferred to the read buffer. During a write cycle, data is written into the shift register, then the SR150 waits for a clock train form the master to shift the data out on the MISO line.

Both master and slave devices must operate with the same timing. The master device always places data on the MOSI line a half cycle before the clock edge SCK, for the slave device to latch the data.

Figure 11: SR150 SPI Data Frame (CPHA = 0)



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Figure 12: SR150 SPI Data Frame (CPHA = 1)

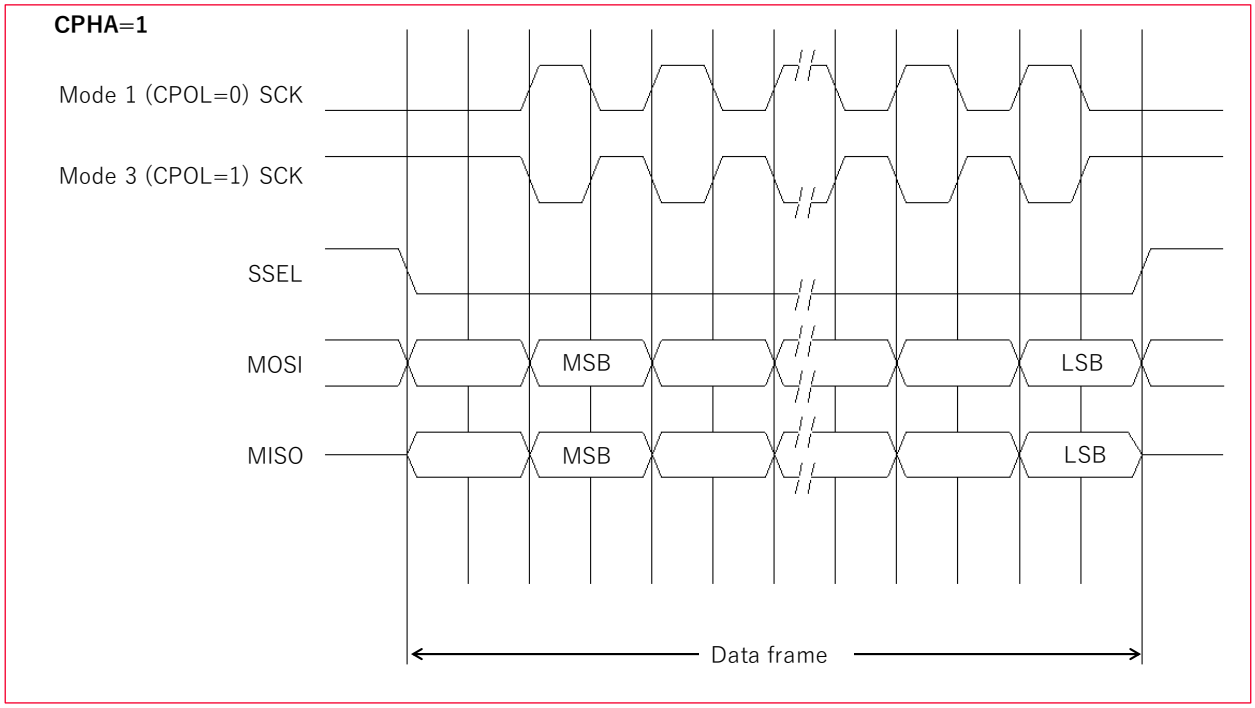
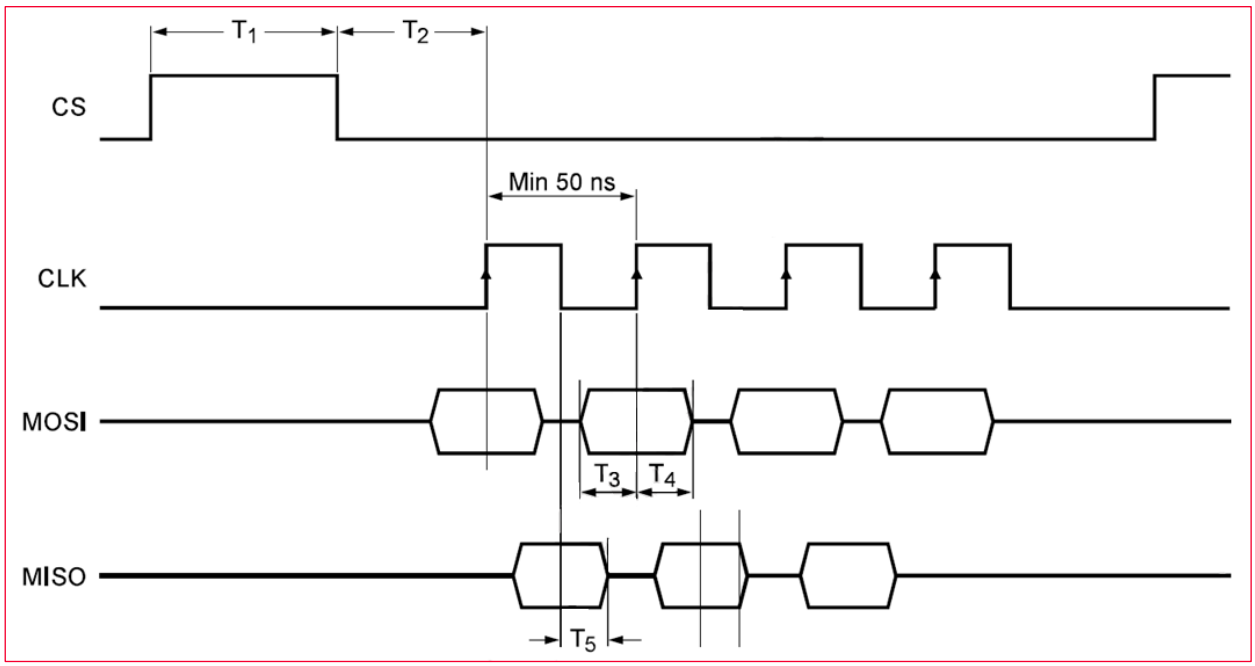


Figure 13: SPI-bus timings



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Table 16: SPI-bus slave timing specification

Timing	Max	Typ	Min	Unit
T1	–	–	–	Minimum CS high level between 2 frames transfer
T2	–	–	–	CS_low to first clock rising front
T3	8 ns	–	–	MOSI T_{setup} time
T4	–	–	1 ns	MOSI T_{hold} time
T5	12 ns	–	2.75 ns	MISO output valid time

12 DC/RF Characteristics

Conditions: 25 ˚C, VDD_1V8_DIG = 1.8V, VDD_1V8_RF = 1.8V, calibrated value in the OTP applied.

12.1 Current Consumption

Table 17 describes the current consumption.

Table 17: Current consumption

Items	Minimum	Typical	Maximum	Unit
Hard Power Down State (HPD)		24	80	uA
DPD State retention mode		50		uA
Active State, CPU idle		15		mA
Active State, Active State, signed and encrypted FW download		18		mA
Active State, UWB time base maintenance and frame processing during active ranging		55		mA
Peak current TX/RX				
TX @-41.3 dBm/MHz		160	240	mA
Dual Rx		315	390	mA

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12.2 Reference Data

These specs are defined at the module pin out.

The reference data specification is shown in **Table 18**.

Table 18: Reference Data

Items	Conditions	Minimum	Typical	Maximum	Unit
Frequency Range	Ch5, Ch9 support	6.24		8.24	GHz
Data Rate	Supported data rate	6.81	6.81	31.2	Mbps
Output power[1]	Power density	-47		-41.3	dBm/MHz
Rated Output power (peak)	Power density			0	dBm/50Mhz
Pulse Repetition Rate			62.4		MHz
			124.8		MHz
			249.6		MHz
Rx Sensitivity	6.81 Mbps		-92	-85	dBm
	27.24 Mbps		-88	-80	dBm
	31.2 Mbps		-88	-80	dBm
Maximum Input Level	CW signal or other UWB, no damage			7	dBm
Carrier Frequency Offset[1]		-15		15	ppm

12.3 Calibration Value in OTP

There is OTP (One-time programable ROM) in the SR150, and calibration value is stored in the OTP.

Calibration performed in the Murata factory to all of product individually, calibration reference point defined at the module pin.

Three calibration values are stored in the OTP as below.

Table 19: Functionality of SPI Interface Pins For SPI-Bus Configuration

Item	Length
TX_POWER for channel 5	4 bytes
TX_POWER for channel 9	4 bytes
RF_XTAL_CAP (Common for all channels)	3 bytes

These calibration values need to be applied after boot-up or wake up from HPD.
Please refer to the application note to apply these values.
Application note : MCM-21F-0147_Type2BP-Applying_Calibration_Values

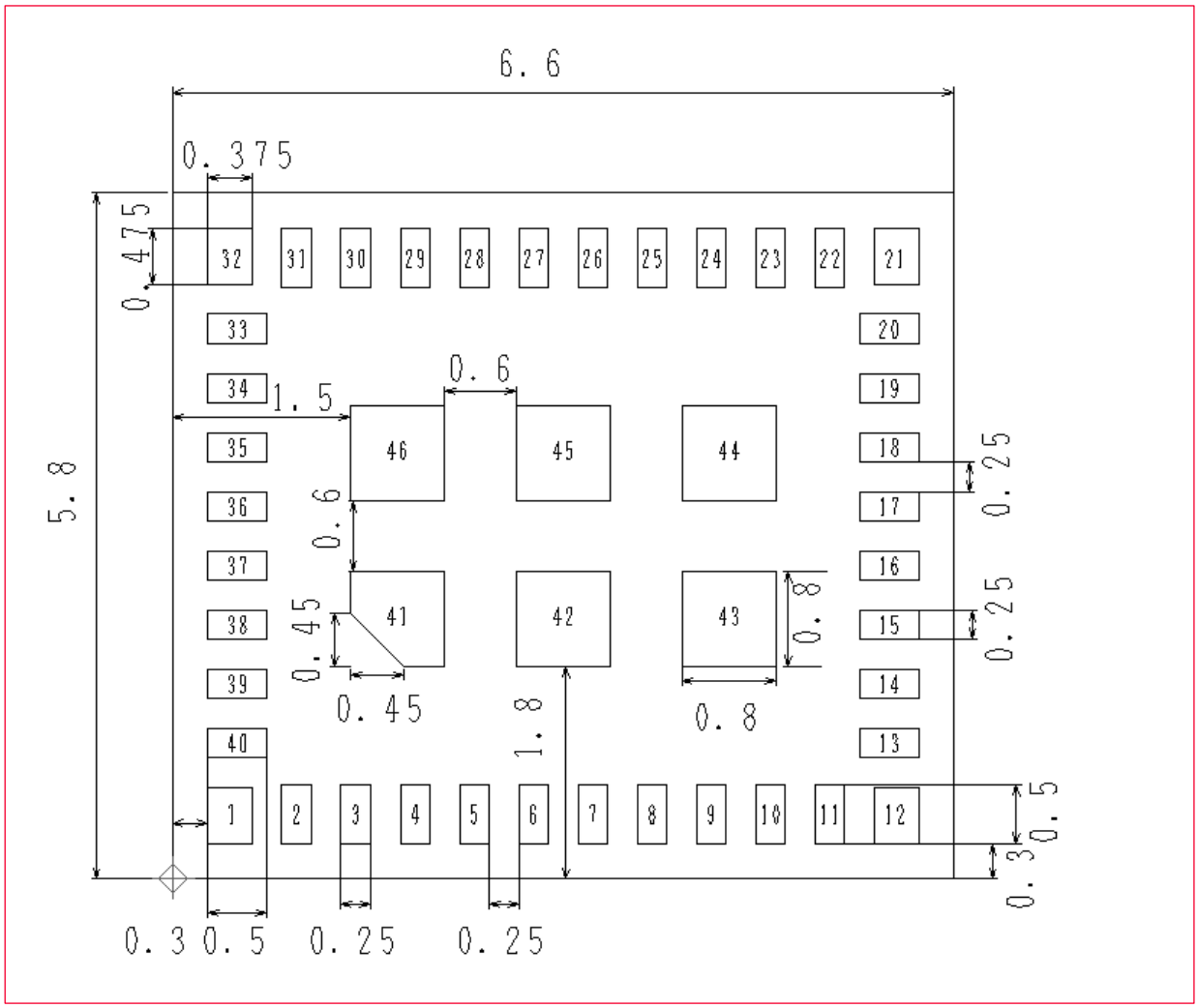
[1] Spec when using calibration value in the OTP.

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13 Recommended Land Pattern

The recommended land pattern (top-view) is shown in **Figure 14**.

Figure 14: Land Pattern (Top-View) in Millimeters

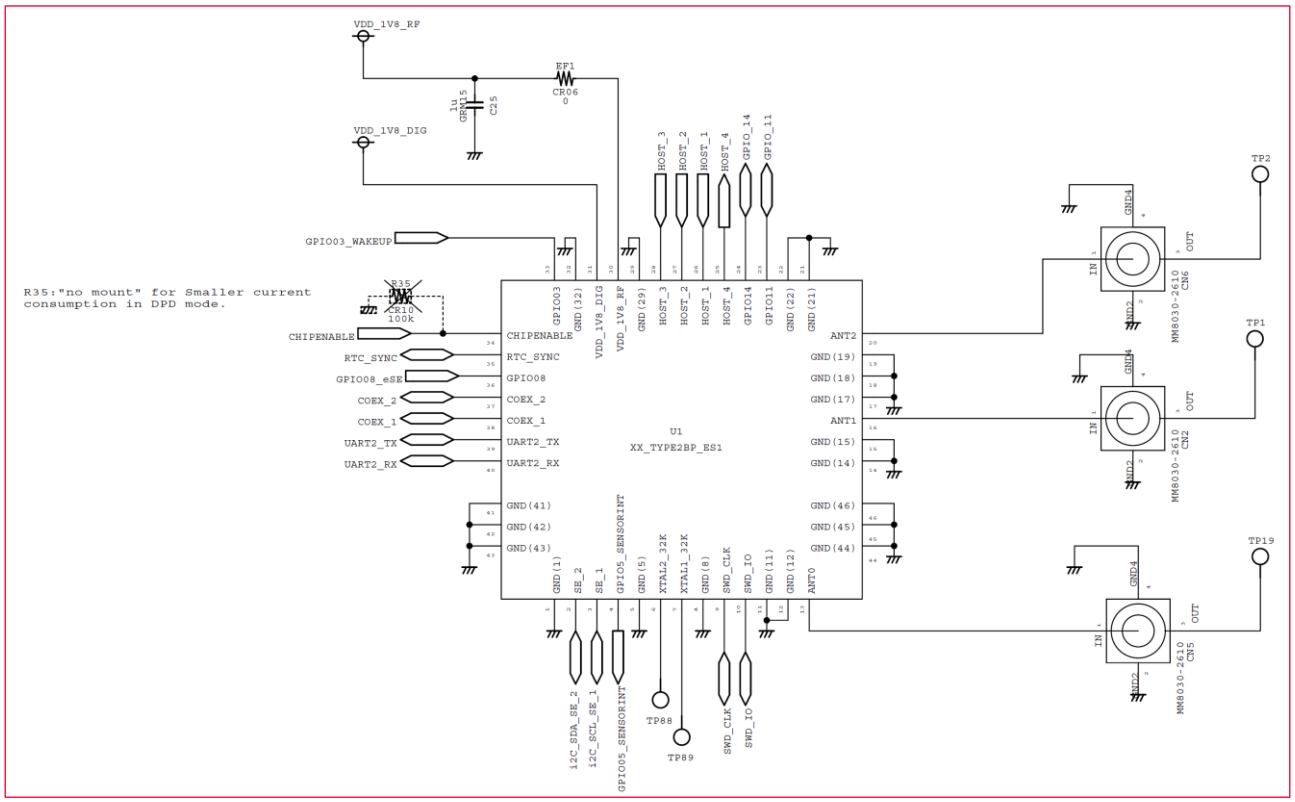


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14 Reference Circuit

Figure 15 shows the reference circuit.

Figure 15: Reference Circuit



15 Tape and Reel Packing

This section provides the general specifications for tape and reel packing.

15.1 Dimensions of Tape (Plastic Tape)

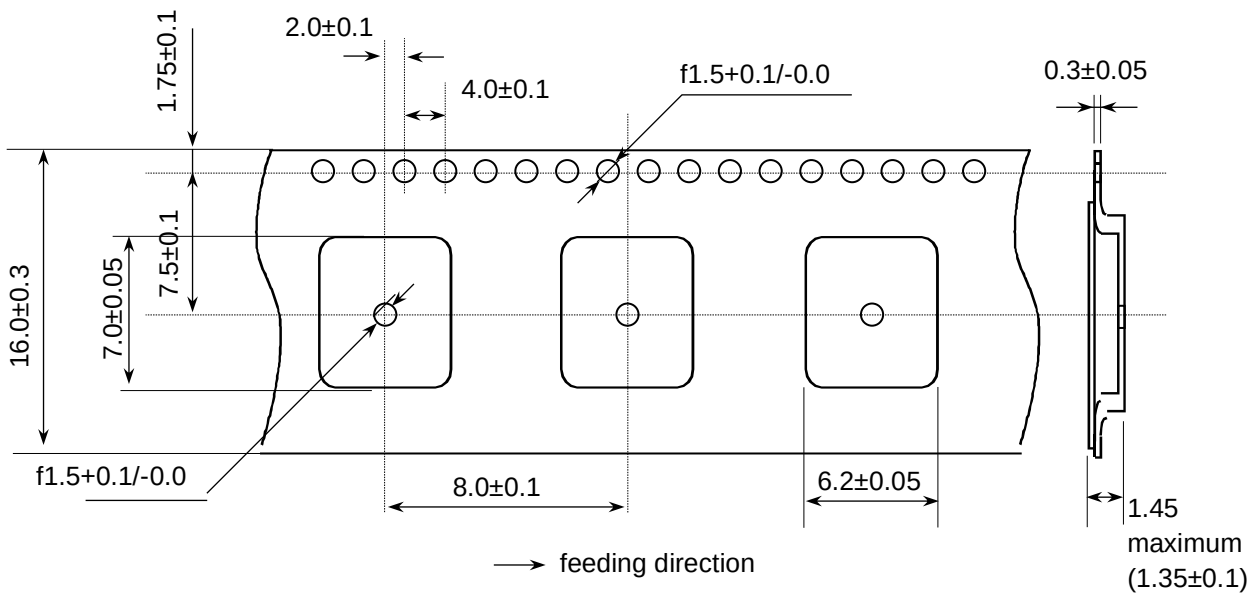
The dimension of the tape is as follows:

- The corner and ridge radiuses (R) of inside cavity are 0.3 mm maximum.
- Cumulative tolerance of 10 pitches of the sprocket hole is +/-0.15 mm.
- Measuring of cavity positioning is based on cavity center in accordance with JIS/IES standard.

Figure 16 is a graphical representation of the tape dimension (plastic tape).

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Figure 16: Dimension of Tape (Plastic Tape)



(Unit: mm)

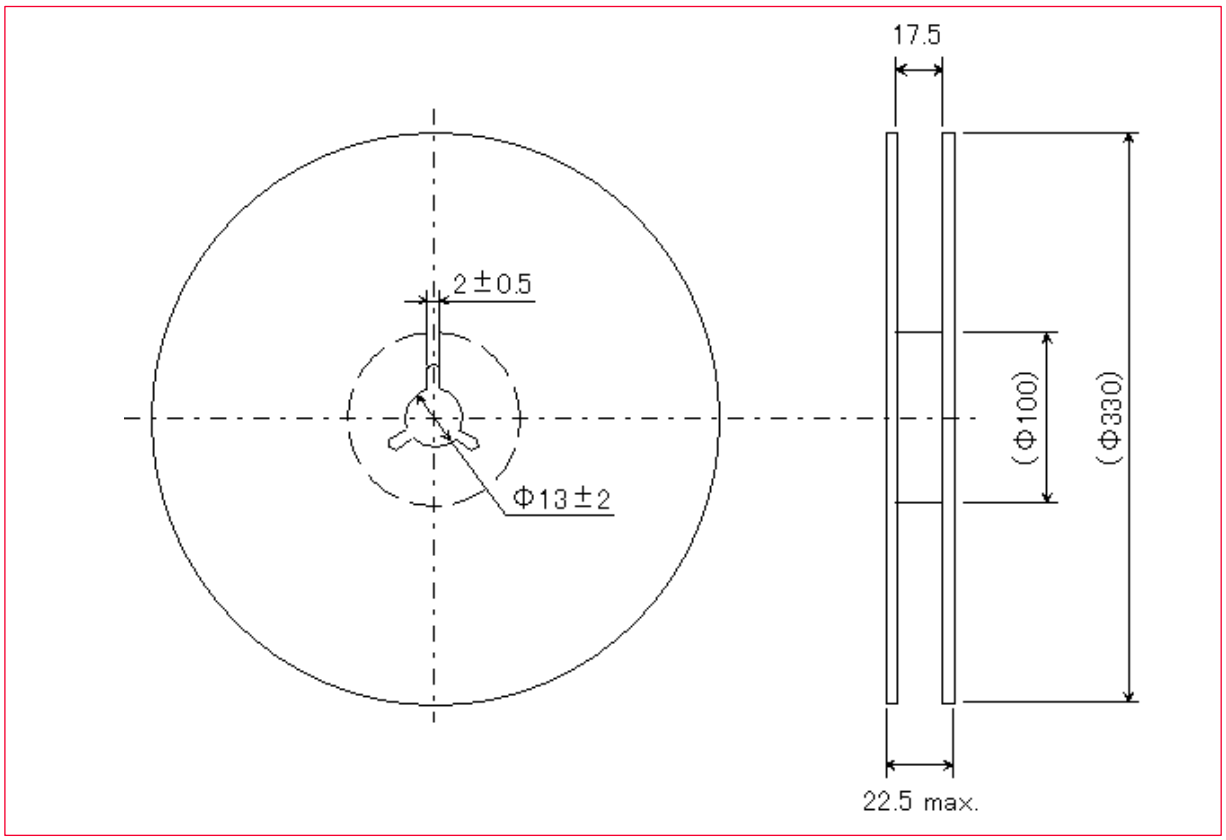
1. The corner and ridge radiuses (R) of the inside cavity are 0.3 millimeters maximum.
2. Cumulative tolerance of 10 pitches of the sprocket hole is +/-0.15 millimeters.
3. Measuring of cavity positioning is based on cavity center in accordance with JIS/IES standard.

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15.2 Dimension of Reel

Figure 17 shows the dimensions of reel in millimeters.

Figure 17: Dimensions of Reel (Unit: Millimeters)

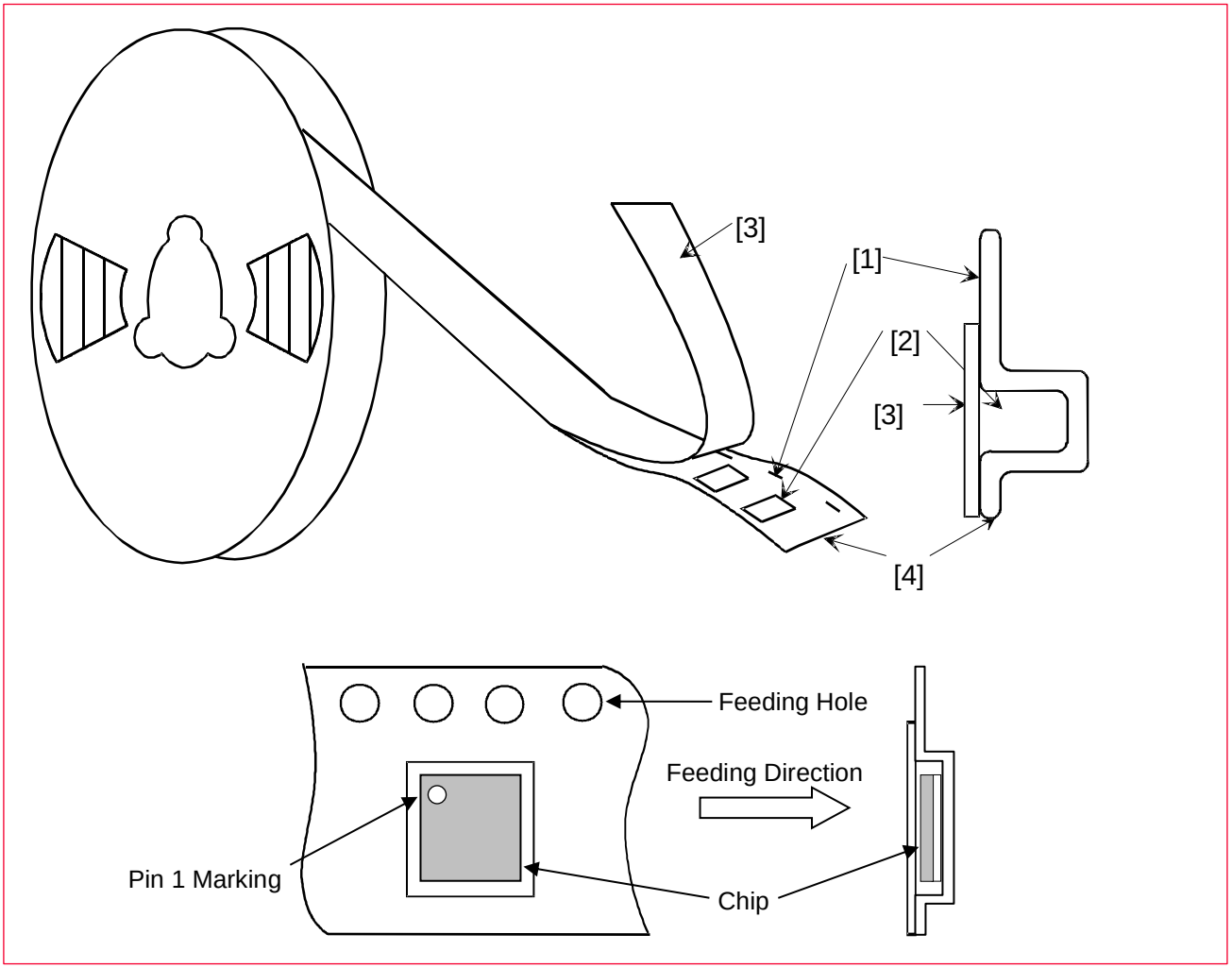


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15.3 Taping Diagrams

Figure 18 show the taping diagrams.

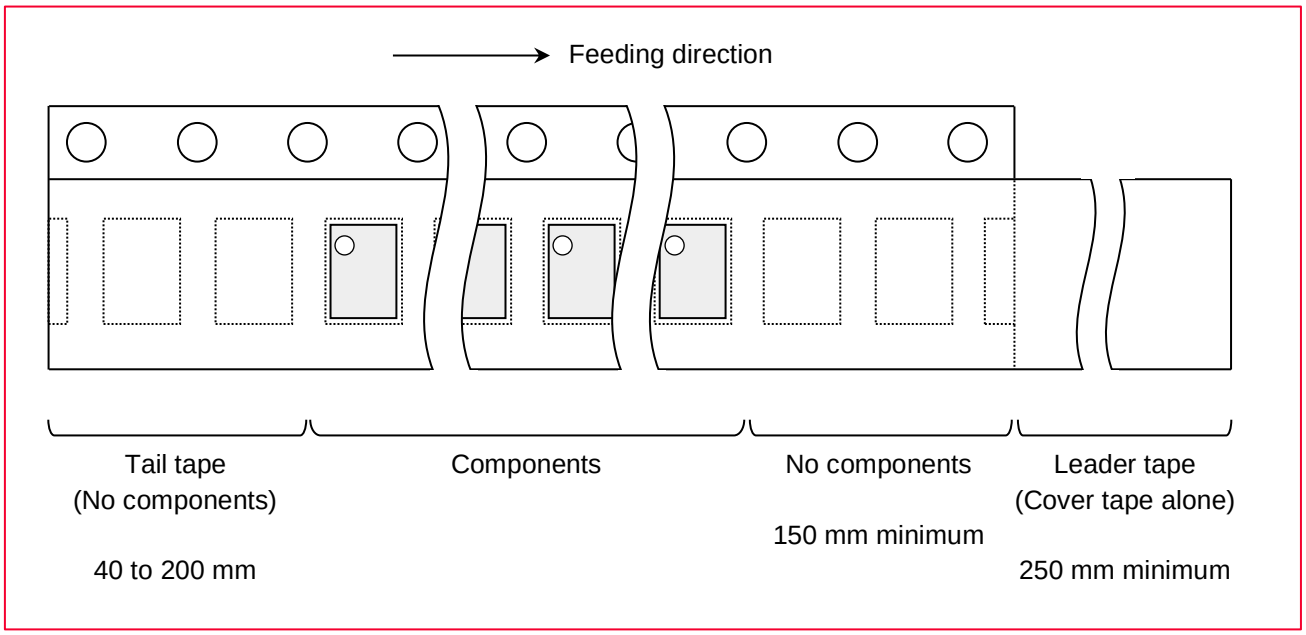
Figure 18: Taping Diagrams



Mark	Description
1	Feeding hole. As specified in Dimensions of Tape (Plastic tape).
2	Hole for Chip. As specified in Dimensions of Tape (Plastic tape).
3	Cover tape. 62 µm in thickness.
4	Base tape. As specified in Dimensions of Tape (Plastic tape).

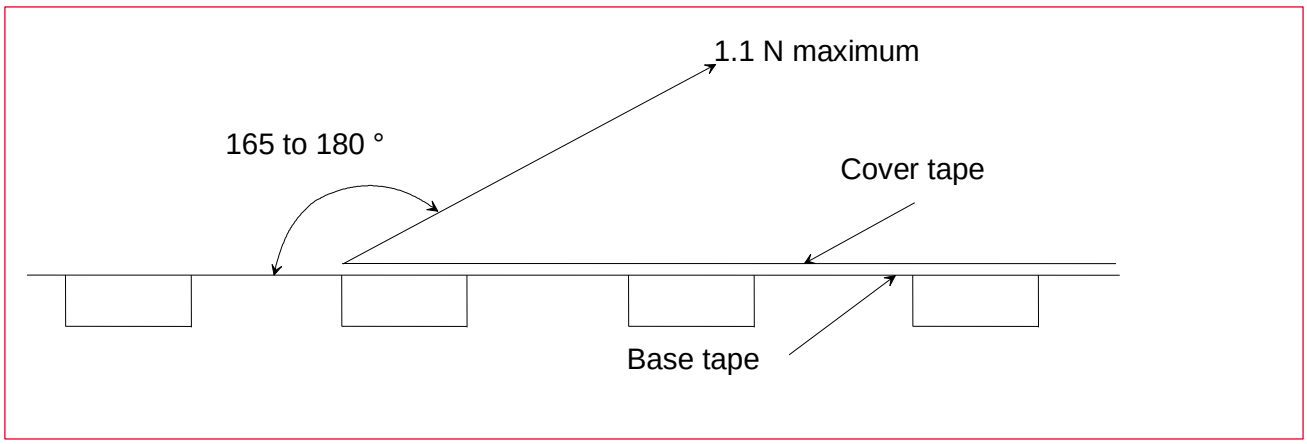
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Figure 19: Leader and Tail Tape



- The tape for chips is wound clockwise, the feeding holes to the right side as the tape is pulled toward the user.
- The cover tape and base tape are not adhered at no components area for 250 mm minimum.
- Tear off strength against pulling of cover tape: 5N minimum.
- Packaging unit: 1000 pcs/reel
- Material :
  - Base tape: Plastic
  - Real: Plastic
  - Cover tape, cavity tape and reel are made the anti-static processing.
- Peeling off force: 1.1N maximum in the direction of peeling as shown in **Figure 20**.

Figure 20: Peeling Force

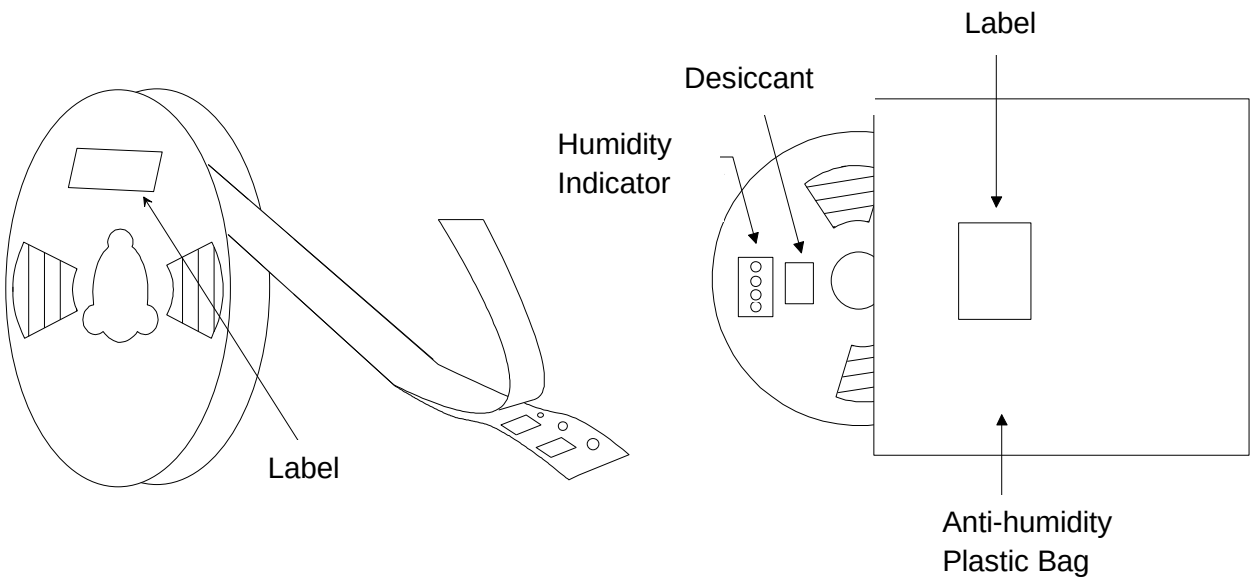


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15.4 Packing (Humidity Proof Packaging)

Figure 21 shows the humidity proof packaging.

Figure 21: Packaging



Tape and reel must be sealed with the anti-humidity plastic bag. The bag contains the desiccant and the humidity indicator.

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16 Radio Regulatory certification by Country for LBUA0VG2BP

This section contains the following country/region specific information:

- FCC
- ISED
- Japan

16.1 FCC

FCC ID: VPYLB2BP

Since this module is not sold to general end users directly, there is no user manual of module. For the details about this module, please refer to the specification sheet of module. This module should be installed in the host device according to the interface specification (installation procedure).

●Warning;

CFR §15.521(a) notice

This module may not be employed for the operation of toys. Operation onboard aircraft, ship or satellite is prohibited.

CFR §15.519 a(2) notice

The use of antennas mounted on outdoor structures, e.g., antennas mounted on the outside of a building or on a telephone pole, or any fixed outdoors infrastructure is prohibited. Antennas may be mounted only on the handheld UWB device.

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

This device complies with below part 15 of FCC Rules.
Part 15 Subpart F

The modular transmitter is only FCC authorized for the specific rule parts (i.e., FCC transmitter rules) listed on the grant, and the host product manufacturer is responsible for compliance to any other FCC rules that apply to the host not covered by the modular transmitter grant of certification. The final host product still requires Part 15 Subpart B compliance testing with the modular transmitter installed.

The OEM integrator is responsible for ensuring that the end-user has no manual instruction to remove or install module, this module has been evaluated stand alone to meet portable use without restriction, however, if a host product also contains other transmitter(s) and antenna(s), necessary test or evaluation needs to be performed in order to meet the requirement.

Antenna Change Notice to Host manufacturer:

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If you desire to increase antenna gain and either change antenna type or use same antenna type certified, a Class II permissive change application is required to be filed by us, or you (host manufacturer) can take responsibility through the change in FCC ID (new application) procedure followed by a Class II permissive change application.

This module needs to supply a regulated voltage from the host device.

- VDD_1V8_DIG: 1.71~1.98 V
- VDD_1V8_RF: 1.71~1.98 V

Since there is no space which indicates FCC ID on this module, FCC ID is indicated in a manual.

If the FCC ID is not visible when the module is installed inside another device,

then the module is installed must also display a label referring to the enclosed module.

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the end user's manual of the end product which integrates this module.

The end user manual shall include all required regulatory information/warning as shown in User manual.

●The following statements must be described on the user manual of the host device of this module;

Contains Transmitter Module FCC ID: VPYLB2BP	or	Contains FCC ID: VPYLB2BP

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) This device must accept any interference received, including interference that may cause undesired operation.

If it is difficult to describe this statement on the host product due to the size, please describe in the User's manual.

FCC CAUTION

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

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16.2 ISED

Model Name: LBUA0VG2BP

IC Number: 772C-LB2BP

Since this module is not sold to general end users directly, there is no user manual of module.
For the details about this module, please refer to the specification sheet of module.
This module should be installed in the host device according to the interface specification (installation procedure).

●The following information must be indicated on the host device of this module.

Contains IC: 772C-LB2BP

●The following statements must be described on the user manual of the host device of this module;

This device complies with Industry Canada's applicable license-exempt RSSs. Operation is subject to the following two conditions: 1. This device may not cause interference; and 2. This device must accept any interference, including interference that may cause undesired operation of the device.
Le présent appareil est conforme aux CNR d' Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes : 1. l'appareil ne doit pas produire de brouillage; 2. l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

If it is difficult to describe this statement on the host product due to the size, please describe in the User's manual.

●Warning;

CFR §15.521(a) notice This module may not be employed for the operation of toys. Operation onboard aircraft, ship or satellite is prohibited. CFR §15.519 a(2) notice The use of antennas mounted on outdoor structures, e.g., antennas mounted on the outside of a building or on a telephone pole, or any fixed outdoors infrastructure is prohibited. Antennas may be mounted only on the handheld UWB device.

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If the antenna of the end product is removed, please describe the follow warning on the manual of the end product which contains this module.

This radio transmitter (IC Number: 772C-LB2BP) identify the device by certification number or model number if Category II) has been approved by Industry Canada to operate with the antenna types listed below with the maximum permissible gain indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device. *Ch.5 : MTD-ANT-027-1-A_UWB_ANT18 mm Patch antenna Gain: +0.9 dBi *Ch.9 : MTD-ANT-027-1-A_UWB_ANT18 mm Patch antenna Gain: +2.7 dBi
Le présent émetteur radio (IC Number : 772C-LB2BP) a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés ci dessous et ayant un gain admissible maximal. Les types d'antenne non inclus dans cette liste, et dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur. Type d'antenne *Ch.5 : MTD-ANT-027-1-A_UWB_ANT18 mm Patch antenna Gain: +0.9 dBi *Ch.9 : MTD-ANT-027-1-A_UWB_ANT18 mm Patch antenna Gain: +2.7 dBi

● The following statements must be described on the user manual of the host device of this module;

Data transmission is always initiated by software, which is the passed down through the MAC, through the digital and analog baseband, and finally to the RF chip. Several special packets are initiated by the MAC. These are the only ways the digital baseband portion will turn on the RF transmitter, which it then turns off at the end of the packet. Therefore, the transmitter will be on only while one of the aforementioned packets is being transmitted. In other words, this device automatically discontinue transmission in case of either absence of information to transmit or operational failure.
La transmission des données est toujours initiée par le logiciel, puis les données sont transmises par l'intermédiaire du MAC, par la bande de base numérique et analogique et, enfin, à la puce RF. Plusieurs paquets spéciaux sont initiés par le MAC. Ce sont les seuls moyens pour qu'une partie de la bande de base numérique active l'émetteur RF, puis désactive celui-ci à la fin du paquet. En conséquence, l'émetteur reste uniquement activé lors de la transmission d'un des paquets susmentionnés. En d'autres termes, ce dispositif interrompt automatiquement toute transmission en cas d'absence d'information à transmettre ou de défaillance.

If it is difficult to describe this statement on the host product due to the size, please describe in the User's manual.

16.2.1 RF Power

Table 20 show the RF Power parameters for UWB.

Table 20: RF Power – UWB (ISED)

Modulation	Channel	Maximum Tune Up Tolerance	
		Peak Power	Average Power
BPM-BPSK	5, 9	0 dBm/50MHz	-41.3 dBm/MHz

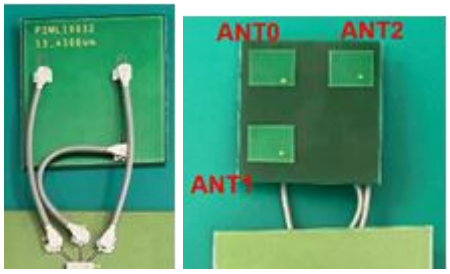
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Modulation	Channel	Maximum Tune Up Tolerance	
		Peak Power	Average Power
BPSK	5, 9	0 dBm/50MHz	-41.3 dBm/MHz

16.2.2 Antenna

Table 21 describes the certified antenna information.

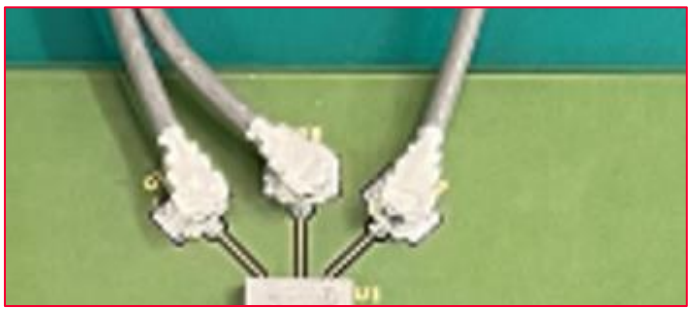
Table 21: Antenna (ISED)

Maker	Supported Antenna				
	P/N	Type	Gain (dBi)		Appearance
			5 ch	9 ch	
Murata	MTD-ANT-027-1-A_UWB_ANT18 mm	Patch	0.9	2.7	

- Please perform the antenna design that followed the specifications of the antenna.
- 50Ω line (microstrip line pattern).

Certification tests are conducted in the patterns shown in **Figure 22**.

Figure 22: Certification Test Patterns



The 50Ω microstrip line needs to be copied when module is installed in the End product.

Murata provides set makers with Gerber data or something similar.

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16.3 Japan

Classification of Specified Radio Equipment: Article 2 paragraph1 item (47)-3

Application Model Name: LBUA0VG2BP

Certification Number: 003-220111

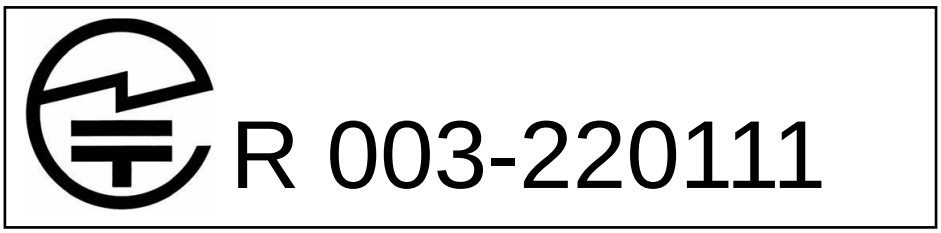
This module has received "CERTIFICATION for TYPE CERTIFICATION" under the Japanese Radio Law.

It is recommended that the indication of (1) or (2) below is described on the product incorporating this module in Japanese. If there is any problem with the indication of (1) or (2) on the product, we recommend indicating (1) or (2) in the user manual or on the package of the product incorporating this module, or electronic display on the product. In the case of the electronic display, it is necessary to describe "using the electronic display" + "how to reach to below indication" in the user manual of the product.

(1)

本製品は、電波法に基づく工事設計認証(認証番号:003-220111)を受けた特定無線設備を内蔵しています。

(2)



English Translation

(1)

This product incorporates specified radio equipment that has received CERTIFICATION for TYPE CERTIFICATION (certification number: 003-220111) based on the Japan Radio Act.

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17 Notice

17.1 Storage Conditions

- Please use this product within 6 months after receipt.
- The product shall be stored without opening the packing under the ambient temperature from 5 to 35 °C and humidity from 20 ~ 70 %RH (Packing materials, in particular, may be deformed at the temperature over 40 °C).
- The product left more than 6 months after reception; it needs to be confirmed the solderability before used.
- The product must be stored in noncorrosive gas (Cl_2, NH_3, SO_2, NO_X, etc.).
- Any excess mechanical shock including, but not limited to, sticking the packing materials by sharp object and dropping the product, must not be applied in order not to damage the packing materials.
- This product is applicable to MSL3 (Based on IPC/JEDEC J-STD-020)
- After the packing opened, the product must be stored at ≤30 °C / <60 %RH and the product should be used within 168 hours after opening.
- When the color of the indicator in the packing changed, the product shall be baked before soldering.
- Baking condition: 125 +5/-0 °C, 24 hours, 1 time
- The products must be baked on the heat-resistant tray because the material (Base Tape, Reel Tape and Cover Tape) is not heat-resistant.

17.2 Handling Conditions

- Be careful in handling or transporting products because excessive stress or mechanical shock may break products.
- Handle with care if products may have cracks or damages on their terminals. If there is any such damage, the characteristics of products may change. Do not touch products with bare hands that may result in poor solder ability and destroy by static electrical charge.

17.3 Standard PCB Design (Land Pattern and Dimensions)

- All the ground terminals should be connected to the ground patterns. Furthermore, the ground pattern should be provided between IN and OUT terminals. Please refer to the specifications for the standard land dimensions.
- The recommended land pattern and dimensions is as Murata's standard. The characteristics of products may vary depending on the pattern drawing method, grounding method, land dimensions, land forming method of the NC terminals and the PCB material and thickness. Therefore, be sure to verify the characteristics in the actual set. When using non-standard lands, contact Murata beforehand.

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17.4 Notice for Chip Placer

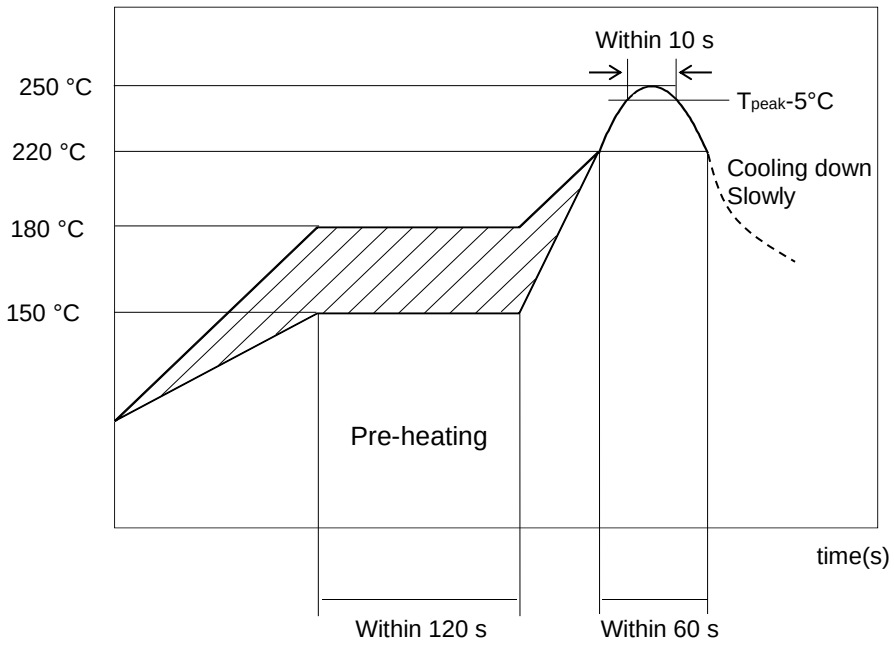
When placing products on the PCB, products may be stressed and broken by uneven forces from a worn-out chucking locating claw or a suction nozzle. To prevent products from damages, be sure to follow the specifications for the maintenance of the chip placer being used. For the positioning of products on the PCB, be aware that mechanical chucking may damage products.

17.5 Soldering Conditions

The recommendation conditions of soldering are as in the following figure.

Soldering must be carried out by the above-mentioned conditions to prevent products from damage. Set up the highest temperature of reflow within 260 °C. Contact Murata before use if concerning other soldering conditions.

Figure 23: Reflow Soldering Standard Conditions (Example)



Please use the reflow within 2 times.

Use rosin type flux or weakly active flux with a chlorine content of 0.2 wt % or less.

17.6 Cleaning

Since this Product is Moisture Sensitive, any cleaning is not recommended. If any cleaning process is done the customer is responsible for any issues or failures caused by the cleaning process.

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17.7 Operational Environment Conditions

Products are designed to work for electronic products under normal environmental conditions (ambient temperature, humidity, and pressure). Therefore, products have no problems to be used under similar conditions to the above-mentioned. However, if products are used under the following circumstances, it may damage products and leakage of electricity and abnormal temperature may occur.

- In an atmosphere containing corrosive gas (Cl_2, NH_3, SO_X, NO_X etc.).
- In an atmosphere containing combustible and volatile gases.
- Dusty place.
- Direct sunlight place.
- Water splashing place.
- Humid place where water condenses.
- Freezing place.



If there are possibilities for products to be used under the preceding clause, consult with Murata before actual use.



Do not apply static electricity or excessive voltage while assembling and measuring, as it might be a cause of degradation or destruction to apply static electricity to products.

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18 Preconditions to Use Our Products

PLEASE READ THIS NOTICE BEFORE USING OUR PRODUCTS.

Please make sure that your product has been evaluated and confirmed from the aspect of the fitness for the specifications of our product when our product is mounted to your product.

All the items and parameters in this product specification/datasheet/catalog have been prescribed on the premise that our product is used for the purpose, under the condition and in the environment specified in this specification. You are requested not to use our product deviating from the condition and the environment specified in this specification.

Please note that the only warranty that we provide regarding the products is its conformance to the specifications provided herein. Accordingly, we shall not be responsible for any defects in products or equipment incorporating such products, which are caused under the conditions other than those specified in this specification.

WE HEREBY DISCLAIM ALL OTHER WARRANTIES REGARDING THE PRODUCTS, EXPRESS OR IMPLIED, INCLUDING WITHOUT LIMITATION ANY WARRANTY OF FITNESS FOR A PARTICULAR PURPOSE, THAT THEY ARE DEFECT-FREE, OR AGAINST INFRINGEMENT OF INTELLECTUAL PROPERTY RIGHTS.

You agree that you will use any and all software or program code (including but not limited to firmware and calibration parameters) we may provide or to be embedded into our product ("Software") provided that you use the Software bundled with our product. YOU AGREE THAT THE SOFTWARE SHALL BE PROVIDED TO YOU "AS IS" BASIS, MURATA MAKES NO REPRESENTATIONS OR WARRANTIES THAT THE SOFTWARE IS ERROR-FREE OR WILL OPERATE WITHOUT INTERRUPTION. AND MORE, MURATA MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED WITH RESPECT TO THE SOFTWARE. MURATA EXPRESSLY DISCLAIM ANY AND ALL WARRANTIES OR CONDITIONS OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE NOR THE WARRANTY OF TITLE OR NON-INFRINGEMENT OF INTELLECTUAL PROPERTY RIGHTS.

You shall indemnify and hold harmless us, our affiliates, and our licensor from and against any and all claims, costs, expenses and liabilities (including attorney's fees), which arise in connection with the using the Software.

The product shall not be used in any application listed below which requires especially high reliability for the prevention of such defect as may directly cause damage to the third party's life, body or property. You acknowledge and agree that, if you use our products in such applications, we will not be responsible for any failure to meet such requirements. Furthermore, YOU AGREE TO INDEMNIFY AND DEFEND US AND OUR AFFILIATES AGAINST ALL CLAIMS, DAMAGES, COSTS, AND EXPENSES THAT MAY BE INCURRED, INCLUDING WITHOUT LIMITATION, ATTORNEY FEES AND COSTS, DUE TO THE USE OF OUR PRODUCTS AND THE SOFTWARE IN SUCH APPLICATIONS.

- Aircraft equipment.
- Aerospace equipment.
- Undersea equipment.
- Power plant control equipment.
- Medical equipment.
- Traffic signal equipment.

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- Burning / explosion control equipment.
- Disaster prevention / crime prevention equipment.
- Transportation equipment (vehicles, trains, ships, elevator, etc.).
- Application of similar complexity and/ or reliability requirements to the applications listed in the above.

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Revision History

Revision Code	Date	Changed Item	Comment
	Nov 26, 2020	First Issue	
A	Aug 17, 2021	• 2 Key Features • 7.1 Pin Assignment • 7.2 Pin Description • 10.1 Power on sequence • 11 Host Interface (SPI) • 12 DC/RF Characteristics • 14. Tape and Reel Packing	• Updated • Updated • Updated • Added • Added • Updated • Updated
B	Jan 11, 2022	• 2 Key Features • 6. Dimensions, Marking and Terminal Configurations • 10. System power status and power sequence • 12 DC/RF Characteristics • 13. Recommended land pattern • 14. Reference Circuit	• Updated • Updated • Added/Updated • Updated • Added • Updated
C	Feb 04, 2022	• 12.3 Calibration data in OTP	• Updated
D	Oct 21, 2022	• 5.1 Radio Certification • Appendix	• Updated • Added
E	Nov 29, 2022	• Appendix	• Revised
F	Dec 09, 2022	• 10.1 System modes • 10.3 Power mode entry and exit conditions • 10.5 Power Timing diagrams	• Updated • Updated • Updated
G	Jan 10, 2023	• 3 Ordering Information	• Updated
H	Apr 20, 2023	• 14. Reference Circuit	• Updated
I	Aug 09, 2024	• Format	• Updated format
J	Jan 16, 2026	• 11 Host Interface (SPI)	• Updated

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