Structure Silicon Monolithic Integrated Circuit

Function Synchronous Rectifier Step-down DC-DC Converter

Product BU9006GUZ

Function
- Input voltage range 2.5V ~ 4.5V
- Output voltage range 0.95 V ~ 4.5V(REF input voltage range 0.5V~VIN)
- Current mode control
- Integrated output FET synchronous rectifier step-down DC-DC converter
- Switching frequency 2.0MHz typ.
- Maximum output current 750mA (Switching regulator part)
- Maximum output current 1200mA (Bypass switch part)
- PchFET on resistance at bypass mode: (70mohm) typ.
- 1.6mm x 1.6mm, t=0.4mm MAX, WLCSP

Absolute Maximum rating (Ta=25c)

Item	Symbol	Rating	Unit
Maximum input power supply voltage	VIN	7	V
Power dissipation	Pd	0.48(*1)	W
Operating temperature range	Topr	-35 ~ +85	C
Storage temperature range	Tstg	-55 ~ +125	C
Junction temperature	Tjmax	+125	C

(*1) When mounted on the specified PCB (50 mm x 58 mm). Deducted by 4.8m W/c when used over Ta=25c.

Operating range (Ta=25c)

Item	Symbol	Rating			Unit	Condition
		Min.	Typ.	Max.		
Power supply voltage	VIN	2.5	-	4.5	V	

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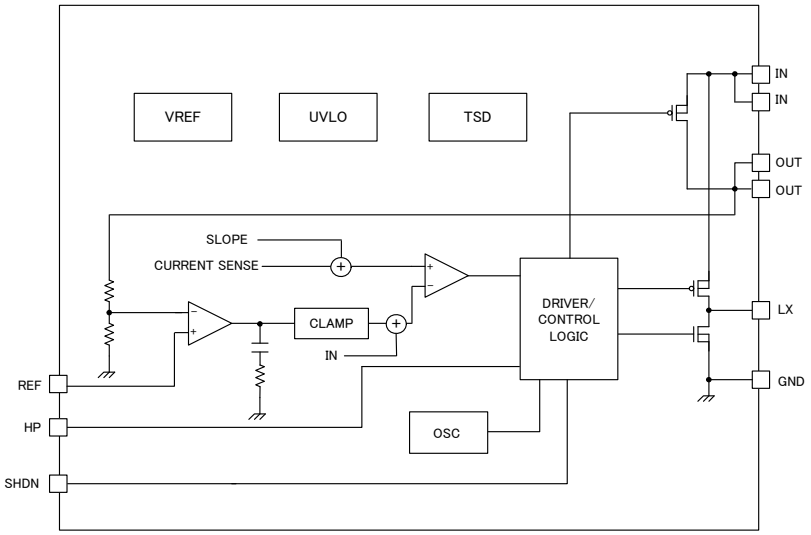
Electrical characteristics (unless otherwise specified IN=3.6[v], Ta=25[c])

Item		Symbol	Rating			Unit	Condition
			Min.	Typ.	Max.		
[Switching regulator part]							
Output voltage 1		VOUT1	1.15	1.20	1.25	V	REFIN=0.60 V
Output voltage 2		VOUT2	1.45	1.50	1.55	V	REFIN=0.75 V
[Soft start part]							
Soft start time		Tss	-	40	70	usec	
[Oscillator circuit]							
Switching frequency		fosc	1.5	2.0	2.5	MHz	
[Driver part]							
PchFET on resistance		RonP	-	300	500	mΩ	
NchFET on resistance		RonN	-	250	450	mΩ	
[Bypass switch part]							
On resistance		RBYP	-	70	120	mΩ	
[Error Amp part]							
REF input bias current		IAMPIN	-	0	500	nA	
[Control pin part]							
SHDN pin pull down resistor		RSHDN	0.5	1	2	MΩ	
SHDN pin control voltage	Operation	VSHDNH	1.4	-	VIN	V	
	Non operation	VSHDNL	0	-	0.4	V	
HP pin pull down resistor		RHP	0.5	1	2	MΩ	
HP pin control voltage	Operation	VHPH	1.4	-	VIN	V	
	Non operation	VHPL	0	-	0.4	V	
【UVLO】							
Release voltage threshold		Uvth	1.95	2.2	2.45	V	
Hysteresis		Uvhy	70	90	110	mV	
[Circuit current]							
Circuit current at shutdown		IIN	-	0	10	uA	SHDN=0V

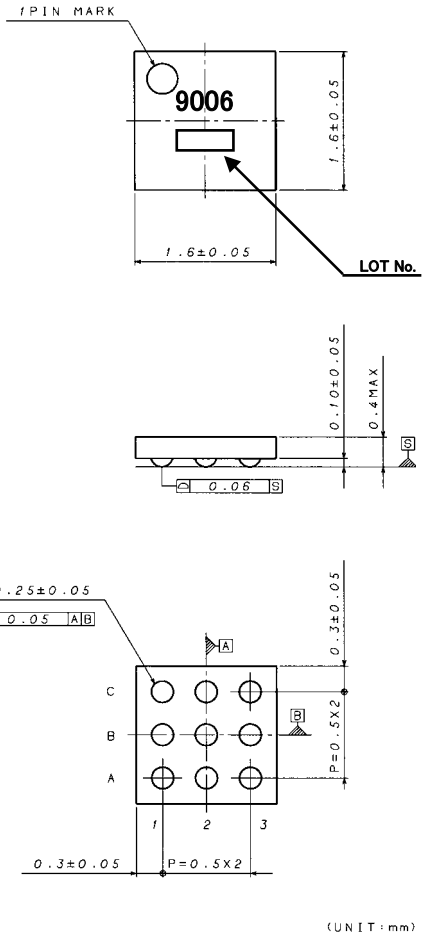
* No design for durability against radiation

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Block diagram



External dimention/Pin layout



	1	2	3
A	GND	HP	REF
B	LX	SHDN	IN
C	IN	OUT	OUT

Pin layout (TOP VIEW)

Pin number/name/function

Pin nr	Name	Function
A1	GND	GND pin
A2	HP	Bypass switch on pin
A3	REF	Reference voltage input pin
B1	LX	Inductor connection pin
B2	SHDN	Shutdown pin
B3	IN	Power supply input pin
C1	IN	
C2	OUT	Output pin
C3	OUT	

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Operation Notes

1) Absolute maximum ratings

An excess in the absolute maximum rating, such as supply voltage, temperature range of operating conditions, etc., can break down the devices, thus making impossible to identify breaking mode, such as a short circuit or an open circuit.
If any over rated values will expect to exceed the absolute maximum ratings, consider adding circuit protection devices, such as fuses.

2) GND voltage

The potential of GND pin must be minimum potential in all condition. As an exception, the circuit design allows voltages up to -0.3 V to be applied to the IC pin.

3) Thermal design

Use a thermal design that allows for a sufficient margin in light of the power dissipation (Pd) in actual operating conditions.

4) Inter-pin shorts and mounting errors

Use caution when positioning the IC for mounting on printed circuit boards. The IC may be damaged if there is any connection error or if pins are shorted together.

5) Actions in strong electromagnetic field

Use caution when using the IC in the presence of a strong electromagnetic field as doing so may cause the IC to malfunction.

6) Mutual impedance

Power supply and ground wiring should reflect consideration of the need to lower mutual impedance and minimize ripple as much as possible (by making wiring as short and thick as possible or rejecting ripple by incorporating inductance and capacitance).

7) Thermal shutdown Circuit (TSD Circuit)

This model IC has a built-in TSD circuit. This circuit is only to cut off the IC from thermal runaway, and has not been design to protect or guarantee the IC. Therefore, the user should not plan to activate this circuit with continued operation in mind.

8) Regarding input pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of these P layers with the N layers of other elements, creating a parasitic diode or transistor. For example, as shown in the figures below, the relation between each potential is as follows:

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.

When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes can occur inevitable in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Accordingly, methods by which parasitic diodes operate, such as applying a voltage that is lower than the GND (P substrate) voltage to an input pin, should not be used.

9) Mounting Condition

As mounting condition to the substrate may cause the affect to the electrical character of IC. The design margin for the shift value as mount is required, considering the evaluation result for IC to mount the substrate you will use.

10) External Components

The IC evaluation with the external components you will use is required to check the margin within all operating condition. Because some external inductors and capacitors change its character drastically depending on the DC current, DC voltage, temperature, and so on.

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