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# NDD03N40Z, NDT03N40Z

## N-Channel Power MOSFET 400 V, 3.4 $\Omega$

### Features

- 100% Avalanche Tested
- Extremely High dv/dt Capability
- Gate Charge Minimized
- Very Low Intrinsic Capacitance
- Improved Diode Reverse Recovery Characteristics
- Zener-protected
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

### ABSOLUTE MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	NDD	NDT	Unit
Drain-to-Source Voltage	$V_{DSS}$	400		V
Gate-to-Source Voltage	$V_{GS}$	$\pm 30$		V
Continuous Drain Current Steady State, $T_C = 25^\circ\text{C}$ (Note 1)	$I_D$	2.1	0.5	A
Continuous Drain Current Steady State, $T_C = 100^\circ\text{C}$ (Note 1)	$I_D$	1.3	0.3	A
Power Dissipation Steady State, $T_C = 25^\circ\text{C}$	$P_D$	37	2.0	W
Pulsed Drain Current	$I_{DM}$	8.0	7.2	A
Continuous Source Current (Body Diode)	$I_S$	2.1	0.5	A
Single Pulse Drain-to-Source Avalanche Energy ( $I_D = 1\text{ A}$ )	EAS	42		mJ
Peak Diode Recovery (Note 2)	dV/dt	12		V/ns
Maximum Temperature for Soldering Leads	$T_L$	260		$^\circ\text{C}$
Operating Junction and Storage Temperature	$T_J, T_{STG}$	-55 to +150		$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Limited by maximum junction temperature
2.  $I_S \leq 2.4\text{ A}$ ,  $dI/dt \leq 400\text{ A}/\mu\text{s}$ ,  $V_{DD} \leq BV_{DSS}$ ,  $T_J = +150^\circ\text{C}$

### THERMAL RESISTANCE

Parameter	Symbol	Value	Unit
Junction-to-Case (Drain)	$R_{\theta JC}$	3.4	$^\circ\text{C}/\text{W}$
Junction-to-Ambient Steady State	$R_{\theta JA}$		$^\circ\text{C}/\text{W}$
NDD03N40Z (Note 4)		42	
NDD03N40Z-1 (Note 3)		96	
NDT03N40Z (Note 4)		62	
NDT03N40Z (Note 5)		149	

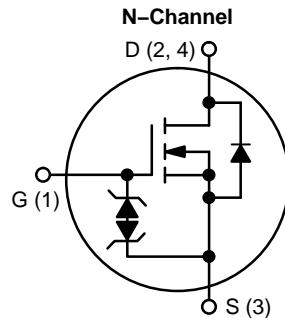
3. Insertion mounted
4. Surface mounted on FR4 board using 1" sq. pad size  
(Cu area = 1.127" sq. [2 oz] including traces)
5. Surface-mounted on FR4 board using minimum recommended pad size  
(Cu area = 0.026" sq. [2 oz]).



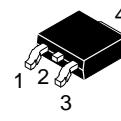
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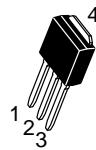
$V_{(BR)DSS}$	$R_{DS(ON)} \text{ MAX}$
400 V	3.4 $\Omega$ @ 10 V



SOT-223  
CASE 318E  
STYLE 3



DPAK  
CASE 369C  
STYLE 2



IPAK  
CASE 369D  
STYLE 2

### MARKING & ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 3 of this data sheet.

# NDD03N40Z, NDT03N40Z

**ELECTRICAL CHARACTERISTICS** ( $T_J = 25^\circ\text{C}$  unless otherwise noted)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
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## OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(\text{BR})\text{DSS}}$	$V_{\text{GS}} = 0 \text{ V}, I_D = 1 \text{ mA}$	400			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(\text{BR})\text{DSS}}/T_J$	Reference to $25^\circ\text{C}$ , $I_D = 1 \text{ mA}$		450		$\text{mV}/^\circ\text{C}$
Drain-to-Source Leakage Current	$I_{\text{DSS}}$	$V_{\text{DS}} = 400 \text{ V}, V_{\text{GS}} = 0 \text{ V}$	$T_J = 25^\circ\text{C}$		1	$\mu\text{A}$
			$T_J = 125^\circ\text{C}$		50	
Gate-to-Source Leakage Current	$I_{\text{GSS}}$	$V_{\text{GS}} = \pm 20 \text{ V}$			$\pm 10$	$\mu\text{A}$

## ON CHARACTERISTICS (Note 6)

Gate Threshold Voltage	$V_{\text{GS}(\text{TH})}$	$V_{\text{DS}} = V_{\text{GS}}, I_D = 50 \mu\text{A}$	3.0	3.9	4.5	V
Negative Threshold Temperature Coefficient	$V_{\text{GS}(\text{TH})}/T_J$	Reference to $25^\circ\text{C}$ , $I_D = 50 \mu\text{A}$		9.8		$\text{mV}/^\circ\text{C}$
Static Drain-to-Source On Resistance	$R_{\text{DS}(\text{on})}$	$V_{\text{GS}} = 10 \text{ V}, I_D = 0.6 \text{ A}$		3.0	3.4	$\Omega$
Forward Transconductance	$g_{\text{FS}}$	$V_{\text{DS}} = 15 \text{ V}, I_D = 0.6 \text{ A}$		1.2		S

## DYNAMIC CHARACTERISTICS

Input Capacitance (Note 7)	$C_{\text{iss}}$	$V_{\text{DS}} = 50 \text{ V}, V_{\text{GS}} = 0 \text{ V}, f = 1 \text{ MHz}$		140		pF
Output Capacitance (Note 7)	$C_{\text{oss}}$			17		
Reverse Transfer Capacitance (Note 7)	$C_{\text{rss}}$			3.0		
Effective output capacitance, energy related (Note 9)	$C_{\text{o(er)}}$	$V_{\text{GS}} = 0 \text{ V}, V_{\text{DS}} = 0 \text{ to } 320 \text{ V}$		10		nC
Effective output capacitance, time related (Note 10)	$C_{\text{o(tr)}}$		$I_D = \text{constant}, V_{\text{GS}} = 0 \text{ V}, V_{\text{DS}} = 0 \text{ to } 320 \text{ V}$	20		
Total Gate Charge (Note 7)	$Q_g$			6.6		
Gate-to-Source Charge (Note 7)	$Q_{\text{gs}}$			1.7		
Gate-to-Drain ("Miller") Charge (Note 7)	$Q_{\text{gd}}$	$V_{\text{DS}} = 200 \text{ V}, I_D = 2.4 \text{ A}, V_{\text{GS}} = 10 \text{ V}$		3.5		nC
Plateau Voltage	$V_{\text{GP}}$			6.9		
Gate Resistance	$R_g$			9.0		

## RESISTIVE SWITCHING CHARACTERISTICS (Note 8)

Turn-on Delay Time	$t_{\text{d}(\text{on})}$	$V_{\text{DD}} = 200 \text{ V}, I_D = 2.4 \text{ A}, V_{\text{GS}} = 10 \text{ V}, R_{\text{G}} = 0 \Omega$		10		ns
Rise Time	$t_r$			7.0		
Turn-off Delay Time	$t_{\text{d}(\text{off})}$			13		
Fall Time	$t_f$			5.0		

## SOURCE-DRAIN DIODE CHARACTERISTICS

Diode Forward Voltage	$V_{\text{SD}}$	$I_S = 0.5 \text{ A}, V_{\text{GS}} = 0 \text{ V}$	$T_J = 25^\circ\text{C}$		0.8	1.5	V
			$T_J = 100^\circ\text{C}$		0.7		
Reverse Recovery Time	$t_{\text{rr}}$	$V_{\text{GS}} = 0 \text{ V}, V_{\text{DD}} = 30 \text{ V}, I_S = 2.4 \text{ A}, d_i/d_t = 100 \text{ A}/\mu\text{s}$			152		ns
Charge Time	$t_a$				62		
Discharge Time	$t_b$				90		
Reverse Recovery Charge	$Q_{\text{rr}}$				452		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

6. Pulse Width  $\leq 380 \mu\text{s}$ , Duty Cycle  $\leq 2\%$ .

7. Guaranteed by design.

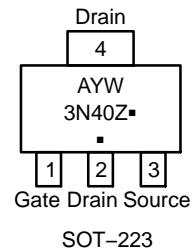
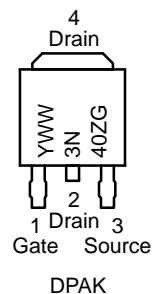
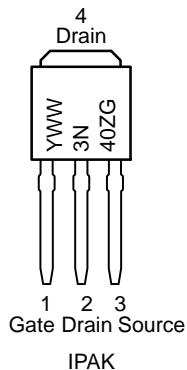
8. Switching characteristics are independent of operating junction temperatures.

9.  $C_{\text{o(er)}}$  is a fixed capacitance that gives the same stored energy as  $C_{\text{oss}}$  while  $V_{\text{DS}}$  is rising from 0 to 80%  $V_{(\text{BR})\text{DSS}}$

10.  $C_{\text{o(tr)}}$  is a fixed capacitance that gives the same charging time as  $C_{\text{oss}}$  while  $V_{\text{DS}}$  is rising from 0 to 80%  $V_{(\text{BR})\text{DSS}}$

# NDD03N40Z, NDT03N40Z

## MARKING DIAGRAMS



A = Assembly Location

Y = Year

W, WW = Work Week

3N40Z = Specific Device Code

G or ■ = Pb-Free Package

(\*Note: Microdot may be in either location)

## ORDERING INFORMATION

Device	Package	Shipping <sup>†</sup>
NDD03N40Z-1G	IPAK (Pb-Free, Halogen Free)	75 Units / Rail
NDT03N40ZT4G	DPAK (Pb-Free, Halogen Free)	2500 / Tape & Reel
NDT03N40ZT1G	SOT-223 (Pb-Free, Halogen Free)	1000 / Tape & Reel
NDT03N40ZT3G	SOT-223 (Pb-Free, Halogen Free)	4000 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# NDD03N40Z, NDT03N40Z

## TYPICAL CHARACTERISTICS

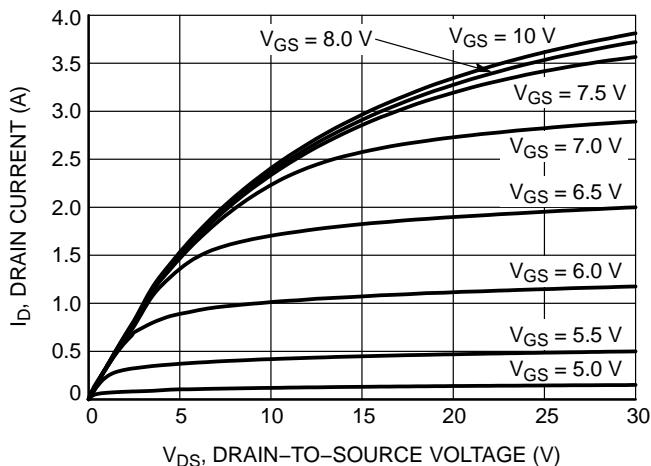


Figure 1. On-Region Characteristics

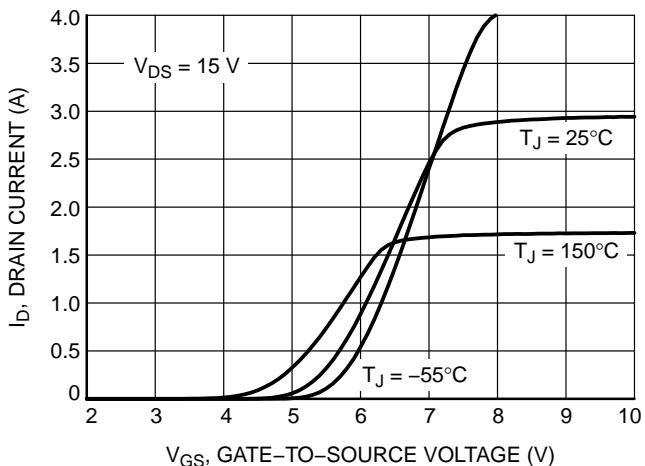


Figure 2. Transfer Characteristics

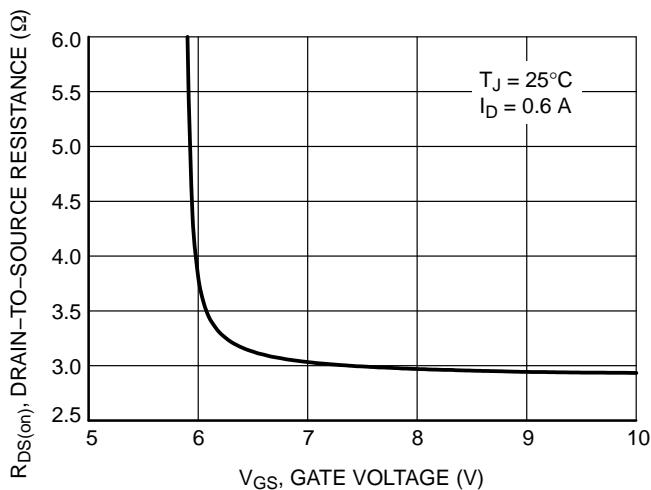


Figure 3. On-Resistance vs. Gate-to-Source Voltage

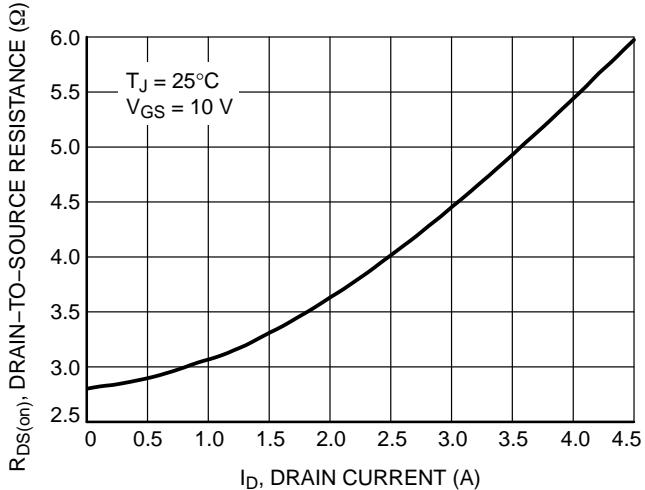


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

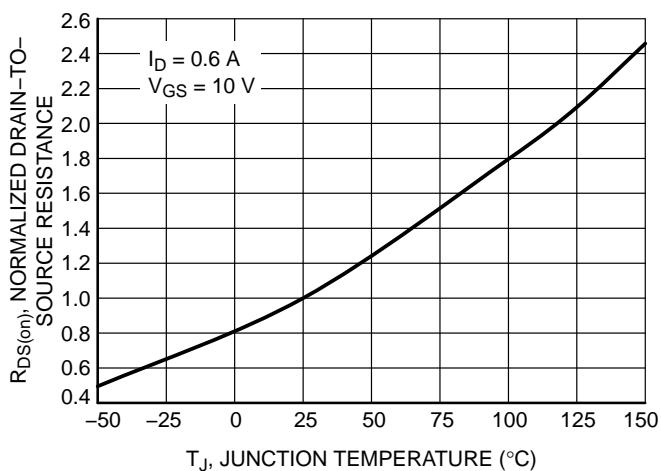


Figure 5. On-Resistance Variation with Temperature

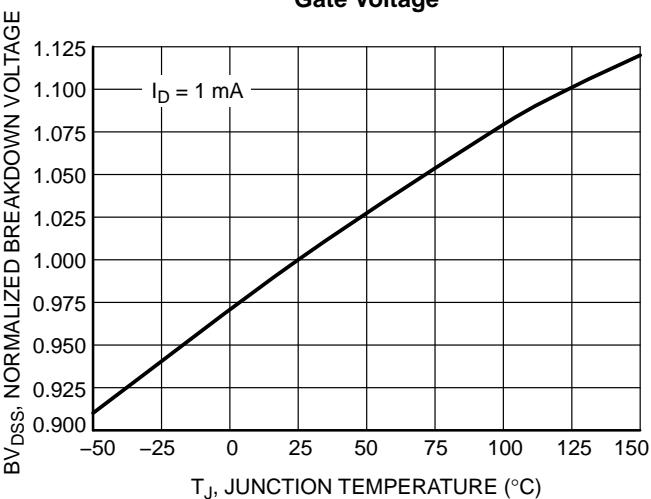
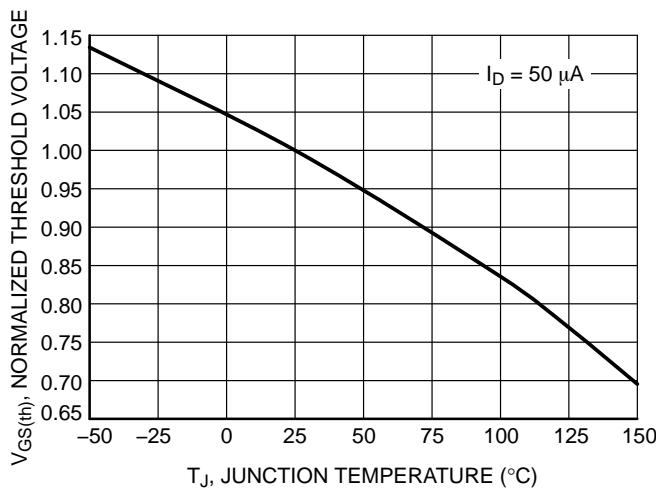


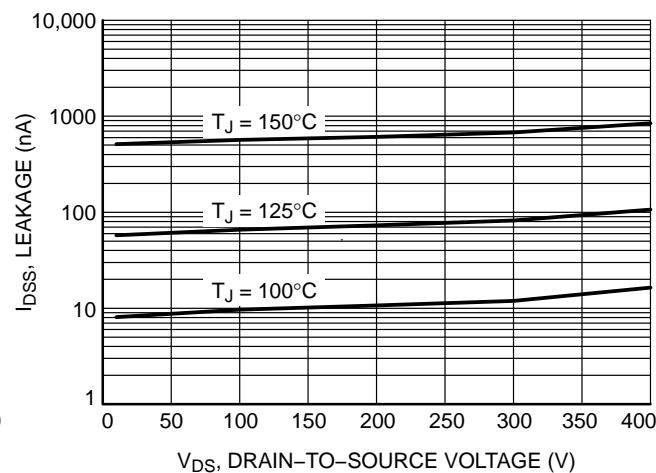
Figure 6. Breakdown Voltage Variation with Temperature

# NDD03N40Z, NDT03N40Z

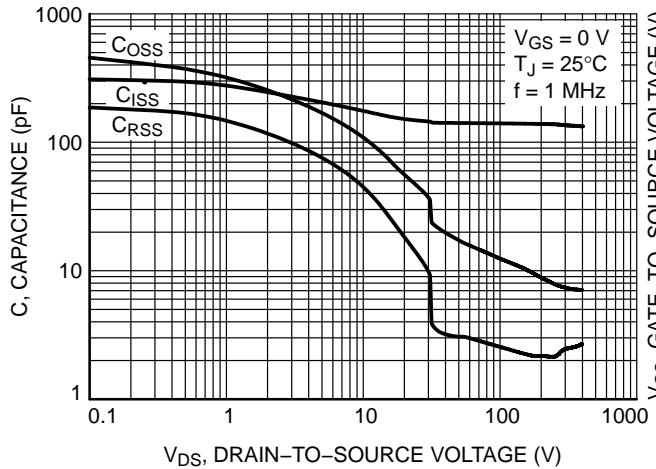
## TYPICAL CHARACTERISTICS



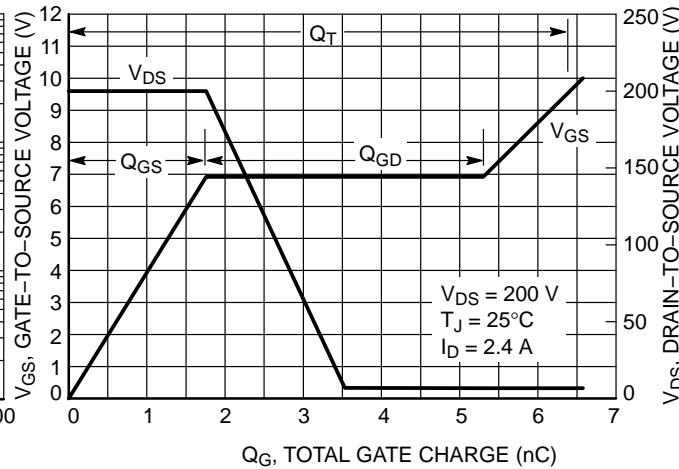
**Figure 7. Threshold Voltage Variation with Temperature**



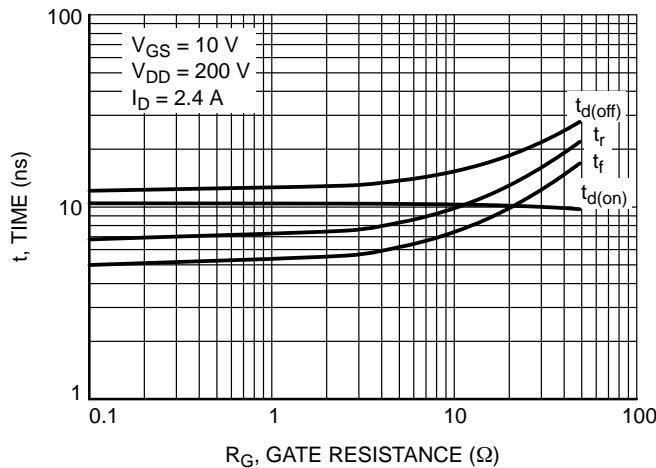
**Figure 8. Drain-to-Source Leakage Current vs. Voltage**



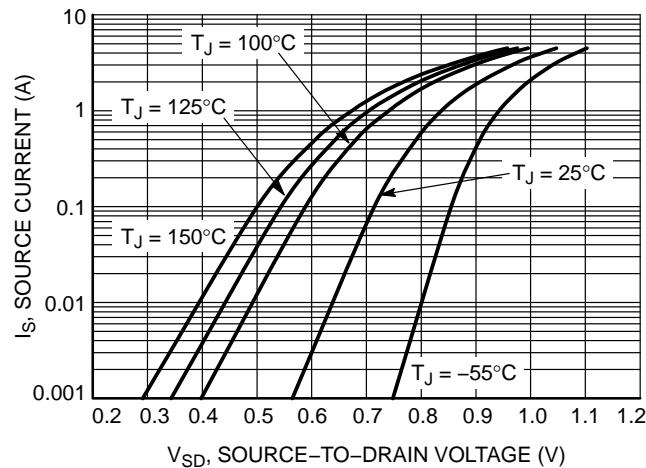
**Figure 9. Capacitance Variation**



**Figure 10. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge**



**Figure 11. Resistive Switching Time Variation vs. Gate Resistance**



**Figure 12. Diode Forward Voltage vs. Current**

# NDD03N40Z, NDT03N40Z

## TYPICAL CHARACTERISTICS

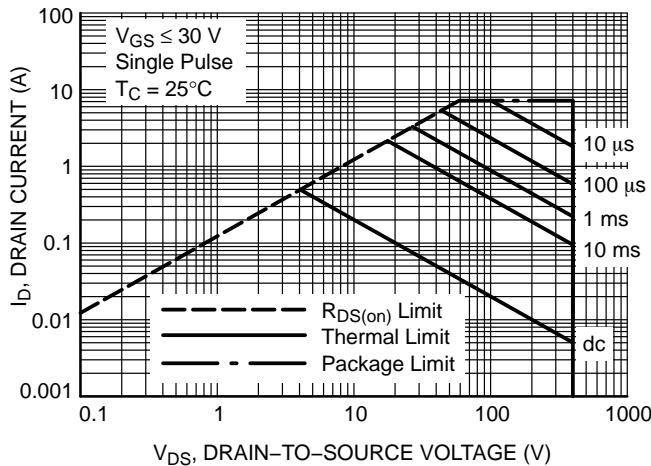


Figure 13. Maximum Rated Forward Biased Safe Operating Area for NDT03N40Z

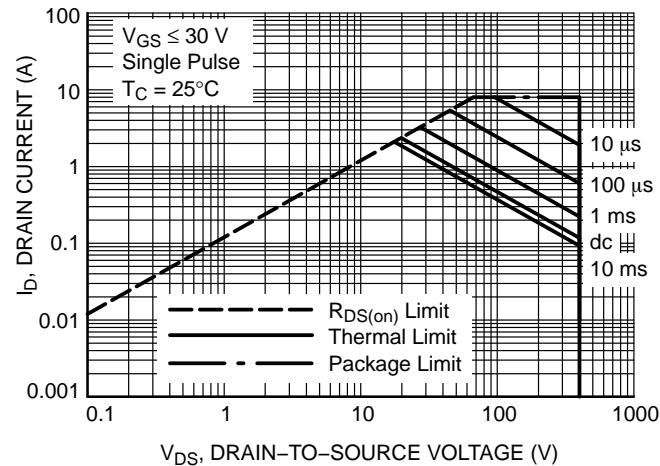


Figure 14. Maximum Rated Forward Biased Safe Operating Area for NDD03N40Z

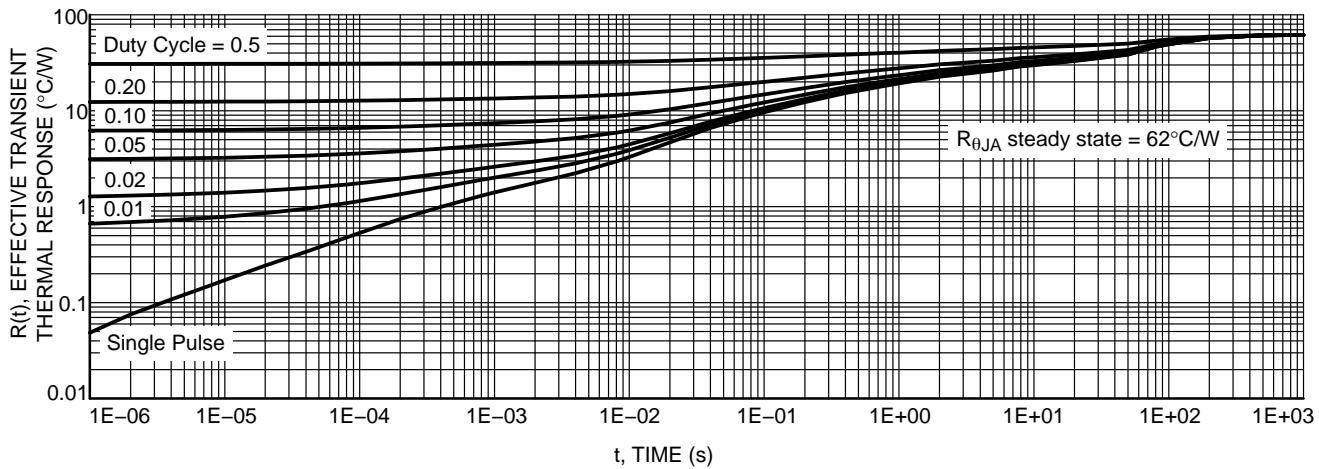


Figure 15. Thermal Impedance (Junction-to-Ambient) for NDT03N40Z

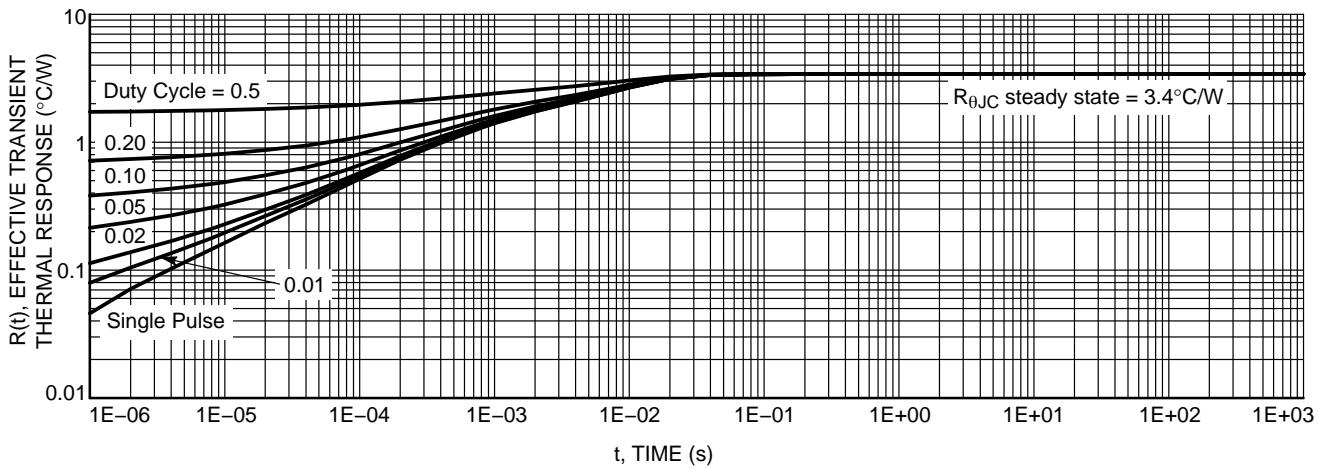


Figure 16. Thermal Impedance (Junction-to-Case) for NDD03N40Z

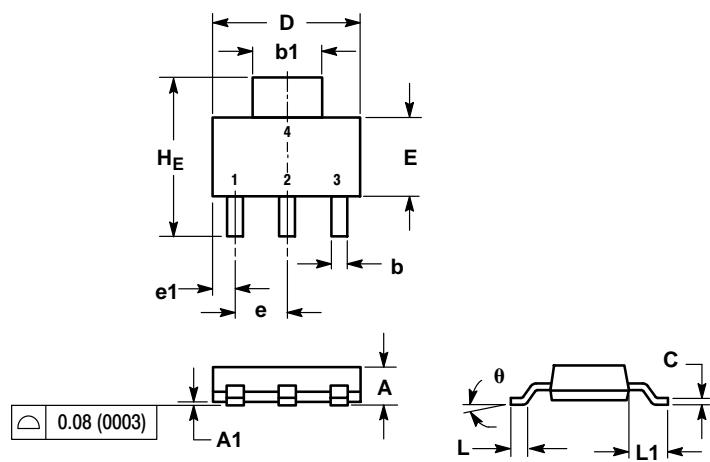
# NDD03N40Z, NDT03N40Z

## PACKAGE DIMENSIONS

### SOT-223 (TO-261)

CASE 318E-04

ISSUE N



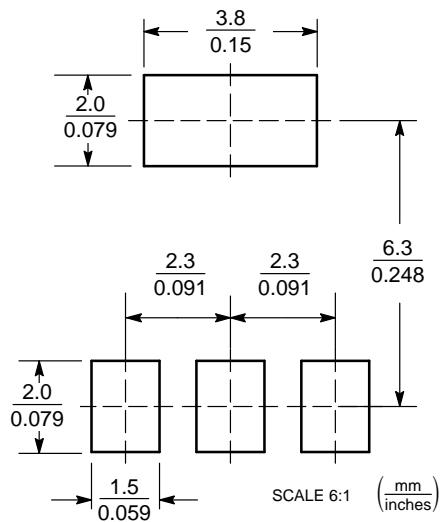
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCH.

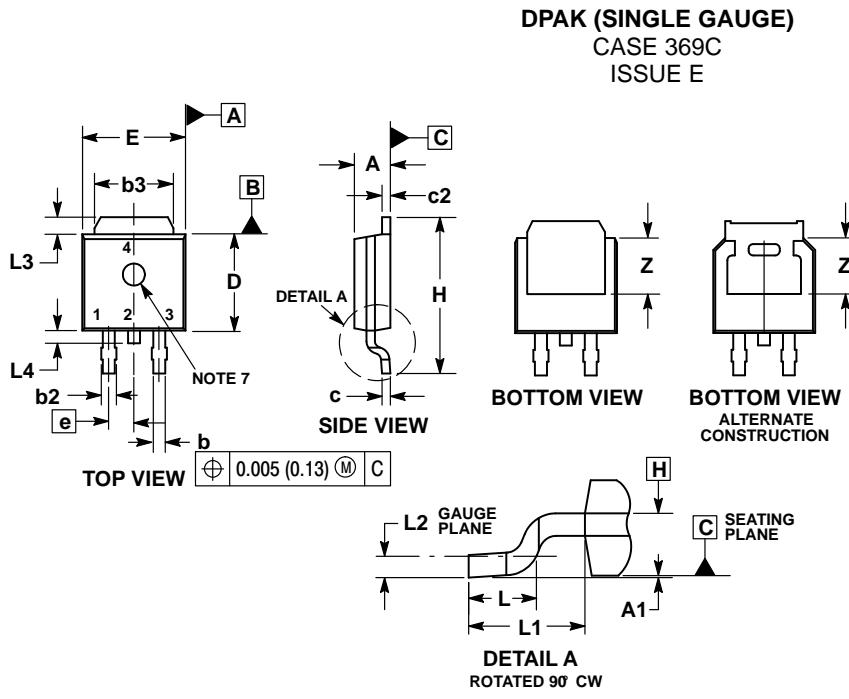
DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.50	1.63	1.75	0.060	0.064	0.068
A1	0.02	0.06	0.10	0.001	0.002	0.004
b	0.60	0.75	0.89	0.024	0.030	0.035
b1	2.90	3.06	3.20	0.115	0.121	0.126
c	0.24	0.29	0.35	0.009	0.012	0.014
D	6.30	6.50	6.70	0.249	0.256	0.263
E	3.30	3.50	3.70	0.130	0.138	0.145
e	2.20	2.30	2.40	0.087	0.091	0.094
e1	0.85	0.94	1.05	0.033	0.037	0.041
L	0.20	—	—	0.008	—	—
L1	1.50	1.75	2.00	0.060	0.069	0.078
H_E	6.70	7.00	7.30	0.264	0.276	0.287
θ	0°	—	10°	0°	—	10°

STYLE 3:  
 PIN 1. GATE  
 2. DRAIN  
 3. SOURCE  
 4. DRAIN

### SOLDERING FOOTPRINT



## PACKAGE DIMENSIONS



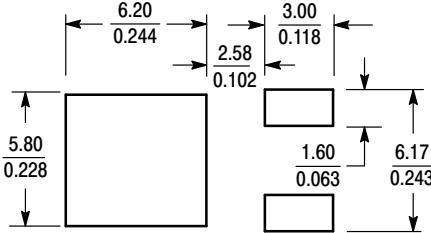
## NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3 and Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. OPTIONAL MOLD FEATURE.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.028	0.045	0.72	1.14
b3	0.180	0.215	4.57	5.46
c	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
e	0.090	BSC	2.29	BSC
H	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.114	REF	2.90	REF
L2	0.020	BSC	0.51	BSC
L3	0.035	0.050	0.89	1.27
L4	---	0.040	---	1.01
Z	0.155	---	3.93	---

STYLE 2:  
PIN 1. GATE  
2. DRAIN  
3. SOURCE  
4. DRAIN

## SOLDERING FOOTPRINT\*



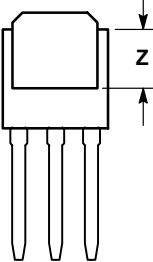
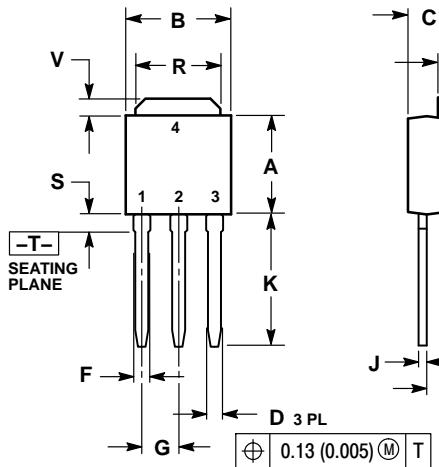
SCALE 3:1  $\left( \frac{\text{mm}}{\text{inches}} \right)$

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

# NDD03N40Z, NDT03N40Z

## PACKAGE DIMENSIONS

**IPAK**  
CASE 369D  
ISSUE C



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.35
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.096	BSC	2.29	BSC
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.350	0.380	8.89	9.65
R	0.180	0.215	4.45	5.45
S	0.025	0.040	0.63	1.01
V	0.035	0.050	0.89	1.27
Z	0.155	—	3.93	—

STYLE 2:

1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

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