TC358867XBG

Bridge IC from SoC/FPGA to Embedded DisplayPort™ Display Panels

The TC358867XBG is a bridge IC that enables conversion of input MIPI® DSI or DPI (RGB parallel) video streaming to embedded DisplayPort™ (eDP) or DisplayPort™ output. More and more companies are starting to adopt mobile application processers to make smarter information terminals such as point-of-sale (POS) terminals. Additionally, there is increasing demand for higher-definition, medium-sized eDP panels of 10 - 20 inches capable of showing more information on monitors. However, interfacing mismatch to eDP panels often happens because a common display interface of mobile SoC/CPU is MIPI® DSI.
By bridging these display interfaces, the TC358867XBG makes traditional applications smarter and suitable for larger panels offering higher resolution. Sample shipments start today and mass production is scheduled to start in April 2018.
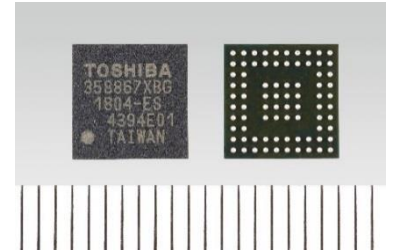
Features

- MIPI® DSI interface bridge suitable for eDP:

  The TC358876XBG can translate MIPI® DSI/DPI (RGB parallel) Link video stream from host to DisplayPort™ Link data for external display devices and supports LCD panels up to WXUGA (1920×1200) with 24 bits per pixel (bpp) at 60 frames per second (fps).

- I2S Audio Interface:

  It supports one I2S port for audio streaming from the host to the TC358867XBG. DP transmitter is used to send audio data to the display panels.

- Supports 2 packages for suitable PCB design:

  The TC358867XBG's wide ball pitch reduces the cost of your PCB board.
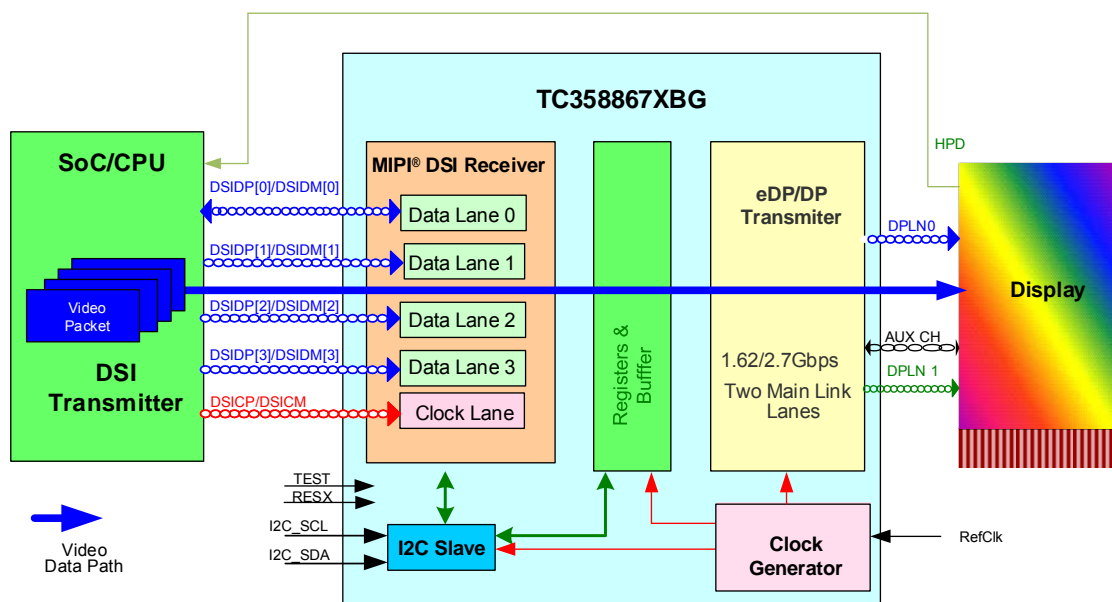 The TC358767AXBG's small body size reduces your PCB area.

Applications

- Information equipment such as point-of-sale (POS) terminals
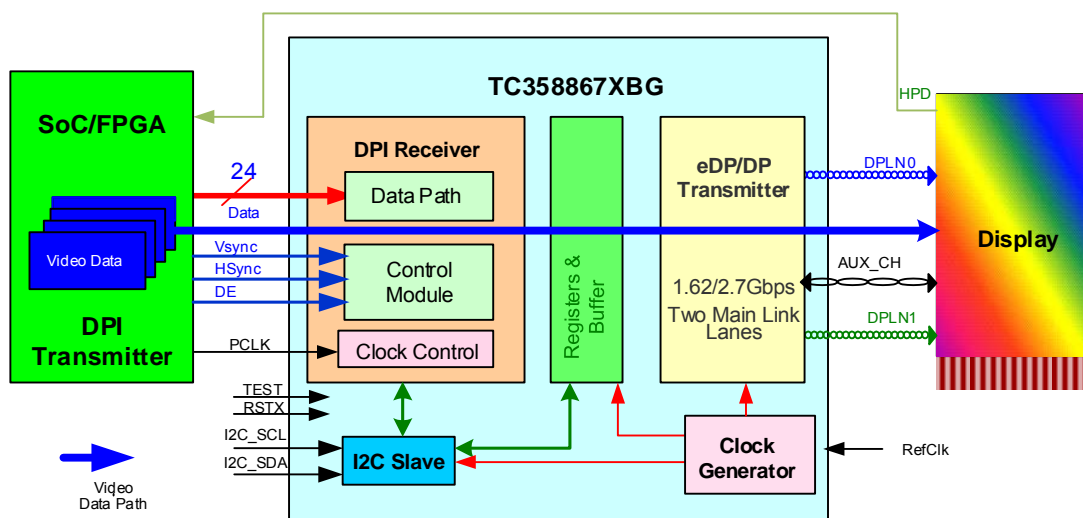- Tablets, entertainment equipment

Block Diagram

(1) MIPI® DSI to eDP/DP conversion
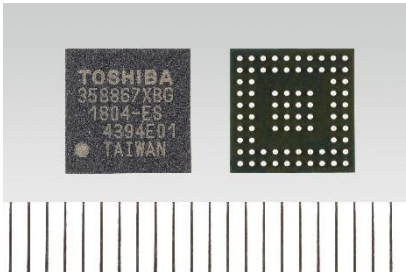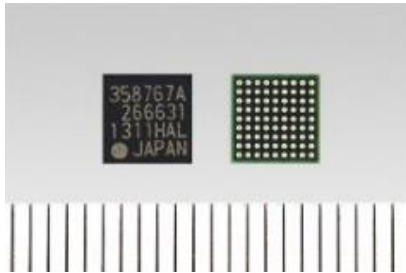

(2) MIPI® DPI（RGB parallel）to eDP/DP conversion

Note: Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purposes.

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Product Specifications

| Item	Description	
Input video stream format (Rx)	MIPI$^®$ DSI 1.01	MIPI$^®$ DPI 2.0 (RGB Parallel)
Rx data rate	1Gbps/lane x 4	24bit, PCLK 154MHz (Max)
Audio input	2 channels	
Output video stream (Tx)	VESA$^®$ DisplayPort^{TM} 1.1a	
Tx data rate	1.62Gbps/lane x 2or 2.7Gbps/lane x 2	
Maximum resolution	WUXGA　（1920×1200）	
Voltage	Core, MIPI$^®$ D-PHY: 1.2 V ± 0.06 V, Digital I/O: 1.8 V ± 0.09 V, DisplayPort^{TM}: 1.8 V ± 0.09 V, 1.2 V ± 0.06 V	

Package Line-up

Part number	TC358867XBG	TC358767AXBG
Overview		
Package type	BGA	BGA
Ball pitch	0.65 mm	0.5 mm
Ball count	80	81
Package size	7 × 7 mm	5 × 5 mm
ES	Available	Available
MP	April, 2018	Available

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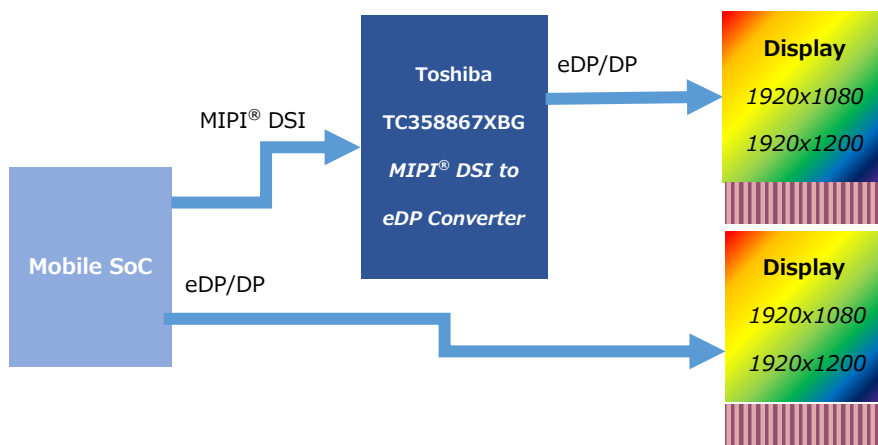# Application Circuit Example

(1) Connection from mobile SoC to eDP display panel
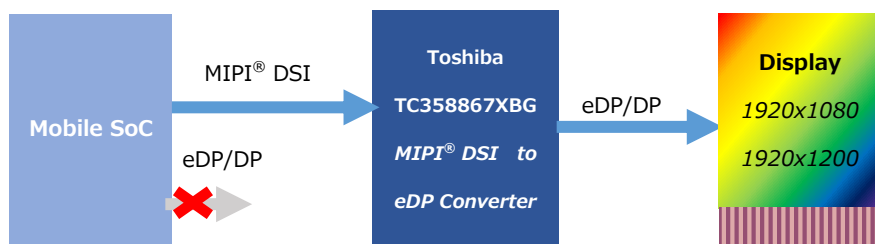
(2) Connection from SoC or FPGA to eDP display panel
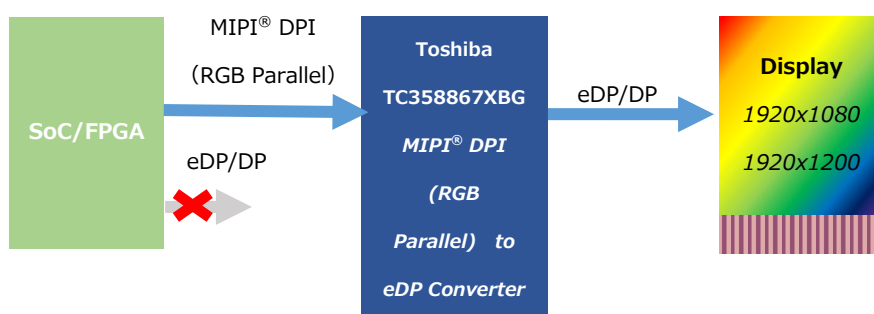
(3) Dual panel

Note: The system configuration example shown above is provided for reference purposes only. Thorough evaluation is required, especially at the mass production design stage. Any license to any industrial property rights is not by providing this example.

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