Dear customer

ROHM Co., Ltd. ("ROHM"), on the 1st day of April, 2024,
has absorbed into merger with 100%-owned subsidiary of LAPIS Technology Co., Ltd.

Therefore, all references to "LAPIS Technology Co., Ltd.", "LAPIS Technology"
and/or "LAPIS" in this document shall be replaced with "ROHM Co., Ltd."
Furthermore, there are no changes to the documents relating to our products other than
the company name, the company trademark, logo, etc.

Thank you for your understanding.

ROHM Co., Ltd.
April 1, 2024

ML86112

CVBS-MIPI CSI2/LVTTL conversion LSI

■ General Description

The ML86112 is a video decoder that converts NTSC and PAL analog video signals into MIPI-CSI2 output or LVTTL output.
This LSI has a built-in 1-channel 10-bit A/D converter, an accept 2 differential composite video inputs or 4 single-ended composite video inputs.
The composite signal is separated into a luminance signal and a chrominance signal with a 2-dimensional Y/C separation filter, and these two signals are then output as digital video signals.
The video signals is sampled with a line lock clock sampling method using the built-in PLL.
The format of MIPI-CSI2 output is YUV422 8bit. And the format of LVTTL is ITU-R BT.601/BT.656 YCbCr standard digital format.

■ Features

•Analog video decoder:

Input format:	:	NTSC-M、J、443	
		PAL-B、B1、D、G、H、I、K、M、N、Nc、60	
Analog input port:	:	Single End	Composit video input 4ch
		Differential	Conposit video input 2ch
A/D converter:	:	10bit ADC	
Build-in oscillator buffer	:	External crystal oscillator as a reference clock (32MHz or 25MHz)	
Sampling frequency			
NTSC（ITU-R BT.601）	:	27.0000 MHz	
NTSC（Square pixel）	:	24.5454 MHz	
NTSC（4fsc）	:	28.6363 MHz	
PAL（ITU-R BT.601）	:	27.0000 MHz	
PAL（Square pixel）	:	29.5000 MHz	
Sampling method	:	Line lock clock sampling method	
Y/C separation	:	Adaptive two-dimensional Y/C separation filter	
Luminance level adjustment	:	AGC (automatic gain control) / MGC (manual gain control) / Peak AGC	
Color level adjustment	:	ACC (automatic color coltrol) / MCC (manual color control)	
Contrast adjustment	:	Adjustable between 1/32 to 63/32 around 128	
Luminance offset adjustment	:	Adjustable between -7IRE to 7IRE	
Contour compansation	:	Emphasizes higher frequencies (luminance signal)	
Hue adjustment	:	Adjustable between -180° to 180°	
CTI	:	Color level change improved	
Automatic judgment of input video signal method			
	:	NTSC / PAL automatic recognition (in ITU-R BT.601 mode and in NTSC4fsc mode.)	
VBI data detection	:	Closed caption	for NTSC
	:	CGMS	for NTSC
	:	WSS	for PAL

- IP conversion function: : Intra-field interpolation
- Digital video output : MIPI-CSI2 output or LVTTL output (BT.656) selectable.
  Equipped with MIPI-CSI2 Transmitter (1 lane).
  - Output format : MIPI-CSI2 YUV422 8bit
    Continuous clock operation
    Output can be stopped by external pin/register control (LP mode)
    LVTTL ITU-R BT.656-4 (YCbCr4:2:2 8-bit with synchronization information)
  - Output frequency : MIPI-CSI2 196.4M to 472Mbps
    LVTTL 24.5454MHz to 59MHz (Single edge clock)
    12.2727MHz to 29.5MHz(Dual edge clock)
    (Pixel frequency: 12.2727MHz to 29.5MHz)
- Clock : MIPI-CSI2 PLL uses line lock PLL as reference clock
- Detection function : Input synchronization detection
- STATUS output : Open drain output (1.8V-3.6V external pull up)
- Sleep function : Sleep by register control
- Host interface : I^2C Slave, maximum 400 kHz
  Slave address: 80h(1000_000x), 82h(1000_001x) selectable
- Power voltage :

I/O part	3.3 V ± 0.3 V
Analog part (AFE/ADC)	3.3 V ± 0.3 V
MIPI-Tx part (HS driver)	3.3 V ± 0.3 V
Logic core part	1.2 V ± 0.06 V
PLL part	1.2 V ± 0.06 V
MIPI-Tx part (PLL/LP driver)	1.2 V ± 0.06 V

- Operational temperature (ambient temperature): -40 to +105 ℃
- Package : 32 pin 0.5 pitch plastic WQFN (WQFN32-0505-0.50)
  Wettable frank, exposed PAD (back surface GND)

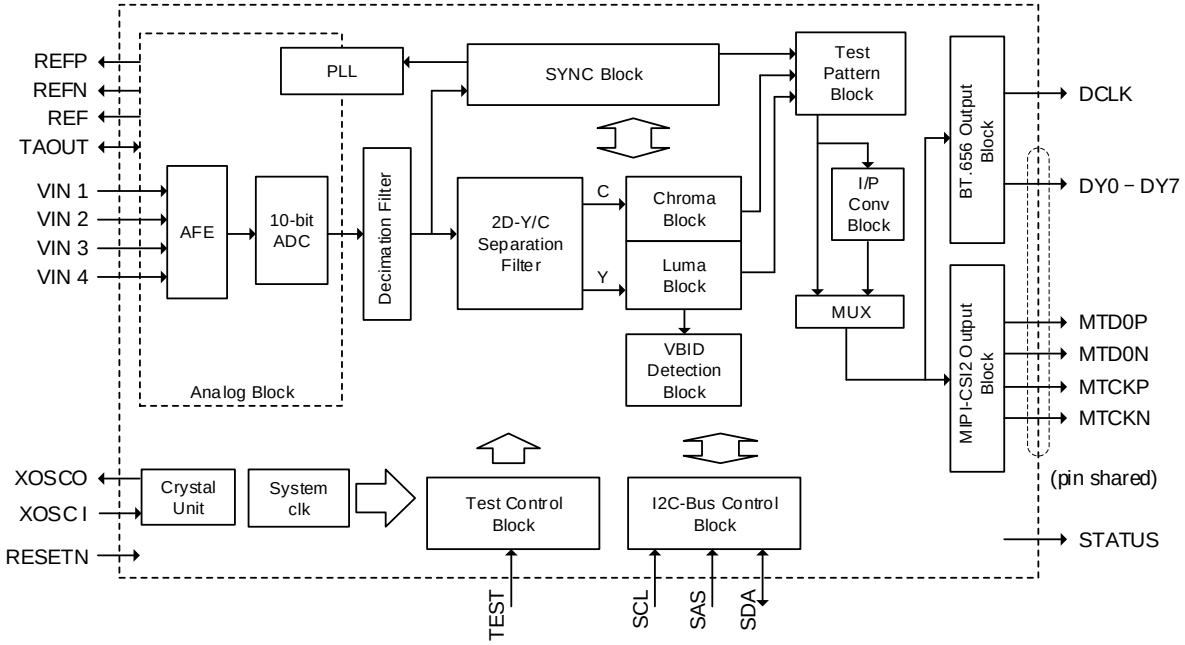
■ Application

- Car Navigation
- Display audio
- RSE (Rear Seat Entertainment)

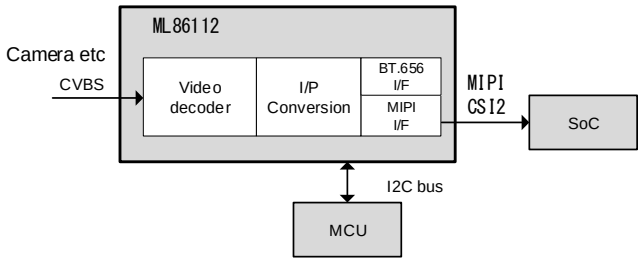
■ Line up

Part Number	Shipping form
ML86112GDZ0AX	Tray

■ Block Diagram

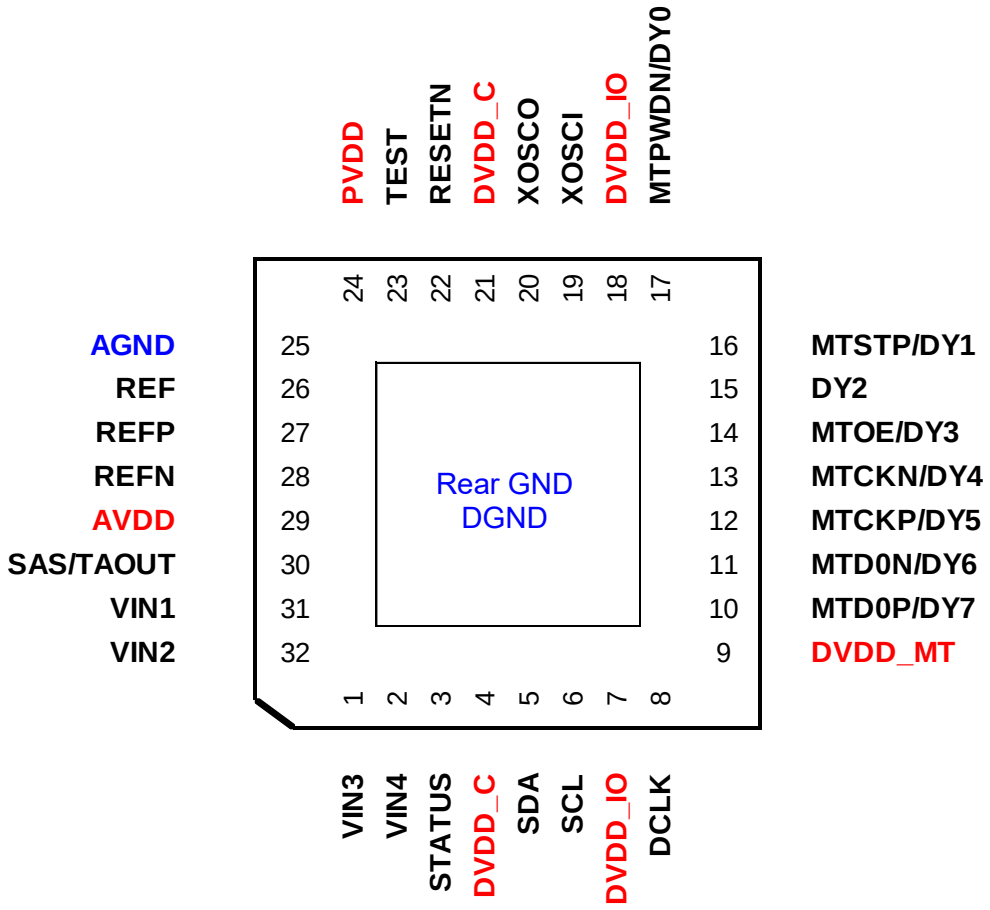


■ Application Example



■ Pin Connections (Top View)

32 pin 0.5 pitch plastic WQFN, Wettable frank, exposed PAD (back surface GND)
(WQFN32-0505-0.50)



Note: The same power voltage should be applied to the power supply pins with the same name.
Unused input pins should be fixed to "L" or "H" level.
However, when an unused input pin is a pull-down pin, it should be fixed to "L" level.
The rear GND is DGND. Arrange a pad having the same size as the rear GND area on the board side for connection.

■ List of Pins

Pin number	Pin name	I/O	Primary/Secondary function	Remarks
1	VIN3	I	Analog video input3 (Composite)	
2	VIN4	I	Analog video input4 (Composite)	
3	STATUS	O	Status output Open Drain output (Nch)	
4	DVDD_C	—	Power supply for digital core (1.2V)	
5	SDA	I/O	I^2C bus serial data	ST,5V-tolerant
6	SCL	I	I^2C bus serial clock	ST,5V-tolerant
7	DVDD_IO	—	Power supply for digital I/O (3.3V)	
8	DCLK	O	Digital video output TTL clock	
9	DVDD_MT	—	Power supply for MIPI-Tx (1.2V)	
10	MTD0P/DY7	O	Digital video output MIPI data / TTL data7	
11	MTD0N/DY6	O	Digital video output MIPI data / TTL data6	
12	MTCKP/DY5	O	Digital video output MIPI clock / TTL data5	
13	MTCKN/DY4	O	Digital video output MIPI clock / TTL data4	
14	MTOE/DY3	O	Digital video output MIPI output status TTL output/ TTL data3	
15	DY2	O	Digital video output TTL data2	
16	MTSTP/DY1	I/O	Digital video output MIPI output stop (LP mode) control TTL input/TTL data1	
17	MTPWDN/DY0	I/O	Digital video output MIPI operation stop control TTL input/TTL data0	
18	DVDD_IO	—	Power supply for digital I/O (3.3V)	
19	XOSCI	I	Clock oscillation input (HPLL reference clock input)	ST
20	XOSCO	O	Clock oscillation output	
21	DVDD_C	—	Power supply for digital core (1.2V)	
22	RESETN	I	System reset input (active “L”)	ST,5V-tolerant
23	TEST	I	Test mode select	PD
24	PVDD	—	Power supply for PLL (1.2 V)	
25	AGND	I/O	Ground for analog	
26	REF	I/O	Reference voltage for ADC (external grounding through 0.01uF)	
27	REFP	—	Reference voltage for ADC (external grounding through 0.1uF)	
28	REFN	—	Reference voltage for ADC (external grounding through 0.1uF)	
29	AVDD	—	Power supply for analog (3.3V)	
30	SAS/TAOUT	I/O	I^2C Bus Slave Address Selection / Output for testing SAS=0、80h（1000_000x）/ SAS=1、82h（1000_001x）	PD
31	VIN1	I	Analog video input1 (Composite)	
32	VIN2	I	Analog video input2 (Composite)	

PD = pull-down. ST = Schmitt Trigger. SL = Slew Rate Cont.
Note: The pull-down resistance is 40kΩ.

■ Pin Descriptions

Pin name	I/O	Function Description	Initial state
External CLK			
XOSCI	I	Clock oscillation input (PLL reference clock input) A crystal oscillator is attached between the XOSCI and XOSCO pins. The clock frequency to be input is as follows: 32.000MHz: Register # 70h / bit [6: 5] (OSC_SEL [1: 0]) = ”00” (default) 25.000MHz: Register # 70h / bit [6: 5] (OSC_SEL [1: 0]) = ”01” The sampling frequency (twice) is the following frequency by changing the register #00h/bit [2:1] (SPMD [1:0]). 27.0000MHz: NTSC / PAL ITU-R BT.601 24.5454MHz: NTSC Square pixel 28.6363MHz: NTSC 4fsc 29.5000MHz: PAL Square pixel	Input
XOSCO	O		“X”
System			
RESETN	I	System reset input (active "L")	Input
TEST	I	Test mode selection, Set to "L"	Input PD
Host interface			
SCL	I/O	I^2C bus serial clock Pull-up this pin outside the device.	Input
SDA	I/O	I^2C bus serial data Pull-up this pin outside the device.	Input
SAS	I	I^2C Bus Slave Address Selection “L” : 80h (1000_000X) “H” : 82h (1000_001X)	Input PD
Analog video input Pin name with “()” is secondary function of another pin.			
VIN1 VIN2 VIN3 VIN4	I	Analog video input pin Input the composite signal. Note: This pin needs an external circuit. Connect an unused VIN pin directly to AGND or connect 0.1uF between pin and AGND. When directly connected to AGND, current (tens uA) will flow.	Input
REF, REFP, REFN	O	AD converter Reference voltage output Note: This pin needs an external circuit.	Output
(TAOUT)	O	Analog test pin	—

Note: PD = pull-down
Note: The pull-down resistance is 40kΩ.
Note: The initial state is the primary function.

Pin name	I/O	Function Description	Initial state
MIPI-CSI2 digital video output Output analog video signals (after digital conversion). The format is YUV422 8bit.			
MTD0P MTD0N	O	MIPI-CSI2 output data	HiZ
MTCKP MTCKN	O	MIPI-CSI2 output clock	HiZ
MTOE	O	Digital video output MIPI output status TTL output "L": Output disabled (waiting for startup) "H": Output possible	"L"
MTSTP	I	Digital video output MIPI output stop control TTL input "L": Output enable "H": Output stopped (LP mpde)	Input
MTPWDN	I	Digital video output MIPI operation stop control TTL input "L": Operation enable "H": Operation stopped (HiZ output)	Input
LVTTL digital video output Output analog video signals (after digital conversion). The format is ITU-R BT.656-4 (YCbCr4:2:2 8-bit with synchronization information). Pin name with "()" is secondary function of another pin.			
(DCLK)	O	LVTTL output data clock The clock corresponding to the sampling rate selected by register #00/bit [2:1] (SPMD [1:0]) is output. When the input format is automatically determined, the clock corresponding to the sampling rate of the identified mode is output. When SDR operation register #03h/bit [1] (DDRO_MODE)="0" (default), Clock frequency at interlaced output: Sampling rate x 1 Clock frequency during progressive output: Sampling rate x2 DDR operation register #03h/bit [0] (DDRO_MODE)="1", Clock frequency at interlaced output: Sampling rate x1/2 Clock frequency during progressive output: Sampling rate x1	"L"
(DY7-0)	O	LVTTL output data Outputs video signal multiplexed in 8 bits. The initial state is as follows for MIPI-CSI2 operation. DY7-DY4: HiZ DY3-DY2: "L" DY1-DY0: Input (*) (*) DY1 and DY0 pins are input in the initial state. Therefore, it is recommended to use Pull-Up when using LVTTL.	HiZ/ "L"/ Input

Note: PD = pull-down
Note: The pull-down resistance is 40kΩ.
Note: The initial state is the primary function.

Pin name	I/O	Function Description	Initial State
Status			
STATUS	O	Status output (“L” output only. HiZ output at “H” operation) When using the status output, pull-up (1.8V-3.6V) this pin outside the device. By setting register #78h/bit [7:4] STATUS_SEL, any signal can be output from Horizontal valid period (HVALID), vertical valid period (VVALID), field signal (ODD / EVEN), composite sync signal (CSYNC), valid area signal (VHVALID), field frequency judgment signal (NTPAL), sync detection flag (HLOCK) , VBI data detection flag (VBID_DET), HPLL lock flag (LKFLG) and interrupt output (INT) Register #78h/bit [7:4] = “0000”: Horizontal valid period (HVALID) Register #78h/bit [7:4] = “0001”: Vertical valid period (VVALID) Register #78h/bit [7:4] = “0010”: Field signal (ODD/EVEN) Register #78h/bit [7:4] = “0011”: Composite sync signal (CSYNC) Register #78h/bit [7:4] = “0100”: Valid area signal (VHVALID) Register #78h/bit [7:4] = “0101”: Field frequency judgment signal (NTPAL) Register #78h/bit [7:4] = “0110”: Sync detection flag (HLOCK) (default) Register #78h/bit [7:4] = “1001”: VBI data detection flag (VBID_DET) Register #78h/bit [7:4] = “1110”: HPLL lock flag (LKFLG) Register #78h/bit [7:4] = “1111”: Interrupt output (INT)	HiZ
Power supply			
AVDD	—	3.3V Power supply for analog	
AGND	—	Ground for analog	
PVDD	—	1.2V Power supply for PLL	
DVDD_MT	—	1.2V Power supply for MIPI-Tx	
DVDD_IO	—	3.3V Power supply for digital I/O, MIPI-Tx	
DVDD_C	—	1.2V Power supply for digital core	
DGND	—	Ground for digital (rear GND)	

PD = pull-down. ST = Schmitt Trigger. SL = Slew Rate Cont.
Note: The pull-down resistance is 40kΩ.
Note: The initial state is the primary function.

■ Function Description

1. Analog Video Input

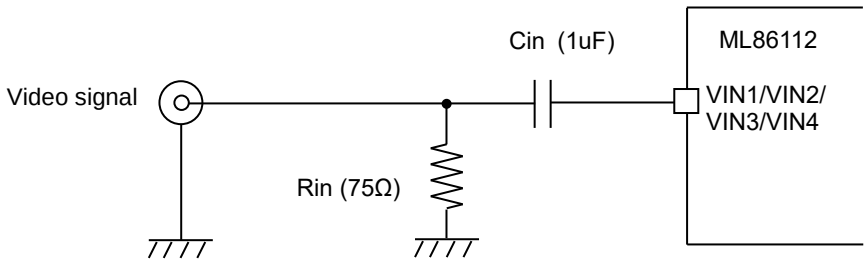
1.1. Analog Video Input

The ML86112 offers the composite video input for analog video input.
For analog input, it supports the composite video signal defined in ITU-R BT.470.

Analog video signal is input using capacitive-coupling. Level of the synchronization signal is detected through the internal clamp circuit to reproduce in DC. (Sync-chip clamp)
The internal ADC performs sampling on the analog signals that are clamped. Unused A/D converter enters sleep mode to reduce power consumption.

An external circuit must be configured as shown below when the analog video signal is input.
The input resistance in terms of ML86112 must be about 75Ω. At maximum 300Ω or less must be connected if the termination resistance cannot result in 75Ω due to a selector or amplifier of the input stage.

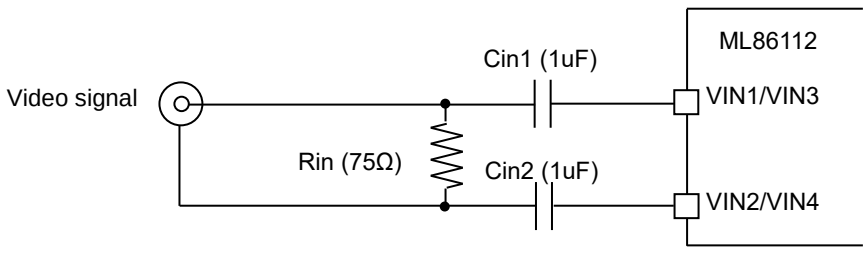
(1) Single end input



Cin: Laminated ceramic capacitor (electrostatic capacity allowance ±10%, temperature characteristics ±10%)
Rin: Resistor (accuracy of ±5%))

(2) Pseudo differential input

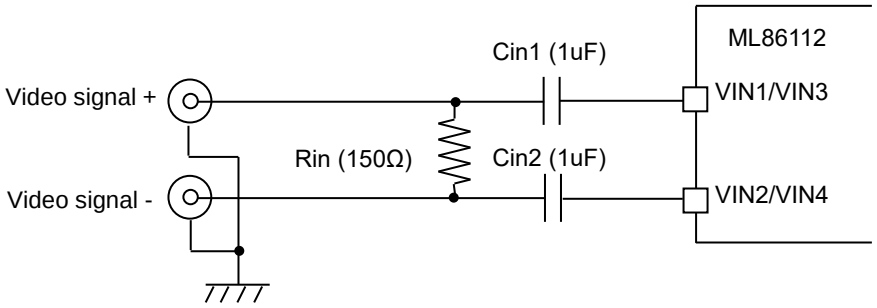
Pseudo differential input can be performed by setting #68h/bit[3:0]=1000 (VIN1, VIN2) or 1001 (VIN3, VIN4), and making the following connection.To perform pseudo differential input, set #30h/bit[3]=1 and #62h/bit[7]=1.



Cin: Laminated ceramic capacitor (electrostatic capacity allowance ±10%, temperature characteristics ±10%)
Rin: Resistor (accuracy of ±5%))

(3) Differential input

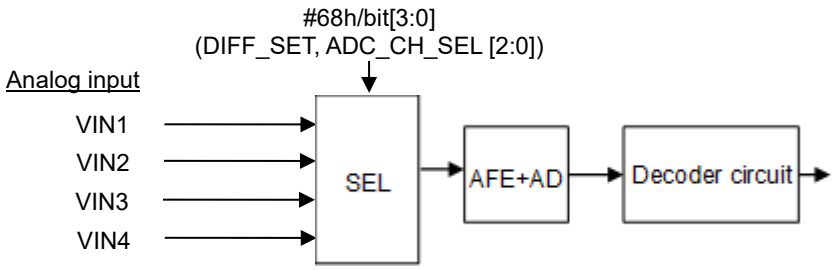
Differential input can be performed by setting #68h/bit[3:0]=1000 (VIN1, VIN2) or 1001 (VIN3, VIN4), and making the following connection. To perform pseudo differential input, set #30h/bit[3]=1 and #62h/bit[7]=1.



Cin: Laminated ceramic capacitor (electrostatic capacity allowance ±10%, Input selection of internal processing circuit(#02Ch ADC_CH_SEL[2:0]) temperature characteristics ±10%)

Rin: Resistor (accuracy of ±5%)

The ML86112 selects and uses one analog video input system to convert to digital video.



Input selection of internal processing circuit (#68h/bit[3:0] DIFF_SET, ADC_CH_SEL[2:0])

Input selection #68h/bit[3:0]	VIN	Input video signal
0000	Single end VIN1	Composite video signal
0001	Single end VIN2	Composite video signal
0010	Single end VIN3	Composite video signal
0011	Single end VIN4	Composite video signal
1000	Differential VIN1(+)VIN2(-)	Composite video signal
1001	Differential VIN3(+)VIN4(-)	Composite video signal
1010-1110	Setting prohibited	-
1111	Analog sleep	-

1.2. Sampling Clock

1.2.1. Sampling Clock Method

Sampling method by line lock PLL.
Because a sampling clock is adjusted to divide a time of one line by a specified clock count, this method has an advantage that the clock count of one line and one frame (field) always obtain a constant output.
However, since traceability is poor for a nonstandard video signal input, a normal output image may not be obtained in some cases.

The clock frequency generated by the built-in HPLL is set by the register, #00h/bit[2:1] (SPMD[1:0]).
Note: When Square-Pixel mode is used, select NTSC or PAL by the register #00h/bit[7:4](VIF[3:0])with above register setting.

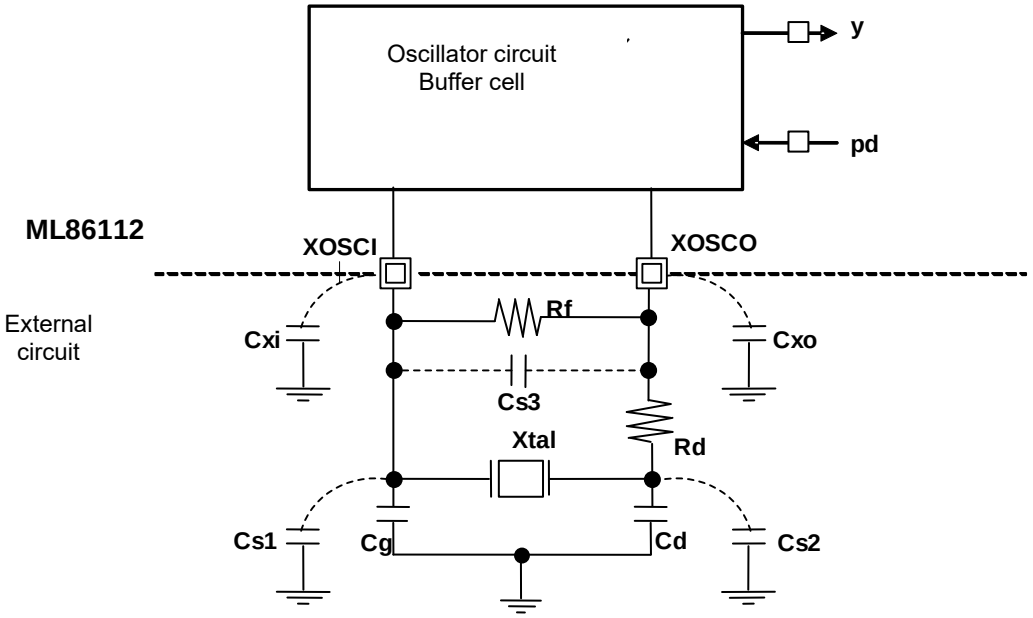
Register #00/bit[2:1]	Sampling Frequency	Supported video method
00	27 MHz	NTSC/PAL (ITU-R BT.601)
01(*)	24.545454 MHz 29.5 MHz	NTSC (Square pixel) PAL (Square pixel)
10	28.6363 MHz 27 MHz	NTSC (4fsc)/ PAL (ITU-R BT.601)
11	-	Setting prohibited

The externally supplied clock frequency can be selected by the register setting, #70h/bit[6:5] (OSC_SEL[1:0]).

Register #70h/bit[6:5]	Input clock frequency
00	32.000 MHz
01	25.000 MHz

1.2.2. External Reference Clock

The following figure shows the external circuit configuration diagram of the external clock to which the internal PLL refers, and an example of the component layout.
Use 32MHz or 25MHz for the frequency of an external crystal oscillator.
To ensure the line clock stability, use an external crystal with the frequency accuracy of 100 ppm or less.



Circuit constants

The following shows an example of the circuit constants to stabilize operation of the above circuit as a reference:

Rf	Rd	Cg(*)	Cd(*)	Load capacity, CL of available oscillator
1MΩ	1kΩ	12pF	12pF	8pF

(*) This value does not include the stray capacitance, Cs1, Cs2, and Cs3, and LSI input capacitance, Cxi and Cxo.
The stray capacitance may vary depending on the wiring pattern of the print board. Their values must be determined by an experiment.
For details, contact the manufacturer of the crystal oscillator.

$$CL \fallingdotseq (Cg + Cs1 + Cxi) // (Cd + Cs2 + Cxo) + Cs3$$
$$= ((Cg + Cs1 + Cxi)*(Cd + Cs2 + Cxo)) / ((Cg + Cs1 + Cxi) + (Cd + Cs2 + Cxo)) + Cs3$$

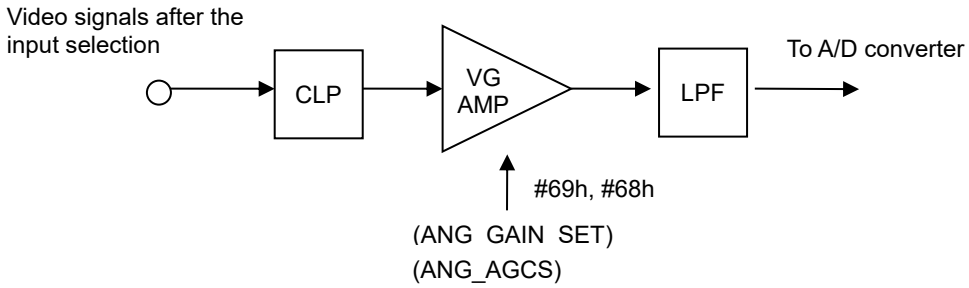
[Note] Modulation noise may occur due to analog signal noise.
In this case, you may need to change the crystal frequency between 32MHz and 25MHz.

1.3. Analog Front End Section (Clamp, LPF, Amplifier)

The analog front end (AFE) performs the following processes:

- Detection of the analog video signal sync chip
- Clamp operation for converting to the built-in ADC input range
- Level adjustment using the analog AGC (Auto Gain Control) function
- Anti-aliasing using the LPF

AGC function has the output level adjustment function of the digital section (luminance block) as well as the input adjustment function by the internal amplifier. Manual gain setting is also available for the internal amplifier.



1.4. CVBS Video Decoder Section

The CVBS video decoder section has Y/C separation, automatic judgment of input signal method, luminance processing, chrominance processing, synchronization processing, VBID detection, and decode data output.

1.4.1. Decimation filter

Decimation filter is a filter to match the data sampled at twice the pixel frequency with the AD converter to the pixel frequency.

1.4.2. YC Separation

Y/C separation function separates the composite video data into Y (luminance) component and C (chrominance) component.
The Y/C separation method is two-dimensional separation method without inter-field calculation. The format of Y/C separation filter used differs depending on the input video signal method. You can specify the mode to select the Y/C separation filter for each signal type.

Mode selection #10h/bit[5:4]	Y/C separation method	
	NTSC	NTSC
00	Adaptive filter	Adaptive filter
01	Three-line comb filter	Three-line comb filter
10	Trap filter	Trap filter
11	Setting prohibited	Setting prohibited

1.4.3. Automatic judgment of input signal method

The CVBS input signal method is discriminated based on the following specifications:

signal format	Number of lines (frames)	Field frequency [Hz]	Sub-carrier frequency (MHz)	Black level (IRE)
NTSC-M	525	59.94	3.58	7.5
NTSC-Japan	525	59.94	3.58	0
PAL-B, B1, D, D1, G, H, I, K	625	50	4.43	0
NTSC-443	525	59.94	4.43	0
PAL-M	525	59.94	3.576	7.5
PAL-N	625	50	4.43	7.5
PAL-Nc	625	50	3.582	0
PAL-60	525	59.94	4.43	0

For input signal methods, you choose to automatically detect from the cycle of horizontal and vertical synchronization signals reproducing from synchronizing separation and the color burst signal or to fix to use the specified format.
The automatic discrimination is available for the input signal methods, NTSC, NTSC-443, PAL, PAL-M, PAL-N, and PAL-Nc.
NTSC-M and NTSC-J cannot be discriminated. Their discrimination depends on the register setting, #00h/bit[7:4] (VIF[3:0]).
NTSC-443 and PAL-60 cannot be discriminated concurrently. The masked video signal is set the register, #04h/bit[7:0].
This automatic discrimination function is enabled when the sampling frequency is 27MHz (ITU-R BT.601) and when the NTSC sampling frequency is set to 4fsc.
If the register, #000h/bit [0] (AVMD) is set to "0", the input video signal method must be set by the register, #00h/bit [7:4] (VIF [3:0]).

Register #00h/bit [7:4]	Input video Method
0 0 0 0	NTSC-M
0 0 0 1	NTSC-J
0 0 1 0	NTSC-443
0 0 1 1	PAL
0 1 0 0	PAL-M
0 1 0 1	PAL-N
0 1 1 0	PAL-Nc
0 1 1 1	PAL-60

1.4.4. Luminance Processing

Level adjustment (AGC) processing is available for Y (luminance) data after Y/C separation.
As the level adjustment, there are digital AGC (Automatic Gain Control) and analog amplifier AGC.
The upper limit of the digital AGC scaling factor is about four times. If the amplitude of input signal is small, analog amplifier AGC adjusts it. The analog amplifier AGC scaling factor is from about 0.608 times to 5.4 times.

Digital AGC refers the depth of SYNC of Y (luminance) data after Y/C separation, and then adjusts the scaling factor of the luminance processing. The control register#31h/bit[7:0] (AGC_REF[7:0]) enables fine adjustment of the luminance level.
In addition, digital MGC (Manual Gain Control) mode which determines luminance scaling factor by the register is available, regardless of depth of SYNC.

Digital AGC/MGC mode is divided into the following combinations, depending on the combination of settings of control registers #30h/bit[7:6] (AGC_FT[1:0]) and#3 0h/bit[4] (LOSET_E):

#30h/bit[7:6]	#30h/bit[4]	動作
00	0	AGC slow
01	0	AGC medium
10	0	AGC fast
11	0	Setting prohibited
XX	1	MGC black level = Pedestal level detected

1.4.5. Chrominance Processing

C (chrominance) data after Y/C separation is separated into two components of Cb and Cr by the chrominance processing section. Chrominance processing section adjusts the level of the data based on the color burst signals (digital ACC: Automatic Color Control), demodulates them by reproducing color sub-carriers based on each video signal format, and then separates them into Cb data and Cr data. The hue of Cb and Cr data can be adjusted.
Chrominace processing is adjusted by the control registers #40h to #49h.

#40h/bit[7:6]	Operation
00	ACC fast
01	ACC slow
10	ACC medium
11	MCC

If the color demodulation is determined not to be performed correctly, the color killer processing (erases colors) is performed.
Color killer processing is adjusted by the control register #43h.

1.4.6. Synchronization Processing Section

Separates into the vertical synchronization signals and the horizontal synchronization signals using Y (brightness) data of composite video data.
Synchronization processing section generates synchronizing separation threshold from input signals automatically, and then generates vertical valid range/horizontal valid range.

Based on the results of horizontal synchronization signals detection and vertical synchronization signal detection, any color display processing on the full screen is performed. Any color display processing is adjusted by the control registers #50h to #54h. Results of the synchronization signal detection (HLOCK) can be monitored by status register #91h bit[1] (ST_HLCK_DT).

HLOCK judgment conditions are shown below.

・When synchronous detection judgement is performed in no input (synchronous non-detection) statement
If the input continues to be detected for the number of continuous fields and the number of continuous lines set in #56h/bit[2:0] (HDET_FLD_R) and #57h/bit[2:0] (HDET_LINE_R), input detection judgment is performed and HLOCK is transed from “L” to “H”.

・When non-input (synchronous non-detection) judgement is performed in the synchronization detection state
If no input is detected for the number of continuous fields and the number of continuous lines set in #56h/bit[6:4] (HDET_FLD_F) and #57h/bit [6:4] (HDET_LINE_F), non-input judgment is performed and HLOCK is transed from “H” to “L”.

The built-in circuit detects the input status of the VTR signal based on pixel errors in the horizontal synchronization detection and line errors in the horizontal synchronization detection. The detection result of the VTR signal input can be monitored by the status register, #91h/bit[5] (ST_VTR_DT).

1.4.7. VBI Data Slicer, Detection of Copy Protection

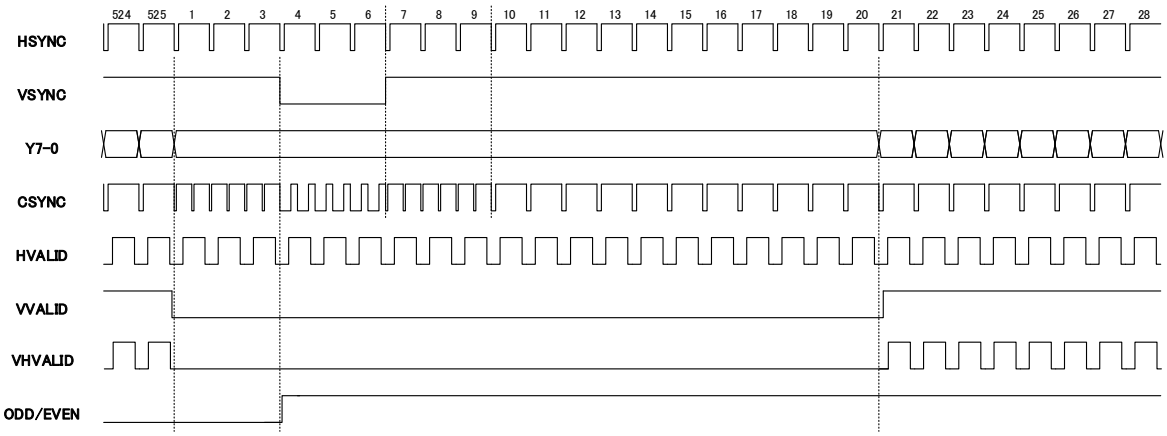
Copy protect information and various data superimposed to the vertical blanking interval (VBI: Vertical Blanking Interval) of input video signals can be extracted and read from the control register.
The following data can be read:

(1) Closed caption
Keeps characters information such as caption, odd number line/even number line (NTSC/PAL)
(2) WSS (Wide Screen Signaling)
Wide video identification signal defined by ETS 300 294 (PAL)
(3) CGMS-A (Copy Generation Management System - Analog)
Copy generation management information defined by IEC61880 (NTSC)

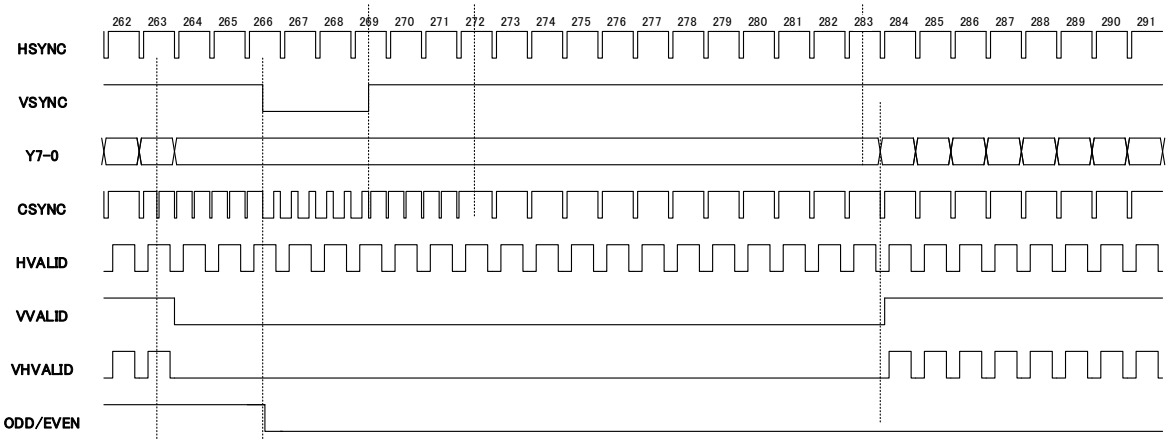
1.4.8. Internal Synchronization Signal Timing

The following shows an internal synchronization signal generated from an input video signal. For details on signals that can be output from the STATUS pin, refer to "5.1 STATUS Pin Output".

◆ NTSC vertical timing

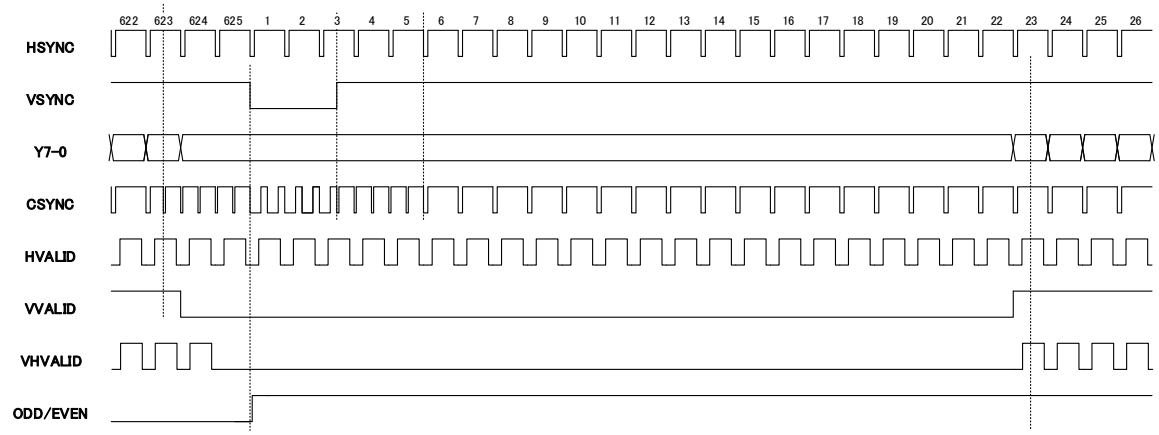


ODD field timing

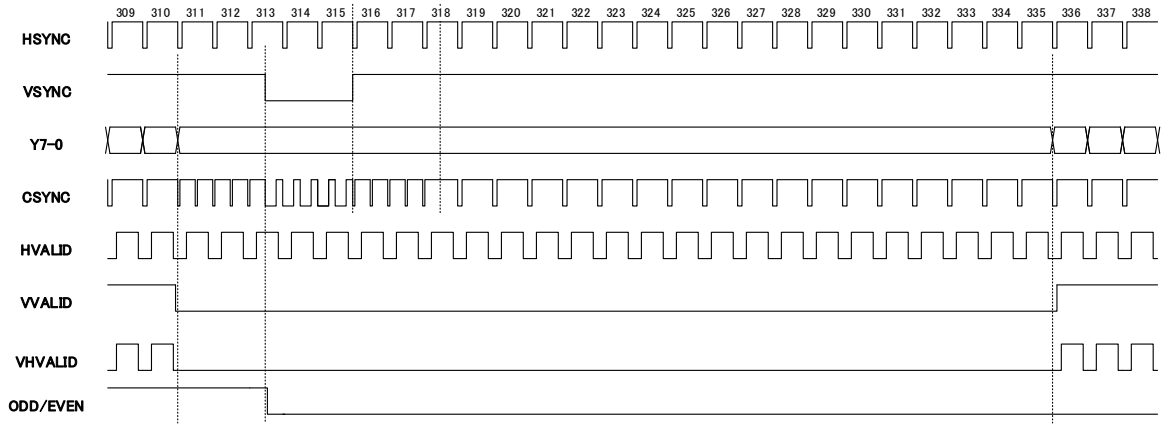


EVEN field timing

◆ PAL vertical timing



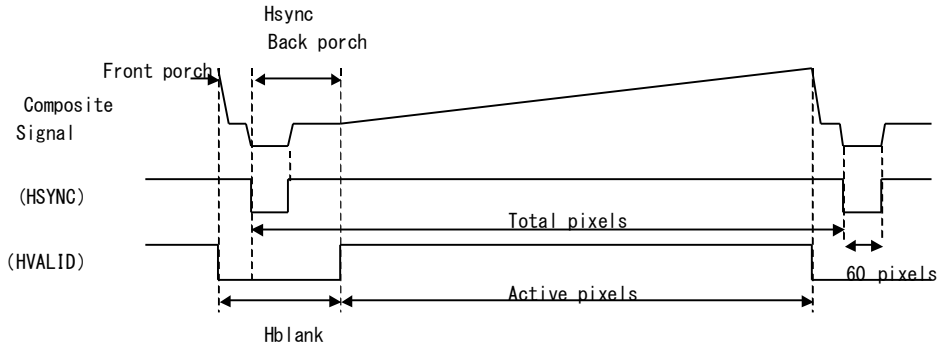
ODD field timing



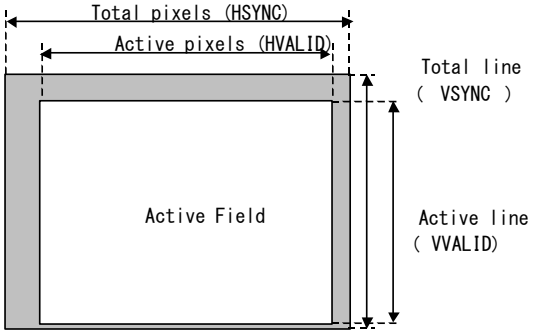
EVEN field timing

1.4.9. Input Video Mode and Number of Pixels/Lines

Synchronization signals of analog video input are reproduced by being separated from the composite synchronization signals that are superimposed on the composite video signals. For the clock, an external input clock or the clock generated by HPLL is used.
(VSYNC, HSYNC, VVALID, and HVALID are internal signals.)



Note: Actually, when the video signal is input , the output is performed after about 1.5 H delay.



The following shows each analog video input and the built-in video decoding pixels and lines:

・Video Mode and Number of Pixels/Lines (at Standard Signal Input)

Input signal format	Sampling frequency	Horizontal (number of pixels)				Vertical (number of lines)		
		Front porch	Back porch	Valid period	1H total	Front porch	Back porch	1V total
NTSC (ITU-R BT.601)	27.000MHz	16	122	720	858	Odd/20 Even/20	Odd/244 Even/243	Odd/262.5 Even/262.5
NTSC (Square pixel)	24.545MHz	22	118	640	780	Odd/20 Even/20	Odd/244 Even/243	Odd/262.5 Even/262.5
NTSC (4FSC)	28.636MHz	16	126	768	910	Odd/20 Even/20	Odd/244 Even/243	Odd/262.5 Even/262.5
PAL (ITU-R BT.601)	27.000MHz	12	132	720	864	Odd/24 Even/25	Odd/288 Even/288	Odd/312.5 Even/312.5
PAL (Square pixel)	29.500MHz	34	154	768	944	Odd/24 Even/25	Odd/288 Even/288	Odd/312.5 Even/312.5

2. Image Quality Adjustment Function

There are the following image quality adjustment functions in the video decoder section:

• Luminance level adjustment	:	Adjusts the level of luminance. AGC (automatic gain control), MGC (manual gain control), and Peak AGC can be set. Related registers #30h, #31h, #33h
• Chrominance level adjustment	:	Adjusts the level of chrominance. ACC (automatic color control) and MCC (manual color control) can be set. Related registers #40h, #41h, #46h, #47h
• Contour correction and coring	:	Corrects contour of analog video input luminance signal. Related registers #35h
• CTI	:	Improves the color level change time of analog video input. Related registers #38h
• Contrast Adjustment	:	Adjustable around 128 with a slope ranging from 1/32 to 63/32. Related registers #36h
• Luminance offset adjustment	:	Brightness can be adjusted between -7 and +7 IRE. Related registers #37h
• Hue control	:	Color phase can be adjusted by the adjustment angle from -178.6 to +180.0° Related registers #45h

3. I/P Conversion

It is possible to perform I/P (interlace/progressive) conversion according to the scanning method (progressive scanning) of used video processing system. The I/P conversion generates interpolation pixels through the intra-field interpolation method that uses two lines.

Register #06h/bit[2]	Register #28h/bit[7:0]	Output
0	00h	Interlace
1	44h	Progressive

The number of output pixels/lines with and without I/P (interlace/progressive) conversion is shown below:

[Without I/P conversion] Video mode and number of output pixels/lines (at standard signal input)

Input signal	Pixel frequency	Horizontal (number of pixels)			Vertical (number of output lines)		
		Blanking period	Valid period	1H Toatl	Blanking period	Valid period	1V Toatl
NTSC (ITU-R BT.601)	13.500MHz	138	720	858	Odd/19 Even/19	Odd/244 Even/243	Odd/262.5 Even/262.5
NTSC (Square pixel)	12.2727MHz	140	640	780	Odd/19 Even/19	Odd/244 Even/243	Odd/262.5 Even/262.5
NTSC (4FSC)	14.318MHz	142	768	910	Odd/19 Even/19	Odd/244 Even/243	Odd/262.5 Even/262.5
PAL (ITU-R BT.601)	13.500MHz	144	720	864	Odd/24 Even/25	Odd/288 Even/288	Odd/312.5 Even/312.5
PAL (Square pixel)	14.750MHz	188	768	944	Odd/24 Even/25	Odd/288 Even/288	Odd/312.5 Even/312.5

[With I/P conversion] Video mode and number of output pixels/lines (at standard signal input)

Input signal	Pixel frequency	Horizontal (number of pixels)			Vertical (number of output lines)		
		Blanking period	Valid period	1H Toatl	Blanking period	Valid period	1V Toatl
NTSC (ITU-R BT.601)	27.000MHz	138	720	858	45	480	525
NTSC (Square pixel)	24.5454MHz	140	640	780	45	480	525
NTSC (4FSC)	28.636MHz	142	768	910	45	480	525
PAL (ITU-R BT.601)	27.000MHz	144	720	864	49	576	625
PAL (Square pixel)	29.500MHz	188	768	944	49	576	625

4. Digital Video Output

MIPI-CSI2 output or LVTTL output can be selected. (# 06h / bit [7])

Register #06h/bit[7]	Outpur
0	MIPI-CSI2
1	LVTTL

4.1. MIPI-CSI2 output

MIPI-CSI2 output can support only 1 lane, YUV422 8bit.

In this product, MIPI CSI-2 output does not support 8b/9b Line Coding and CCI. Also it does not support short packets except Frame Start/End.
In this product, MIPI CSI-2 output is a continuous clock operation. Make sure the MIPI-CSI2 input device is ready to receive before starting MIPI-CSI2 output so that the MIPI-CSI2 input device can detect the MIPI clock.

4.1.1. MIPI-CSI2 Output Pin Swapping

MIPI-CSI2 output pins can be swapped. (#07h/bit[4])

Register	MIPI-CSI2 output pin			
#07h/bit[4]	MTD0P	MTD0N	MTCKP	MTCKN
0	D0P	D0N	CKP	CKN
1	D0N	D0P	CKN	CKP

4.1.2. MIPI-CSI2 Output Control

MIPI-CSI2 data output starts and stops in synchronization with the vertical synchronization signal. MIPI-CSI2 output can be started and stopped with external pins or registers.

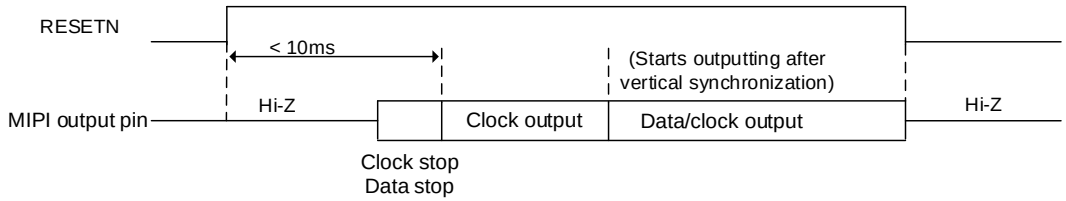
(1) External pin control

Data output can be started/stopped with the external input pins MTPWDN and MTSTP. Use the default values for the registers MIT_ENB (#07h/bit[7]) and MIT_STP (#09h/bit[0]).
"H" represents VDDIO potential while "L" represents GND potential.

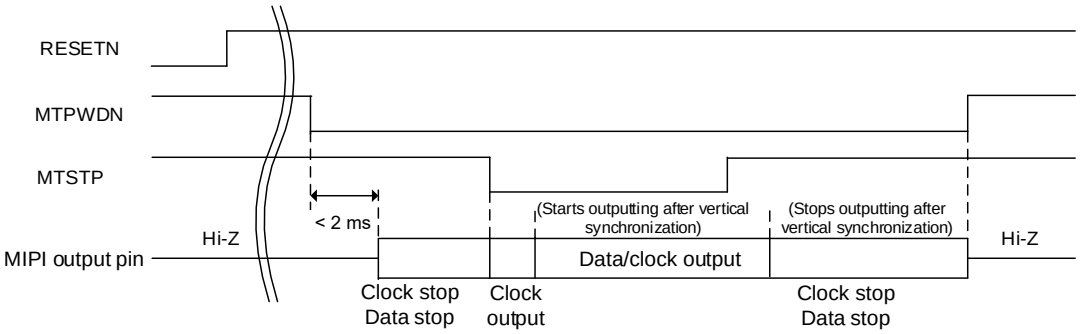
External pin		Register		MIPI-CSI2 internal operation	MIPI-CSI2 output
MTPWDN	MTSTP	MIT_ENB #07h/bit[7]	MIT_STP #09h/bit[0]		
"H"	X	0 (default)	1 (default)	Operation OFF	HiZ
"L"	"H"			Operation ON Output stop	LP11 output
"L"	"L"			Operation ON Normal operation	Normal output

Control sequence example

- When not controlling MIPI-CSI2 output (always outputting)
  With the MTPWDN pin and MTSTP pin fixed to GND, MIPI-CSI2 output can be started just by releasing the reset. Within 10 ms after the reset is released, MTCKP/N output enters the HS mode. Then, data output starts in synchronization with the vertical synchronization signal.



- When controlling MIPI-CSI2 output with pins
  MIPI-CSI2 operation and output can be turned ON/OFF at any timing using the MTPWDN pin and MTSTP pin. MIPI output starts within 2 ms after the MTPWDN pin is set to "L".
  Use the MTSTP pin when the MTPWDN pin is "L".



(2) Register control

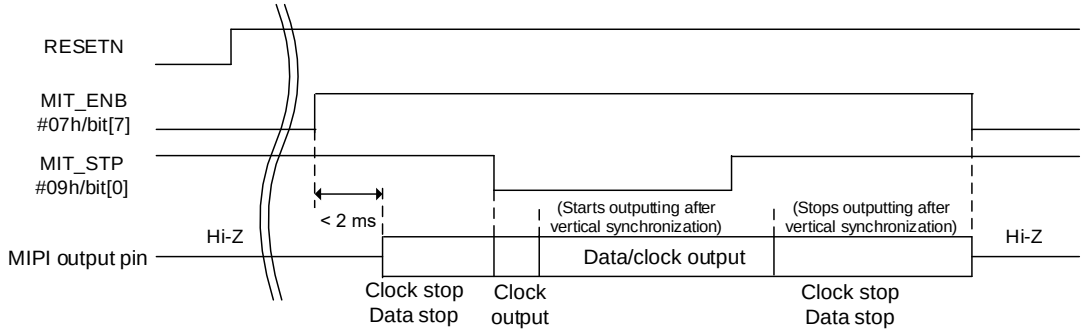
Data output can be started/stopped with registers. Use the MTPWDN pin and MTSTP pin with them set to "H" (VDDIO).

External pin (input)		Register		MIPI-CSI2 internal operation	MIPI-CSI2 output
MTPWDN	MTSTP	MIT_ENB #07h/bit[7]	MIT_STP #09h/bit[0]		
"H"	"H"	0	X	Operation OFF	HiZ
		1	1	Operation ON Output stop	LP11 output
		1	0	Operation ON Normal operation	Normal output

Control sequence example

MIPI output starts within 2 ms after MIT_ENB (#07h/bit[0]) is set to "1".

Use MIT_STP (#09h/bit[0]) when MIT_ENB (#07h/bit[0]) is "1".

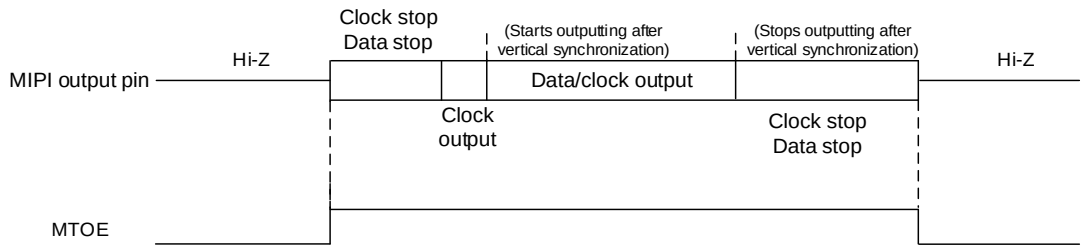


(3) MIPI-CSI2 output status

The MTOE pin allows the monitoring of the MIPI-CSI2 internal status. "H" represents VDDIO potential while "L" represents GND potential.

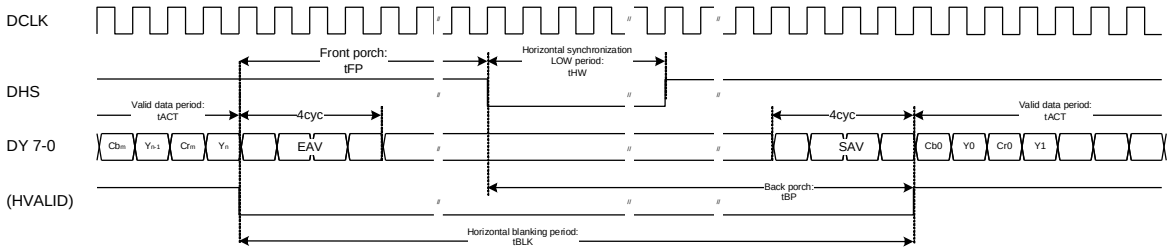
MTOE	MIPI-CSI2 operation
"L"	Operation OFF or startup
"H"	Operation ON Ready for output

MTOE pin output timing



4.2. LVTTL Output (BT.656)

For LVTTL output, output format is BT.656 (8bit) output.
At intrerlace output whithout I/P conversion, video decoding result is output to DCLK and DY7-0 in the format complying with the ITU standard BT.656.
At progressive output with I/P conversion, DCLK and DY7-0 are output in the format in which the BT.656 style SAV and EAV codes are inserted. SAV is added to the data start position and EAV is added to the end position.



*) HSYNC, HVALID is internal signal

Output timing for ITU-BT.656

[Without I/P conversion] Video mode and number of output pixels/lines (at standard signal input)

Input signal	Pixel frequency	Horizontal (number of pixels)			Vertical (number of output lines)		
		Blanking period	Valid period	1H Toatl	Blanking period	Valid period	1V Toatl
NTSC (ITU-R BT.601)	13.500MHz	138	720	858	Odd/19 Even/19	Odd/243 Even/242	Odd/262.5 Even/262.5
NTSC (Square pixel)	12.2727MHz	140	640	780	Odd/19 Even/19	Odd/243 Even/242	Odd/262.5 Even/262.5
NTSC (4FSC)	14.318MHz	142	768	910	Odd/19 Even/19	Odd/243 Even/242	Odd/262.5 Even/262.5
PAL (ITU-R BT.601)	13.500MHz	144	720	864	Odd/24 Even/25	Odd/288 Even/288	Odd/312.5 Even/312.5
PAL (Square pixel)	14.750MHz	188	768	944	Odd/24 Even/25	Odd/288 Even/288	Odd/312.5 Even/312.5

[With I/P conversion] Video mode and number of output pixels/lines (at standard signal input)

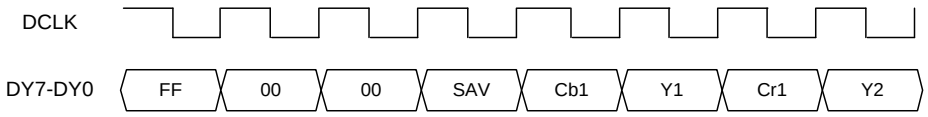
Input signal	Pixel frequency	Horizontal (number of pixels)			Vertical (number of output lines)		
		Blanking period	Valid period	1H Toatl	Blanking period	Valid period	1V Toatl
NTSC (ITU-R BT.601)	27.000MHz	138	720	858	45	480	525
NTSC (Square pixel)	24.5454MHz	140	640	780	45	480	525
NTSC (4FSC)	28.636MHz	142	768	910	45	480	525
PAL (ITU-R BT.601)	27.000MHz	144	720	864	49	576	625
PAL (Square pixel)	29.500MHz	188	768	944	49	576	625

BT.656 output format can be selected from the following formats. Each mode and register setting are shown below.

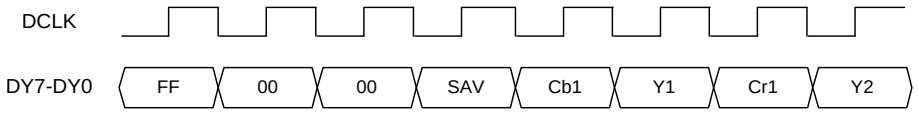
Output format	DDRO_MODE (#03h[1])	DDRO_SEL (#03h[0])	CLK_ INV (#02h[0])	DDRO_CLKPH (#03h[3])
Single Edge output mode rising edge output	0	-	0	-
Single Edge output mode falling edge output (default)	0	-	1	-
Dual Edge output mode1 clock edge output	1	0	-	0
Dual Edge output mode1 clock half-phase output	1	0	-	1
Dual Edge output mode2 clock edge output (rising)	1	1	0	0
Dual Edge output mode2 clock edge output (falling)	1	1	1	0
Dual Edge output mode2 clock half-phase output (rising)	1	1	0	1
Dual Edge output mode2 clock half-phase output (falling)	1	1	1	1

4.2.1. Single Edge output mode

The Single Edge output mode outputs data in synchronization with the rising or falling edge of the clock. Whether to synchronize with a rising clock edge or falling clock edge can be selected in #02h/bit[0].



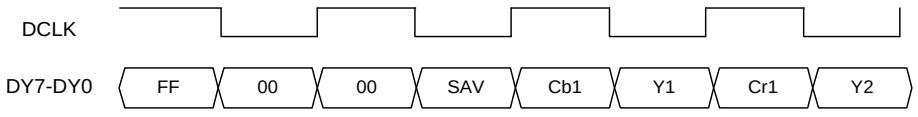
Single Edge rising edge output mode



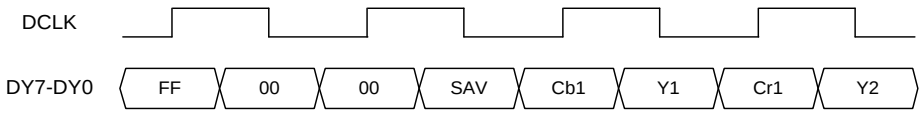
Single Edge falling edge output mode

4.2.2. Dual Edge output mode 1

The Dual Edge output mode 1 outputs data in synchronization with the rising and falling edges of the clock. The #03h/bit[3] setting allows data phase shifted by half a clock.
(The relation between DCLK and DY7-DY0 may be reversed against the figure below.)



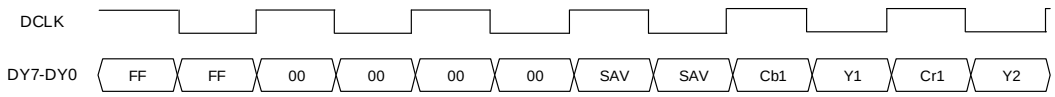
Dual Edge output mode 1 clock edge output mode



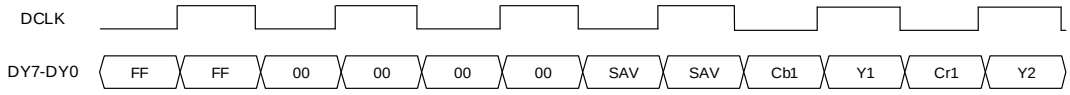
Dual Edge output mode 1 clock half-phase output mode

4.2.3. Dual Edge output mode 2

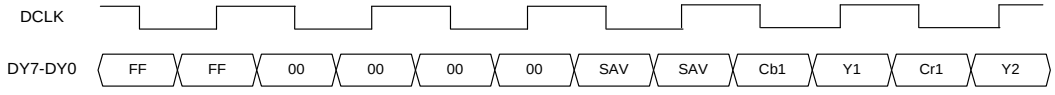
The Dual Edge output mode 2 outputs SAV/EAV every two clocks.
Whether to synchronize the first data of SAV/EAV with a rising clock edge or falling clock edge can be selected in #02h/bit[0]. The #03h/bit[3] setting allows data output out of phase by half a clock.



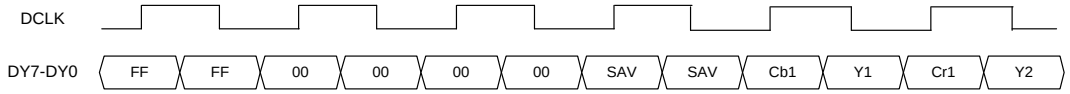
Dual Edge output mode 2 clock edge output mode (rising)



Dual Edge output mode 2 clock edge output mode (falling)



Dual Edge output mode 2 clock clock half-phase output mode (rising)



Dual Edge output mode 2 clock clock half-phase output mode (falling)

5. Status output/interrupt output function

5.1. STATUS pin output

The analog video input status detection result can be output as a status or interrupt from the STATUS pin. The following signals can be output with the STATUS_SEL setting (#78h/bit[7:4]).

Register #78h/bit[7:4]	Output signal	Output logic	
		"L"	"H" (Hi-Z)
0000	HVALID Horizontal valid period	Blanking period (*1)	Valid period (*1)
0001	VVALID Vertical valid period	Blanking period (*1)	Valid period (*1)
0010	ODD/EVEN Field signal	EVEN	ODD
0011	CSYNC Composite sync information	(*1)	
0100	VHVALID Valid area signal	Blanking period (*1)	Valid period (*1)
0101	NTSC/PAL Field frequency judgment signal	NTSC (60Hz)	PAL (50Hz)
0110	HLOCK Sync detection flag	No signal Asynchronous state	Synchronous state
0111	Setting prohibited	-	-
1000	Setting prohibited	-	-
1001	VBID_DET VBID detection flag	Non-detection	Detection
1010	Setting prohibited	-	-
1011	Setting prohibited	-	-
1100	Setting prohibited	-	-
1101	Setting prohibited	-	-
1110	LKFLG HPLL Lock flag	Unlock Unstable state	Lock Stable state
1111	INT Interrupt notification	Notification (*2)	Non-notification (*2)

(*1) Refer to 1.4.8. Internal Synchronization Signal Timing.
(*2) The interrupt notification polarity can be selected with the INT_POL setting (#78h/bit[2]).

5.2. Interrupt Output

Detection information about the synchronization state of analog video input and the lock state of line-lock PLL can be output as an interrupt notification from the STATUS pin.

There are functions to check the current input synchronization state and line-lock state, mask detection information to be reported, and retain and clear the detection result.

(1) Checking the current states

The synchronization state of analog video input and the lock state of line-lock PLL can be checked in the status register 2 (#91h/bit[7:0]). Check the line lock status (ST_LKFLG #91h/bit[6]) after enabling the monitor register (LKFLG_MON #80h/bit[0] = “1”).

Register #91h		Function	Read value
bit[6]	ST_LKFLG	Line-lock state	"1": Locked (stable) "0": Unlocked (unstable)
bit[1]	ST_HLCK_DT	Input synchronization state	"1": Sync (signal detected) "2": Async (no signal detected)

(2) Detection information that can be reported

The following four types of information can be detected:
The line lock state can be detected even when the monitor is disabled (LKFLG_MON #80h/bit[0] = “0”).

- Line-lock state: Lock detected (ST_LKFLG=1 is detected)
- Line-lock state: Unlock detected (ST_LKFLG=0 is detected)
- Input synchronization state: Sync detected (ST_HLCK_DT=1 is detected)
- Input synchronization state: Async detected (ST_HLCK_DT=0 is detected)

(3) Masking detection information

Use the STATUS output setting 2 register (#79h/bit[3:0]) to mask detection information to be reported.
When there are multiple valid detection information (unmasked detection information), if any interrupt cause occurs, a notification is sent.

Register #79h		Interrupt type	Setting value
bit[3]	MASK_LKFLG	Line-lock state: Lock detected	"0": Does not mask the interrupt. "1": Masks the interrupt. (default)
bit[2]	MASK_LKFLG_B	Line-lock state: Unlock detected	
bit[1]	MASK_HDET	Input synchronization state: Signal detected	
bit[0]	MASK_HDET_B	Input synchronization state: No signal detected	

(4) Retaining and clearing the detection result

The result of masked detection information is retained. The retained detection result can be checked in the status clear/status register (#7Ah/bit[3:0]).
Writing "1" to the corresponding bit clears the retained detection result.

Register #7Ah		Interrupt type	Read value
bit[3]	INT_LKFLG	Line-lock state: Lock detected	"0": Detected "1": Not detected (When the state is "0", writing "1" to the bit clears the result.)
bit[2]	INT_LKFLG_B	Line-lock state: Unlock detected	
bit[1]	INT_HDET	Input synchronization state: Signal detected	
bit[0]	INT_HDET_B	Input synchronization state: No signal detected	

(5) Interrupt notification

Detection information can be notified from the STATUS pin. To output notifications, set STATUS_SEL (#78h/bit[7:4])="1111".

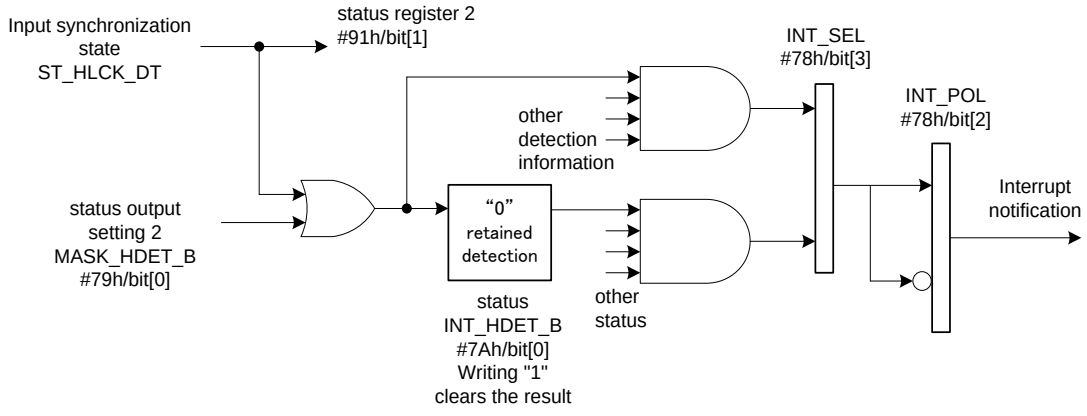
The interrupt level output and the interrupt cause monitoring can be selected as notification operations in INT_SEL (#78h/bit[3]).
The interrupt level output operation continues to send a notification once an interrupt cause occurs until the corresponding bit of the status clear/status register (#7Ah/bit[3:0]) is cleared.
The interrupt cause monitoring operation sends a notification when an interrupt cause occurs and automatically resets the notification when the cause no longer exists.

INT_SEL #78h/bit[3]	Notification operation
0	Interrupt level output
1	Interrupt factor monitor

The polarity of the notification output can be selected with INT_POL (#78h/bit[2]).

INT_POL #78h/bit[2]	STATUS output
0	"L": Notification (active) "H": Not notified
1	"L": Not notified "H": Notification (active)

Structure of the interrupt notification function
Example of input async detected (no signal detected)



5.3. Status register

It is possible to monitor the following condition detection result with status registr #90h to #91h.

- The distinction result of the input format
- The distinction result of the NTSC/PAL field frequency
- The detection existence or non-existence of the VBID
- The detection existence or non-existence of the VTR input signal
- The monitor with input signal synchronous detection condition (HLOCK)
- The monitor of the line-lock by built-in PLL

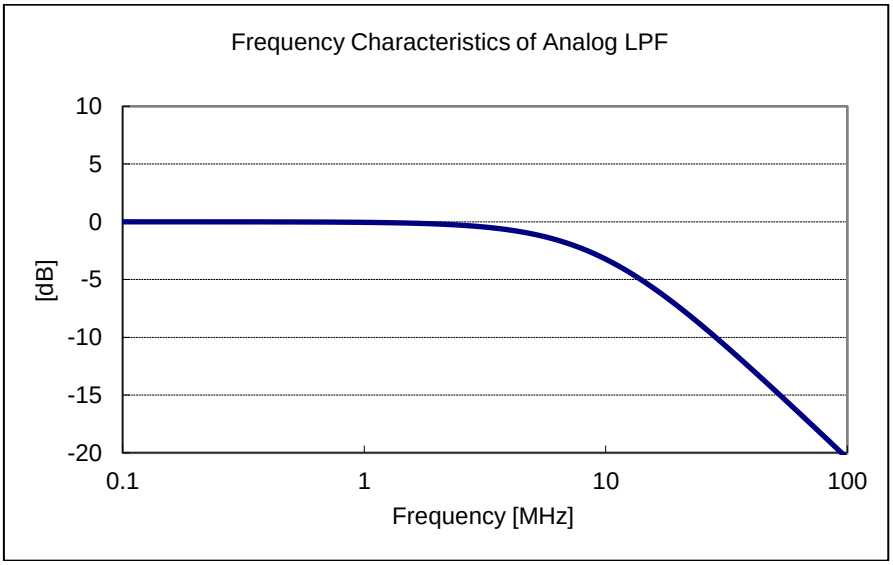
6. Sleep Function

The ML86112 has a sleep function for stopping internal operation and suppressing the power consumption by using the control register (#0Dh/bit[7]).

7. Filter Characteristics

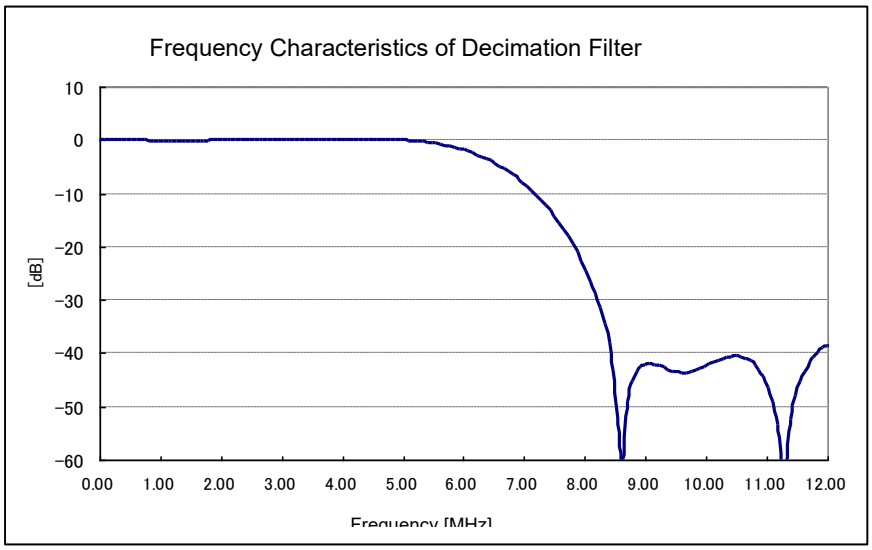
The following figures show the frequency characteristics of various filters.

◆ Analog LPF



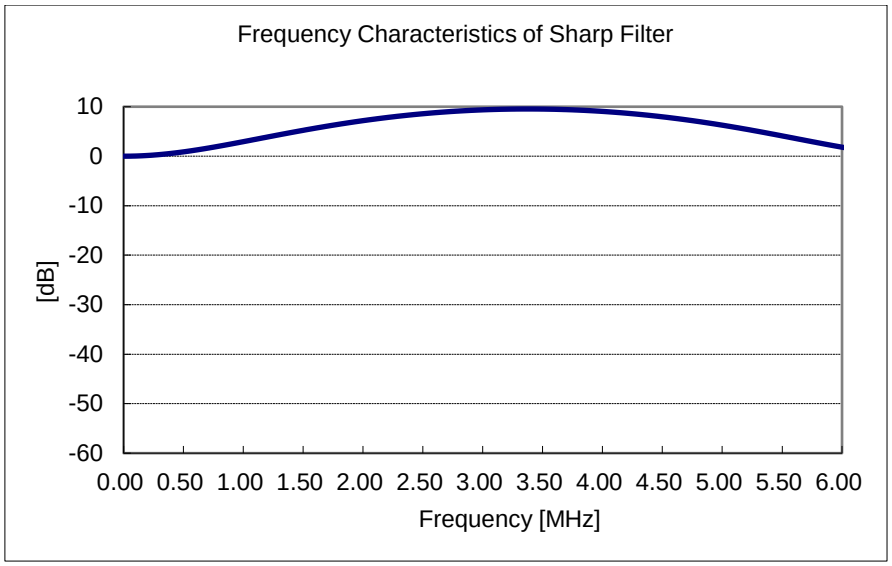
Frequency Characteristics of Analog LPF

◆ Decimation filter



Frequency Characteristics of Decimation Filter

◆Sharp filter



Frequency Characteristics of Sharp Filter

8. I^2C Bus Interface

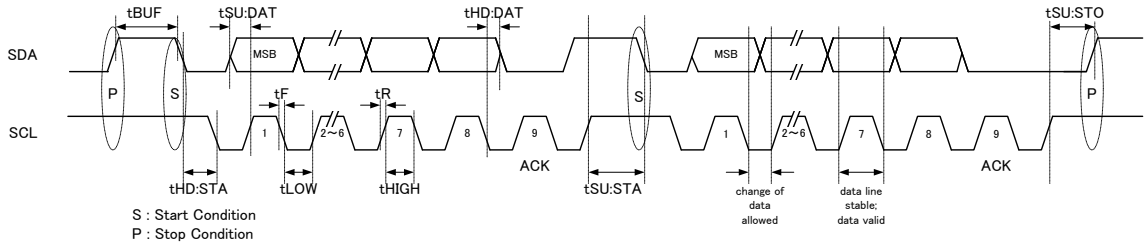
Each function block of the ML86112 controls the operation by writing data to the control register.
These control registers can be accessed through the I^2C bus interface. I^2C bus operation needs clock input to XOSCI.

ML86112 can select slave address via SAS/TAOUT pin.

SAS/TAOUT	Slave address
0	80h (1000_000x)
1	82h (1000_001x)

8.1. I²C Bus Interface Basic Timing

The SDA value should not be changed while SCL is "H" except for the start condition/stop condition (S/P).



I2C Standard Table (Standard Mode)

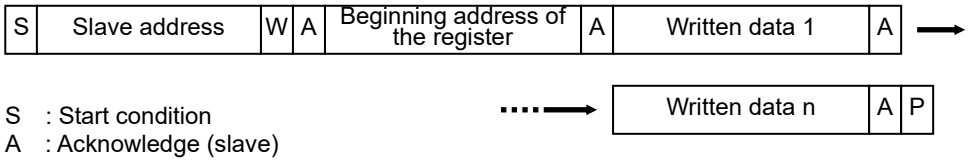
Symbol	Parameter	Min	Typ	Max	Unit
fSCL	SCL frequency	0	-	100	KHz
tBUF	Bus open time	4.7	-	-	µs
tHD:STA	Start condition hold time	4.0	-	-	µs
tLOW	Clock LOW period	4.7	-	-	µs
tHIGH	Clock HIGH period	4.0	-	-	µs
tSU:STA	Start condition setup time	4.7	-	-	µs
tHD:DAT	Data hold time	0(300)	-	-	ns
tSU:DAT	Data setup time	250	-	-	ns
tR	Line rise time	-	-	1000	ns
tF	Line fall time	-	-	300	ns
tSU:STO	Stop condition setup time	4.0	-	-	µs

I2C Standard Table (Fast Mode)

Symbol	Parameter	Min	Typ	Max	Unit
fSCL	SCL frequency	0	-	400	KHz
tBUF	Bus open time	1.3	-	-	µs
tHD:STA	Start condition hold time	0.6	-	-	µs
tLOW	Clock LOW period	1.3	-	-	µs
tHIGH	Clock HIGH period	0.6	-	-	µs
tSU:STA	Start condition setup time	0.6	-	-	µs
tHD:DAT	Data hold time	0(300)	-	-	ns
tSU:DAT	Data setup time	100	-	-	ns
tR	Line rise time	-	-	300	ns
tF	Line fall time	-	-	300	ns
tSU:STO	Stop condition setup time	0.6	-	-	µs

(a) Register Write Format

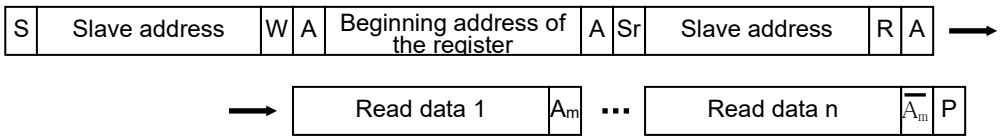
Write data to the specified register address.



S : Start condition
A : Acknowledge (slave)
P : Stop condition
W = "0" (write)

(b) Register Read Format

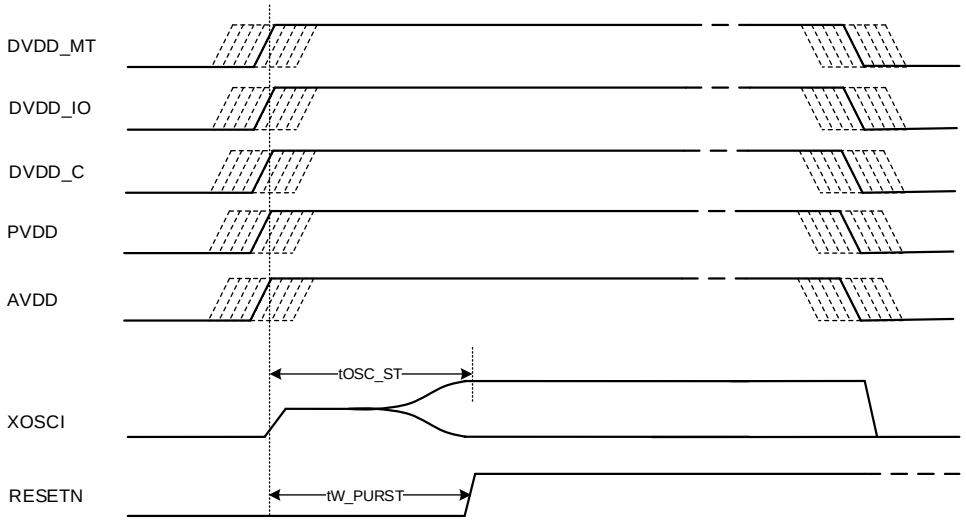
Read data from the specified register address.



S : Start
Sr : Restart
A : Acknowledge (slave)
Am : Acknowledge (master)
P : Stop
W = "0" (write)
R = "1" (read)

■ Power on Sequence

There are no restrictions on power-on and power-off orders among DVDD_MT, DVDD_IO, DVDD_C, PVDD and AVDD.

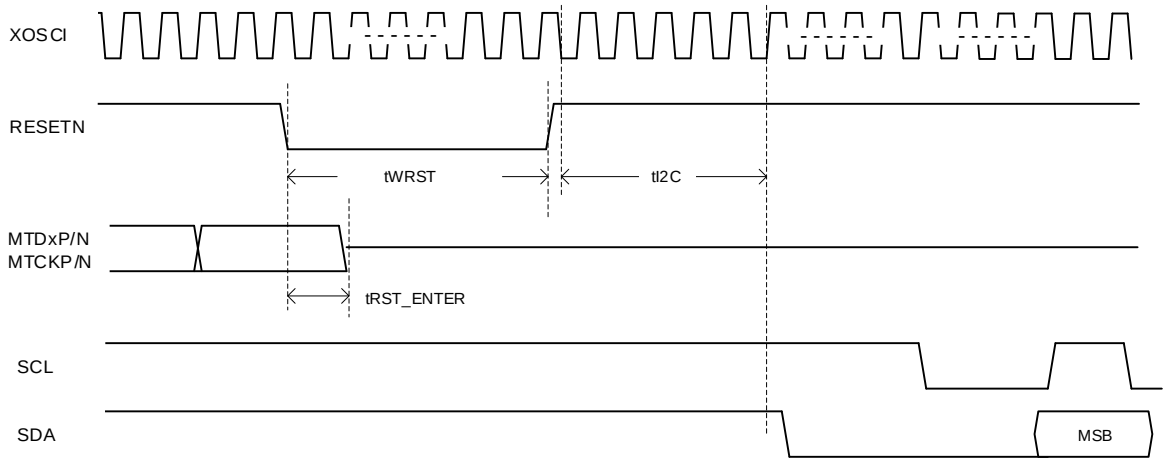


Power on/off flow

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remarks
Time to start oscillation	tOSC_ST	—	—	10	ms	—
Reset time after power on	tW_PURST	10	—	—	ms	—
Internal PLL lock time	—	—	—	10	ms	—
MIPI-Tx- PLL lock time	—	—	—	1	ms	—

When using this LSI, apply the specified voltage to all the power supplies.
Never apply voltage to the input pin before the power-supply voltage becomes stable.
Perform the reset after all the power supplies reached the specified value to input a stable clock.
All the power supplies must be turned off at the power-off.

■ Reset operation



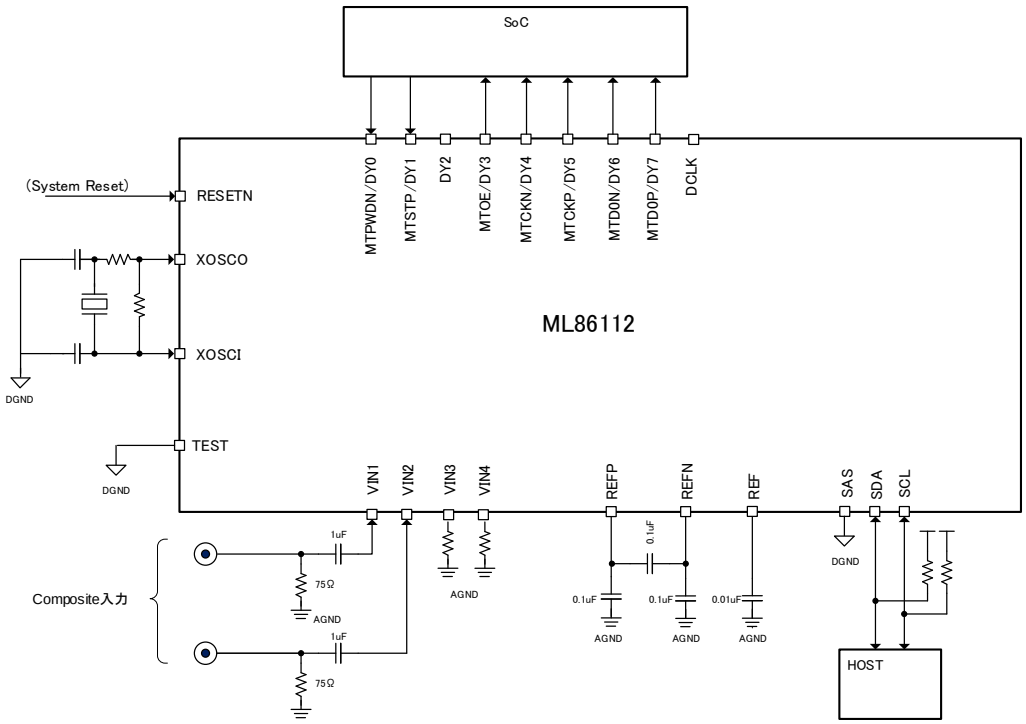
Output delay from the reset release and I^2C access start

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remarks
Reset "L" pulse width (except power on)	tWRST	200	—	—	ns	—
Output stop time from reset	tRST_ENTER	—	—	50	ns	—
I^2C access time	tI2C	5	—	—	CLK	—

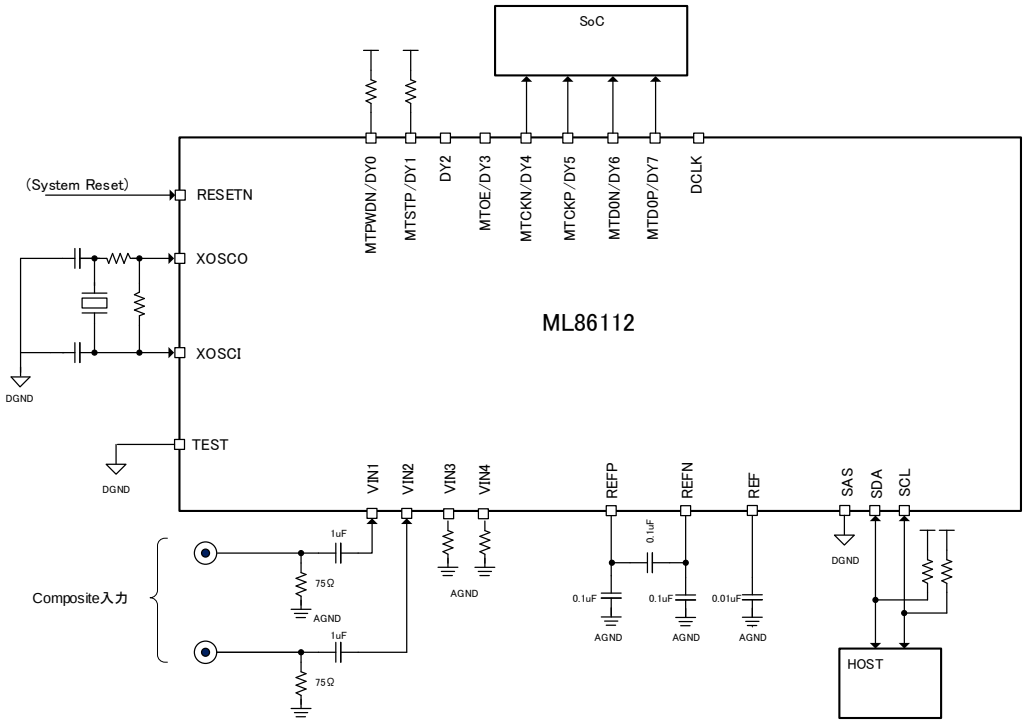
tI2C is the time taken to control the I^2C bus from the reset release.

■ Example of Application Circuit

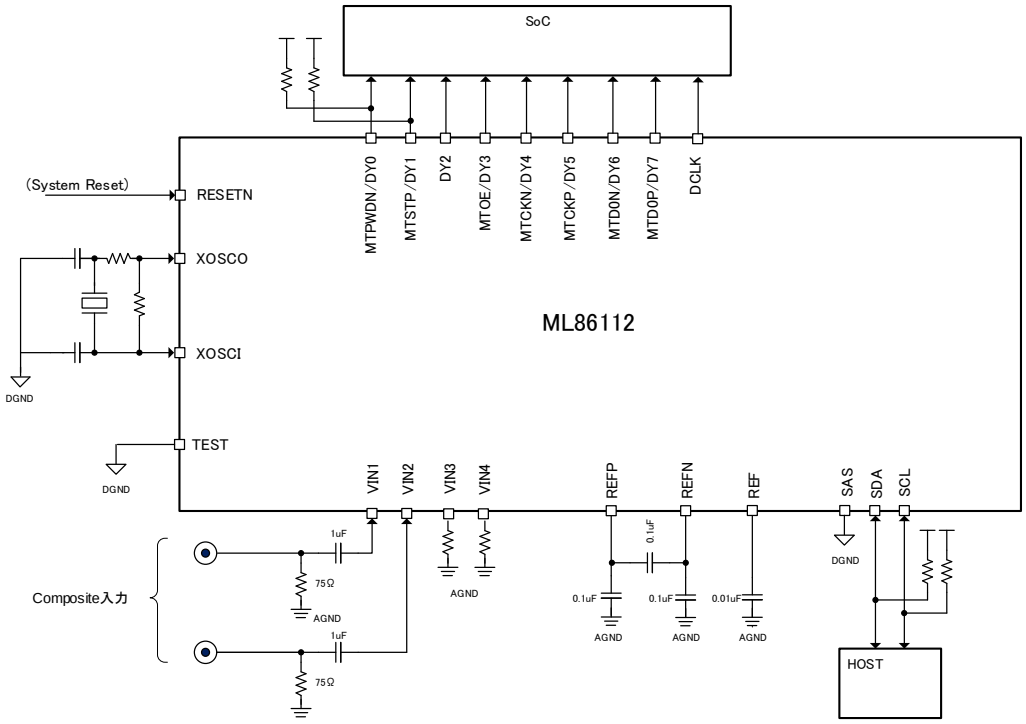
○ Example of Generic Application Circuit (MIPI-CSI2 Output, MTPWDN Output, MTSTP)



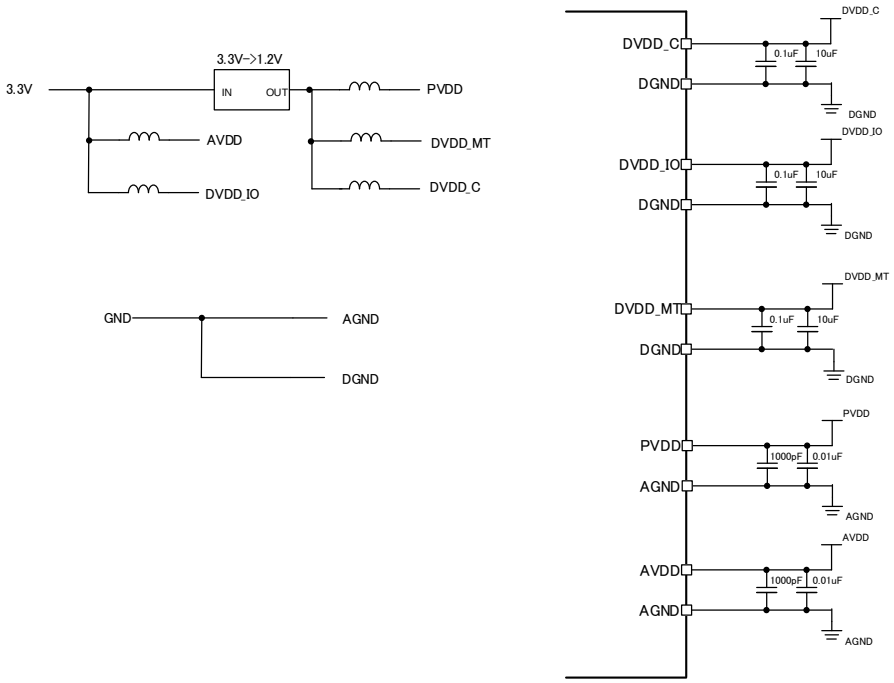
○ Example of Generic Application Circuit (MIPI-CSI2 Output, MIT_ENB, MIT_STP Control)



○ Example of Generic Application Circuit (LVTTL BT.656 Output)



○ Example of Power Supply/ Ground Separation



[Notes on Board Layout]

1. It is recommended to connect ceramic capacitors of about 0.1µF and 10µF between each of digital power supply (DVDD_IO, DVDD_MT, DVDD_C) and digital ground (DGND).
2. It is recommended to connect ceramic capacitors of about 0.1µF and 10µF between analog power supply (AVDD) and analog ground (AGND) and between PLL power supply (PVDD) and.
3. Avoid placing any noise source around the SAS/TAOUT pin
4. Avoid placing any noise source around REF, REFP, and REFN pins. Wire as short as possible.
5. For the analog video signals, shorten the distance from the coupling capacitor to the input pin of the device as much as possible to avoid inducement interference.

The example of the circuit appears here just for the purpose to show the application example, and then does not guarantee its characteristics. When using this LSI, verify the operation with the best suited circuit elements and circuit configurations for your system.
Use the ferrite bead (inductor) between each power supply and GND, if necessary. (It is not always required.)

■ Absolute Maximum Ratings

DGND, AGND = 0V

Item	Item	Condition	Rating	Unit
Power supply voltage (for analog)	AVDD	Ta = 25°C	–0. 3 to +4.6	V
Power supply voltage (for PLL)	PVDD		–0.3 to +2.0	
Power supply voltage (for logic core)	DVDD_C		–0.3 to +2.0	
Power supply voltage (for I/O)	DVDD_IO		–0.3 to +4.6	
Power supply voltage (for MIPI-Tx)	DVDD_MT		–0.3 to +2.0	
Analog input voltage	VAI		–0.3 to AVDD+0.3	
LVTTL input voltage 1	VDI1		–0.3 to DVDD_IO+0.3	
LVTTL input voltage 2 (5 V tolerant)	VDI2		–0.3 to +6.0 (*2)	
MIPI input voltage (*1)	VOM		–0.3 to DVDD_MT+0.3	
Output short-circuit current	IOS	—	16	mA
Power dissipation	PD	Ta = 105°C	0.9	W
Storage temperature	Tstg	—	–55 to +125	°C

Note: Absolute maximum ratings are the marginal values that do not cause physical damage to the device. The device quality might be damaged if the rating of any one of these items is exceeded even for a moment. Be sure to use within this rating.

*1: MIPI output voltage is applied to the following pins.
MTD0P, MTD0A, MTCKP, MTCKN

*2: This is a specification when a power supply voltage is supplied.

■ Recommended Operation Conditions

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Power supply voltage (for analog)	AVDD	AGND = 0 V	3.0	3.3	3.6	V
Power supply voltage (for PLL)	PVDD	AGND = 0 V	1.14	1.2	1.26	
Power supply voltage (for logic core)	DVDD_C	DGND = 0 V	1.14	1.2	1.26	
Power supply voltage (for I/O)	DVDD_IO	DGND = 0 V	3.0	3.3	3.6	
Power supply voltage (for MIPI-Tx)	DVDD_MT	DGND = 0 V	1.14	1.2	1.26	
Ambient temperature	Ta	—	–40	25	+105	°C

Note: Avoid the situation where only some power supplies are powered on/off. All power supplies must be on or off.

■ Electrical Characteristics

DC Characteristics (LVCMOS)

DVDD_IO, AVDD = 3.3V±0.3V
DVDD_MT, PVDD, DVDD_C = 1.2V±0.06V
DGND, AGND = 0V , Ta = -40～+105℃

Item		Symbol	Condition		Min.	Typ.	Max.	Unit
Analog input voltage		VVIN	Capacitance coupling		—	1.3	—	Vpp
Differential analog input voltage		VVIN_dif	Capacitance coupling		—	1.3	—	Vpp
"H" level input voltage 1		VIH1*1	LVTTL		DVDD_IO *0.7	—	DVDD_IO+ 0.3	V
"L" level input voltage 1		VIL1*1	LVTTL		-0.3	—	DVDD_IO *0.3	V
"H" level input voltage 2		VIH2	5V tolerant/Schmitt		2.1	—	5.5	V
"L" level input voltage 2		VIL2	Schmitt		-0.3	—	0.7	V
"H" level output voltage 1		VOH1	IOH = -2, -4mA		2.4	—	—	V
"L" level output voltage 1		VOL1	IOL = 2, 4mA		—	—	0.4	V
"H" level output voltage 2		VOH2*2	IOH = -6mA		2.4	—	—	V
"L" level output voltage 2		VOL2*2	IOL = 6mA		—	—	0.4	V
"H" level output voltage 3		VOH3*4	IOH = -4, -8mA		2.4	—	—	V
"L" level output voltage 3		VOL3*4	IOL = 4, 8mA		—	—	0.4	V
Input leakage current 1		IIL1	VIN = DVDD_IO or DGND		-10	—	+10	µA
Input leakage current 2		IIL2*3	XOSCI=DVDD_IO or DGND		-1.0	—	+1.0	µA
Output leakage current		IOL	VIN = DVDD_IO or DGND		-10	—	+10	µA
"H" level input current (pull-down)		IIHd	VIN = DVDD_IO		20	—	200	µA
Operation current	Analog section	IAVDD	PAL Square Pixel (29.5MHz)	Single End	—	22	30	mA
				Differential	—	25	34	mA
	HPLL section	IPVDD	At 29.5 MHzoscillation		—	1	5	mA
	Logic section	IDVDD_C	PAL Square Pixel I/P conversion (100% color bar image)		—	25	30	mA
	Logic I/O section MIPI-Tx 3.3V	IDVDD_IO	PAL Square Pixel I/P conversion MIPI-Tx output 472Mbps		—	20	27	mA
			PAL Square Pixel I/P conversion LVTTL output CL=10pF		—	25	40	mA
	MIPI-Tx 1.2V	IDVDD_MT	MIPI output 472Mbps		—	10	14	mA
Power down current	Analog section	IAVDD	Input non-selection		—	0.02	0.5	mA
	HPLL section	IPVDD	Oscillation stop		—	0.01	0.2	mA
	Logic section	IDVDD_C	Input/output and clock stop		—	0.05	5.0	mA
	Logic IO section MIPI-Tx 3.3V	IDVDD_IO	Input/output and clock stop		—	0.01	2.0	mA
	MIPI-Tx 1.2V	IDVDD_MT	Input/output stop		—	0.01	2.0	mA

*1: VIH2 and VIL2 is applied to the SCL, SDA and RESETN pins.
*2: VOH2 amd VOL2 is applied to the XOSCO pin.
*3: IIL2 is applied to the XOSCI pin.
*4: VOH3 amd VOL3 is applied to the DCLK pin.

AC Characteristics (LVCMOS)

DVDD_IO, AVDD = 3.3V±0.3V
DVDD_MT, PVDD, DVDD_C = 1.2V±0.06V
DGND, AGND = 0V , Ta = -40 to +105°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
SN ratio	SNR	fin=1 MHz, fck=27MHz	—	50	—	dB
Differentiation linearity error margin	DLE	Lamp wave, fck=1MHz	—	0.5	—	LSB
Integration linearity error margin	ILE	Lamp wave, fck=1MHz	—	0.75	—	LSB

AFE Characteristics

DVDD_IO, AVDD = 3.3V±0.3V
DVDD_MT, PVDD, DVDD_C = 1.2V±0.06V
DGND, AGND = 0V, Ta = -40 to +105°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Gain setting value deviation	ΔG	—	-3.0	—	3.0	dB
Clamp voltage	Vclp	—	—	1.088	—	V
Clamp current	Iclp	When clamp operates	140	280	420	μA
		When clamp is stopped	-3	-7	-15	μA
Common-mode rejection ratio	CMR	When CVBS differential input f=100kHz	—	55	—	dB

Note: The clamp section is 10% or less in one line. Other sections are treated equally as when the clamp is stopped.

AFE + ADC General Characteristics

DVDD_IO, AVDD = 3.3V±0.3V
DVDD_MT, PVDD, DVDD_C = 1.2V±0.06V
DGND, AGND = 0V, Ta = -40 to +105°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Differentiation gain	DG	Input 3.58 MHz	—	3.0	—	%
Differentiation phase	DP	Input 3.58 MHz	—	3.0	—	deg.
Input bandwidth	FC	DC 0dB when the set to 4 MHz	-1.5	—	1.0	dB

PLL Characteristics

DVDD_IO, AVDD = 3.3V±0.3V
DVDD_MT, PVDD, DVDD_C = 1.2V±0.06V
DGND, AGND = 0V, Ta = -40 to +105°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
HPLL frequency	Hvco	At 27MHz sampling setting	—	27.00	—	MHz
HPLL frequency	Hvco	NTSC(Square Pixel)	—	24.5454	—	MHz
HPLL frequency	Hvco	NTSC(4fsc)	—	28.6363	—	MHz
HPLL frequency	Hvco	PAL(Square Pixel)	—	29.50	—	MHz

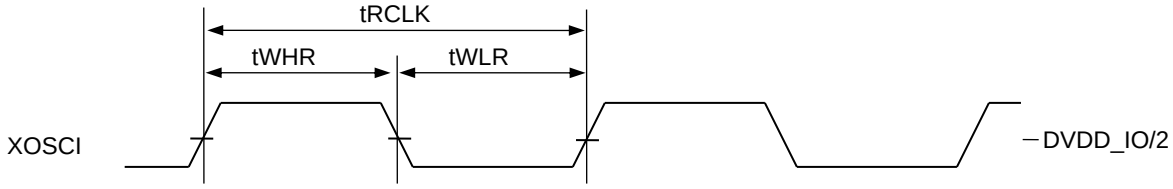
AC Characteristics(LVCMOS)

DVDD_IO, AVDD = 3.3V±0.3V
DVDD_MT, PVDD, DVDD_C = 1.2V±0.06V
DGND, AGND = 0V, Ta = -40 to +105°C

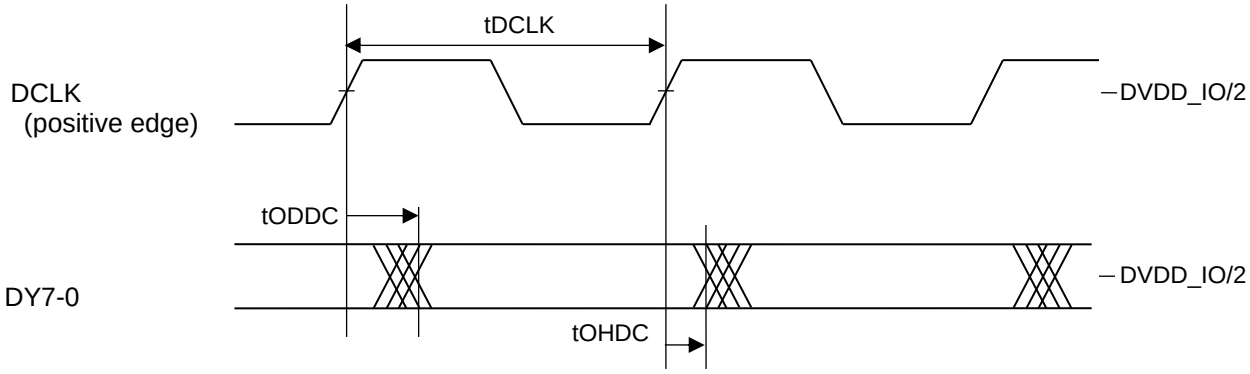
Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Reference clock frequency	fREFCLK	—	—	32	—	MHz
ADC sampling frequency	fADC	—	—	27	—	MHz
XOSCI clock cycle	tRCLK	—	30.0	—	—	ns
XOSCI H level pulse width*1	tWHR	—	12.0	—	—	ns
XOSCI L level pulse width*1	tWLR	—	12.0	—	—	ns
DCLK single output clock cycle	tDCLK	CL=15pF,4mA	16.95	—	—	ns
DCLK dual output clock cycle	tDCLK	CL=15pF,4mA	33.90	—	—	ns
Video output hold time (DCLK→)	tOHDC	CL=15pF,4mA	-3.0	—	—	ns
Video output delay time (DCLK→)	tODDC	CL=15pF,4mA	—	—	3.0	ns
DCLK clock duty ratio	dtDCLK	CL=15pF	40	—	60	%

The characteristics value of the input signal is prescribed using theDVDD_IO or 0V. The output signal characteristics value is measured at the output voltage of DVDD_IO/2.

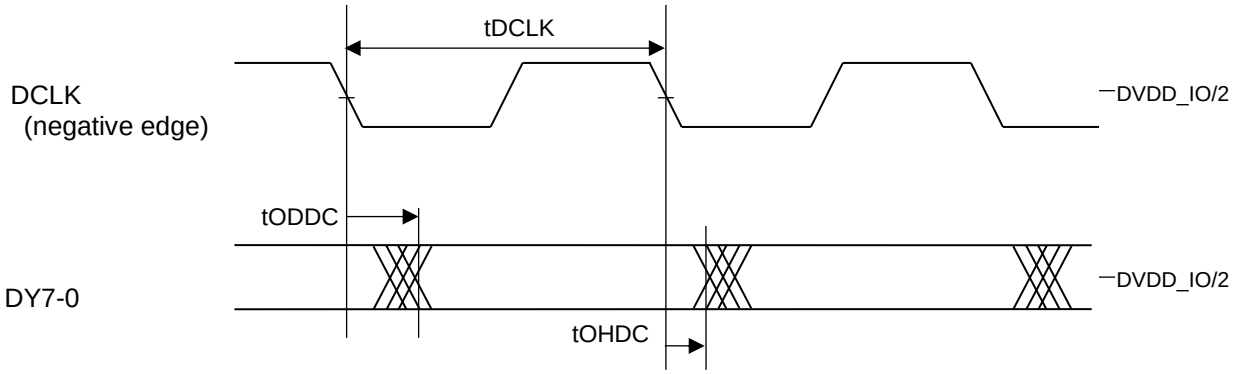
* 1: This is a specification when there is a clock input including the external oscillator. Maximum of 5ns or lower is recommended as the tr/tf of the input clock.



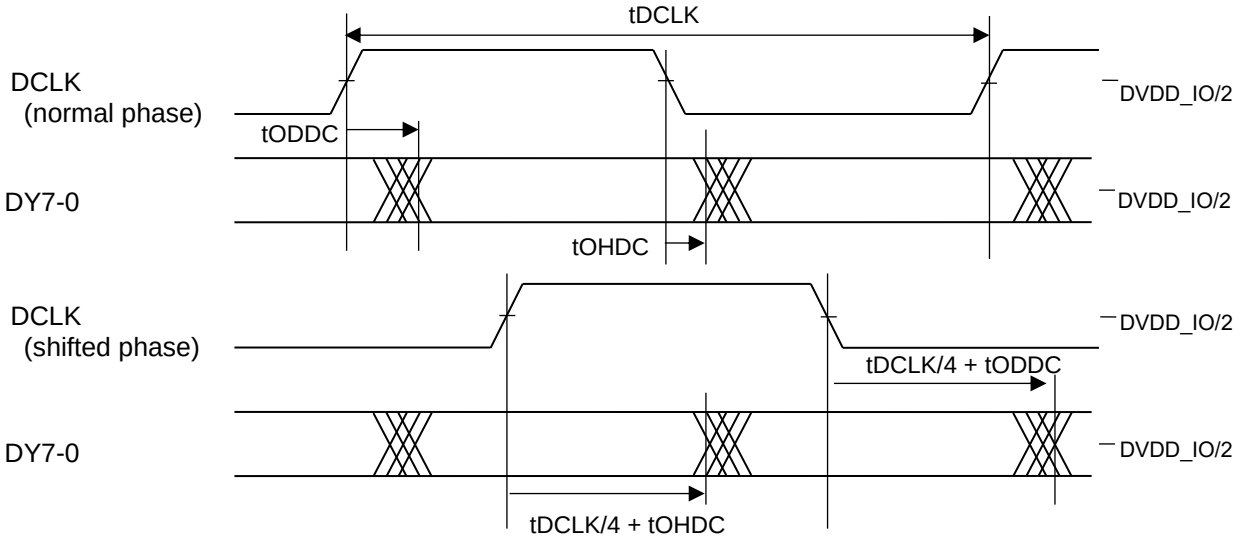
AC Characteristic External Clock System



AC Characteristics Video Output(Single, positive edge)



AC Characteristics Video Output(Single, negative edge)



AC Characteristics Video Output(Dual edge)

DC Characteristics(MIPI output)

DVDD_IO, AVDD = 3.3V±0.3V
DVDD_MT, PVDD, DVDD_C = 1.2V±0.06V
DGND, AGND = 0V, Ta = -40 to +105°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
HS Transmitter						
HS Transmit static common-mode voltage	VCMTX(DC)		150	200	250	mV
HS transmit differential voltage	VOD		140	200	270	mV
HS output high voltage	VOHHS		—	—	360	mV
LP Transmitter						
Thevenin output high level	VOH		1.1	1.2	1.3	V
Thevenin output low level	VOL		-50	—	50	mV
Output impedance of LP transmitter	ZOLP		110	—	—	Ω

AC Characteristics(MIPI output) (*1)

DVDD_IO, AVDD = 3.3V
DVDD_MT, PVDD, DVDD_C = 1.2V
DGND, AGND = 0V, Ta = 25°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
HS Transmitter						
Common-mode variation between above 450MHz	VCMTX(HF)		—	—	15	mVpeak
Common-mode variation between 50MHz-450MHz	VCMTX(LF)		—	—	25	mVpeak
20%-80% rise time and fall time	tR and tF		—	—	0.3	UI
			150	—	—	ps
UI instantaneous	UIINSTTx		2.12	—	5.09	ns
LP Transmitter						
15%-85% rise time and fall time	TRLP/TFLP		—	—	25	ns
30%-85% rise time and fall time	TREOT		—	—	35	ns

*1) MIPI output AC characteristics show the design assurance values. A shipment inspection has not been conducted.

■ Control registers

9. Control registers

The registers of the ML86112 provide control through the I^2C bus.
#00h to #0Fh are related for system control and input/output control, #10h to #76h are related for video decoder, #78h to #AFh are related for status and interrupt, #BCh to #BFh are related for internal test pattern, #C0h to #FFh are related for other control.
The sub-addresses that are not described in Control Register List do not implement any register. Note that an acknowledge is returned if these sub-addresses are accessed.
Various operations such as the image quality adjustment and the mode switching can be set by register control.
Data detected by VBI data detection function can be read sequentially from the control register via the internal registers.
The following section describes each register in the order of each address. A register value with "*" or "(default)" is the initial value.

9.1. Control register list

Register address	W/R	Register name								Initial value	Function
		bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0		
#00h	W/R	VIF[3:0]				(res)	SPMD[1:0]		AVMD	11h	Input signal format
#01h	W/R	(res)				CbCr_EDGE	DSL CEN	CLK_DRV	DO_DRV	00h	Output signal format 1
#02h	W/R	SLEEP_HIZ	(res)	OUT_HIZ	FIELD_INV	(res)			CLK_INV	89h	Output signal format 2
#03h	W/R	(res)				DDRO_CLKPH	(res)	DDRO_MODE	DDRO_SEL	00h	Output signal format 3
#04h	W/R	(res)	VMSK-NTSC-443	(res)	VMSK-PAL-M	VMSK-PAL-N	VMSK-PAL-Nc	VMSK-PAL-60	(res)	5Fh	Input mode auto detection mask
#05h	W/R	(res)								00h	Reserved Register
#06h	W/R	SEL TTL	(res)				IP_OSEL	(res)		00h	Output signal format 4
#07h	W/R	MIT_ENB	(res)		MIT_PN_SEL	(res)				08h	Output signal format 5
#08h	W/R	(res)								08h	Reserved Register
#09h	W/R	(res)	MIT_FIDINV	(res)					MIT_STP	01h	Output signal format 6
#0Ah	W/R	(res)								00h	Reserved Register
#0Bh	-	-								-	-
#0Ch	-	-								-	-
#0Dh	W/R	ALL_PDEN	(res)							00h	Power Down Setting
#0Eh	R	(res)								xxh	Reserved Register
#0Fh	W/R	(res)								00h	Reserved Register
#10h	W/R	(res)		YC_SFM[1:0]		(res)				00h	Y/C separation setting 1
#11h	W/R	(res)					CT_THR	(res)		00h	Y/C separation setting 2
#12h	W/R	(res)		ADP_THR3 [1:0]		ADP_THR2 [1:0]		ADP_THR1 [1:0]		10h	Y/C separation setting 3
#13h	-	-								-	-
#14h	-	-								-	-
#15h	-	-								-	-
#16h	-	-								-	-
#17h	-	-								-	-
#18h	W/R	(res)								C0h	Reserved Register
#19h	-	-								-	-
#1Ah	-	-								-	-
#1Bh	-	-								-	-
#1Ch	-	-								-	-
#1Dh	-	-								-	-
#1Eh	-	-								-	-
#1Fh	-	-								-	-

Register address	W/R	Register name bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Initial value	Function
#20h	W/R	(res)								24h	Reserved Register
#21h	W/R	(res)								0Ch	Reserved Register
#22h	W/R	(res)	FID AINV	(res)						04h	Sync detection setting
#23h	W/R	(res)								1Fh	Reserved Register
#24h	W/R	(res)								C0h	Reserved Register
#25h	W/R	HSDLY[7:0]								00h	Hsync position adjustment
#26h	W/R	HVLDST[3:0]				HVLDSP[3:0]				00h	HVALID position adjustment
#27h	W/R	VVLDST[3:0]				VVLDSP[3:0]				00h	VVALID position adjustment
#28h	W/R	VVLD_IP[7:0]								00h	I/P valid area setting
#29h	W/R	(res)								00h	Reserved Register
#2Ah	W/R	(res)								00h	Reserved Register
#2Bh	-	-								-	-
#2Ch	-	-								-	-
#2Dh	-	-								-	-
#2Eh	-	-								-	-
#2Fh	-	-								-	-
#30h	W/R	AGC_FT[1:0]		(res)	LOSET_E	DIFF_LUM	(res)			50h	AGC setting
#31h	W/R	AGC_REF[7:0]								00h	AGC Reference Setting
#32h	W/R	Y_LMT	(res)							80h	Luminance Output Level Adjustment 1
#33h	W/R	LGAIN_WTPK	(res)							84h	Luminance Output Level Adjustment 2
#34h	W/R	(res)								00h	Reserved Register
#35h	W/R	PRE_FIL	APTR_FIL[1:0]		CORING_SEL [1:0]		APTR_FIL_WT[2:0]			00h	Luminance Output Level Adjustment 3
#36h	W/R	(res)	CTCNT[5:0]						(res)	00h	Contrast setting
#37h	W/R	(res)	LOSET_LV[6:0]							00h	Luminance offset setting
#38h	W/R	CTI_BAND[2:0]			CTI_CORING [1:0]		CTI_GAIN[2:0]			00h	CTI setting
#39h	-	-								-	-
#3Ah	-	-								-	-
#3Bh	-	-								-	-
#3Ch	-	-								-	-
#3Dh	-	-								-	-
#3Eh	-	-								-	-
#3Fh	-	-								-	-

Register address	W/R	Register name bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Initial value	Function
#40h	W/R	ACC_LF_TM[1:0]		(res)						40h	ACC Loop Filter & Chroma Setting
#41h	W/R	ACC_REF[5:0]						(res)		00h	ACC Reference Setting
#42h	W/R	C_LMT	(res)		CFORM	(res)				80h	Chroma Output Level Adjustment
#43h	W/R	CKIL_MD	CKIL TH[1:0]		CKIL_PHS	CKIL_TV	(res)			40h	Color Killer Setting 1
#44h	W/R	(res)								14h	Reserved Register
#45h	W/R	HUE_CNT[7:0]								00h	Hue Control
#46h	W/R	U_LV_CNT[6:0]							(res)	00h	Chroma Cb Level Control
#47h	W/R	V_LV_CNT[6:0]							(res)	00h	Chroma Cr Level Control
#48h	W/R	(res)								80h	Reserved Register
#49h	W/R	(res)								00h	Reserved Register
#4Ah	-	-								-	-
#4Bh	-	-								-	-
#4Ch	-	-								-	-
#4Dh	-	-								-	-
#4Eh	-	-								-	-
#4Fh	-	-								-	-
#50h	W/R	(res)	BB_FMODE	(res)						89h	Free-running Synchronization Output Control 1
#51h	W/R	BB_DSEL[1:0]		(res)						80h	Free-running Synchronization Output Control 2
#52h	W/R	BB_Y[7:0]								26h	Free-running Synchronization Output Control 3
#53h	W/R	BB_CB[7:0]								5Ah	Free-running Synchronization Output Control 4
#54h	W/R	BB_CR[7:0]								ECh	Free-running Synchronization Output Control 5
#55h	W/R	(res)								47h	Reserved Register
#56h	W/R	(res)	HDET_FLD_F[2:0]			(res)	HDET_FLD_R[2:0]			23h	Free-running Synchronization Output Control 6
#57h	W/R	(res)	HDET_LINE_F[2:0]			(res)	HDET_LINE_R[2:0]			41h	Free-running Synchronization Output Control 7
#58h	W/R	(res)								80h	Reserved Register
#59h	-	-								-	-
#5Ah	-	-								-	-
#5Bh	-	-								-	-
#5Ch	-	-								-	-
#5Dh	-	-								-	-
#5Eh	-	-								-	-
#5Fh	-	-								-	-

Register address	W/R	Register name								Initial value	Function
		bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0		
#60h	W/R	LDWID	GLMOD	FMS	(res)			Y_FRC	Y_FMS	00h	FRC Control Setting
#61h	-	-								-	-
#62h	W/R	DIFF_SET2	(res)							20h	Analog Setting 3
#63h	W/R	(res)								34h	Reserved Register
#64h	W/R	(res)								FFh	Reserved Register
#65h	W/R	(res)								00h	Reserved Register
#66h	W/R	(res)								00h	Reserved Register
#67h	-	-								-	-
#68h	W/R	(res)	ANG_AGCS	(res)		DIFF_SET	ADC_CH_SEL[2:0]			A0h	Analog Setting 1
#69h	W/R	(res)		ANG_GAIN_SET[5:0]						7Fh	Analog Setting 2
#6Ah	W/R	(res)								44h	Reserved Register
#6Bh	W/R	(res)								00h	Reserved Register
#6Ch	W/R	(res)								00h	Reserved Register
#6Dh	R	(res)								xxh	Reserved Register
#6Eh	R	(res)								xxh	Reserved Register
#6Fh	W/R	(res)								00h	Reserved Register
#70h	W/R	(res)	OSC_SEL[1:0]		SCFB_SEL	(res)	HS_RNG_SEL	(res)		14h	HPLL Setting 1
#71h	W/R	(res)								80h	Reserved Register
#72h	W/R	(res)								00h	Reserved Register
#73h	W/R	(res)								00h	Reserved Register
#74h	W/R	(res)	LKFLG_FLD_F[2:0]			(res)	LKFLG_FLD_R[2:0]			14h	HPLL Line lock Control 1
#75h	W/R	(res)	LKFLG_LINE_F[2:0]			(res)	LKFLG_LINE_R[2:0]			57h	HPLL Line lock Control 2
#76h	W/R	(res)								8Dh	Reserved Register
#77h	-	-								-	-
#78h	W/R	STATUS_SEL[3:0]				INT_SEL	INT_POL	(res)		60h	STATUS Output Setting 1
#79h	W/R	(res)				MASK_LKFLG	MASK_LKFLG_B	MASK_HDET	MASK_HDET_B	FFh	STATUS Output Setting 2
#7Ah	W&C,R	(res)				INT_LKFLG	INT_LKFLG_B	INT_HDET	INT_HDET_B	xxh	Status Clear / Status
#7Bh	-	-								-	-
#7Ch	-	-								-	-
#7Dh	-	-								-	-
#7Eh	-	-								-	-
#7Fh	-	-								-	-

Register address	W/R	Register name bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Initial value	Function
#80h	W/R	VBID_DT	(res)						LKFLG_MON	00h	VBID Detection Monitor Setting
#81h	-	-								-	-
#82h	W/R	(res)								00h	Reserved Register
#83h	-	-								-	-
#84h	W/R	(res)								00h	Reserved Register
#85h	-	-								-	-
#86h	W/R	(res)								00h	Reserved Register
#87h	-	-								-	-
#88h	W/R	(res)								00h	Reserved Register
#89h	W/R	(res)	RST_C.C_O	RST_C.C_E	RST_CGMS_O	RST_CGMS_E	(res)		RST_WSS	00h	VBID Detection Reset Setting
#8Ah	R	(res)								xxh	Reserved Register
#8Bh	R	(res)								xxh	Reserved Register
#8Ch	R	(res)								xxh	Reserved Register
#8Dh	R	(res)								xxh	Reserved Register
#8Eh	R	(res)								xxh	Reserved Register
#8Fh	R	(res)								xxh	Reserved Register
#90h	R	FLD_FLAG	(res)	NTPAL	(res)	ST_IFM_DET[3:0]				xxh	Status Register 1
#91h	R	ST_RAS_DT	ST_LKFLG	(res)	ST_VBID_DT	(res)		ST_HLCK_DT	(res)	xxh	Status Register 2
#92h	R	(res)	VF_C.C_O	VF_C.C_E	VF_CGMS_O	VF_CGMS_E	(res)		VF_WSS	xxh	VBID Flag Register
#93h	R	C.C_O_DT2[7:0]								xxh	C.C Data buffer Register in ODD Field 2
#94h	R	C.C_O_DT1[7:0]								xxh	C.C Data buffer Register in ODD Field 1
#95h	R	C.C_E_DT2[7:0]								xxh	C.C Data buffer Register in EVEN Field 2
#96h	R	C.C_E_DT1[7:0]								xxh	C.C Data buffer Register in EVEN Field 1
#97h	R	CGMS_O_DT3[7:0]								xxh	CGMS Data buffer Register in ODD Field 3
#98h	R	CGMS_O_DT2[7:0]								xxh	CGMS Data buffer Register in ODD Field 2
#99h	R	C.C_O_P1_ER	C.C_O_P2_ER	(res)	CGMS_O_CRC_ER	CGMS_O_DT1[3:0]				xxh	CGMS Data buffer Register in ODD Field 1
#9Ah	R	CGMS_E_DT3[7:0]								xxh	CGMS Data buffer Register in EVEN Field 3
#9Bh	R	CGMS_E_DT2[7:0]								xxh	CGMS Data buffer Register in EVEN Field 2
#9Ch	R	C.C_E_P1_ER	C.C_E_P2_ER	(res)	CGMS_E_CRC_ER	CGMS_E_DT1[3:0]				xxh	CGMS Data buffer Register in EVEN Field 1
#9Dh	R	WSS_DG2[1:0]		WSS_DG3[2:0]			WSS_DG4[2:0]			xxh	WSS Data buffer Register 2
#9Eh	R	WSS_P_ER	(res)	WSS_DG1[3:0]				WSS_DG2[3:2]		xxh	WSS Data buffer Register 1
#9Fh	R	(res)								xxh	Reserved Register

Register address	W/R	Register name bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Initial value	Function
#A0h	W/R	(res)								82h	Reserved Register
#A1h	W/R	(res)								41h	Reserved Register
#A2h	W/R	(res)								41h	Reserved Register
#A3h	W/R	(res)								82h	Reserved Register
#A4h	W/R	(res)								14h	Reserved Register
#A5h	W/R	(res)								28h	Reserved Register
#A6h	W/R	(res)								28h	Reserved Register
#A7h	W/R	(res)								14h	Reserved Register
#A8h	W/R	(res)								A5h	Reserved Register
#A9h	W/R	(res)								A5h	Reserved Register
#AAh	W/R	(res)								5Ah	Reserved Register
#ABh	W/R	(res)								5Ah	Reserved Register
#ACh	W/R	(res)								A5h	Reserved Register
#ADh	W/R	(res)								A5h	Reserved Register
#AEh	W/R	(res)								5Ah	Reserved Register
#AFh	W/R	(res)								5Ah	Reserved Register
#B0h	-	-								-	-
#B1h	-	-								-	-
#B2h	-	-								-	-
#B3h	-	-								-	-
#B4h	-	-								-	-
#B5h	-	-								-	-
#B6h	-	-								-	-
#B7h	-	-								-	-
#B8h	-	-								-	-
#B9h	-	-								-	-
#BAh	-	-								-	-
#BBh	-	-								-	-
#BCh	W/R	TMDEN	TMDSEL[2:0]			TOPT	TRENB	TGENB	TBENB	00h	Built-in test pattern output setting
#BDh	W/R	TPATCOL[7:0]								00h	Built-in Test Pattern Output Color Setting
#BEh	W/R	(res)								00h	Reserved Register
#BFh	W/R	(res)								00h	Reserved Register

Register address	W/R	Register name bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Initial value	Function
#C0h	W/R	(res)				-		(res)		00h	Reserved Register
#C1h	W/R	(res)								00h	Reserved Register
#C2h	W/R	(res)								00h	Reserved Register
#C3h	W/R	(res)								00h	Reserved Register
#C4h	W/R	-							(res)	00h	Reserved Register
#C5h	W/R	(res)								00h	Reserved Register
#C6h	W/R	-						(res)		00h	Reserved Register
#C7h	-	-								-	-
#C8h	-	-								-	-
#C9h	-	-								-	-
#CAh	W/R	(res)								00h	Reserved Register
#CBh	W/R	(res)								00h	Reserved Register
#CCh	W/R	(res)								00h	Reserved Register
#CDh	W/R	(res)								00h	Reserved Register
#CEh	W/R	(res)								00h	Reserved Register
#CFh	W/R	(res)								00h	Reserved Register
#D0h	W/R	(res)								02h	Reserved Register
#D1h	-	-								-	-
#D2h	W/R	(res)								00h	Reserved Register
#D3h	W/R	(res)								00h	Reserved Register
#D4h	W/R	(res)								00h	Reserved Register
#D5h	W/R	(res)								00h	Reserved Register
#D6h	W/R	(res)								00h	Reserved Register
#D7h	W/R	(res)								00h	Reserved Register
#D8h	W/R	(res)								00h	Reserved Register
#D9h	W/R	(res)								00h	Reserved Register
#DAh	W/R	(res)								00h	Reserved Register
#DBh	W/R	(res)								00h	Reserved Register
#DCh	W/R	(res)								00h	Reserved Register
#DDh	W/R	(res)								00h	Reserved Register
#DEh	W/R	(res)								2Ah	Reserved Register
#DFh	W/R	(res)								0Ah	Reserved Register

Register address	W/R	Register name								Initial value	Function
		bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0		
#E0h	W/R	(res)								00h	Reserved Register
#E1h	W/R	(res)								00h	Reserved Register
#E2h	W/R	(res)								00h	Reserved Register
#E3h	W/R	(res)								00h	Reserved Register
#E4h	W/R	(res)								00h	Reserved Register
#E5h	W/R	(res)								00h	Reserved Register
#E6h	W/R	(res)								00h	Reserved Register
#E7h	W/R	(res)								00h	Reserved Register
#E8h	W/R	(res)								00h	Reserved Register
#E9h	W/R	(res)								00h	Reserved Register
#EAh	W/R	(res)								00h	Reserved Register
#EBh	W/R	(res)								00h	Reserved Register
#ECh	W/R	(res)								00h	Reserved Register
#EDh	W/R	(res)								40h	Reserved Register
#EEh	W/R	(res)								00h	Reserved Register
#EFh	W/R	(res)								00h	Reserved Register
#F0h	W/R	(res)								00h	Reserved Register
#F1h	W/R	(res)								00h	Reserved Register
#F2h	W/R	(res)								00h	Reserved Register
#F3h	W/R	(res)								00h	Reserved Register
#F4h	W/R	(res)								00h	Reserved Register
#F5h	W/R	(res)								00h	Reserved Register
#F6h	-	-								-	-
#F7h	-	-								-	-
#F8h	-	-								-	-
#F9h	-	-								-	-
#FAh	W/R	(res)								80h	Reserved Register
#FBh	W/R	(res)								00h	Reserved Register
#FCh	W/R	(res)								00h	Reserved Register
#FDh	W/R	(res)								00h	Reserved Register
#FEh	W/R	(res)								00h	Reserved Register
#FFh	W/R	(res)								00h	Reserved Register

9.2. Input output control / System control register

9.2.1. Sub Address #00h / Input signal format（W/R）

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#00h	VIF[3:0]				(res)	SPMD[1:0]		AVMD	11h

#00h/bit[7:4] VIF[3:0], Video Input Format Select

It is valid in bit[0] AVMD="0" setting, but bit[0] In AVMD="1" setting (the automatic distinction), too, as for the choice of NTSC-M and NTSC-J, this set value is valid.

"0000": NTSC-M
"0001": NTSC-J (default)
"0010": NTSC443
"0011": PAL
"0100": PAL-M
"0101": PAL-N
"0110": PAL-Nc
"0111": PAL-60
"1000"～ "1111": Setting prohibited

#00h/bit[3] Not defined

Set to "0".

#00h/bit[2:1] SPMD[1:0], Input Sampling Mode Select

This register is for setting the sampling frequency in operating mode.
Operating clock is double.

"00" :	NTSC/PAL	ITU-R BT.601 27MHz (default)
"01" :	NTSC	Square-Pixel 24.5454MHz
	PAL	Square-Pixel 29.5MHz
"10" :	NTSC	4FSC 28.6363MHz
	PAL	ITU-R BT.601 27MHz
"11" :	Setting prohibited	

In square-pixel mode, #00h/bit[0] is "0" and in addition to choose NTSC or PAL in #00h/bit[7:4]

【Note】 When set to "10", PAL is avaliable only auto detection mode (#00h/bit[0] AVMD="1").
NTSC 4FSC is operated when auto detection result is NTSC.
#00h/bit[7:4] VIF[3:0] is valid for selection between NTSC-M and NTSC-J.

#00h/bit[0] AVMD, Auto Video Mode Select

The input video signal format is automatically detected when the sampling frequency of input video signals is set to ITU-R BT.601 or NTSC 4fsc.

The type of the video signal format to be detected can be set by the mask setting in #04h.

0 : Fixed (The setting of #00h/bit[7:4], VIF[3:0] is valid.)
1 : Automatically recognized (default)

The automatic judgement is possible only at the time of "00" or "10" in bit[2:1]SPMD.
By the mask setting of #04h , the input signal to judge can be limited.
The distinction of NTSC-M and NTSC-J follows #00h/bit[7:4] ,VIF[3:0] register.

9.2.2. Sub Address #01h / Output signal format 1 （W/R）

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#01h	(res)				CbCr_ EDGE	DSL CEN	CLK_ DRV	DO_ DRV	00h

#01h/bit[7:4] Not defined

Set to “0000” (Initial value).

#01h/bit[3] CbCr_EDGE、Cb/Cr standard position

It chooses the standard of the chrominance components output in LVTTL(BT.656) mode.

“0” : It outputs CbCr in the standard in EAV. (default)

“1” : It outputs CbCr in the standard in SAV.

#01h/bit[2] DSLCEN、DCLK slew rate control

Controls the slew rate of the DCLK and DY7-0 pins when LVTTL(BT.656) output.
When the slew rate is turned ON, the output change becomes moderate.
The slew rate function is enabled when the drive capacity is 4 mA (DCLK_DRV = "0", DO_DRV ="0").

“0” : Slew rate OFF (default)

“1” : Slew rate ON

#01h/bit[1] CLK_DRV, Drive Ability of DCLK

This register is select the drive ability of the DCLK terminal in LVTTL(BT.656) mode.

“0” : 4mA (default)

“1” : 2mA

#01h/bit[0] DO_DRV, Drive Ability of except DCLK

This register is select the drive ability of the output pin terminal in LVTTL(BT.656) mode.

“0” : 4mA (default)

“1” : 2mA

9.2.3. Sub Address #02h / Output signal format 2 （W/R）

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#02h	SLEEP_HIZ	(res)	OUT_HIZ	FIELD_INV	(res)			CLK_INV	89h

#02h/bit[7] SLEEP_HIZ、Output pin condition at SLEEP

This register is for placing the digital output pins(DY7-0,DCLK) in LVTTL(BT.656) mode and the sleep mode.
The register is avaliable when #02h/bit[5](OUT_HIZ)="0"
When using by the Hi-Z mode, make the output terminal the pull-up or the pull-down.

"0" : High or Low Level（not placed in Hi-Z）
"1" : Hi-Z (default)

#02h/bit[6] Not defined

Set to "0" (Initial value).

#02h/bit[5] OUT_HIZ, Output pin State Select

This register is for placing the digital output pins(DY7-DY0) in Hi-Z during normal operation (SLEEP = "0").
When using by the Hi-Z mode, make the output terminal the pull-up or the pull-down.

"0" : Active (default)
"1" : Hi-Z

#02h/bit[4] FIELD_INV, Field Sync Polarity Select

This register is for inverting the polarity of the field signal at STATUS pin and output field signal in LVTTL(ITU-R BT656) mode .
Field signals ODD and EVEN can be output from the pin STATUS according to the settings of #78h/bit[7:4]STATUS_SEL.

"0" : ODD="H"、EVEN="L" (default)
"1" : ODD="L"、EVEN="H"

#02h/bit[3:1] Not defined

Set to "100" (Initial value).

#02h/bit[0] CLK_INV, Output clock setting

Inverts the clock output(DCLK) logic when LVTTL(BT.656) output.
Refer 4.2 LVTTL output(BT.656) about relation register value and clock, data.

"0" : Positive logic (data synchronizes to the clock rise)
"1" : Negative logic (data synchronizes to the clock fall) (default)

9.2.4. Sub Address #03h / Output signal format 3 （W/R）

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#03h	(res)				DDRO_ CLKPH	(res)	DDRO_ MODE	DDRO_ SEL	00h

#03h/bit[7:4] Not defined

Set to “0000” (Initial value).

#03h/bit[3] DDRO_CLKPH, DDR clock phase selection

Selects the clock and data phase when Dual-Edge is used for LVTTL (BT.656) output. For details on the relationship between setting values and clock/data, refer to the figure in "4.2 LVTTL Output (BT.656)".

“0” : Outputs data in phase with the clock edge. (default)

“1” : Outputs data out of phase by half with the clock edge.

#03h/bit[2] Not defined

Set to “0” (Initial value).

#03h/bit[1] DDRO_MODE、Dual Edge clock output setting

Selects the clock when LVTTL (BT.656) output. For details on the relationship between setting values and clock/data, refer to the figure in "4.2 LVTTL Output (BT.656)".

“0” : Single Edge clock (default)

“1” : Dual Edge clock

#03h/bit[0] DDRO_SEL、Dual Edge operation mode setting

Selects the operation mode when Dual-Edge is used for LVTTL (BT.656) output. Set to “0” when Single edge mode. For details on the relationship between setting values and clock/data, refer to the figure in "4.2 LVTTL Output (BT.656)".

“0” : Dual Edge mode 1 (default)

“1” : Dual Edge mode 2

9.2.5. Sub Address #04h / Input mode auto detection mask（W/R）

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#04h	(res)	VMSK-NTSC-443	(res)	VMSK-PAL-M	VMSK-PAL-N	VMSK-PAL-Nc	VMSK-PAL-60	(res)	5Fh

#04h/bit[7]
Set this register to “0”.

#04h/bit[6] VMSK-NTSC-443
This register is the mask of NTSC-443 mode when automatically detecting the mode of the input video signal. When automatically detecting NTSC-443, mask PAL-60.

“0” : Detect
“1” : Masked (default)

#04h/bit[5]
Set this register to “0”.

#04h/bit[4] VMSK-PAL-M
This register is the mask of PAL-M mode when automatically detecting the mode of the input video signal.

“0” : Detect
“1” : Masked (default)

#04h/bit[3] VMSK-PAL-N
This register is the mask of PAL-N mode when automatically detecting the mode of the input video signal.

“0” : Detect
“1” : Masked (default)

#04h/bit[2] VMSK-PAL-Nc
This register is the mask of PAL-Nc mode when automatically detecting the mode of the input video signal.

“0” : Detect
“1” : Masked (default)

#04h/bit[1] VMSK-PAL-60
This register is the mask of PAL-60 mode when automatically detecting the mode of the input video signal. When automatically detecting PAL-60, mask NTSC-443.

“0” : Detect
“1” : Masked (default)

#04h/bit[0] Not defined
Set to “1” (Initial value)

[Note:]
Since automatic judgment for both NTSC-443 and PAL-60 results in incorrect judgment, mask either of them.

9.2.6. Sub Address #05h / Reserved Register （W/R）

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#05h	(res)								00h

#05h/bit[7:0] Not defined

Set to “00h” (Initial value).

9.2.7. Sub Address #06h / Output signal format 4 （W/R）

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#06h	SELTTL	(res)				IP_OSEL	(res)		00h

#06h/bit[7] SELTTL, Output select

Select output.

“0”: MIPI CSI2 output (default) / “1”: LVTTL BT.656 output

#06h/bit[6:3] Not defined

Set to “0000” (Initial value).

#06h/bit[2] IP_OSEL, Internal IP conversion select

Select internal field IP conversion mode

“0” : Not use internal field IP conversion, interlace output (default)

“1” : Use internal field IP conversion, progressive output

Change #28h/bit[7:0] register when using internal field IP conversion.

#06h/bit[0] Not defined

Set to “0” (Initial value).

9.2.8. Sub Address #07h / Output singal format 5 （W/R）

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#07h	MIT_ENB	(res)		MIT_PN_SEL	(res)				08h

#07h/bit[7] MIT_ENB, MIPI-Tx output setting

Enables MIPI CSI2. output.

This function can also be controlled with the external pin MTPWDN

“0”: MIPI CSI2 OFF (default)/ “1”: MIPI CSI2 ON

#07h/bit[6:5] Not defined

Set to “00” (Initial value).

#07h/bit[4] MIT_PN_SEL, MIPI-Tx port P/N selection

MIPI-TxoutputportPandNcanbeswapped.

“0”: Normal (default)

10 pin: MTD0P

11 pin: MTD0N

12 pin: MTCKP

13 pin: MTCKN

“1”: Swap

10 pin: MTD0N

11 pin: MTD0P

12 pin: MTCKN

13 pin: MTCKP

#07h/bit[3:0] Not defined

Set to “1000” (Initial value).

9.2.9. Sub Address #08h / Reserved Register （W/R）

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#08h	(res)								08h

#08h/bit[7:0] Not defined

Set to “08h” (Initial value).

9.2.10. Sub Address #09h / Output signal format 6 （W/R）

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#09h	(res)	MIT_FIDINV	(res)					MIT_STP	01h

#09h/bit[7] Not defined

Set to “0” (Initial value).

#09h/bit[6] MIT_FIDINV, MIPI-Tx Field invert setting

Toggles the mapping of MIPI CSI2 output Field Number to the field flag between ODD and EVEN.
This setting is valid only for interlace output.

“0”: Normal (default)
ODD / Field Number1
EVEN/ Field Number2

“1”: Invert
ODD / Field Number2
EVEN/ Field Number1

#09h/bit[5:1] Not defined

Set to “00000” (Initial value).

#09h/bit[0] MIT_STP, MIPI-Tx output stop setting

Stops MIPI CSI2 data and clock output.
This function can control by external pin MTSTP.

“0” : Output
“1” : Not output (default)

9.2.11. Sub Address #0Ah / Reserved Register （W/R）

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#0Ah	(res)								00h

#0Ah/bit[7:0] Not defined

Set to “00h” (Initial value).

9.2.12. Sub Address #0Dh/ Power Down Setting （W/R）

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#0Dh	ALL_ PDEN	(res)							00h

#0Dh/bit[7] ALL_PDEN, Power Down Setting

Minimizes the internal operation of the Products to go to the power down mode.
When ALL_PDEN = "1", the synchronization signal and data output of the video output and lcd output are also stopped.
“0” :Normal operation (default) / “1” Power down mode

#0Dh/bit[6:0] Not defined

Set to “0000000” (Initial value).

9.2.13. Sub Address #0Eh / Reserved Register （R only）

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#0Eh	(res)								xxh

#0Eh/bit[7:0] Not defined

“0” or “1” is output when readlng.

9.2.14. Sub Address #0Fh / Reserved Register （W/R）

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#0Fh	(res)								00h

#0Fh/bit[7:0] Not defined

Set to “00h” (Initial value).

9.3. Details of Decoder Section Control Register

9.3.1. Sub Address #10h / Y/C separation setting 1 （W/R）

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#10h	(res)		YC_SFM[1:0]		(res)				00h

#10h/bit[7:6] Not defined

Set to“00” (Initial value).

#10h/bit[5:4] YC_SFM[1:0] , YC Separation Filter Select

This register is filter for separation from composite video signal to luminance(Y) and chrominance(C).

“00”: [NTSC] adaptive / [PAL] adaptive (default)

This filter adaptively selects the 2Line-Comb filter, the 3Line-Comb filter, or the trap filter based on the line-to-line correlation. YC separation characteristics will be improved in both the horizontal and vertical directions.

“01”: [NTSC] Comb filter / [PAL] Comb filter

Filter with good Y/C separation characteristics in the vertical direction.

“10”: [NTSC] Trap filter / [PAL] Trap filte

Filter with good Y/C separation characteristics in the horizontal direction.

“11”: Setting prohibited

YC_SFM [1:0]	NTSC Y/Cseparation method	PAL Y/Cseparation method
00	Adaptive filter	Adaptive filter
01	3line Comb filter	2line Comb filter
10	Trap filte	Trap filte
11	Setting prohibited	Setting prohibited

#10h/bit[3:0] Not defined

Set to “0000” (Initial value).

9.3.2. Sub Address #11h / Y/C separation setting 2 （W/R）

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#11h	(res)					CT_THR	(res)		00h

#11h/bit[7:3] Not defined
Set to “00000” (Intial value).

#11h/bit[2] CT_THR, Y/C Separation , COMB/TRAP filter threshold value select
This register is select the COMB filter or the TRAP filter threshold. of the adaptive filter

“0” : Easy to judge the COMB filter. (default)
“1” : Easy to judge the TRAP filter.

#11h/bit[1:0] Not defined
Set to “00” (Intial value).

9.3.3. Sub Address #12h / Y/C separation setting 3 （W/R）

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#12h	(res)		ADP_THR3[1:0]		ADP_THR2[1:0]		ADP_THR1[1:0]		10h

#12h/bit[7:6] Not defined
Set to “00” (Intial value).

#12h/bit[5:4] ADP_THR3[1:0] , Y/C Separation , The edge judgment threshold value select
This register is select the luminance edge correlation judgment threshold value of the adaptive filter.
When detecting the luminance edge, this filter works by COMB filter.

“00” : Easy to judge the COMB filter.
“01” : ↑ (default)
“10” : ↓
“11” : Easy to judge the TRAP filter

#12h/bit[3:2] ADP_THR2[1:0] , Y/C Separation ,The luminance correlation judgment threshold value select
This register is select the luminance correlation judgment threshold value of the adaptive filter.

“10” : Easy to judge to be in the correlation.
“01” : ↑
“00” : ↓ (default)
“11” : Easy to judge not to be in the correlation.

#12h/bit[1:0] ADP_THR1[1:0] , Y/C Separation ,The chrominance correlation judgment threshold value select
This register is select the chrominance correlation judgment threshold value of the adaptive filter.

“10” : Easy to judge to be in the correlation.
“01” : ↑
“00” : ↓ (default)
“11” : Easy to judge not to be in the correlation.

9.3.4. Sub Address #18h/ Reserved Register （W/R）

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#18h	(res)								C0h

#18h/bit[7:0] Not defined

Set to “C0h” (Initial value).

9.3.5. Sub Address #20h/ Reserved Register （W/R）

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#20h	(res)								24h

#20h/bit[7:0] Not defined

Set to “24h” (Initial value).

9.3.6. Sub Address #21h/ Reserved Register （W/R）

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#21h	(res)								0Ch

#21h/bit[7:0] Not defined

Set to “0Ch” (Initial value).

9.3.7. Sub Address #22h / Sync detection setting （W/R）

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#22h	(res)	FID AINV	(res)						04h

#22h/bit[7] Not defined

Set to “0” (Initial value).

#22h/bit[6] FIDAINV, Automatic Toggle Mode of Field Sync

This register is for automatically inverting the ODD/EVEN signal when an only-odd-fields or only-even-fields signal is input.

When this bit is set to “1”, if consecutive ODD or EVEN fields are found, the ODD/EVEN signal is inverted for each field.

This also toggles the Frame Number for MIPI-CSI2 output and the F flag (field information) for LVTTL (BT.656) output (including progressive output).

“0”: OFF (default) / “1”: ON

#22h/bit[5:0] Not defined

Set to “000100” (Initial value).

9.3.8. Sub Address #23h / Reserved Register （W/R）

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#23h	(res)								1Fh

#23h/bit[7:0] Not defined

Set to “1Fh” (Initial value).

9.3.9. Sub Address #24h / Reserved Register （W/R）

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#24h	(res)								C0h

#24h/bit[7:0] Not defined

Set to “C0h” (Initial value).

9.3.10. Sub Address #25h / Hsync position adjustment （W/R）

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#25h	HSDLY[7:0]								00h

#25h/bit[7:0] HSDLY[7:0], HSYNC output delay

This register is for adjusting the output position of HSYNC_L.

Since VSYNC_L is also adjusted at the same time, the phase between HSYNC_L and VSYNC_L does not change.

Normally, it can be used with the default state.

“0111_1111”: +127 pixel

|

“0000_0000”: 0 pixel (default)

|

“1000_0000”: -128 pixel

9.3.11. Sub Address #26h / HVALID position adjustment （W/R）

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#26h	HVLDST[3:0]				HVLDSP[3:0]				00h

#26h/bit[7:4] HVLDST[3:0], HVALID start position adjustment

This register is used to adjust the rise position of the horizontal valid data period HVALID detected in the analog video input. Normally, it can be used with the default state.

"0111": +7 pixel
|
"0000": 0 pixel (default)
|
"1000": -8 pixel

#26h/bit[3:0] HVLDSP[3:0], HVALID stop position adjustment

This register is used to adjust the fall position of the horizontal valid data period HVALID detected in the analog video input. Normally, it can be used with the default state.

"0111": +7 pixel
|
"0000": 0 pixel (default)
|
"1000": -8 pixel

9.3.12. Sub Address #27h / VVALID position adjustment （W/R）

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#27h	VVLDST[3:0]				VVLDSP[3:0]				00h

#27h/bit[7:4] VVLDST[3:0], VVALID start position adjustment

This register is used to adjust the rise position of the vertical valid data period VVALID detected in the analog video input. Normally, it can be used with the default state.

"0111": +7 line
|
"0000": 0 line (default)
|
"1000": -8 line

#27h/bit[3:0] VVLDSP[3:0], VVALID stop position adjustment

This register is used to adjust the fall position of the vertical valid data period VVALID detected in the analog video input. Normally, it can be used with the default state.

"0111": +7 line
|
"0000": 0 line (default)
|
"1000": -8 line

9.3.13. Sub Address #28h / I/P valid area setting （W/R）

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#28h	VVLD_IP[7:0]								00h

#28h/bit[7:0] VVLD_IP, I/P valid area setting

Select to output operation : interlace operation(#06h/bit[2]="0") or progressive operation(#06h/bit[2]="1").

"00h": Interlace operation (default)

"44h": Progressive operation

Others : Setting prohibited

9.3.14. Sub Address #29h / Reserved Register （W/R）

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#29h	(res)								00h

#29h/bit[7:0] Not defined

Set to "00h" (Initial value).

9.3.15. Sub Address #2Ah / Reserved Register （W/R）

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#2Ah	(res)								00h

#2Ah/bit[7:0] Not defined

Set to "00h" (Initial value).

9.3.16. Sub Address #30h / AGC setting （W/R）

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#30h	AGC_FT[1:0]		(res)	LOSET_E	DIFF_LUM	(res)			50h

#30h/bit[7:6] AGC_FT[1:0], Luminance digital AGC function convergence time setting

Sets the luminance digital AGC function convergence time.

The digital AGC automatically sets a coefficient by assuming the detected SYNC depth to be 40IRE, and then automatically adjust the luminance level according to that coefficient.

This allows the video to always get the constant luminance data level regardless of the different input level.

The convergence time changes by approximately 4 times for each step from Slow through Medium to Fast.

"0000" : Slow AGC mode

"0101" : Medium AGC mode (default)

"1010" : Fast AGC mode

"1111" : Setting prohibited

The gain value is adjusted by #31h/AGC_REF[7:0], and the offset value is adjusted by #37h/LOSET_LV[6:0].

#30h/bit[5] Not defined

Set to "0" (Initial value).

#30h/bit[4] LOSET_E, Luminance data offset setting

Adjusts the luminance by MGC when this bit is set to "1".

The gain value is adjusted by #014h/AGC_REF[7:0], and the offset value is adjusted by #001Ah/LOSET_LV[6:0].

"0" : Luminance offset function OFF (AGC)

"1" : Luminance offset function ON (MGC) (default)

AGC/MGC mode can be categorized as follows based on the combination of the settings of bit[7:6] AGC_FT and bit[4] LOSET_E.

#30/bit[7:6]	#30/bit[4]	Operation
00	0	AGC Slow
01	0	AGC Medium
10	0	AGC Fast
11	0	Setting prohibited
XX	1	MGC

#30h/bit[3] DIFF_LUM, Differential input luminance setting

When differential input(#68h/bit[3]="1"), set to "1".

"0": Single end input (default)

"1": Differential input

#30h/bit[2:0] Not defined

Set to "000" (Initial value).

9.3.17. Sub Address #31h / AGC Reference Setting （W/R）

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#31h	AGC_REF[7:0]								00h

#31h/bit[7:0] AGC_REF[7:0], AGC reference level

Adjusts the slope of luminance level.
The slope is adjusted by using the pedestal level as a starting point.
This setting is enabled in either of the two modes, the digital AGC mode and MGC mode settings.
Gain coefficient at AGC mode is approximately (350 + AGCRC value)/350 times.
Gain coefficient at MGC mode is approximately (227 + AGCRC value)/227 times.

"0111 1111" : Approx. 1.36 times (at AGC), approx. 1.56 times (at MGC)
|
"0000 0000" : Approx. 1 time (at AGC), approx. 1 time (at MGC) (default)
|
"1000 0000" : Approx. 0.63 times (at AGC), approx. 0.44 times (at MGC)

9.3.18. Sub Address #32h / Luminance Output Level Adjustment 1 （W/R）

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#32h	Y_LMT	(res)							80h

#32h/bit[7] Y_LMT, Output luminance data limiter setting

Selects the limit range of the luminance output data.

"0" : Without limit control Luminance output range LVTTL(BT.656)output =1 to 254, MIPI-CSI2 output =0 to 255
"1" : With limit control (default) Luminance output range 16 to 235

#32h/bit[6:0] Not defined

Set to "0000000" (Initial value).

9.3.19. Sub Address #33h / Luminance Output Level Adjustment 2 （W/R）

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#33h	LGAIN_WTPK	(res)							84h

#33h/bit[7] LGAIN_WTPK, Gain adjustment when the luminance level peak detection is performed

Sets the luminance level peak detection.

Adjusts the luminance data gain when the luminance level peak detection is performed.

This setting is enabled only in the AGC mode. Refer to the related register #30h bit[7:6].

"0": ON / "1": OFF (default)

#33h/bit[6:0] Not defined

Set to "000_0100" (Initial value).

9.3.20. Sub Address #34h / Reserved Register （W/R）

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#34h	(res)								00h

#34h/bit[7:0] Not defined

Set to "00" (Initial value).

9.3.21. Sub Address #35h / Luminance Output Level Adjustment 3 （W/R）

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#35h	PRE_FIL	APTR_FIL[1:0]		CORING_SEL[1:0]		APTR_FIL_WT[2:0]			00h

#35h/bit[7] PRE_FIL, Filter for image quality adjustment

This causes the pre-filter and sharp filter to function simultaneously, and emphasizes the frequency around the 3 MHz.
When #33h/bit[7] LGAIN_WTPK = "0" is set, the emphasized frequency around the 3MHz may trigger the luminance level peak detection, resulting in a smaller output level.

"0": OFF (default) / "1": ON

#35h/bit[6:5] APTR_FIL[1:0] , Filter for contour correction

This register is for setting the characteristics of the contour compensation filter.
Use this register in combination with #35h/bit[4:0].
This register chooses the frequency band to emphasize. The frequency of the high area is emphasized as much as the hige range.

"00" : middle range0 (default)
"01" : range1
"10" : range2
"11" : high range3

#35h/bit[4:3] CORING_SEL[1:0] , Coring Range Select

This register is for setting the sensitivity for enhancing the contour component using the contour compensation filter.
Use this register in combination with #35h/bit[6:5] and bit[2:0].
By the data finite difference quantity of the next to each other pixel, the register chooses whether or not to emphasize the line ingredient.

"00" : Always enhanced (default)
"01" : Enhancement sensitivity High (It emphasizes, when even if there is little data finite difference quantity.)
"10" : Enhancement sensitivity Middle
"11" : Enhancement sensitivity Low (It doesn't emphasizes, when even if there is little data finite difference quantity.)

#35h/bit[2:0] APTR_FIL_WT[2:0], Coefficient setting of filter for contour correction

This register is for setting the enhancement level for the contour compensation filter
Used in combination with #35h/bit[6:5] and bit[4:3]. High frequency is emphasized.

"000" : Enhancement level 0 (Contour compensation OFF) (default)
"001" : Enhancement level 1
"010" : Enhancement level 2
"011" : Enhancement level 3
"100" : Enhancement level 4
"101" : Enhancement level 5
"110" : Enhancement level 6
"111" : Enhancement level 7 (Contour is enhanced most significantly）

Note: When emphasizing the edge, the undershoot and the overshoot occur.

9.3.22. Sub Address #36h / Contrast setting （W/R）

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#36h	(res)	CTCNT[5:0]						(res)	00h

#36h/bit[7] Not defined
Set to “0” (Initial value).

#36h/bit[6:1] CTCNT[5:0], Contrast level adjustment
Function to adjust the contrast level. Adjusts the slope around 128.

“01 1111” : 63/32 times (maximum slope)
|
“00 0000” : 32/32 times (default)
|
“10 0001” : 1/32 times (minimum slope)
“10 0000” : Setting prohibited

#36h/bit[0] Not defined
Set to “0” (initial value).

9.3.23. Sub Address #37h / Luminance offset setting （W/R）

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#37h	(res)	LOSET_LV[6:0]							00h

#37h/bit[7] Not defined
Set to “0” (initial value).

#37h/bit[6:0] LOSET_LV, Luminance offset
Sets the offset value added to the luminance level for the pedestal level.
The luminance adjustment can be enabled by setting this register.
“011 1111” : -7 IRE (The luminance level becomes low.)
|
“000 0000” : ±0 IRE (default)
|
“100 0000” : +7 IRE (The luminance level becomes high.)

9.3.24. Sub Address #38h / CTI setting （W/R）

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#38h	CTI_BAND[2:0]			CTI_CORING[1:0]		CTI_GAIN[2:0]			00h

#38h/bit[7:5] CTI_BAND[2:0], CTI limit setting

Sets the limit level for chroma signal contour correction.

The "Large limit value" setting is more emphasized than the "Small limit value" setting.

“000” : Large limit value (default)

“001” : Medium limit value

“010” : Small limit value

Other : Setting prohibited

#38h/bit[4:3] CTI_CORING[1:0], Level setting for the contour correction

Sets intensity for the contour correction object. Used in combination with the [7:5][2:0].

This selects whether or not to emphasize the contour component depending on the data difference between adjacent pixels.

“00” : Always emphasized (default)

“01” : Emphasis sensitivity is strong (The emphasis correction is performed even when the data difference is small)

“10” : Emphasis sensitivity is medium

“11” : Emphasis sensitivity is weak (The emphasis correction is not performed when the data difference is small)

#38h/bit[2:0] CTI_GAIN[2:0], Coefficient setting of filter for contour correction

Sets the emphasis level of the filter for contour correction. Used in combination with the upper bit [7:3].

“000” : Emphasis level 0 (contour correction OFF)(default)

“001” : Emphasis level 1

“010” : Emphasis level 2

“011” : Emphasis level 3

“100” : Emphasis level 4

“101” : Emphasis level 5

“110” : Emphasis level 6

“111” : Emphasis level 7 (most emphasized)

9.3.25. Sub Address #40h / ACC Loop Filter & Chroma Setting (W/R)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#40h	ACC_LF_TM[1:0]		(res)						40h

#40h/bit[7:6] ACC_LF_TM[1:0], Chroma digital ACC function convergence characteristics setting

Sets the chroma digital ACC or MCC mode, and the ACC function convergence time.
The digital ACC automatically sets a coefficient by assuming the detected burst signal amplitude to be 40IRE, and then automatically adjust the chroma data gain according to that coefficient.
This allows the video to always get the constant chroma data level regardless of the different input level.
The convergence time is 4 times faster when comparing between slow and medium , and 64 times between slow and fast.
In MCC mode, the chroma scaling factor is determined based on the register #41h ACC_REF[5:0] regardless of the burst signal amplitude of the input color.

"00" : Fast ACC Mode
"01" : Slow ACC Mode (default)
"10" : Medium ACC Mode
"11" : MCC Mode

#40/bit[5:0] Not defined

Set to "00_0000" (Initial value).

9.3.26. Sub Address #41h / ACC Reference Setting (W/R)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	initial value
#41h	ACC_REF[5:0]						(res)		00h

#41h/bit[7:2] ACC_REF[5:0], ACC reference level

Adjusts the chroma level (color level).
Gain coefficient at ACC mode is approximately (44 + (ACCRC value/4))/44 times.
Gain coefficient at MCC mode is approximately (32 + (ACCRC value/4))/32 times.

"0111 1111" : Approx. 1.7 times (at ACC), approx. 1.97 times (at MCC)
|
"0000 0000" : Approx. 1 times (at ACC), approx. 1 times (at MCC) (default)
|
"1000 0000" : Approx. 0.27 times (at ACC), approx. 0 times (at MCC)

In addition to the above, the level of Cb and Cr signals can be adjusted independently using #46h bit[7:1] U_LV_CNT[6:0] and #47h bit[7:1] V_LV_CNT[6:0]

#41h/bit[1:0] Not defined

Set to "00" (Initial value).

9.3.27. Sub Address #42h / Chroma Output Level Adjustment (W/R)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#42h	C_LMT	(res)		CFORM	(res)				80h

#42h/bit[7] C_LMT, Output chroma data limiter setting

Selects the limit range of the chroma output data.

"0" : Without limit control

Chroma output range LVTTL (BT.656) output = 1 to 254, MIPI-CSI2 output = 0 to 255

"1" : With limit control (default)

Chroma output range 16 to 2400

#42h/bit[6:5] Not defined

Set to "00" (Initial value).

#42h/bit[4] CFORM, Output chroma data format selection

Selects the chroma data output format for LVTTL (BT.656) output.

"0" : offset binary (default)

"1" : 2's complement

#42h/bit[3:0] Not defined

Set to "0000" (Initial value).

9.3.28. Sub Address #43h / Color Killer Setting 1 (W/R)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#43h	CKIL_MD	CKIL TH[1:0]		CKIL_PHS	CKIL_TV	(res)			40h

#43h/bit[7] CKIL_MD, Color killer mode setting

"0" : Automatic color killer mode (default)
Using the setting of the color killer threshold, bit[6:5] CKIL_TH[1:0], output is automatically performed in monochrome based on the color burst signal amplitude level, sub-carrier phase, and TV system automatic judgment.

"1" : Forced color killer mode
Forcibly outputs the chroma data in monochrome.

#43h/bit[6:5] CKIL_TH[1:0], Color killer threshold

Detection setting in the automatic color killer mode (bit[7] CKIL_MD = "0").
When input is NTSC or PAL, the color killer judge level is set as the ratio to the reference color burst signal amplitude level (40IRE).

•In NTSC/PAL input
"00" : 10% or below
"01" : 5% or below
"10" : 3% or below (default)
"11" : Color killer Off

#43 h/bit[4] CKIL_PHS, Color killer sub-carrier phase lock judgment

This is the detection setting in the auto color killer mode (bit [7] CKIL_MD = "0").
Judges if the sub-carrier phase is locked, and performs the color killer if it is not locked.
"0" : OFF (default) / "1 : ON"

#43 h/bit[3] CKIL_TV, Color killer TV system judgment

This is the detection setting in the auto color killer mode (bit [7] CKIL_MD = "0").
Performs color killer if the TV system automatic judgment cannot make a judgment or during judgment.
"0" : OFF (default) / "1 : ON"

#43 h/bit[2:0] Not defined

Set to "000" (Initial value).

9.3.29. Sub Address #44h / Reserved Register (W/R)

Address	bit[7]	bit[6]	bit[5]	bit[4]		bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#44h		(res)								14h

#44h/bit[7:0] Not defined

Set to “14h” (Initial value).

9.3.30. Sub Address #45h / Hue Control (W/R)

アドレス	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	初期値
#45h	HUE_CNT[7:0]								00h

#45h/bit[7:0] HUE_CNT[7:0], Hue adjustment

Adjusts phase. The degree changes by approximately 1.4 per 1 bit. (-178.6°~+180°)

“0111_1111” : -178.6°
|
“0000_0000” : 0° (default)
|
“1000_0000” : +180°

9.3.31. Sub Address #46h / Chroma Cb Level Control (W/R)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	initial value
#46h	U_LV_CNT[6:0]							(res)	00h

#46h/bit[7:1] U_LV_CNT[6:0], Chroma data Cb level adjustment

“011_1111” : 95/32 times
|
“000_0000” : 32/32 times (default)
|
“110_0001” : 1/32 times
“110_0000” : Setting prohibited
|
“100_0000” : Setting prohibited

#46h/bit[0] Not defined

Set to “0” (Initial value).

9.3.32. Sub Address #47h / Chroma Cr Level Control (W/R)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#47h	V_LV_CNT[6:0]							(res)	00h

#47h/bit[7:1] V_LV_CNT[6:0], Chroma data Cr level adjustment

"011_1111" : 95/32 times
|
"000_0000" : 32/32 times (default)
|
"110_0001" : 1/32 times
"110_0000" : Setting prohibited
|
"100_0000" : Setting prohibited

#47h/bit[0] Not defined

Set to "0" (Initial value).

9.3.33. Sub Address #48h - #49h / Reserved Register (W/R)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#48h	(res)								80h
#49h	(res)								00h

#48h/bit[7:0] Not defined

Set to "80h" (Initial value).

#49h/bit[7:0] Not defined

Set to "00h" (Initial value).

9.3.34. Sub Address #50h / Free-running Synchronization Output Control 1(W/R)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#50h	(res)	BB_ FMODE	(res)						89h

#50h/bit[7] Not defined

Set to “1” (Initial value).

#50h/bit[6] BB_FMODE, Forced free-running synchronization output mode setting

Regardless of the input signal, forces the free-running output of the synchronization signal, and outputs the video selected by #51h bit[7:6] BB_DSEL.

Even when in the forced free-running synchronization output mode, the HLOCK signal is detected by the input signal.

When #51h bit[7:6] is set to "10" or "11", the forced free-running synchronization output mode is disabled.

“0” : OFF (default) / “1” : ON

#50h/bit[5:0] Not defined

Set to “00_1001” (Initial value).

9.3.35. Sub Address #51h / Free-running Synchronization Output Control 2 (W/R)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#51h	BB_DSEL[1:0]		(res)						80h

#51h/bit[7:6] BB_DSEL[1:0], Output data selection during free-running synchronization output

Selects the output video data during the free-running synchronization output.

"00" : Any Color (set by #52h-#54h)
"01" : Black
"10" : Input signal (default)
"11" : Input signal (monochrome signal output)

[Note] For the forced free-running synchronization output (#50h bit[6] = "1"), set to any color or black ("00" or "01").

#51h/bit[5:0] Not defined

Set to "00_0000" (Initial value).

9.3.36. Sub Address #52h / Free-running Synchronization Output Control 3(W/R)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#52h	BB_Y[7:0]								26h

#52h/bit[7:0] BB_Y[7:0], Output data setting during free-running synchronization output 1

Sets the level of luminance when the #51h bit[7:6] BB_DSEL is set to "00" (any color).

9.3.37. Sub Address #53h / Free-running Synchronization Output Control 4 (W/R)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#53h	BB_CB[7:0]								5Ah

#53h/bit[7:0] BB_CB[7:0], Output data setting during free-running synchronization output 2

Sets the level of chrominance (Cb) when the #51h bit[7:6] BB_DSEL is set to "00" (any color).
Set the value in two's complement format.

9.3.38. Sub Address #54h / Free-running Synchronization Output Control 5 (W/R)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#54h	BB_CR[7:0]								ECh

#54h/bit[7:0] BB_CR[7:0], Output data setting during free-running synchronization output3

Sets the level of chrominance (Cr) when the #51h bit[7:6] BB_DSEL is set to "00" (any color).
Set the value in two's complement format.

9.3.39. Sub Address #55h / Reserved Register (W/R)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#55h	(res)								47h

#55h/bit[7:0] Not defined

Set to “47h” (Initial value).

9.3.40. Sub Address #56h / Free-running Synchronization Output Control 6 (W/R)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#56h	(res)	HDET_FLD_F[2:0]			(res)	HDET_FLD_R[2:0]			23h

#56h/bit[7] Not defined

Set to “0” (Initial value).

#56h/bit[6:4] HDET_FLD_F[2:0], Synchronization detection setting (field) 1

This setting is used to check the synchronization detection state to judge if it is sync not detected.
It judges the state as sync not detected (#91h[1] ST_HLCK_DT="0") based on the number of consecutive fields set as follows during the no-signal period. The number of inter-field judgment lines is set in #57h/bit[6:4] (HDET_LINE_F).

“000”: No field judgment
(Line judgment only. Line judgment is set in #57h/bit[6:4].)
“001”: 1 Field
“010”: 2 Field (default)
“011”: 5 Field
“100”: 10 Field
“101”: 50 Field
“110”: 100 Field
“111”: 255 Field

#56h/bit[3] Not defined

Set to “0” (Initial valye).

#56h/bit[2:0] HDET_FLD_R[2:0], Synchronization detection setting (field) 2

This setting is used to check the synchronization detection state to judge if it is sync detected.
It judges the state as sync not detected (#91h[1] ST_HLCK_DT="1") based on the number of consecutive fields set as follows during the input-signal period. The number of inter-field judgment lines is set in #57h/bit[2:0] (HDET_LINE_R).

“000”: No field judgment
(Line judgment only. Line judgment is set in #57h/bit[2:0].)
“001”: 1 Field
“010”: 2 Field
“011”: 5 Field (default)
“100”: 10 Field
“101”: 50 Field
“110”: 100 Field
“111”: 255 Field

9.3.41. Sub Address #57h / Free-running Synchronization Output Control 7 (W/R)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#57h	(res)	HDET_LINE_F[2:0]			(res)	HDET_LINE_R[2:0]			41h

#57h/bit[7] Not defined

Set to “0” (Initial value).

#57h/bit[6:4] HDET_LINE_F[2:0], Synchronization detection setting (line) 1

This setting is used to check the synchronization detection state to judge if it is sync not detected.
It judges the state as sync not detected (#91h[1] ST_HLCK_DT="0") based on the number of consecutive lines set as follows during the no-signal period. For any other value than #56h/bit[6:4] (HDET_FLD_F)="000", judgment is made first based on the number of consecutive lines per field in this setting and then the number of consecutive fields according to the HDET_FLD_F setting. If this setting exceeds the total number of lines per field, the total number is used for judgment.
When #56h/bit[6:4] (HDET_FLD_F)= "000", judgment is made only based on the number of consecutive lines in this setting regardless of whether there is a field border.
When # 56h / bit [6: 4] (HDET_FLD_F) = “000” and # 56h / bit [2: 0] (HDET_FLD_R) = “000” are set, # 57h / bit [6: 4] (HDET_LINE_F) and # 57h / bit [2: 0] (HDET_LINE_R) should be set to different values.

“000”: Setting prohibited
“001”: 1 Line
“010”: 2 Line
“011”: 5 Line
“100”: 10 Line (default)
“101”: 100 Line
“110”: 500 Line
“111”: 1000 Line

#57h/bit[3] Not defined

Set to “0” (Initial value).

#57h/bit[2:0] HDET_LINE_R[2:0], Synchronization detection setting (line) 2

This setting is used to check the synchronization detection state to judge if it is sync detected.
It judges the state as sync not detected (#91h[1] ST_HLCK_DT="1") based on the number of consecutive lines set as follows during the input-signal period. For any other value than #56h/bit[2:0] (HDET_FLD_R)="000", judgment is made first based on the number of consecutive lines per field in this setting and then the number of consecutive fields according to the HDET_FLD_R setting. If this setting exceeds the total number of lines per field, the total number is used for judgment.
When #56h/bit[2:0] (HDET_FLD_R)= "000", judgment is made only based on the number of consecutive lines in this setting regardless of whether there is a field border.
When # 56h / bit [6: 4] (HDET_FLD_F) = “000” and # 56h / bit [2: 0] (HDET_FLD_R) = “000” are set, # 57h / bit [6: 4] (HDET_LINE_F) and # 57h / bit [2: 0] (HDET_LINE_R) should be set to different values.

“000”: Setting prohibited
“001”: 1 Line (default)
“010”: 2 Line
“011”: 5 Line
“100”: 10 Line
“101”: 100 Line
“110”: 500 Line
“111”: 1000 Line

9.3.42. Sub Address #58h / Reserved Register (W/R)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#58h	(res)								80h

#58h/bit[7:0] Not defined

Set to “80h” (Initial value).

9.3.43. Sub Address #60h / FRC Control Setting (W/R)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#60h	LDWID	GLMOD	FMS	(res)			Y_FRC	Y_FMS	00h

#60h/bit[7] LDWID, Selection of output data bit width

When LVTTL (BT.656) output, select the effective number of bits of data output to DY7-DY0.
In 6bit mode, use DY7-DY2 as a valid bit. SAV and EAV are output in 8bit.

"0": 8bit mode (default)
"1": 6bit mode

#60h/bit[6] GLMOD, Selection of output data gray scale mode

This setting is valid when bit [7] (LDWID) = "1" (6bit mode).
When LVTTL (BT.656) output, select rounding processing and multi-gradation processing (brightness only) of the output data.

"0": Rounded mode (default)
"1": Multi-gradation

#60h/bit[5] FMS, Selection of output data Multi-gradation mode

This setting is valid when bit [7] (LDWID) = "1" (6bit mode).
When LVTTL (BT.656) output, select the multi-gradation mode of output data.
It is used when the ML86112 outputs interlace signal. Set "0" (initial value) for progressive output.

"0": When field processing is performed by interlaced / progressive conversion in the latter stage (default)
"1": When line-doubler processing is performed by interlaced / progressive conversion in the latter stage

#60h/bit[4:2] Not defined

Set to "000" (Initial value).

#60h/bit[1] Y_FRC, Selection of internal luminaces data gray scale mode

Select rounding processing and multi-gradation processing of the internal luminance data.

"0": Rounded mode (default)
"1": Multi-gradation

#60h/bit[0] Y_FMS, Selection of internal luminance data Multi-gradation mode

Select the multi-gradation mode of internal luminance data.
It is used when the ML86112 outputs interlace signal. Set "0" (initial value) for progressive output.

"0": When field processing is performed by interlaced / progressive conversion in the latter stage (default)
"1": When line-doubler processing is performed by interlaced / progressive conversion in the latter stage

9.3.44. Sub Address #62h / Analog Setting 3 (W/R)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#62h	DIFF_SET2	(res)							20h

#62h/bit[7] DIFF_SET2, Differential input setting 2
Set to "1" when differential input (#68h/bit[3]="1").
"0": Single-ended input (default)
"1": Differential input

#62h/bit[6:0] Not difined
Set to "0100000" (Initial value).

9.3.45. Sub Address #63h - #66h / Reserved Register (W/R)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#63h	(res)								34h
#64h	(res)								FFh
#65h	(res)								00h
#66h	(res)								00h

#63h/bit[7:0] Not defined
Set to "34h" (Initial value).
#64h/bit[7:0] Not defined
Set to "FFh" (Initial value).
#65h/bit[7:0] Not defined
Set to "00h" (Initial value).
#66h/bit[7:0] Not defined
Set to "00h" (Initial value).

9.3.46. Sub Address #68h / Analog Setting 1 (W/R)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	initial value
#68h	(res)	ANG_ AGCS	(res)		DIFF_ SET	ADC_CH_SEL[2:0]			A0h

#68h/bit[7] Not defined

Set to “1” (Initial value).

#68h/bit[6] ANG_AGCS, Analog AGC function setting

Detects the SYNC level, and automatically adjusts the amplifier gain.

In the manual mode, #69h/bit[5:0](ANG_GAIN_SET[5:0]) is used to set the amplifier gain.

“0” : Manual setting (default) / “1” : Automatic setting

#68h/bit[5:4] Not defined

Set to “10” (Initial value).

#68h/bit[3] DIFF_SET, Differential input setting

This setting uses a differential analog signal.

“0”: Single-ended input (default) / “1”: Differential input

To perform differential input (# 68h / bit [3] = “1”), set # 30h / bit [3] = 1 and # 62h / bit [7] = 1.

#68h/bit[2:0] ADC_CH_SEL[2:0], Analog Input Select

This register is used to select the input pin for analog video signals.

Select one of the following according to the differential input setting #68h/bit[3] (DIFF_SET).

“0000”: CVBS1 VIN1 (default)
“0001”: CVBS2 VIN2
“0010”: CVBS3 VIN3
“0011”: CVBS4 VIN4
“1000”: Differential CVBS1 VIN1(Positive) VIN2(Negative)
“1001”: Differential CVBS2 VIN3(Positive) VIN4(Negative)
“1111”: Sleep
Others : Setting prohibited

To perform differential input (# 68h / bit [3] = “1”), set # 30h / bit [3] = 1 and # 62h / bit [7] = 1.

9.3.47. Sub Address #69h / Analog Setting 2 (W/R)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#69h	(res)		ANG_GAIN_SET[5:0]						7Fh

#69h/bit[7:6] Not defined

Set to "01" (Initial value).

#69h/bit[5:0] ANG_GAIN_SET[5:0], Analog amplifier gain manual setting

Gain setting when the analog amplifier gain is set in manual mode.

The gain value is a design value.

"00_0000" : 0 Maximum gain

|

"11_1111" : 63 Minimum gain (default)

Register #69h/bit[5:0]	Setting Value	gain
00_0000	0	5.40
00_0010	2	4.32
00_0100	4	3.60
00_0111	7	2.88
00_1011	13	2.06
01_0000	16	1.80
01_0110	22	1.44
01_1101	29	1.17
10_0110	37	0.96
11_0001	49	0.76
11_1111 (*)	63	0.61

(*) default value

[Calculation formula] Gain = 0.6 x 504 / (7 x Setting Value + 56)

9.3.48. Sub Address #6Ah - #6Ch / Reserved Register (W/R)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#6Ah	(res)								44h
#6Bh	(res)								00h
#6Ch	(res)								00h

#6Ah/bit[7:0] Not defined
Set to “44h” (Initial value).
#6Bh/bit[7:0] Not defined
Set to “00h” (Initial value).
#6Ch/bit[7:0] Not defined
Set to “00h” (Initial value).

9.3.49. Sub Address #6Dh - #6Eh / Reserved Register (R only)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#6Dh	(res)								xxh
#6Eh	(res)								xxh

#6Dh/bit[7:0] Not defined
“0” or “1” is output when reading.
#6Eh/bit[7:0] Not defined
“0” or “1” is output when reading.

9.3.50. Sub Address #6Fh / Reserved Register (W/R)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#6Fh	(res)								00h

#6Fh/bit[7:0] Not defined
Set to “00h” (Initial value).

9.3.51. Sub Address #70h / HPLL Setting 1 (W/R)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#70h	(res)	OSC_SEL[1:0]		SCFB_SEL	(res)	HS_RNG_SEL	(res)		14h

#70h/bit[7] Not defined
Set to “0” (Initial value).

#70h/bit[6:5] OSC_SEL[1:0] , Reference clock selection
Selects the reference clock when using PLL.
“00” : 32.000MHz (default)
“01” : 25.000MHz
“10” : Setting prohibited
“11” : Setting prohibited

#70h/bit[4] SCFB_SEL, Sub-carrier feedback selection
This register provides the feedback of color sub-carrier depending on the PLL oscillation frequency. "Feedback" setting is effective when the color sub-carrier frequency is a fixed value while the line frequency is not.
“0” : No feedback / “1” : Feedback (default)

#70h/bit[3] Not defined
Set to “0” (Initial value).

#70h/bit[2] HS_RNG_SEL, Horizontal period range selection
In case horizontal frequency variation is larger to video specification, horizontal frequency tolerance is enhanced by setting HS_RNG_SEL to “1”
“0” : Do not extend
“1” : Extend (default)

#70h/bit[1:0] Not defined
Set to “00” (Initial value).

9.3.52. Sub Address #71h - #73h / Reserved Register (W/R)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#71h	(res)								80h
#72h	(res)								00h
#73h	(res)								00h

#71h/bit[7:0] Not defined
Set to “80h” (Initial value).
#72h/bit[7:0] Not defined
Set to “00h” (Initial value)。
#73h/bit[7:0] Not defined
Set to “00h” (Initial value).

9.3.53. Sub Address #74h / HPLL Line lock Control 1 (W/R)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#74h	(res)	LKFLG_FLD_F[2:0]			(res)	LKFLG_FLD_R[2:0]			14h

#74h/bit[7] Not defined

Set to “0” (Initial value).

#74h/bit[6:4] LKFLG_FLD_F[2:0], PLL Line lock Detection Setting (field) 1

This setting is used to check the line-lock detection state to judge if it is line-lock not detected.
It judges the state as line-lock not detected (#91h[6] ST_LKFLG="0") based on the number of consecutive lines set as follows during the no-signal period. The number of inter-field judgment lines is set in #75h/bit[6:4] (LKFLG_LINE_F).

“000”: No field judgment
(Line judgment only. Line judgment is set in #75h/bit[6:4].)
“001”: 1 Field (default)
“010”: 2 Field
“011”: 5 Field
“100”: 10 Field
“101”: 50 Field
“110”: 100 Field
“111”: 255 Field

#74h/bit[3] Not defined

Set to “0” (Initial value).

#74h/bit[2:0] LKFLG_FLD_R[2:0], PLL Line lock Detection Setting (field) 2

This setting is used to check the line-lock detection state to judge if it is line-lock detected.
It judges the state as line-lock detected (#91h[6] ST_LKFLG="1") based on the number of consecutive lines set as follows during the input-signal period. The number of inter-field judgment lines is set in #75h/bit[2:0] (LKFLG_LINE_R).

“000”: No field judgment
(Line judgment only. Line judgment is set in #75h/bit[2:0].)
“001”: 1 Field
“010”: 2 Field
“011”: 5 Field
“100”: 10 Field (default)
“101”: 50 Field
“110”: 100 Field
“111”: 255 Field

9.3.54. Sub Address #75h / HPLL Line lock Control 2 (W/R)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial valu
#75h	(res)	LKFLG_LINE_F[2:0]			(res)	LKFLG_LINE_R[2:0]			57h

#75h/bit[7] Not defined

Set to “0” (Initial value).

#75h/bit[6:4] LKFLG_LINE_F[2:0], PLL Line lock Detection Setting (line) 1

This setting is used to check the line-lock detection state to judge if it is line-lock not detected.
It judges the state as line-lock not detected (#91h[6] ST_LKFLG="0") based on the number of consecutive lines set as follows during the no-signal period. For any other value than #74h/bit[6:4] (LKFLG_FLD_F)="000", judgment is made first based on the number of consecutive lines per field in this setting and then the number of consecutive fields according to the LKFLG_FLD_F setting.
If this setting exceeds the total number of lines per field, the total number is used for judgment.
When #74h/bit[6:4] (LKFLG_FLD_F) = "000", judgment is made only based on the number of consecutive lines in this setting regardless of whether there is a field border.
When # 74h / bit [6: 4] (LKFLG_FLD_F) = “000” and # 74h / bit [2: 0] (LKFLG_FLD_R) = “000” are set, # 75h / bit [6: 4] (LKFLG_LINE_F) and # 75h / bit [2: 0] (LKFLG_LINE_R) should be set to different values.

“000”: Setting prohibited
“001”: 1 Line
“010”: 2 Line
“011”: 5 Line
“100”: 10 Line
“101”: 100 Line (default)
“110”: 500 Line
“111”: 1000 Line

#75h/bit[3] Not defined

Set to “0” (Initial value).

#75h/bit[2:0] LKFLG_LINE_R[2:0], PLL Line lock Detection Setting (line) 2

This setting is used to check the line-lock detection state to judge if it is line-lock detected.
It judges the state as line-lock not detected (#91h[6] ST_LKFLG="1") based on the number of consecutive lines set as follows during the no-signal period. For any other value than #74h/bit[2:0] (LKFLG_FLD_R)="000", judgment is made first based on the number of consecutive lines per field in this setting and then the number of consecutive fields according to the LKFLG_FLD_R setting.
If this setting exceeds the total number of lines per field, the total number is used for judgment.
When #74h/bit[2:0] (LKFLG_FLD_R) = "000", judgment is made only based on the number of consecutive lines in this setting regardless of whether there is a field border.
When # 74h / bit [6: 4] (LKFLG_FLD_F) = “000” and # 74h / bit [2: 0] (LKFLG_FLD_R) = “000” are set, # 75h / bit [6: 4] (LKFLG_LINE_F) and # 75h / bit [2: 0] (LKFLG_LINE_R) should be set to different values.

“000”: Setting prohibited
“001”: 1 Line
“010”: 2 Line
“011”: 5 Line
“100”: 10 Line
“101”: 100 Line
“110”: 500 Line
“111”: 1000 Line (default)

9.3.55. Sub Address #76h / Reserved Register (W/R)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#76h	(res)								8Dh

#76h/bit[7:0] Not defined

Set to “8Dh” (Initial value).

9.4. Status / Interrupt control unit control register details

9.4.1. Sub Address #78h / STATUS Output Setting 1 (W/R)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#78h	STATUS_SEL[3:0]				INT_ SEL	INT_ POL	(res)		60h

#78h/bit[7:4] STATUS_SEL[3:0], STATUS Output Selection

Select output status from the STATUS pin.

"0000": HVALID
"0001": VVALID
"0010": ODD/EVEN("L"EVEN/"H"ODD)
"0011": CSYNC
"0100": VHVALID
"0101": NTPALfield frequency judgement
"0110": HLOCK detection (default)
"0111": Setting prohibited
"1000": Setting prohibited
"1001": VBID detection("L"not detection/"H"detection)
"1010": Setting prohibited
"1011": Setting prohibited
"1100": Setting prohibited
"1101": Setting prohibited
"1110": PLL lock flag
"1111": Interrupt output

#78h/bit[3] INT_SEL, Interrupt output operation selection

Select the operation of the interrupt output.
This is valid when "Interrupt output" is selected in # 78h / bit [7: 4] (STATUS_SEL).

"0": Interrupt level output (default)
Continues to send a notification once an interrupt cause occurs until it is cleared.
To clear the notification, overwrite the corresponding bit of #7Ah (INT_xx).

"1": Interrupt cause monitor
Sends a notification when an interrupt cause occurs and automatically resets the notification when the cause no longer exists.

#78h/bit[2] INT_POL, Interrupt output polarity selection

Selects the polarity of the interrupt output.
This is valid when "Interrupt output" is selected in # 78h / bit [7: 4] (STATUS_SEL).

"0": "L"Notification (Active) "H"Not Notification (default)
"1": "H"Notification (Active) "L"Not Notification

#78h/bit[1:0] Not defined

Set to "00" (Initial value).

9.4.2. Sub Address #79h / STATUS Output Setting 2 (W/R)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#79h	(res)				MASK_ LKFLG	MASK_ LKFLG_ B	MASK_ HDET	MASK_ HDET_ B	FFh

Select the information to be masked in the interrupt detection function.
When interrupt notification is selected in STATUS_SEL (# 78h / bit [7: 4]), an interrupt notification is output from the STATUS pin when any of the unmasked information is detected.

#79h/bit[7:4] Not defined
Set to "0000" (Initial value).

#79h/bit[3] MASK_LKFLG, PLL Line lock detection mask
Mask interrupt notification when line lock detection (#91h/bit[6]) = 1.
"0": Not Mask
"1": Mask (default)

#79h/bit[2] MASK_LKFLG_B, PLL Line lock not detection mask
Mask interrupt notification when line lock detection (#91h/bit[6]) = 0.
"0": Not Nask
"1": Mask (default)

#79h/bit[1] MASK_HDET, Analog input signal detection mask
Mask interrupt notification when analog input HLOCK detection (#91h/bit[1]) = 1.
"0": Not Mask
"1": Mask (default)

#79h/bit[0] MASK_HDET_B, Analog input signal not detection mask
Mask interrupt notification when analog input HLOCK detection (#91h/bit[1]) = 0.
"0": Not Mask
"1": Mask (default)

9.4.3. Sub Address #7Ah / Status Clear / Status (W&C,R)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#7Ah	(res)				INT_LKFLG	INT_LKFLG_B	INT_HDET	INT_HDET_B	xxh

Monitor / clear the detection flag set to unmask in STATUS output setting 2 (# 79h).
The flag becomes "0" at the time of detection, and writing "1" clears the flag.
When interrupt notification is selected in STATUS_SEL (#78h/bit[7:4]) and "interrupt level output" is selected in INT_SEL (#78h/bit[3]), if any flag is detected, an interrupt notification is output from the STATUS pin and reset when it is cleared.

#7Ah/bit[7:4] Not defined

"0" or "1" is output when reading.

#7Ah/bit[3] INT_LKFLG, PLL Line lock detect

The bit is set to "0" when line-lock is detected.
Line lock detection can be monitored with # 91h / bit [6] when # 80h / bit [0] (LKFLG_MON) is set to "1".

"0": Detect (Flag cleard when "1" write)
"1": Not detect

#7Ah/bit[2] INT_LKFLG_B, PLL Line lock not detect

The bit is set to "0" when line-lock is not detected.
Line lock detection can be monitored with # 91h / bit [6] when # 80h / bit [0] (LKFLG_MON) is set to "1".

"0": Detect (Flag cleard when "1" write)
"1": Not detect

#7Ah/bit[1] INT_HDET, Analog input signal detection

The bit is set to "0" when analog input HLOCK detection (#91h/bit[1])=1.

"0": Detect (Flag cleard when "1" write)
"1": Not detect

#7Ah/bit[0] INT_HDET_B, Analog input no signal detection

The bit is set to "0" when analog input HLOCK detection (#91h/bit[1])=0.

"0": Detect (Flag cleard when "1" write)
"1": Not detect

9.4.4. Sub Address #80h / VBID Detection Monitor Setting （W/R）

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#80h	VBID_DT	(res)						LKFLG_MON	00h

#80h/bit[7] VBID_DT, Data detection mode during VBID period

Sets the data detection during VBI period. To detect the VBI data, set this register to "1".

"0" : Do not perform detection (default) / "1" : Perform detection

#80h/bit[6:1] Not defined

Set to "00_0000" (Initial value).

#80h/bit[0] LKFLG_MON, Line lock flag monitor setting

Sets the line lock flag monitor. Set this register to "1" to monitor the line lock flag at #91h/bit[6](ST_LKFLG).

"0": Do not monitor (default) / "1": monitor

9.4.5. Sub Address #82h / Reserved Register （W/R）

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#82h	(res)								00h

#82h/bit[7:0] Not defined

Set to "00h" (Initial value).

9.4.6. Sub Address #84h / Reserved Register （W/R）

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#84h	(res)								00h

#84h/bit[7:0] Not defined

Set to "00h" (Initial value).

9.4.7. Sub Address #86h / Reserved Register （W/R）

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#86h	(res)								00h

#86h/bit[7:0] Not defined

Set to "00h" (Initial value).

9.4.8. Sub Address #88h / Reserved Register （W/R）

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#88h	(res)								00h

#88h/bit[7:0] Not defined

Set to "00h" (Initial value).

9.4.9. Sub Address #89h / VBID Detection Reset Setting （W/R）

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#89h	(res)	RST_C.C_O	RST_C.C_E	RST_CGMS_O	RST_CGMS_E	(res)		RST_WSS	00h

Whether each data was present or not is stored within the decoder.
The result can be read from the #0092h VBID Flag Register.
However, the result that has been stored is not deleted unless it is reset.
However, the information may not be detected depending on the condition or contents of the signal.
An example of the VBID flag read sequence is shown below.

[Note] When this function is used, the information of the presence of VBID data or contents may be output incorrectly depending on the input signal state. To ensure a stable operation of this function, read the signal over several fields to confirm that it is stable, before using the detected data.

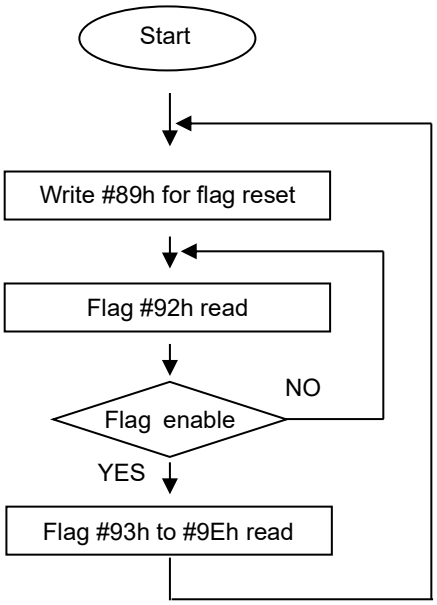


Figure : VBID Flag Read Sequence

Each reset request sets it to "1" to execute a reset.
It is automatically returning to "0" after a reset is executed.

#89h/bit[7] Not defined
Set to “0” (Initial value).

#89h/bit[6] RST_C.C_O, C.C. data (ODD Field) reset request
“1” : Flag Reset
“0” : Flag No Reset (default)

#89h/bit[5] RST_C.C_E, C.C. data (EVEN Field) reset request
“1” : Flag Reset
“0” : Flag No Reset (default)

#89h/bit[4] RST_CGMS_O, CGMS data(ODD Field) reset request
“1” : Flag Reset
“0” : Flag No Reset (default)

#89h/bit[3] RST_CGMS_E, CGMS data(EVEN Field) reset request
“1” : Flag Reset
“0” : Flag No Reset (default)

#89h/bit[2:1] Not defined
Set to “00” (Initial value).

#89h/bit[0] RST_WSS, WSS data reset request
“1” : Flag Reset
“0” : Flag No Reset (default)

9.4.10. Sub Address #8Ah - #8Fh / Reserved Register （R only）

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#8Ah	(res)								xxh
#8Bh	(res)								xxh
#8Ch	(res)								xxh
#8Dh	(res)								xxh
#8Eh	(res)								xxh
#8Fh	(res)								xxh

#8Ah/bit[7:0] Not defined
"0" or "1" is output when reading.
#8Bh/bit[7:0] Not defined
"0" or "1" is output when reading.
#8Ch/bit[7:0] Not defined
"0" or "1" is output when reading.
#8Dh/bit[7:0] Not defined
"0" or "1" is output when reading.
#8Eh/bit[7:0] Not defined
"0" or "1" is output when reading.
#8Fh/bit[7:0] Not defined
"0" or "1" is output when reading.

9.4.11. Sub Address #90h / Status Register 1 （R only）

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#90h	FLD_FLAG	(res)	NTPAL	(res)	ST_IFM_DET[3:0]				xxh

#90h/bit[7] FLD_FLAG, Reading the field information

Able to monitor the field information of the analog input video signal.

"0": EVEN field

"1": ODD field

#90h/bit[6] Not defined

"0" or "1" is output when reading.

#90h/bit[5] NTPAL, Reading NTSC / PAL field frequency judgement

Able to monitor the field frequency judgement of the analog input video signal.

"0": NTSC(60Hz)

"1": PAL(50Hz)

#90h/bit[4] Not defined

"0" or "1" is output when reading.

#90h/bit[3:0] ST_IFM_DET[3:0], Reading the input format automatic judgment result

Stores the results of the automatic judgment of the analog input video signal.

"0000": NTSC-M

"0001": NTSC-J

"0010": NTSC-443

"0011": PAL

"0100": PAL-M

"0101": PAL-N

"0110": PAL-Nc

"0111": PAL-60

9.4.12. Sub Address #91h / Status Register 2 （R only）

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#91h	(res)	ST_LKFLG	ST_VTR_DT	ST_VBID_DT	(res)		ST_HLCK_DT	(res)	xxh

#91h/bit[7] Not defined

"0" or "1" is output when reading.

#91h/bit[6] ST_LKFLG, Line lock flag monitor

Able to monitor the line lock flag. To enable the monitor, set #080h/bit[0] (LKFLG_MON) to "1". When the monitor is disabled, "0" is output.

"0": Unlock(Unstable) / "1": Lock (Stable)

#91h/bit[5] ST_VTR_DT, VTR detection monitor

Able to monitor whether the VTR is detected or not.

"0": Not detected / "1": Detected

#91h/bit[4] ST_VBID_DT, VBID data detection

Able to monitor whether each of the VBID flag (#92h/bit[7:0]) is detected or not.

"0": Not detected / "1": Detected

#91h/bit[3] Not defined

"0" or "1" is output when reading.

#91h/bit[2] Not defined

"0" or "1" is output when reading.

#91h/bit[1] ST_HLCK_DT, HLOCK detection monitor

Able to monitor the synchronization detection of the input signal based on the HLOCK judgement conditions described in the synchronization processing section (section 1.4.6.).

"0": Not detected / "1": Detected

#91h/bit[0] Not defined

"0" or "1" is output when reading.

9.4.13. Sub Address #92h / VBID Flag Register （R only）

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#92h	(res)	VF_C.C_O	VF_C.C_E	VF_CGMS_O	VF_CGMS_E	(res)		VF_WSS	xxh

This register stores the VBID detection result and the VBID data readable flag.
For CC, CGMS, and WSS, the readable data is stored in #93h to #9Eh.

#92h/bit[7] Not defined
"0" is output when reading.

#92h/bit[6] VF_C.C_O, CC data Ready(odd field)
#92h/bit[5] VF_C.C_E, CC data Ready(even field)
#92h/bit[4] VF_CGMS_E, CGMS data Ready(odd field)
#92h/bit[3] VF_CGMS_E, CGMS data Ready(even field)

#92h/bit[2] Not defined
"0" is output when reading.

#92h/bit[1] Not defined
"0" is output when reading.

#92h/bit[0] VF_WSS, WSS data Ready

9.4.14. Sub Address #93h / C.C Data buffer Register in ODD Field 2 （R only）

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#93h	C.C_O_DT2[7:0]								xxh

#93h/bit[7:0] C.C_O_DT2[7:0], character two b0,,b6,p2

Able to read out the value of the character2 of the ODD closed caption data.

9.4.15. Sub Address #94h / C.C Data buffer Register in ODD Field 1 （R only）

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#94h	C.C_O_DT1[7:0]								xxh

#94h/bit[7:0] C.C_O_DT1[7:0], character one b0,,b6,p1

Able to read out the value of the character1 of the ODD closed caption data.

9.4.16. Sub Address #95h / C.C Data buffer Register in EVEN Field 2 （R only）

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#95h	C.C_E_DT2[7:0]								xxh

#95h/bit[7:0] C.C_E_DT2[7:0], character two b0,,b6,p2

Able to read out the value of the character2 of the EVEN closed caption data.

9.4.17. Sub Address #96h / C.C Data buffer Register in EVEN Field 1 （R only）

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#96h	C.C_E_DT1[7:0]								xxh

#96h/bit[7:0] C.C.E_DT1[7:0], character one b0,,b6,p1

Able to read out the value of the character1 of the EVEN closed caption data.

9.4.18. Sub Address #97h / CGMS Data buffer Register in ODD Field 3 （R only）

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#97h	CGMS_O_DT3[7:0]								xxh

#97h/bit[7:0] CGMS_O_DT3[7:0], Bit13,,20

Able to read out the values of Bit13 to Bit20 of the ODD CGMS data.

9.4.19. Sub Address #98h / CGMS Data buffer Register in ODD Field 2 （R only）

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#98h	CGMS_O_DT2[7:0]								xxh

#98h/bit[7:0] CGMS_O_DT2[7:0], Bit5,,12

Able to read out the values of Bit5 to Bit12 of the ODD CGMS data.

9.4.20. Sub Address #99h / CGMS Data buffer Register in ODD Field 1 （R only）

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#99h	C.C_O_P1_ER	C.C_O_P2_ER	(res)	CGMS_O_CRC_ER	CGMS_O_DT1[3:0]				xxh

#99h/bit[7] C.C_O_P1_ER, C.C. ODD PTY1 error detection

Able to read out the parity error judgment results of the ODD closed caption data PTY1.

“0” : No error / “1” : Error

#99h/bit[6] C.C_O_P2_ER, C.C. ODD PTY2 error detection

Able to read out the parity error judgment results of the ODD closed caption data PTY2.

“0” : No error / “1” : Error

#99h/bit[5] Not defined

“0” is output when reading.

#99h/bit[4] CGMS_O_CRC_ER, CGMS ODD CRC error detection

Able to read out the CRC error judgment result of the ODD CGMS data.

“0” : No error / “1” : Error

#99h/bit[3:0] CGMS_O_DT1[3:0]、Bit1,,4

Able to read out the values of Bit1 to Bit4 of the ODD CGMS data.

9.4.21. Sub Address #9Ah / CGMS Data buffer Register in EVEN Field 3 （R only）

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#9Ah	CGMS_E_DT3[7:0]								xxh

#9Ah/bit[7:0] CGMS_E_DT3[7:0], Bit13,,20

Able to read out the values of Bit13 to Bit20 of the EVEN CGMS data.

9.4.22. Sub Address #9Bh / CGMS Data buffer Register in EVEN Field 2 （R only）

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#9Bh	CGMS_E_DT2[7:0]								xxh

#9Bh/bit[7:0] CGMS_E_DT2[7:0], Bit5,,12

Able to read out the values of Bit5 to Bit12 of the EVEN CGMS data.

9.4.23. Sub Address #9Ch / CGMS Data buffer Register in EVEN Field 1 （R only）

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#9Ch	C.C_E_P1_ER	C.C_E_P2_ER	(res)	CGMS_E_CRC_ER	CGMS_E_DT1[3:0]				xxh

#9Ch/bit[7] C.C_E_P1_ER, C.C. EVEN PTY1 error detection

Able to read out the parity error judgment results of the EVEN closed caption data PTY1.

“0” : No error / “1” : Error

#9Ch/bit[6] C.C_E_P2_ER, C.C. EVEN PTY2 error detection

Able to read out the parity error judgment results of the EVEN closed caption data PTY2.

“0” : No error / “1” : Error

#9Ch/bit[5] Not defined

"0" is output when reading.

#9Ch/bit[4] CGMS_E_CRC_ER, CGMS EVEN CRC error detection

Able to read out the CRC error judgment result of the EVEN CGMS data.

“0” : No error / “1” : Error

#9Ch/bit[3:0] CGMS_E_DT1[3:0], Bit1,,4

Able to read out the values of Bit1 to Bit4 of the EVEN CGMS data.

9.4.24. Sub Address #9Dh / WSS Data buffer Register 2 （R only）

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#9Dh	WSS_DG2[1:0]		WSS_DG3[2:0]			WSS_DG4[2:0]			xxh

#9Dh/bit[7:6] WSS_DG2[1:0], Group2 Bit6,7
Able to read out the values of the WSS data group 2 (Bit6, 7).

#9Dh/bit[5:3] WSS_DG3[2:0], Group3 Bit8,9,10
Able to read out the values of the WSS data group 3 (Bit10, 9, 8).

#9Dh/bit[2:0] WSS_DG4[2:0], Group4 Bit11,12,13
Able to read out the values of the WSS data group 4 (Bit11, 12, 13).

9.4.25. Sub Address #9Eh / WSS Data buffer Register 1 （R only）

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#9Eh	WSS_P_ER	(res)	WSS_DG1[3:0]				WSS_DG2[3:2]		xxh

#9Eh/bit[7] WSS_P_ER, WSS PTY error detection
Able to read out the parity error judgment results of the WSS data.
“0” : No error / “1” : Error

#9Eh/bit[6] Not defined
"0" is output when reading.

#9Eh/bit[5:2] WSS_DG1[3:0], Group1 Bit0,1,2,3
Able to read out the values of the WSS data group 1 (Bit0, 1, 2, 3).

#9Eh/WSS[1:0] WSS_DG2[3:2], Group2 Bit4,5
Able to read out the values of the WSS data group 2 (Bit4, 5).

9.4.26. Sub Address #9Fh / Reserved Register （R only）

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#9Fh	(res)								xxh

#9Fh/bit[7:0] Not defined
"0" or "1" is output when reading.

9.4.27. Sub Address #A0h - #A7h / Reserved Register （W/R）

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#A0h	(res)								82h
#A1h	(res)								41h
#A2h	(res)								41h
#A3h	(res)								82h
#A4h	(res)								14h
#A5h	(res)								28h
#A6h	(res)								28h
#A7h	(res)								14h

#A0h/bit[7:0] Not defined
Set to “82h” (initial value).
#A1h/bit[7:0] Not defined
Set to “41h” (initial value).
#A2h/bit[7:0] Not defined
Set to “41h” (initial value).
#A3h/bit[7:0] Not defined
Set to “82h” (initial value).
#A4h/bit[7:0] Not defined
Set to “14h” (initial value).
#A5h/bit[7:0] Not defined
Set to “28h” (initial value).
#A6h/bit[7:0] Not defined
Set to “28h” (initial value).
#A7h/bit[7:0] Not defined
Set to “14h” (initial value).

9.4.28. Sub Address #A8h - #AFh / Reserved Register （W/R）

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#A8h	(res)								A5h
#A9h	(res)								A5h
#AAh	(res)								5Ah
#ABh	(res)								5Ah
#ACh	(res)								A5h
#ADh	(res)								A5h
#AEh	(res)								5Ah
#AFh	(res)								5Ah

#A8h/bit[7:0] Not defined
Set to “A5h” (initial value).
#A9h/bit[7:0] Not defined
Set to “A5h” (initial value).
#AAh/bit[7:0] Not defined
Set to “5Ah” (initial value).
#ABh/bit[7:0] Not defined
Set to “5Ah” (initial value).
#ACh/bit[7:0] Not defined
Set to “A5h” (initial value).
#ADh/bit[7:0] Not defined
Set to “A5h” (initial value).
#AEh/bit[7:0] Not defined
Set to “5Ah” (initial value).
#AFh/bit[7:0] Not defined
Set to “5Ah” (initial value).

9.5. Details of test pattern generation control register

9.5.1. Sub Address #BCh/ Built-in test pattern output setting (W/R)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#BCh	TMDEN	TMDSEL[2:0]			TOPT	TRENB	TGENB	TBENB	00h

#BCh/bit[7] TMDEN, Test pattern output mode

Outputs a test pattern that contains the block diagram "Test Pattern Block".
When this bit is set to "1", the built-in test pattern is output.

"0": Disable (default) / "1": Enable

#BCh/bit[6:4] TMDSEL, Selection of internal test pattern output

"000": Horizontal linear gradation 1 (default)

Refer to #BCh/bit[3], TOPT.

"001": Horizontal linear gradation 2

The gray scale increases by one level every one pixel.

"010": Crosshatch

Outputs a pattern of 20 x 20 pixel grids with 2-pixel-width lines.

Refer to #BCh/bit[3], TOPT

"011": Vertical linear gradation

The gray scale increases by one level every one line.

"100": Color bar

Refer to #BCh/bit[3], TOPT

"101": Raster

The color set in #BCh[2:0] and #BDh is output in the full-screen.

"110": Setting prohibited

"101": Setting prohibited

#BCh/bit[3] TOPT, Test pattern output option setting

Outputs the test pattern set in TMDSEL as the following table.

TMDSEL	TOPT	Test pattern output
000	0	The gray scale increases by one level every three pixels.
	1	The gray scale increases by one level every two pixels.
010	0	Outputs a crosshatch pattern of white lines on a black background.
	1	Outputs a crosshatch pattern of black lines on a white background.
100	0	The output color changes every 80 pixels.
	1	The output color changes every 40 pixels.

#BCh/bit[2] TRENB, Test Cr output

This setting is valid except for TMDSEL="010" (crosshatch) and "100" (color bar).
For gradation output (TMDSEL = “000/001/011”), if “1” is set for this bit, the Cr component is fully output.
For raster output (TMDSEL = “101”), the level setting of the Cr component is selected. After setting "1" for this bit, set the level with TPATCOL[7:0].

(For gradation output)

“0”: Do not output (default) / “1”: Output

(For raster output)

“0”: Do not set (default) / “1”: Set

#BCh/bit[1] TGENB, Test Y output

This setting is valid except for TMDSEL="010"（crosshatch） and "100" (color bar).
For gradation output (TMDSEL = “000/001/011”), if “1” is set for this bit, the Y component is fully output.
For raster output (TMDSEL = “101”), the level setting of the Y component is selected. After setting "1" for this bit, set the level with TPATCOL[7:0].

(For gradation output)

“0”: Do not output (default) / “1”: Output

(For raster output)

“0”: Do not set (default) / “1”: Set

#BCh/bit[0] TBENB, Test Cb output

This setting is valid except for TMDSEL=“010”(crosshatch) and "100" (color bar).
For gradation output (TMDSEL = “000/001/011”), if “1” is set for this bit, the Cb component is fully output.
For raster output (TMDSEL = “101”), the level setting of the Cb component is selected. After setting "1" for this bit, set the level with TPATCOL[7:0].

(For gradation output)

“0”: Do not output (default) / “1”: Output

(For raster output)

“0”: Do not set (default) / “1”: Set

For gradation output, seven types of gradation can be output by combining the TRENB, TGENB, and TBENB settings.

9.5.2. Sub Address #BDh/ Built-in Test Pattern Output Color Setting (W/R)

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#BDh	TPATCOL[7:0]								00h

#BDh/bit[7:0] TPATCOL, Test output level

The TPATCOL setting is valid when #BCh/bit[6:4] TMDSEL="101"(Raster). When the raster pattern is selected, this sets the output level of the color component that is set to "1" in #BCh[2:0].

9.5.3. Sub Address #BE - #BFh / Reserved Register （W/R）

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#BEh	(res)								00h
#BFh	(res)								00h

#BEh/bit[7:0] Not defined

Set to "00h" (Initial value).

#BFh/bit[7:0] Not defined

Set to "00h" (Initial value).

9.6. Others, Details of control register

9.6.1. Sub Address #C0h - #C6h / Reserved Register （W/R）

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#C0h	(res)				-		(res)		00h
#C1h	(res)								00h
#C2h	(res)								00h
#C3h	(res)								00h
#C4h	-							(res)	00h
#C5h	(res)								00h
#C6h	-						(res)		00h

#C0h/bit[7:0] Not defined
Set to “00h” (Initial value)
#C1h/bit[7:0] Not defined
Set to “00h” (Initial value)
#C2h/bit[7:0] Not defined
Set to “00h” (Initial value)
#C3h/bit[7:0] Not defined
Set to “00h” (Initial value)
#C4h/bit[7:0] Not defined
Set to “00h” (Initial value)
#C5h/bit[7:0] Not defined
Set to “00h” (Initial value)
#C6h/bit[7:0] Not defined
Set to “00h” (Initial value)

9.6.2. Sub Address #CAh - #CFh / Reserved Register （W/R）

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#CAh	(res)								00h
#CBh	(res)								00h
#CCh	(res)								00h
#CDh	(res)								00h
#CEh	(res)								00h
#CFh	(res)								00h

#CAh/bit[7:0] Not defined
Set to “00h” (Initial value)
#CBh/bit[7:0] Not defined
Set to “00h” (Initial value)
#CCh/bit[7:0] Not defined
Set to “00h” (Initial value)
#CDh/bit[7:0] Not defined
Set to “00h” (Initial value)
#CEh/bit[7:0] Not defined
Set to “00h” (Initial value)
#CFh/bit[7:0] Not defined
Set to “00h” (Initial value)

9.6.3. Sub Address #D0h / Reserved Register （W/R）

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#D0h	(res)								02h

#D0h/bit[7:0] Not defined
Set to “02h” (Initial value)

9.6.4. Sub Address #D2h - #DBh / Reserved Register （W/R）

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#D2h	(res)								00h
#D3h	(res)								00h
#D4h	(res)								00h
#D5h	(res)								00h
#D6h	(res)								00h
#D7h	(res)								00h
#D8h	(res)								00h
#D9h	(res)								00h
#DAh	(res)								00h
#DBh	(res)								00h

#D2h/bit[7:0] Not defined
Set to “00h” (Initial value)
#D3h/bit[7:0] Not defined
Set to “00h” (Initial value)
#D4h/bit[7:0] Not defined
Set to “00h” (Initial value)
#D5h/bit[7:0] Not defined
Set to “00h” (Initial value)
#D6h/bit[7:0] Not defined
Set to “00h” (Initial value)
#D7h/bit[7:0] Not defined
Set to “00h” (Initial value)
#D8h/bit[7:0] Not defined
Set to “00h” (Initial value)
#D9h/bit[7:0] Not defined
Set to “00h” (Initial value)
#DAh/bit[7:0] Not defined
Set to “00h” (Initial value)
#DBh/bit[7:0] Not defined
Set to “00h” (Initial value)

9.6.5. Sub Address #DCh - #DFh / Reserved Register （W/R）

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#DCh	(res)								00h
#DDh	(res)								00h
#DEh	(res)								2Ah
#DFh	(res)								0Ah

#DCh/bit[7:0] Not defined
Set to “00h” (Initial value)
#DDh/bit[7:0] Not defined
Set to “00h” (Initial value)
#DEh/bit[7:0] Not defined
Set to “2Ah” (Initial value)
#DFh/bit[7:0] Not defined
Set to “0Ah” (Initial value)

9.6.6. Sub Address #E0h - #E9h / Reserved Register （W/R）

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#E0h	(res)								00h
#E1h	(res)								00h
#E2h	(res)								00h
#E3h	(res)								00h
#E4h	(res)								00h
#E5h	(res)								00h
#E6h	(res)								00h
#E7h	(res)								00h
#E8h	(res)								00h
#E9h	(res)								00h

#E0h/bit[7:0] Not defined
Set to “00h” (Initial value)
#E1h/bit[7:0] Not defined
Set to “00h” (Initial value)
#E2h/bit[7:0] Not defined
Set to “00h” (Initial value)
#E3h/bit[7:0] Not defined
Set to “00h” (Initial value)
#E4h/bit[7:0] Not defined
Set to “00h” (Initial value)
#E5h/bit[7:0] Not defined
Set to “00h” (Initial value)
#E6h/bit[7:0] Not defined
Set to “00h” (Initial value)
#E7h/bit[7:0] Not defined
Set to “00h” (Initial value)
#E8h/bit[7:0] Not defined
Set to “00h” (Initial value)
#E9h/bit[7:0] Not defined
Set to “00h” (Initial value)

9.6.7. Sub Address #EAh - #EFh / Reserved Register （W/R）

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#EAh	(res)								00h
#EBh	(res)								00h
#ECh	(res)								00h
#EDh	(res)								40h
#EEh	(res)								00h
#EFh	(res)								00h

#EAh/bit[7:0] Not defined
Set to “00h” (Initial value)
#EBh/bit[7:0] Not defined
Set to “00h” (Initial value)
#ECh/bit[7:0] Not defined
Set to “00h” (Initial value)
#EDh/bit[7:0] Not defined
Set to “00h” (Initial value)
#EEh/bit[7:0] Not defined
Set to “00h” (Initial value)
#EFh/bit[7:0] Not defined
Set to “00h” (Initial value)

9.6.8. Sub Address #F0h - #F5h / Reserved Register （W/R）

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#F0h	(res)								00h
#F1h	(res)								00h
#F2h	(res)								00h
#F3h	(res)								00h
#F4h	(res)								00h
#F5h	(res)								00h

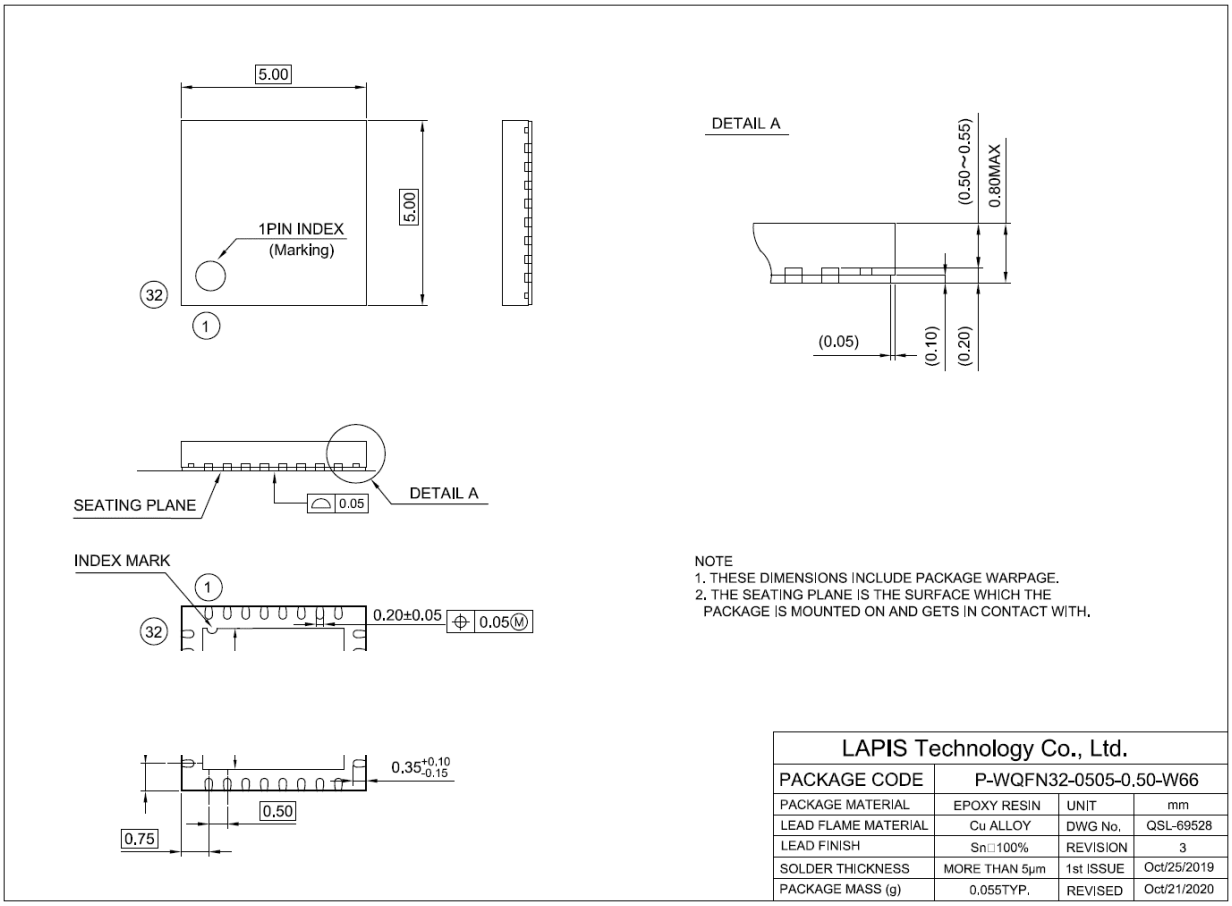
#F0h/bit[7:0] Not defined
Set to “00h” (Initial value)
#F1h/bit[7:0] Not defined
Set to “00h” (Initial value)
#F2h/bit[7:0] Not defined
Set to “00h” (Initial value)
#F3h/bit[7:0] Not defined
Set to “00h” (Initial value)
#F4h/bit[7:0] Not defined
Set to “00h” (Initial value)
#F5h/bit[7:0] Not defined
Set to “00h” (Initial value)

9.6.9. Sub Address #FAh - #FFh / Reserved Register （W/R）

Address	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]	Initial value
#FAh	(res)								80h
#FBh	(res)								00h
#FCh	(res)								00h
#FDh	(res)								00h
#FEh	(res)								00h
#FFh	(res)								00h

#FAh/bit[7:0] Not defined
Set to “80h” (Initial value)
#FBh/bit[7:0] Not defined
Set to “00h” (Initial value)
#FCh/bit[7:0] Not defined
Set to “00h” (Initial value)
#FDh/bit[7:0] Not defined
Set to “00h” (Initial value)
#FEh/bit[7:0] Not defined
Set to “00h” (Initial value)
#FFh/bit[7:0] Not defined
Set to “00h” (Initial value)

■ Package Dimensions



LAPIS Technology Co., Ltd.			
PACKAGE CODE	P-WQFN32-0505-0.50-W66		
PACKAGE MATERIAL	EPOXY RESIN	UNIT	mm
LEAD FLAME MATERIAL	Cu ALLOY	DWG No.	QSL-69528
LEAD FINISH	Sn□100%	REVISION	3
SOLDER THICKNESS	MORE THAN 5μm	1st ISSUE	Oct/25/2019
PACKAGE MASS (g)	0.055TYP.	REVISED	Oct/21/2020

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact ROHM's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

[Notes in Use]

The analog input section of ML86112 is developed based on the standard video signal. We have improved it to obtain a stable behavior for nonstandard video signals as well. However, a stable behavior for every signal is not guaranteed, since there are various situations in the signal condition and usage environment such as airwave signals received in light electric field areas, VTR playback signals, video signals with switching signal sources, noise contamination signals, and simplified video signals of various cameras and game machines.
Please thoroughly evaluate and examine the product in assumed signal conditions and usage environments before you adopt it.

■ Revision History

Document No.	Issue Date	Page		Description
		Previous Edition	New Edition	
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FEDL86112-02	2024.02.22	129	129	No changes in 2nd edition
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LAPIS Technology Co.,Ltd.

2-4-8 Shinyokohama, Kouhoku-ku, Yokohama 222-8575, Japan
https://www.lapis-tech.com/en/

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