A4911-1

Automotive Three-Phase MOSFET Driver

FEATURES AND BENEFITS

- Three-phase bridge MOSFET driver
- Bootstrap gate drive for N-channel MOSFET bridge
- Cross-conduction protection with adjustable dead time
- Charge pump for low supply voltage operation
- Programmable gate drive voltage and strength
- 5.5 to 50 V supply voltage operating range
- Integrated logic supply
- Logic level phase state outputs
- Three current sense amplifiers
- Programmable gain and offset with offset output
- SPI-compatible serial interface
- Bridge control by direct logic inputs or serial interface
- TTL compatible logic inputs

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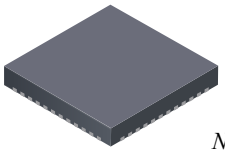
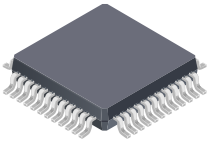
ISO 26262 ASIL Compliant

PACKAGES:

48-pin QFN with exposed thermal pad and wettable flank (suffix EV)



48-pin LQFP with exposed thermal pad (suffix JP)



Not to scale

DESCRIPTION

The A4911 is an N-channel power MOSFET driver capable of controlling MOSFETs connected in a three-phase bridge arrangement and is specifically designed for automotive applications with high-power inductive loads, such as BLDC motors.

The A4911 was developed in accordance with ISO 26262 as a hardware safety element out-of-context with ASIL D capability for use in automotive safety-related systems when integrated and used in the manner prescribed in the applicable safety manual and datasheet.

A unique charge pump regulator provides the supply for the MOSFET gate drive for battery voltages down to 7 V and allows the A4911 to operate with a reduced gate drive down to 5.5 V. Gate drive voltage and strength are programmable to help reduce EMC issues. A bootstrap capacitor is used to provide the above-battery supply voltage required for N-channel MOSFETs.

Full control over all six power MOSFETs in the three-phase bridge is provided, allowing motors to be driven with block commutation or sinusoidal excitation. The power MOSFETs are protected from shoot-through by integrated crossover control and optional programmable dead time.

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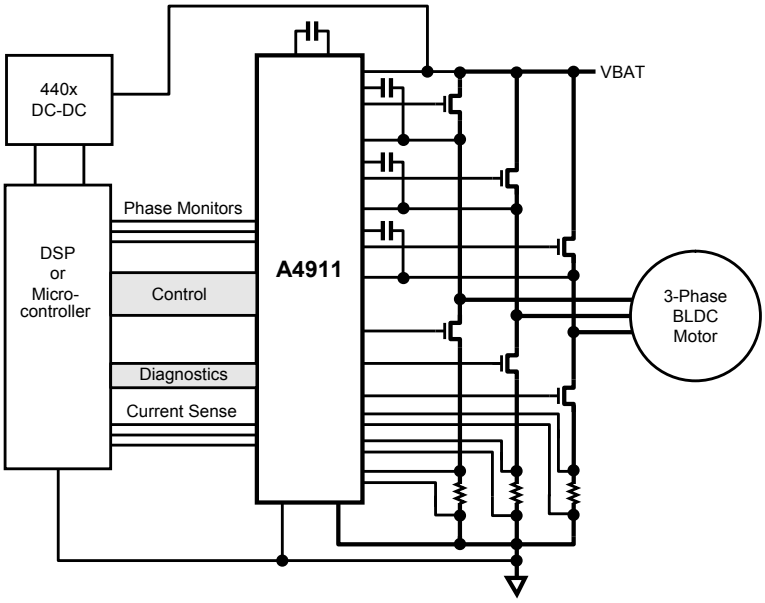
Typical Application Drawing



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FEATURES AND BENEFITS (continued)

- Extensive programmable diagnostics
- Diagnostic verification
- Safety-assist features
- Automotive AEC-Q100 qualified
- ASIL-Compliant: ASIL D safety element out-of-context (SEooC) developed in accordance with ISO 26262, when used as specified in the safety manual

DESCRIPTION (continued)

Integrated diagnostics provide indication of multiple internal faults, system faults, and power bridge faults, and can be configured to protect the power MOSFETs under most short-circuit conditions. For safety-critical systems, the integrated diagnostic operation can be verified under control of the serial interface.

The serial interface is provided to alter programmable settings and read back detailed diagnostic information.

The A4911 is supplied in a 48-terminal wettable flank QFN package (suffix EV) and a 48-pin QFP package (suffix JP), both with exposed thermal pad. These packages are lead (Pb) free with 100% matte-tin leadframe plating.

SELECTION GUIDE

Part Number	Package	Packing*
A4911KEVTR-J-1	7 mm × 7 mm, 0.9 mm nominal height 48-terminal QFN with exposed thermal pad and wettable flank	1000 pieces per 7-in. reel
A4911KJPTR-T-1	7 mm × 7 mm, 1.6 mm nominal height 48-lead LQFP with exposed thermal pad	1500 pieces per 13-in. reel

*Contact Allegro™ for additional packing options.

THERMAL CHARACTERISTICS: May require derating at maximum conditions

Characteristic	Symbol	Test Conditions [4]	Value	Unit
EV Package Thermal Resistance	$R_{\theta JA}$	4-layer PCB based on JEDEC standard	24	°C/W
		2-layer PCB with 3.8 in.^{2} of copper area each side	44	°C/W
	$R_{\theta JP}$		2	°C/W
JP Package Thermal Resistance	$R_{\theta JA}$	4-layer PCB based on JEDEC standard	23	°C/W
		2-layer PCB with 3.8 in.^{2} of copper area each side	44	°C/W
	$R_{\theta JP}$		2	°C/W

[4] Additional thermal information available on the Allegro website.

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ABSOLUTE MAXIMUM RATINGS [1][2]

Characteristic	Symbol	Notes	Rating	Unit
Load Supply Voltage	V_{BB}		–0.3 to 50	V
Between Ground Terminals		Connect GND pins together at package	–0.1 to 0.1	V
Pumped Regulator Terminal	V_{REG}	VREG	–0.3 to 16	V
Charge Pump Capacitor Low Terminal	V_{CP1}	CP1	–0.3 to 16	V
Charge Pump Capacitor High Terminal	V_{CP2}	CP2	V_{CP1} – 0.3 to V_{REG} + 0.3	V
Battery Compliant Logic Input Terminals	V_{IB}	HA, HB, HC, LA, LB, LC, RESETn, ENABLE	–0.3 to 50	V
Logic Input Terminals	V_I	STRn, SCK, SDI	–0.3 to 6	V
Logic Output Terminals	V_O	SDO, SAL, SBL, SCL	–0.3 to 6	V
Diagnostic Output Terminal	V_{DIAG}	DIAG	–0.3 to 50	V
Sense Amplifier Inputs	V_{CSI}	CSxP, CSxM	–4 to 6.5	V
Sense Amplifier Output	V_{CSO}	CSxO	–0.3 to 6	V
Sense Amplifier Output Offset	V_{OOS}	OOS	–0.3 to 6	V
Bridge Drain Monitor Terminals	V_{BRG}	VBRG	–5 to 55	V
Bootstrap Supply Terminals	V_{Cx}	CA, CB, CC	–0.3 to V_{REG} + 50	V
High-Side Gate Drive Output Terminals	V_{GHx}	GHA, GHB, GHC	V_{Cx} – 16 to V_{Cx} + 0.3	V
		GHA, GHB, GHC (Transient)[3]	–18 to V_{Cx} + 0.3	V
Motor Phase Terminals	V_{Sx}	SA, SB, SC	V_{Cx} – 16 to V_{CX} + 0.3	V
		SA, SB, SC (Transient)[3]	–18 to V_{CX} + 0.3	V
Low-Side Gate Drive Output Terminals	V_{GLx}	GLA, GLB, GLC	V_{REG} – 16 to 18	V
		GLA, GLB, GLC (Transient)[3]	–8 to 18	V
Bridge Low-Side Source Terminals	V_{LSS}	LSSA, LSSB, LSSC	V_{REG} – 16 to 18	V
		LSSA, LSSB, LSSC (Transient)[3]	–8 to 18	V
Ambient Operating Temperature Range	T_A	Limited by power dissipation	–40 to 150	°C
Maximum Continuous Junction Temperature	T_J(max)		165	°C
Transient Junction Temperature	T_{Jt}	Overtemperature event not exceeding 10 seconds, lifetime duration not exceeding 10 hours, determined by design characterization	180	°C
Storage Temperature Range	T_{stg}		–55 to 150	°C

[1] With respect to GND. Ratings apply when no other circuit operating constraints are present.
[2] Lowercase “x” in pin names and symbols indicates a variable sequence character
[3] Not tested in production. Confirmed by design and characterisation.

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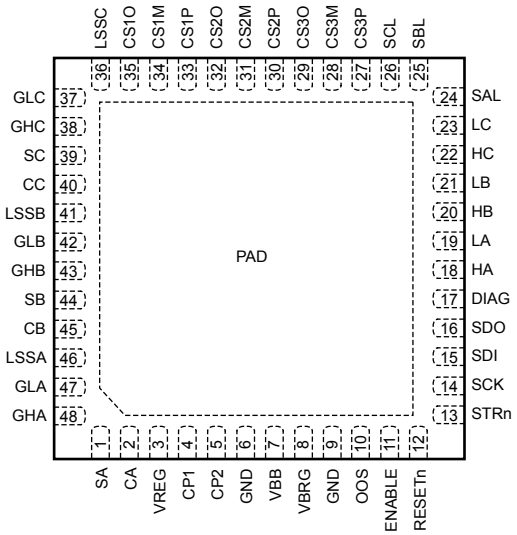
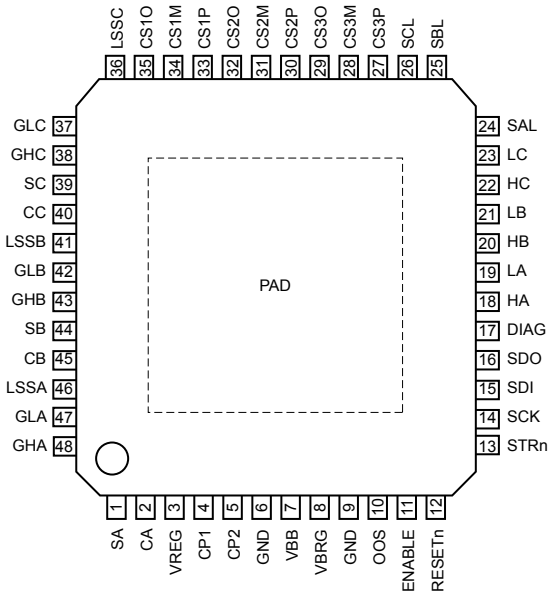


QFN-48 (EV) Package Pinout Diagram



LQFP-48 (JP) Package Pinout Diagram

Terminal List Table

Name	Number	Function
CA	2	Bootstrap Capacitor Phase A
CB	45	Bootstrap Capacitor Phase B
CC	40	Bootstrap Capacitor Phase C
CP1	4	Pump Capacitor
CP2	5	Pump Capacitor
CS1M	34	Current Sense Amp 1 -Input
CS1O	35	Current Sense Amp 1 Output
CS1P	33	Current Sense Amp 1 +Input
CS2M	31	Current Sense Amp 2 -Input
CS2O	32	Current Sense Amp 2 Output
CS2P	30	Current Sense Amp 2 +Input
CS3M	28	Current Sense Amp 3 -Input
CS3O	29	Current Sense Amp 3 Output
CS3P	27	Current Sense Amp 3 +Input
DIAG	17	Programmable Diagnostic Output
ENABLE	11	Direct Output Activity Control
GHA	48	High-Side Gate Drive Phase A
GHB	43	High-Side Gate Drive Phase B
GHC	38	High-Side Gate Drive Phase C
GLA	47	Low-Side Gate Drive Phase A
GLB	42	Low-Side Gate Drive Phase B
GLC	37	Low-Side Gate Drive Phase C
GND	6	Ground
GND	9	Ground
PAD	Pad	Connect To Ground

Name	Number	Function
HA	18	Control Input A High Side
HB	20	Control Input B High Side
HC	22	Control Input C High Side
LA	19	Control Input A Low Side
LB	21	Control Input B Low Side
LC	23	Control Input C Low Side
LSSA	46	Low-Side Source Phase A
LSSB	41	Low-Side Source Phase B
LSSC	36	Low-Side Source Phase C
OOS	10	Sense Amp Programmed Offset Output
RESETn	12	Standby Mode Control
SA	1	Motor Connection Phase A
SAL	24	Phase A Logic Output
SB	44	Motor Connection Phase B
SBL	25	Phase B Logic Output
SC	39	Load Connection Phase C
SCK	14	Serial Clock Input
SCL	26	Phase C Logic Output
SDI	15	Serial Data Input
SDO	16	Serial Data Output
STRn	13	Serial Strobe (Chip Select) Input
VBB	7	Main Power Supply
VBRG	8	High-Side Drain Voltage Sense
VREG	3	Gate Drive Supply Output

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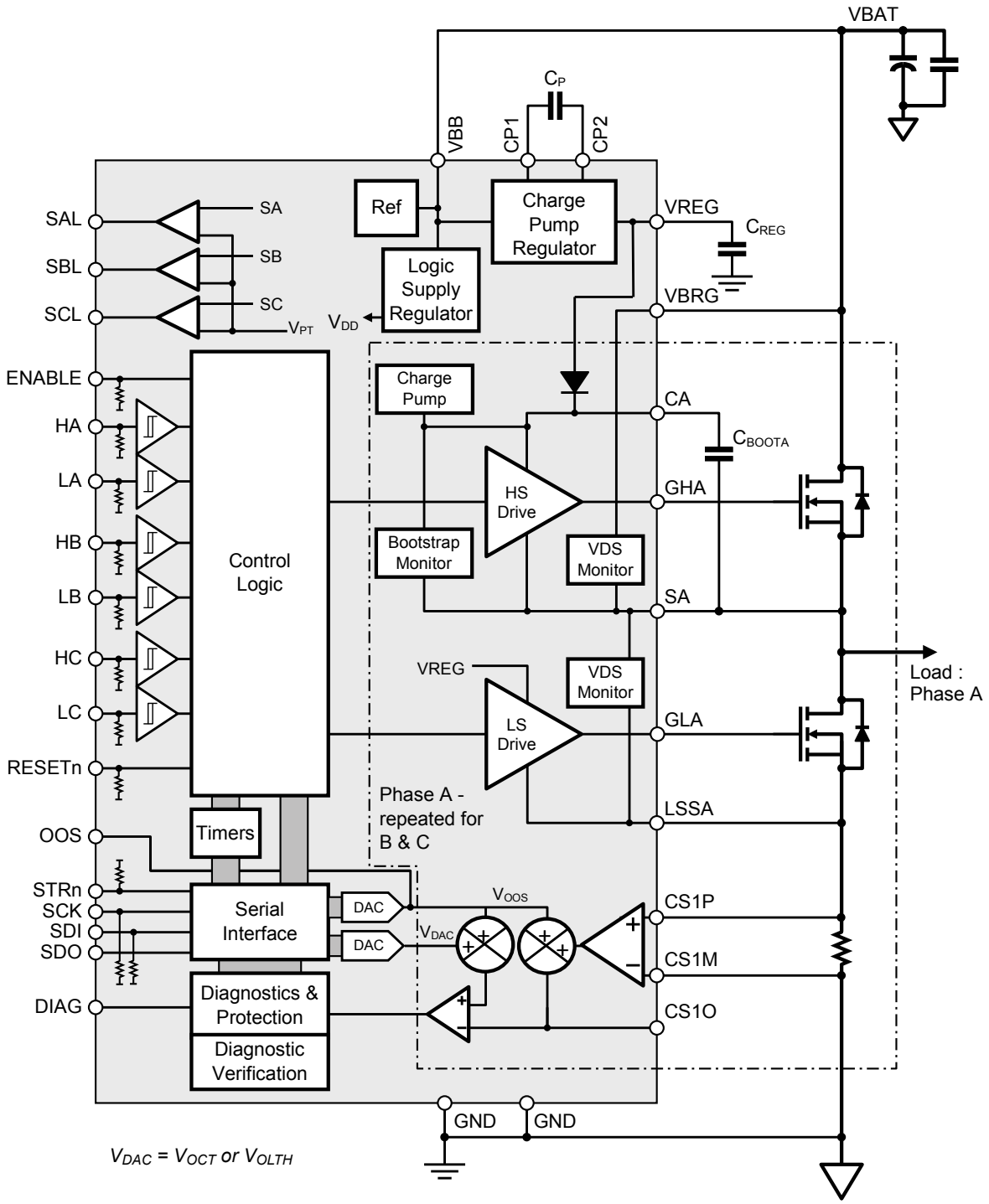
Functional Block Diagram



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ELECTRICAL CHARACTERISTICS: Valid at T_J = –40°C to 150°C, V_{BB} = 5.5 to 50 V, unless otherwise specified

Characteristic	Symbol	Test Conditions		Min.	Typ.	Max.	Unit
SUPPLY AND REFERENCE							
VBB Functional Operating Range	V_{BB}	Operating; outputs active		5.5		50	V
		Operating[1]; outputs disabled		3.4		50	V
		No unsafe states		0		50	V
VBB Quiescent Current	I_{BBQ}	RESETn = high, V_{BB} = 12 V, all gate drive outputs low		–	25	32	mA
	I_{BBS}	RESETn ≤ 300 mV, sleep mode, V_{BB} < 35 V		–	–	10	μA
Internal Logic Supply Regulator Voltage[4][5]	V_{DD}			–	3.3	–	V
VREG Output Voltage	V_{REG}	V_{BB} > 8.5 V, I_{VREG} = 0 to 35 mA	VRG = 0	7.5	8	8.5	V
		7.5 V < V_{BB} ≤ 8.5 V, I_{VREG} = 0 to 30 mA		7.5	8	8.5	V
		6 V < V_{BB} ≤ 7.5 V, I_{VREG} = 0 to 13 mA		7.5	8	8.5	V
		5.5 V < V_{BB} ≤ 6 V, I_{VREG} < 8 mA		7.5	8	8.5	V
		V_{BB} > 9 V, I_{VREG} = 0 to 33 mA	VRG = 1	9	11	11.7	V
		7.5 V < V_{BB} ≤ 9 V, I_{VREG} = 0 to 23 mA		9	11	11.7	V
		6 V < V_{BB} ≤ 7.5 V, I_{VREG} = 0 to 13 mA		7.9	–	–	V
		5.5 V < V_{BB} ≤ 6 V, I_{VREG} < 5 mA		7.9	9.5	–	V
Bootstrap Diode Forward Voltage	V_{fBOOT}	I_D = 10 mA		0.4	0.7	1.0	V
		I_D = 100 mA		1.5	2.2	2.8	V
Bootstrap Diode Resistance	r_D	$r_{D(100\ mA)} = (V_{fBOOT(150\ mA)} - V_{fBOOT(50mA)})/100\ mA$		6	11	24	Ω
Bootstrap Diode Current Limit	I_{DBOOT}			250	500	750	mA
Top-Off Charge Pump Current Limit	I_{TOCPM}			–	100	–	μA
High-Side Gate Drive Static Load Resistance	R_{GSH}			300	–	–	kΩ
System Clock Period	t_{OSC}			42.5	50	57.5	ns
GATE OUTPUT DRIVE							
Turn-On Time	t_r	C_{LOAD} = 10 nF, 20% to 80% points		–	190	–	ns
Turn-Off Time	t_f	C_{LOAD} = 10 nF, 80% to 20% points		–	120	–	ns
Pull-Up On-Resistance	$R_{DS(on)UP}$	T_J = 25°C, I_{GH} = –150 mA[2]		5	8	11	Ω
		T_J = 150°C, I_{GH} = –150 mA[2]		9.16	15	19.16	Ω
Pull-Down On-Resistance	$R_{DS(on)DN}$	T_J = 25°C, I_{GL} = 150 mA[2]		1.5	2.4	3.1	Ω
		T_J = 150°C, I_{GL} = 150 mA[2]		2.9	4	5	Ω
GHx Output Voltage (High)	V_{GHH}	Bootstrap capacitor fully charged		V_{Cx} – 0.2	–	–	V
GHx Output Voltage (Low)	V_{GHL}	–10 μA < I_{GH} < 10 μA		–	–	V_{Sx} + 0.3	V
GLx Output Voltage (High)	V_{GLH}			V_{REG} – 0.2	–	–	V
GLx Output Voltage (Low)	V_{GLL}	–10 μA < I_{GL} < 10 μA		–	–	V_{LSS} + 0.3	V
Gate-Source Voltage – MOSFET On	V_{GSon}	No faults present		V_{ROFF}	–	V_{REG}	V

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Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
GATE OUTPUT DRIVE (continued)						
GHx Passive Pull-Down	R_{GHPD}	V_{BB} = 0 V, $V_{GHx} – V_{Sx}$ < 0.1 V	–	950	–	kΩ
		V_{BB} = 0 V, I_{GHx} = 500 µA	–	4	–	kΩ
GLx Passive Pull-Down	R_{GLPD}	V_{BB} = 0 V, $V_{GLx} – V_{LSSx}$ < 0.1 V	–	950	–	kΩ
		V_{BB} = 0 V, I_{GLx} = 500 µA	–	4	–	kΩ
Turn-Off Propagation Delay	$t_{P(off)}$	Input change to unloaded gate output change (see Figure 3; DT[5:0] = 0	60	90	140	ns
		Input change to unloaded gate output change, excluding jitter[6] (see Figure 3); DT[5:0] > 0	135	165	215	ns
Turn-On Propagation Delay	$t_{P(on)}$	Input change to unloaded gate output change (see figure 5); DT[5:0] = 0	50	80	130	ns
		Input change to unloaded gate output change, excluding jitter[6] (see Figure 3); DT[5:0] > 0	125	155	205	ns
Propagation Delay Matching (Phase-to-Phase)	Δt_{PP}	Same state change, DT[5:0] = 0	–	5	15	ns
Propagation Delay Matching (On-to-Off)	Δt_{OO}	Single phase, DT[5:0] = 0	–	15	30	ns
Propagation Delay Matching (GHx-to-GLx)	Δt_{HL}	Same state change, DT[5:0] = 0	–	–	20	ns
Dead Time (Turn-Off To Turn-On Delay)	t_{DEAD}	DT[5:0] = 100000 (see Figure 3)	1.25	1.6	2.15	µs
LOGIC INPUTS AND OUTPUTS						
Input Low Voltage	V_{IL}		–	–	0.8	V
Input High Voltage	V_{IH}		2.0	–	–	V
Input Hysteresis	V_{Ihys}		250	550	–	mV
Input Pull-Down HA, LA, HB, LB, HC, LC, ENABLE, RESETn	R_{PD}	0 < V_{IN} ≤ 5 V	–	50	–	kΩ
	I_{PD}	5 V < V_{IN} < 50 V	–	100	–	µA
Input Pull-Down SDI, SCK	R_{PDS}	0 < V_{IN} < 5 V	–	50	–	kΩ
Input Pull-Up STRn (to V_{DD})	R_{PUS}		–	50	–	kΩ
Output Low Voltage	V_{OL}	I_{OL}= 1 mA[2]	–	0.2	0.4	V
Output High Voltage	V_{OH}	I_{OL} = –200 µA[2]	3.0	–	–	V
		I_{OL}= –1 mA[2]	2.4	V_{DD} – 0.2	–	V
Output Leakage SDO[2]	I_{OSD}	0 V < V_{SDO} < V_{DD}, STRn=1	–1	–	1	µA
Output Leakage DIAG[2]	I_{ODI}	0 V < V_{DIAG} < 6 V, DG[1:0]=0, 1, 3	–	–	1	µA

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Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
LOGIC I/O – DYNAMIC PARAMETERS						
Reset Pulse Width	t_{RST}		1	–	4.5	µs
Reset Shutdown Time	t_{RSD}	RESETn low to gate drives disabled	30	–	–	µs
Clock High Time	t_{SCKH}	A in Figure 2	50	–	–	ns
Clock Low Time	t_{SCKL}	B in Figure 2	50	–	–	ns
Strobe Lead Time	t_{STLD}	C in Figure 2	30	–	–	ns
Strobe Lag Time	t_{STLG}	D in Figure 2	30	–	–	ns
Strobe High Time	t_{STRH}	E in Figure 2	300	–	–	ns
Data Out Enable Time	t_{SDOE}	F in Figure 2	–	–	40	ns
Data Out Disable Time	t_{SDOD}	G in Figure 2	–	–	30	ns
Data Out Valid Time From Clock Falling	t_{SDOV}	H in Figure 2	–	–	40	ns
Data Out Hold Time From Clock Falling	t_{SDOH}	I in Figure 2	5	–	–	ns
Data In Setup Time To Clock Rising	t_{SDIS}	J in Figure 2	15	–	–	ns
Data In Hold Time From Clock Rising	t_{SDIH}	K in Figure 2	10	–	–	ns
Wake Up from Sleep	t_{EN}	C_{REG} = 22 µF	–	–	5	ms
CURRENT SENSE AMPLIFIERS						
Input Offset Voltage	V_{IOS}		–1	–	+1	mV
Input Offset Voltage Drift	ΔV_{IOS}		–2	–	+2	µV/°C
Input Bias Current [2]	I_{BIAS}	0 V < V_{CSP} < V_{DD}, 0 V < V_{CSM} < V_{DD}	–70	–35	–5	µA
Input Offset Current [2]	I_{OS}	V_{ID} = 0 V, V_{CM} in range	–1.5	–	+1.5	µA
Input Common-Mode Range (DC)	V_{CM}	V_{ID} = 0 V	–1.8	–	2	V
Gain	A_V	Default power-up value	–	20	–	V/V
Gain Error	E_A	V_{CM} in range	–1.6	–	1.6	%
Gain Drift	E_{AD}	V_{CM} in range	–30	–	15	ppm/°C
Output Offset	V_{OOS}	Default power-up value	–	2.5	–	V
Output Offset Error	E_{VO}	V_{CM} in range, V_{OOS} > 0 V	–75	±25	75	mV
Output Offset Drift	V_{OOSD}	V_{CM} in range, V_{OOS} > 0 V	–135	–	135	µV/°C
Small Signal –3 dB Bandwidth	BW	Gain = 20 V/V, V_{IN} = 10 mVpp	2	–	–	MHz
Output Settling Time (to within 40 mV)	t_{SET}	V_{CSO} = 1 Vpp square wave, Gain = 20 V/V, C_{OUT} = 200 pF	–	–	1	µs
Output Dynamic Range	V_{CSOUT}	–100 µA < I_{CSO} < 100 µA	0.3	–	4.8	V
Output Voltage Clamp	V_{CSC}	I_{CSO} = –2 mA	4.8	5.2	5.6	V
Output Current Sink [2]	I_{CSsink}	V_{ID} = 0 V, V_{CSO} = 1.5 V, Gain = 20 V/V	220	–	–	µA
Output Current Sink (Boosted) [2][7]	$I_{CSsinkb}$	V_{OOS} = 1.5 V, V_{ID} = –50 mV, Gain = 20 V/V, V_{CSO} = 1.5 V	1	–	–	mA

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Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
CURRENT SENSE AMPLIFIERS (continued)						
Output Current Source [2]	$I_{CSsource}$	V_{ID} = 0 V, V_{CSO} = 1.5 V, Gain = 20 V/V	–	–	–1	mA
VBB Supply Ripple Rejection	PSRR	V_{ID} = 0V, 100 kHz, Gain = 20 V/V	–	75	–	dB
		V_{CSP} = V_{CSM} = 0 V, DC, Gain = 20 V/V	75	–	–	dB
Common-Mode Rejection	CMRR	V_{CM} step from 0 to 200 mV, Gain = 20 V/V	50	100	–	dB
		V_{CM} = 200 mVpp, 100 kHz, Gain = 20 V/V	–	62	–	dB
		V_{CM} = 200 mVpp, 1 MHz, Gain = 20 V/V	–	43	–	dB
		V_{CM} = 200 mVpp, 10 MHz, Gain = 20 V/V	–	25	–	dB
Common-Mode Recovery Time (to within 100 mV)	t_{CMrec}	V_{CM} step from –4 V to 1 V, Gain = 20 V/V, C_{OUT} = 200 pF	–	1	–	µs
Output Slew Rate 10% to 90%	SR	V_{ID} step from 0 to 175 mV, Gain = 20 V/V, C_{OUT} = 200 pF	–	10	–	V/µs
Input Overload Recovery (to within 40 mV)	t_{IDrec}	V_{ID} step from 250 mA to 0 V, Gain = 20 V/V, C_{OUT} = 200 pF	–	1	–	µs
Offset Calibration Time	t_{Cal}	From STRn rising edge	–	–	100	µs
DIAGNOSTICS AND PROTECTION						
VREG Undervoltage, VRG = 0	V_{RON}	V_{REG} rising	6.4	6.6	6.7	V
	V_{ROFF}	V_{REG} falling	5.5	5.7	5.9	V
VREG Undervoltage, VRG = 1	V_{RON}	V_{REG} rising	7.6	7.95	8.2	V
	V_{ROFF}	V_{REG} falling	6.9	7.18	7.4	V
VREG Overvoltage Warning	V_{ROV}	V_{REG} rising	15.5	15.7	16.1	V
VREG Overvoltage Hysteresis	V_{ROVHys}		1200	1400	–	mV
VBB Overvoltage Warning	V_{BBOV}	V_{BB} rising	32	–	36	V
VBB Overvoltage Hysteresis	$V_{BBOVHys}$		1	–	–	V
VBB Undervoltage	V_{BBUV}	V_{BB} falling	–	4.0	–	V
VBB Undervoltage Hysteresis	$V_{BBUVHys}$		–	500	–	mV
VBB POR Voltage	V_{BBR}	V_{BB} falling	–	3.2	3.4	V
VBB POR Voltage Hysteresis	V_{BBRHys}		75	115	155	mV
Bootstrap Undervoltage	V_{BCUV}	V_{BOOT} falling, V_{BOOT} = V_{Cx} – V_{Sx}	55	–	66	%V_{REG}
Bootstrap Undervoltage Hysteresis	$V_{BCUVHys}$		–	10	–	%V_{REG}
Gate Drive Undervoltage Warning HS	V_{GSHUV}	V_{GSH} falling	V_{BOOT} – 1.4	V_{BOOT} – 1	V_{BOOT} – 0.8	V
Gate Drive Undervoltage Warning LS	V_{GSLUV}	V_{GSL} falling	V_{REG} – 1.4	V_{REG} – 1	V_{REG} – 0.8	V
Logic Terminal Overvoltage Warning	V_{LOV}	V_L rising on HA, LA, HB, LB, HC, LC, RESETn, ENABLE, or DIAG	6.5	–	9	V
ENABLE Input Timeout	t_{ETO}		90	100	110	ms
VBRG Input Voltage	V_{BRG}	When VDS monitor is active	5.5	V_{BB}	50	V

Continued on the next page…

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ELECTRICAL CHARACTERISTICS (continued): Valid at T_J = –40°C to 150°C, V_{BB} = 5.5 to 50 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
DIAGNOSTICS AND PROTECTION (continued)						
VBRG Input Current	I_{VBRG}	V_{DSTH} = default, V_{BB} = 12 V, 0 V < V_{BRG} < V_{BB}	–	–	500	µA
	I_{VBRGQ}	Sleep mode V_{BB} < 35 V	–	–	5	µA
VDS Threshold, High-Side	V_{DSTH}	Default power-up value	1.1	1.2	1.3	V
		V_{BRG} ≥ 7 V [8][9]	–	–	3.15	V
		5.5 V ≤ V_{BRG} < 7 V [8][9]	–	–	1.5	V
High-Side VDS Threshold Offset [3]	V_{DSTHO}	High side on, V_{DSTH} ≥ 1 V	–300	±100	+300	mV
		High side on, V_{DSTH} <1 V	–150	±50	+150	mV
VDS Threshold – Low-Side	V_{DSTL}	Default power-up value	1.1	1.2	1.3	V
		V_{BB} ≥ 5.5 V [8]	–	–	3.15	V
Low-Side VDS Threshold Offset [3]	V_{DSTLO}	Low side on, V_{DSTL} ≥ 1 V	–200	±100	+200	mV
		Low side on, V_{DSTL} <1 V	–150	±50	+150	mV
VDS and VGS Qualify Time	t_{VDQ}	Default power-up value	1.25	1.6	2.15	µs
Phase Comparator Threshold	V_{PT}	Phase voltage rising, default power-up value	47	50	52	%V_{BRG}
Overcurrent Threshold Voltage	V_{OCT}	Default power-up value	0.8	0.9	1.08	V
Overcurrent Qualify Time	t_{OCQ}	Default power-up value	6.75	7.5	8.25	µs
On-State Open-Load Threshold Voltage	V_{OLTH}	Default power-up value	90	200	260	mV
Off-State Open-Load Threshold Voltage	V_{OLTT}		1.2	1.5	1.8	V
Off-State Sink Current on SB	I_{OLTS}		6	10	13	mA
Off-State Source Current on SA, SC	I_{OLTT}	OLI = 0	–	–70	–	µA
Off-State Source Current on SA, SC	I_{OLTT}	OLI = 1	–	–400	–	µA
Open Load Timeout	t_{OLTO}		90	100	110	ms
DIAG Output: Fault Pulse Period	t_{FP}	DG[1:0] = 0,1	90	100	110	ms
DIAG Output: Fault Pulse Duty Cycle	D_{FP}	DG[1:0] = 0,1; no fault present	–	80	–	%
		DG[1:0] = 0,1; fault present	–	20	–	%
DIAG Output: Temperature Range	V_{TJD}	DG[1:0] = 1,0	–	1440	–	mV
DIAG Output: Temperature Slope	A_{TJD}	DG[1:0] = 1,0	–	–3.92	–	mV/°C
DIAG Output: Clock Division Ratio	N_D	DG[1:0] = 1,1		256000		–
Temperature Warning Threshold	T_{JWH}	Temperature increasing	125	135	145	ºC
Temperature Warning Hysteresis	T_{JWHhys}		–	15	–	ºC
Overtemperature Threshold	T_{JF}	Temperature increasing	165	175	185	ºC
Overtemperature Hysteresis	T_{JHyst}	Recovery = T_{JF} – T_{JHyst}	–	15	–	ºC

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ELECTRICAL CHARACTERISTICS (continued): Valid at T_J = –40°C to 150°C, V_{BB} = 5.5 to 50 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
DIAGNOSTIC VERIFICATION						
VBRG Open Threshold	V_{BRO}	V_{BB} – V_{BRG} rising; default value	1.4	2	2.9	V
VBRG Open Threshold Hysteresis	V_{BROHys}		–	500	–	mV
LSS Open Threshold	V_{LSO}		4.5	5	5.5	V
LSS Open Threshold Hysteresis	V_{LSOHys}		–	500	–	mV
LSS Verification Current	I_{LU}		–	–100	–	µA
Sense Amp Verification Current	I_{SAD}	V_{CM} = 1.2 V	–	–40	–	µA
Phase Test Pull-Down Current	I_{SD}		–	280	–	µA
Phase Test Pull-Up Current	I_{SU}		–	-400	–	µA

[1] No internal reset.
[2] For input and output current specifications, negative current is defined as coming out of (being sourced by) the specified device terminal.
[3] VDS offset is the difference between the programmed threshold, V_{DSTH} or V_{DSTL} and the actual trip voltage.
[4] V_{DD} derived from V_{BB} for internal use only. Not accessible on any device pin.
[5] Confirmed by design.
[6] For DT[5:0] > 0, jitter of ±25 ns must be added to the limits shown.
[7] If the amplifier output voltage (V_{CSO}) is more positive than the value demanded by the applied differential input (V_{ID}) and output offset (V_{OOS}) conditions, then output current sink capability is boosted to enhance negative going transient response.
[8] Maximum value of VDS threshold that should be set in the configuration registers for correct operation when V_{BB} is within the stated range.
[9] If V_{BB} – V_{BRG} > V_{BRO} then a VBRG disconnected fault will be detected as will high side VDS Overvoltage faults on all three phases. If ESF = 1, all six gate drive outputs will be disabled.

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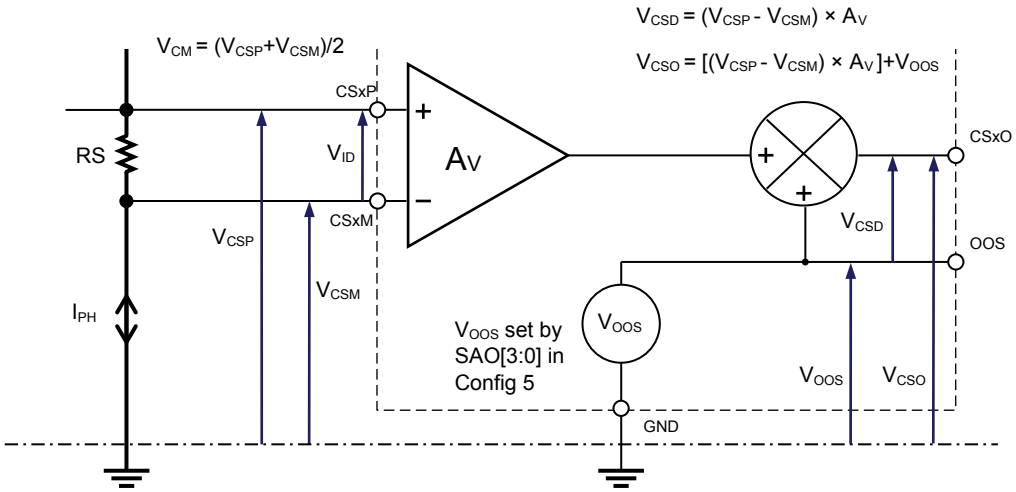
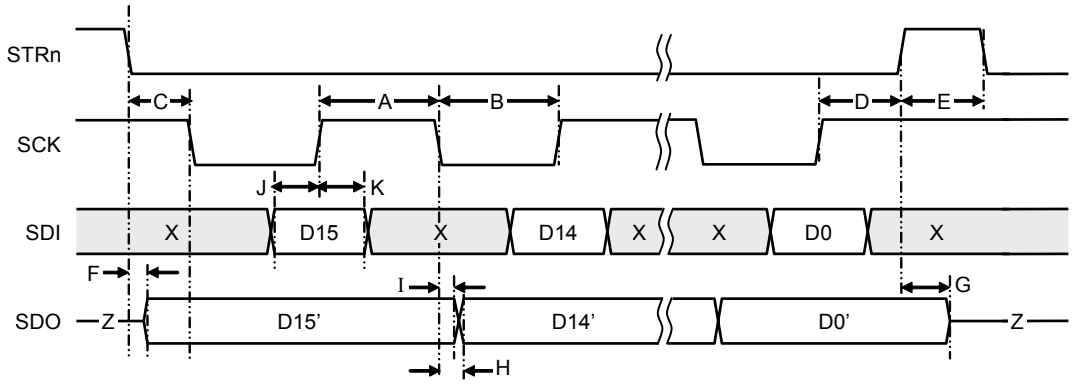


Figure 1: Sense Amplifier Voltage Definitions



X=don't care, Z=high impedance (tri-state)

Figure 2: Serial Interface Timing

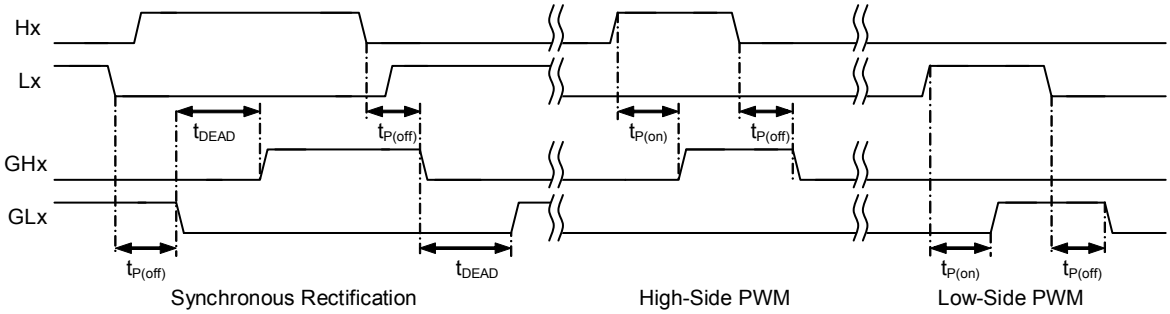


Figure 3: Gate Drive Timing, Phase Logic Inputs

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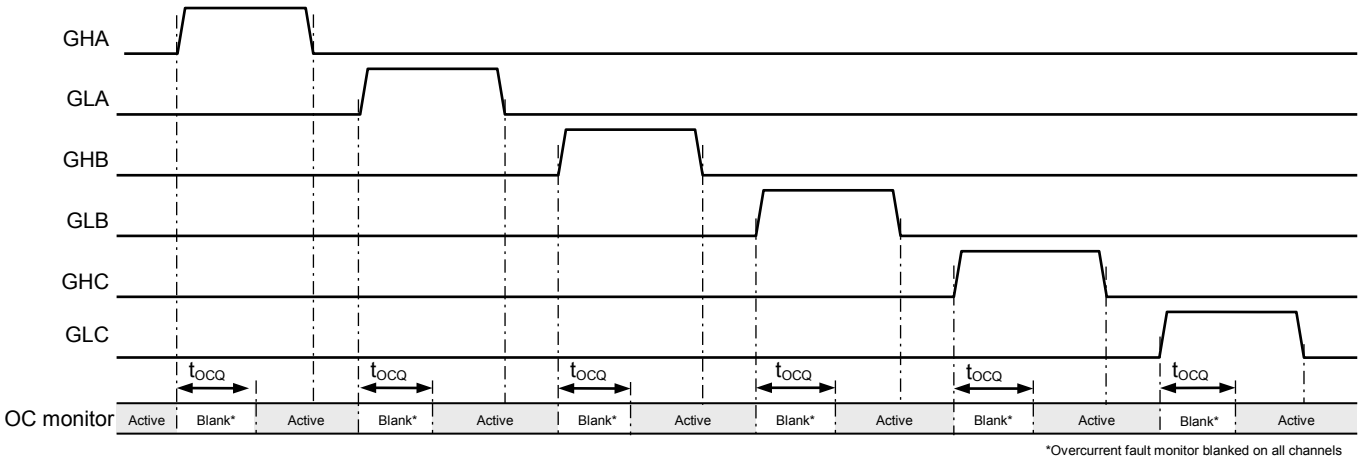

Figure 4: Overcurrent Fault Monitor – Blank Mode Timing (OCQ = 1)

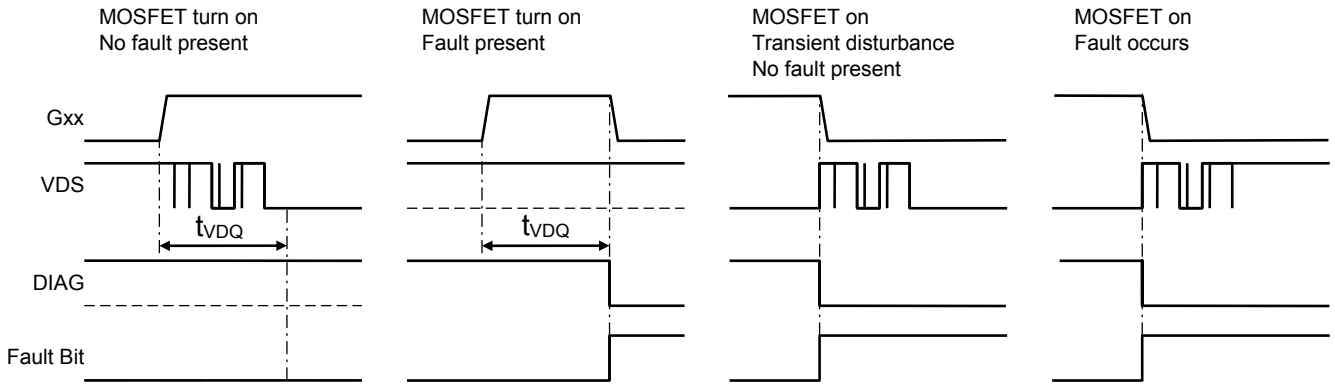

Figure 5: VDS Fault Monitor – Blank Mode Timing (VDQ = 1)

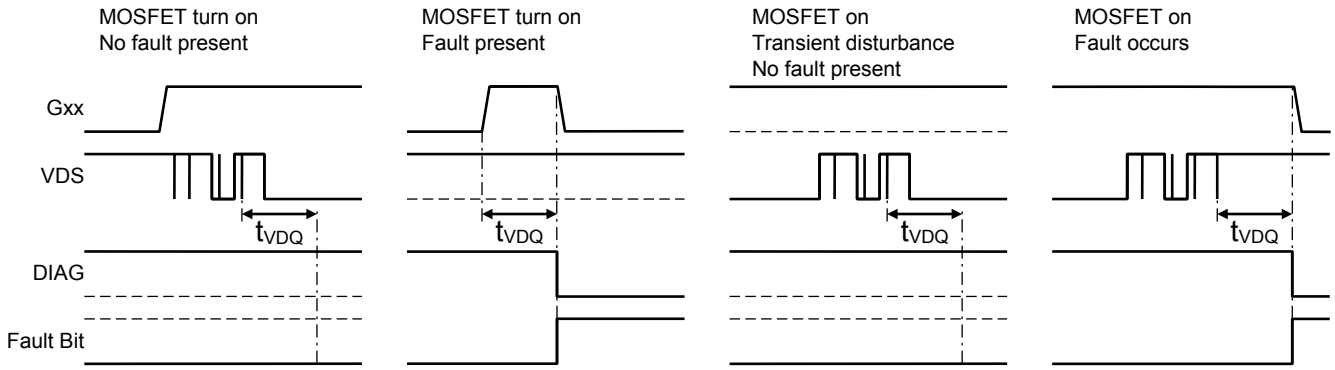

Figure 6: VDS Fault Monitor – Debounce Mode Timing (VDQ = 0)

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Logic Truth Tables

Table 1: Control Logic (Discrete Logic Inputs)

Phase A					Phase B					Phase C				
HA	LA	GHA	GLA	SA	HB	LB	GHB	GLB	SB	HC	LC	GHC	GLC	SC
0	0	LO	LO	Z	0	0	LO	LO	Z	0	0	LO	LO	Z
0	1	LO	HI	LO	0	1	LO	HI	LO	0	1	LO	HI	LO
1	0	HI	LO	HI	1	0	HI	LO	HI	1	0	HI	LO	HI
1	1	LO	LO	Z	1	1	LO	LO	Z	1	1	LO	LO	Z

HI = high-side FET active, LO = low-side FET active
Z = high impedance, both FETs off
Control register bits AH, AL, BH, BL, CH, and CL set to 0; RESETn = 1, ENABLE = 1

Table 2: Control Logic (Serial Register)

Phase A					Phase B					Phase C				
AH	AL	GHA	GLA	SA	BH	BL	GHB	GLB	SB	CH	CL	GHC	GLC	SC
0	0	LO	LO	Z	0	0	LO	LO	Z	0	0	LO	LO	Z
0	1	LO	HI	LO	0	1	LO	HI	LO	0	1	LO	HI	LO
1	0	HI	LO	HI	1	0	HI	LO	HI	1	0	HI	LO	HI
1	1	LO	LO	Z	1	1	LO	LO	Z	1	1	LO	LO	Z

HI = high-side FET active, LO = low-side FET active
Z = high impedance, both FETs off
Logic 0 input on HA, LA, HB, LB, HC, and LC. RESETn = 1, ENABLE = 1

Table 3: Combination of Discrete Logic and Serial Register Control Inputs

Terminal	Register	Internal
Hx	xH	HIx
0	0	0
0	1	1
1	0	1
1	1	1

Terminal	Register	Internal
Lx	xL	LOx
0	0	0
0	1	1
1	0	1
1	1	1

The three phases are controlled independently.

Internal control signals (HIx, LOx) are derived by combining the logic states applied to the control input pins (Hx, Lx) with the bit patterns held in the Control register (xH, xL).

Normally the input pins or the Control register method is used for control with the other being held inactive (all pins or bits at logic 0).

ENABLE	HIx	LOx	GHx	GLx	Sx	Comment
1	0	0	L	L	Z	Phase disabled
1	0	1	L	H	LO	Phase sinking
1	1	0	H	L	HI	Phase sourcing
1	1	1	L	L	Z	Phase disabled
0	X	X	L	L	Z	Phase disabled

X = don't care

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Table 4: Open-Load Detect Mode

						OL detect	
HIA	LOA	HIB	LOB	HIC	LOC	Off-State	On-State
0	0	0	0	0	0	Yes	
0	0	0	0	0	1		
0	0	0	0	1	0		
0	0	0	0	1	1	Yes	
0	0	0	1	0	0		
0	0	0	1	0	1		
0	0	0	1	1	0		Yes
0	0	0	1	1	1		
0	0	1	0	0	0		
0	0	1	0	0	1		Yes
0	0	1	0	1	0		
0	0	1	0	1	1		
0	0	1	1	0	0	Yes	
0	0	1	1	0	1		
0	0	1	1	1	0		
0	0	1	1	1	1	Yes	
0	1	0	0	0	0		
0	1	0	0	0	1		
0	1	0	0	1	0		Yes
0	1	0	0	1	1		
0	1	0	1	0	0		
0	1	0	1	0	1		
0	1	0	1	1	0		Yes
0	1	0	1	1	1		
0	1	1	0	0	0		Yes
0	1	1	0	0	1		Yes
0	1	1	0	1	0		Yes
0	1	1	0	1	1		Yes
0	1	1	1	0	0		
0	1	1	1	0	1		
0	1	1	1	1	0		
0	1	1	1	1	1		

						OL detect	
HIA	LOA	HIB	LOB	HIC	LOC	Off-State	On-State
1	0	0	0	0	0		
1	0	0	0	0	1		Yes
1	0	0	0	1	0		
1	0	0	0	1	1		
1	0	0	1	0	0		Yes
1	0	0	1	0	1		Yes
1	0	0	1	1	0		Yes
1	0	0	1	1	1		Yes
1	0	1	0	0	0		
1	0	1	0	0	1		Yes
1	0	1	0	1	0		
1	0	1	0	1	1		
1	0	1	1	0	0		
1	0	1	1	0	1		Yes
1	0	1	1	1	0		
1	0	1	1	1	1		
1	1	0	0	0	0	Yes	
1	1	0	0	0	1		
1	1	0	0	1	0		
1	1	0	0	1	1	Yes	
1	1	0	1	0	0		
1	1	0	1	0	1		
1	1	0	1	1	0		Yes
1	1	0	1	1	1		
1	1	1	0	0	0		
1	1	1	0	0	1		Yes
1	1	1	0	1	0		
1	1	1	0	1	1		
1	1	1	1	0	0	Yes	
1	1	1	1	0	1		
1	1	1	1	1	0		
1	1	1	1	1	1	Yes	

HIx, LOx derived from Table 3.
RESETn = 1, ENABLE = 1.
AOL = 1.

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FUNCTIONAL DESCRIPTION

The A4911 provides six high current gate drives capable of driving a wide range of N-channel power MOSFETs. The gate drives are configured as three half bridges, each with a high-side drive and a low-side drive. The three half bridges can be operated independently or together as a three-phase bridge driver for BLDC or PMSM motors.

Gate drives have programmable drive voltage and drive strength and can be controlled individually with logic inputs or through the SPI-compatible serial interface. The control logic inputs provide a very flexible solution for many motor control applications. Independent control over each MOSFET allows each driver to be driven with an independent PWM signal for full sinusoidal excitation. All logic inputs are TTL compatible and can be driven by 3.3 or 5 V logic outputs. The logic inputs are battery voltage compliant meaning they can be shorted to ground or supply without damage, up to the maximum battery voltage of 50 V.

The A4911 requires a single unregulated supply of 5.5 to 50 V and includes an integrated linear regulator to generate internal logic supply voltage, V_{DD}.

Circuit functions are provided within the A4911 to ensure that, under normal operating conditions, all external power MOSFETs are fully enhanced at supply voltages down to 5.5 V. For extreme battery voltage drop conditions, the A4911 is guaranteed not to reset any internal states at supply voltages down to 3.4 V. However, below 5.5 V, it is possible that the gate drive output may fall below a safe level and be disabled. A low-power sleep mode allows the A4911, the power bridge, and the load to remain connected to a vehicle battery supply without the need for an additional supply switch.

The A4911 includes a number of diagnostic features to provide indication of and/or protection against undervoltage, overvoltage, overtemperature, and power bridge faults. A single diagnostic output pin can be programmed to provide optional diagnostic outputs, and detailed diagnostic information is available through the serial interface.

For systems requiring a higher level of safety integrity, the A4911 includes additional overvoltage monitors on the supplies and the control inputs. In addition, the integrated diagnostics include self-test and verification circuits to ensure verifiable diagnostic operation. When used in conjunction with appropriate system level control, these features can assist power drive systems using the A4911 to meet stringent ASIL D safety requirements.

The serial interface also provides access to programmable dead time, fault blanking time, programmable V_{DS} threshold for short detection and programmable thresholds and currents for open-load detection.

The A4911 includes three low-side current sense amplifiers with programmable gain and offset. The amplifiers are specifically designed for current sensing in the presence of high voltage and current transients. These amplifiers can be used independently to provide low-side current sensing in three phases or can be used together to provide redundant current sensing. The A4911 can also check the connections from the current sense amplifiers to the sensing links using integrated verification circuits. The programmed output offset voltage is available as the reference potential with respect to which amplifier output voltage should be measured.

Input and Output Terminal Functions

VBB: Main power supply for internal regulators and charge pump. The main power supply should be connected to VBB through a reverse voltage protection circuit and should be decoupled with ceramic capacitors connected close to the supply and ground terminals.

VBRG: Sense input to the top of the external MOSFET bridge. Allows accurate measurement of the voltage at the drain of the high-side MOSFETs in the bridge.

CP1, CP2: Pump capacitor connection for charge pump. Connect a 470 nF or larger ceramic capacitor between CP1 and CP2.

VREG: programmable regulated voltage, 8 or 11 V, used to supply the low-side gate drivers and to charge the bootstrap capacitors. A sufficiently large storage capacitor must be connected to this terminal to provide the transient charging current.

GND (×2): Ground. Connect both GND terminals together at the A4911—see Layout Recommendations section for further information.

CA, CB, CC: High-side connections for the bootstrap capacitors and positive supply for high-side gate drivers.

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GHA, GHB, GHC: High-side, gate-drive outputs for external N-channel MOSFETs.

SA, SB, SC: Load phase connections. These terminals sense the voltages switched across the load. They are also connected to the negative side of the bootstrap capacitors and are the negative supply connections for the floating high-side drivers.

GLA, GLB, GLC: Low-side, gate-drive outputs for external N-channel MOSFETs.

LSSA, LSSB, LSSC: Low-side return path for discharge of the capacitance on the MOSFET gates, connected to the common sources of the low-side external MOSFETs independently through a low-impedance track.

HA, HB, HC: Logic inputs with pull-down to control the high-side gate drive outputs. Battery voltage compliant terminal.

LA, LB, LC: Logic inputs with pull-down to control the low-side gate drive outputs. Battery voltage compliant terminal.

SDI: Serial data logic input with pull-down. 16-bit serial word input MSB first.

SDO: Serial data output. High impedance when STRn is high. Outputs bit 15 of the Status register, the fault flag, as soon as STRn goes low.

SCK: Serial clock logic input with pull-down. Data is latched in from SDI on the rising edge of SCK. There must be 16-rising edges per write and SCK must be held high when STRn changes.

STRn: Serial data strobe and serial access enable logic input with pull-up. When STRn is high, any activity on SCK or SDI is ignored and SDO is high impedance, allowing multiple SDI slaves to have common SDI, SCK, and SDO connections.

CS1P, CS1M, CS2P, CS2M, CS3P, CS3M: Current sense amplifier inputs.

CS1O, CS2O, CS3O: Current sense amplifier outputs.

OOS: Monitor point for programmable analog output offset voltage applied to current sense amplifiers. Set value determined by SAO[3:0].

DIAG: Diagnostic output. Programmable output to provide one of four functions: fault flag, pulsed fault flag, temperature, and internal timer. Default is fault flag.

ENABLE: Disables all gate drive outputs when pulled low in direct mode or after a timeout in watchdog mode. In direct mode, it provides an independent output disable, directly to the gate drive outputs, to allow a fast disconnect on the power bridge. Can be pulled to VBB.

RESETn: Resets fault states when pulsed low. Forces low-power shutdown (sleep) when held low for more than the RESET shutdown time, t_{RSD}. Can be pulled to VBB.

SAL, SBL, SCL: Logic level outputs representing the state of each phase determined by the output of a programmable threshold comparator.

Power Supplies

A single power supply voltage is required. The main power supply, V_{BB}, should be connected to VBB through a reverse voltage protection circuit. A 100 nF ceramic decoupling capacitor must be connected close to the supply and ground terminals.

An independent internal regulator provides the supply to the internal logic defined as V_{DD}. All logic is guaranteed to operate correctly to below the regulator undervoltage levels ensuring that the A4911 will continue to operate safely until all logic is reset when a power-on-reset state is present.

The A4911 will operate within specified parameters with V_{BB} from 5.5 to 50 V and will continue to function with outputs disabled at V_{BB} down to 3.4 V. It will operate safely between 0 and 50 V under all supply switching conditions. This provides a very rugged solution for use in the harsh automotive environment.

Pump Regulator

The gate drivers are powered by a programmable voltage internal regulator which limits the supply to the drivers and therefore the maximum gate voltage. At low supply voltage, the regulated supply is maintained by a charge pump boost converter which requires a pump capacitor of 470 nF or larger connected between the CP1 and CP2 terminals.

The regulated voltage, VREG, can be programmed to 8 or 11 V and is available on the VREG terminal. The voltage level is selected by the value of the VRG bit in the Config 6 register. When VRG = 1, the voltage is set to 11 V; when VRG = 0, the

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voltage is set to 8 V. A sufficiently large storage capacitor (see Applications Information section) must be connected to this terminal to provide the transient charging current to the low-side drivers and the bootstrap capacitors.

Gate Drives

The A4911 is designed to drive external, low on-resistance, power N-channel MOSFETs. It will supply the large transient currents necessary to quickly charge and discharge the external MOSFET gate capacitance in order to reduce dissipation in the external MOSFET during switching. The charge current for the low-side drives and the recharge current for the bootstrap capacitors is provided by the capacitor on the VREG terminal. The charge current for the high-side drives is provided by the bootstrap capacitors connected between the Cx and Sx terminals, one for each phase. MOSFET gate charge and discharge rates may be controlled by setting a group of parameters via the serial interface.

Bootstrap Supply

When the high-side drivers are active, the reference voltage for the driver rises close to the bridge supply voltage. The supply to the driver then must exceed the bridge supply voltage to ensure that the driver remains active. This temporary high-side supply is provided by bootstrap capacitors, one for each high-side driver. These three bootstrap capacitors are connected between the bootstrap supply terminals, CA, CB, CC, and the corresponding high-side reference terminal, SA, SB, SC.

The bootstrap capacitors are independently charged to approximately V_{REG} when the associated reference Sx terminal is low. When the output swings high, the voltage on the bootstrap supply terminal rises with the output to provide the boosted gate voltage needed for the high-side N-channel power MOSFETs.

Bootstrap Charge Management

The A4911 monitors the individual bootstrap capacitor charge voltages to ensure sufficient high-side drive. It also includes an optional bootstrap capacitor charge management system (bootstrap manager) to ensure that the bootstrap capacitor remains sufficiently charged under all conditions. The bootstrap manager is enabled by default, but may be disabled by setting the DBM bit to 1. This may be required in systems where the output MOSFET switching must only be allowed by the controlling processor.

Before a high-side drive can be turned on, the bootstrap capacitor voltage must be higher than the turn-on voltage threshold, $V_{BCUV} + V_{BCUVHys}$. If this is not the case, then the A4911 will attempt to charge the bootstrap capacitor by activating the complementary low-side drive. Under normal circumstances, this will charge the capacitor above the turn-on voltage in a few microseconds and the high-side drive will then be enabled. The bootstrap voltage monitor remains active while the high-side drive is active, and if the voltage drops below the turn-off voltage threshold, V_{BCUV}, a charge cycle is also initiated.

The bootstrap charge management circuit may actively charge the bootstrap capacitor regularly when the PWM duty cycle is very high, particularly when the PWM off-time is too short to permit the bootstrap capacitor to become sufficiently charged.

In some safety systems, the gate driver is not permitted to turn on a MOSFET without a direct command from the controller. In this case, the bootstrap manager may be disabled by setting the DBM bit to 1. If the bootstrap manager is disabled, then the user must ensure that the bootstrap capacitor does not become discharged below the bootstrap undervoltage threshold, V_{BCUV}, or a bootstrap fault will be indicated and the outputs disabled. This can happen with very high PWM duty cycles when the charge time for the bootstrap capacitor is insufficient to ensure a sufficient recharge to match the MOSFET gate charge transfer during turn on.

If, for any reason, the bootstrap capacitor cannot be sufficiently charged, a bootstrap fault will occur—see Diagnostic Monitors section for further details.

Top-Off Charge Pump

An additional “top-off” charge pump is provided for each phase, which will allow the high-side drive to maintain the gate voltage on the external MOSFET indefinitely, ensuring so-called 100% PWM if required. This is a low-current trickle charge pump and is only operated after a high side has been signaled to turn on. There is a small amount of bias current drawn from the Cx terminal to operate the floating high side circuit (<40 μA), and the charge pump simply provides enough drive to ensure the bootstrap voltage, and hence the gate voltage, will not droop due to this bias current.

In some applications, a safety resistor is added between the gate and source of each MOSFET in the bridge. When a high-side MOSFET is held in the on-state, the current through the associated high-side gate-source resistor (R_{GSH}) is provided by the

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high-side driver, and therefore appears as a static resistive load on the top-off charge pump. The minimum value of R_{GSH} for which the top-off charge pump can provide current, without dropping below the bootstrap undervoltage threshold, is defined in the Electrical Characteristics table.

In all cases, the charge required for initial turn-on of the high-side gate is always supplied by the bootstrap capacitor. If the bootstrap capacitor becomes discharged, the top-off charge pump alone will not provide sufficient current to allow the MOSFET to turn on.

High-Side Gate Drive

High-side, gate-drive outputs for external N-channel MOSFETs are provided on pins GHA, GHB, and GHC. GHx = 1 (or "high") means that the upper half of the driver is turned on and its drain will source current to the gate of the high-side MOSFET in the external motor-driving bridge, turning it on. GHx = 0 (or "low") means that the lower half of the driver is turned on and its drain will sink current from the external MOSFET's gate circuit to the respective Sx terminal, turning it off.

The reference points for the high-side drives are the load phase connections, SA, SB, and SC. These terminals sense the voltages at the load connections. These terminals are also connected to the negative side of the bootstrap capacitors and are the negative supply reference connections for the floating high-side drivers. The discharge current from the high-side MOSFET gate capacitance flows through these connections which should have low-impedance traces to the MOSFET bridge.

MOSFET gate charge and discharge rates may be controlled via the serial interface as detailed in the Gate Drive Control section below.

Low-Side Gate Drive

The low-side, gate-drive outputs on GLA, GLB, and GLC are each referenced to the corresponding LSSx terminal. These outputs are designed to drive external N-channel power MOSFETs. GLx = 1 (or "high") means that the upper half of the driver is turned on and its drain will source current to the gate of the low-side MOSFET in the external power bridge, turning it on. GLx = 0 (or "low") means that the lower half of the driver is turned on and its drain will sink current from the external MOSFET's gate circuit to the corresponding LSSx terminal, turning it off.

The LSSx terminals provide the return paths for discharge of the capacitances on the low-side MOSFET gates. These terminals are connected independently to the sources of the low-side external MOSFETs through low-impedance tracks.

MOSFET gate charge and discharge rates may be controlled via the serial interface as detailed in the Gate Drive Control section below.

Gate Drive Passive Pull-Down

Each gate drive output includes a discharge circuit to ensure that any external MOSFET connected to the gate drive output is held off when the power is removed. This discharge circuit appears as a variable resistance pull-down, but is not active when the A4911 is in normal operating mode. At low gate source voltage, the resistance is approximately 950 kΩ to ensure that any charge accumulated on the MOSFET gate has a discharge path. This resistance reduces rapidly as the voltage increases such that any MOSFET gate that becomes charged by external means is rapidly discharged to below the turn-on threshold. In some applications, this can eliminate the requirement for a permanent external gate source resistor.

Dead Time

To prevent cross-conduction (shoot-through) in any phase of the power MOSFET bridge, it is necessary to have a dead-time delay between a high- or low-side turn off and the next complementary turn-on event. The potential for cross-conduction occurs when any complementary high-side and low-side pair of MOSFETs are switched at the same time, for example, at the PWM switchpoint. In the A4911, the dead time for all phases is set by the contents of the DT[5:0] bits in Configuration 0 register. These six bits contain a positive integer that determines the dead time by division from the system clock.

The dead time is defined as:

$$t_{DEAD} = n \times 50 \text{ ns}$$

where n is a positive integer defined by DT[5:0] and t_{DEAD} has a minimum active value of 100 ns.

For example, when DT[5:0] contains [11 0000] (= 48 in decimal), then t_{DEAD} = 2.4 µs, typically.

The accuracy of t_{DEAD} is determined by the accuracy of the system clock as defined in the Electrical Characteristics table. The range of t_{DEAD} is 100 ns to 3.15 µs. A value of 1, or 2 in DT[5:0], sets the minimum active dead time of 100 ns.

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If DT[5:0] is set to zero the dead timer is disabled and no minimum dead time is generated by the A4911. The logic that prevents permanent cross-conduction is, however, still active. Adequate dead time must be generated externally by, for example, the microcontroller producing the drive signals applied to the A4911 logic inputs or Control register.

If the dead timer is disabled (DT[5:0] = 0) and bootstrap management is enabled (DBM = 0), dead time must be controlled by the A4911 on any bootstrap management cycles that are required. In these circumstances, a fixed dead time of 3.15 µs is applied even though DT[5:0] = 0.

If using gate drive control, the extended MOSFET switching times that result must be accounted for when setting dead time as described in the Gate Drive Control section below.

The internally generated dead time is only present if the on command for one MOSFET occurs within one dead time after the off command for its complementary partner. In the case where one side of a phase drive is permanently off, for example when using diode rectification with slow decay, then the dead time does not occur. In this case the gate drive turns on within the specified propagation delay after the corresponding phase input goes high (see Figure 3).

Gate Drive Control

MOSFET gate drives are controlled according to the values set in the Config 8 through Config 13 registers.

High-side off-to-on transitions are controlled as detailed in Figure 7a. When a gate drive is commanded to turn on a current, I_1 (as defined by IHR1[3:0]) is sourced on the relevant GHx pin for a duration, t_1 (defined by THR[3:0]). These parameters should typically be set to quickly charge the MOSFET input capacitance to the start of the Miller region, as drain-source voltage does not change during this period. Thereafter, the current sourced on GHx is set to a value of I_2 (as defined by IHR2[3:0]) and remains at this value while the MOSFET transitions through the Miller region, and reaches the fully on state (fully on being determined by the drain-source voltage dropping below $V_{DS} = V_{BRG} - V_{Sx} < V_{DSTH}$). I_2 should be set to achieve the required input capacitance charge time. Once in the fully on state, the GHx output switches from current to voltage drive to hold the MOSFET in the on state.

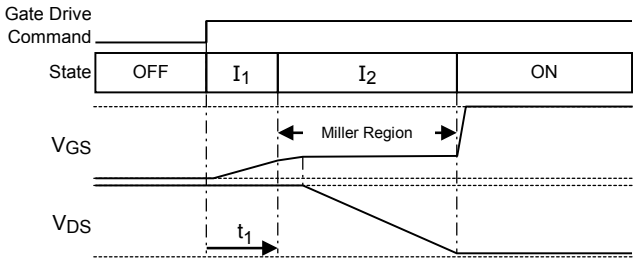

Figure 7a: Off-to-On Transition (Gate Drive)

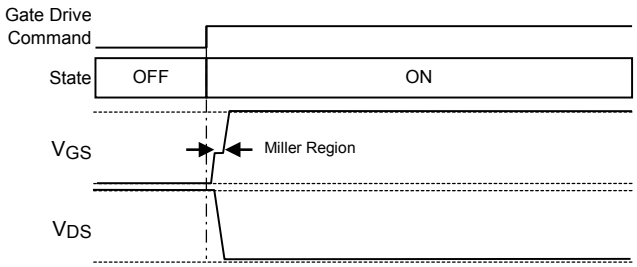

Figure 7b: Off-to-On Transition (Switched)

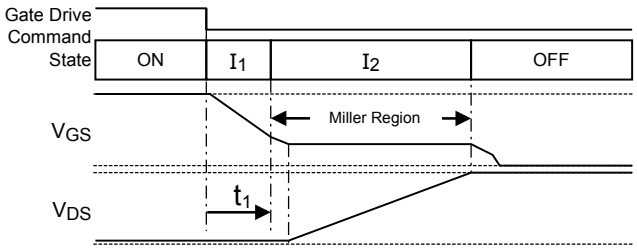

Figure 7c: On-to-Off Transition (Gate Drive)

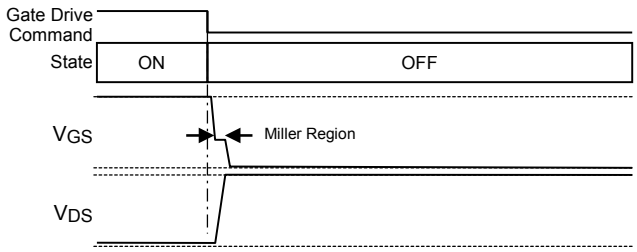

Figure 7d: On-to-Off Transition (Switched)

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If the values of IHR1[3:0] and IHR2[3:0] are set to 0000_2, GHx produces maximum drive to turn on the MOSFET as quickly as possible without attempting to control the input capacitance charge time (Figure 7b). The value of THR[3:0] has no effect on switching speed.

Low-side off-to-on transitions are controlled in a similar manner by setting TLR[3:0], ILR1[3:0] and ILR2[3:0] to control GLx and fully off determined as $V_{DS} = V_{Sx} - V_{LSSx} < V_{DSTL}$.

High-side on-to-off transitions are controlled as detailed in Figure 7c. When a gate drive is commanded to turn off a current, I_1 (as defined by IHF1[3:0]) is sunk by the relevant GHx pin for a duration, t_1 (defined by THF[3:0]). These parameters should typically be set to quickly discharge the MOSFET input capacitance to the start of the Miller region as drain-source voltage does not change during this period. Thereafter, the current sunk by GHx is set to a value of I_2 (as defined by IHF2[3:0]) and remains at this value while the MOSFET transitions through the Miller region and reaches the fully off state (fully off determined as $V_{DS} = V_{Sx} - V_{LSSx} < V_{DSTL}$). I_2 should be set to achieve the required input capacitance discharge time. Once in the fully off condition, the GHx output switches from current to voltage drive to hold the MOSFET in the off state.

If the values of IHF1[3:0] and IHF2[3:0] are set to 0000_2, GLx produces maximum drive to turn off the MOSFET as quickly as possible without attempting to control the input capacitance discharge time (Figure 7d). The value of THF[3:0] has no effect on switching speed.

Low-side on-to-off transitions are controlled in a similar manner by setting TLF[3:0], ILF1[3:0] and ILF2[3:0] to control GLx and fully off determined as $V_{DS} = V_{BRG} - V_{Sx} < V_{DSTH}$).

Dead time, DT[5:0] in the Config 0 register, must be set to a non-zero value for gate drive control to be operational. Otherwise, maximum drive will be produced on all switching transitions to minimize MOSFET switching times.

Dead time commences at the start of gate drive turn off. If using gate drive control (non-zero values of I1 and I2), the value of dead time set by DT[5:0] must be large enough to ensure any MOSFET turning off fully transitions to the off state before the complementary MOSFET in the same phase is allowed to start turning on.

Logic Control Inputs

Six logic level digital inputs, HA, LA, HB, LB, HC, and LC, provide direct control for the gate drives, one for each drive. The Hx inputs correspond to the high-side drives and the Lx inputs correspond to the low-side drives. These TTL threshold logic inputs can be driven from 3.3 or 5 V logic and all have a typical hysteresis of 550 mV to improve noise performance. Each input can be shorted to the VBB supply, up to the absolute maximum supply voltage, without damage to the input. All inputs are active-high and have a pull-down resistor to ensure a safe state if the control becomes disconnected.

The gate drive outputs can also be controlled through the serial interface by setting the appropriate bit in the Control register. In the Control register, all bits are active-high. The logical relationship between the register bit setting and the gate drive outputs is defined in Table 2.

The logic inputs are combined, using logical OR, with the corresponding bits in the serial interface control register to determine the state of the gate drive. The logical relationship between the combination of logic input and register bit setting and the gate drive outputs is defined in Table 3. In most applications, either the logic inputs or the serial control will be used. When using only the logic inputs to control the bridge, the serial register should be left in the reset condition with all control bits set to 0. When using only the serial interface to control the bridge, the logic inputs should be connected to GND. The internal pull-down resistors on these inputs ensure that they go to the inactive state should they become disconnected from the control signal level.

Internal lockout logic ensures that the high-side gate drive and low-side gate drive outputs on a given phase cannot be active (high) simultaneously. If the control inputs request both the high-side and low side gate drives to be active at the same time, then both the high-side and low-side gate drives are switched into the inactive (low) state.

Logic Outputs

A current of up to approximately 10 mA can be drawn out of each of the SxL and SDO outputs. Any one of the SxL and SDO outputs can be shorted to ground without interfering with signal integrity on the others.

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Output Enable / Disable

The ENABLE input is connected directly to the gate drive output command signal, bypassing the main synchronous logic block on the chip (including all phase control logic). This input can be used to provide a fast output disable (emergency cutoff) or to provide nonsynchronous fast decay PWM.

ENABLE can also monitored by a watchdog timer by setting the EWD bit to 1. In this mode, the signal is routed through the synchronous logic block on the chip before connecting to the gate drive output command signal. The first change of state on the ENABLE input will activate the gate drive outputs under command from the corresponding phase control signals and a watchdog timer is started. The ENABLE input must then change state before the end of the ENABLE timeout period, t_{ETO}. If the ENABLE input does not change before the end of the timeout period, then all gate drive outputs will be driven low, the ETO bit will be set in the Status register, and the general fault flag will be active. Any following change of state on the ENABLE input will reactivate the gate drive outputs and reset the general fault flag. The ETO bit remains in the Status register until reset.

Sleep Mode

RESETn is an active-low input that commands the A4911 to enter sleep mode, in which the part is inactive and current consumption from the VBB supply is reduced to a low level as defined by the I_{BBS} quiescent current limit. The gate drive outputs are disabled and quiescent current consumption begins to decay toward I_{BBS} within a Reset Shutdown Time, t_{RSD}, of RESETn going low.

When RESETn is taken high to wake from sleep mode, any fault states existing before sleep was initiated are cleared, and the device EEPROM is read to set all serial registers to their default power-on reset values. This takes approximatley 1200 µs, after which the part may be considered operational: the SPI interface may be read/written, the state of the General Fault Flag on the DIAG pin may considered valid, and the the gate drive outputs are enabled (assuming V_{REG} has exceeded its undervoltage threshold,V_{RON}). Transient system conditions present during the wakeup process may infuence the state of the General Fault Flag and the bit values reported in the Diagnostic and Status registers when first read. For example, the first time the Diagnostic and Status registers are read, the POR and FF bits will be set to indicate that the part has been in sleep. The VRU and VR bits may also be set, as the voltage on VREG rises relatively slowly and may not have exceeded V_{RON} prior to the fault detection circuitry becoming active. V_{REG} will rise to its regulation level within a Wake From Sleep period, t_{EN} (5 ms), with C_{REG} as defined in the Electrical Characteristics table (22 µF).

Pulsing RESETn low for a duration equal to the reset pulse width, t_{RST}, clears any faults, sets the general fault flag on DIAG high and re-enables any gate drives that have been disabled as a result of fault conditions (Table 6) without entering sleep mode. All device registers retain their values during and after RESETn pulses of duration t_{RST}.

To allow the A4911 to start up without the need for an external logic input, the RESETn terminal can be pulled to VBB with an external pull-up resistor.

Current Sense Amplifiers

Three programmable-gain/programmable-offset differential sense amplifiers are provided to allow the use of a low value sense resistor or current shunt as a current sensing element in the low-side connection of each phase. The input common-mode range of the CSxP and CSxM inputs allows below ground current sensing typically required for low-side current sense in PWM control of motors, or other inductive loads, during switching transients. The output of the sense amplifier is available at the CSxO outputs and can be used in peak or average current control systems. The output can drive up to 4.8 V to permit maximum dynamic range with higher input voltage A-to-D converters. Maximum output voltage is clamped to V_{CSC} as defined in the Electrical Characteristics table.

The gain of the sense amplifiers, A_V, is defined by the contents of the SAG[2:0] variable as:

SAG	Gain
0	10
1	15
2	20
3	25

SAG	Gain
4	30
5	35
6	40
7	50

The output offset of the sense amplifiers, V_{OOS}, is defined by the contents of the SAO[3:0] variable as:

SAO	V_{OS}
0	0
1	0
2	100 mV
3	100 mV
4	200 mV
5	300 mV
6	400 mV
7	500 mV

SAO	V_{OS}
8	750 mV
9	1 V
10	1.25 V
11	1.5 V
12	1.75 V
13	2 V
14	2.25 V
15	2.5 V

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Equations describing the relationship between sense amplifier gain and output offset are shown in Figure 1. Current sense amplifier calibration minimizes Input Offset Voltage, V_{IOS}, and is initiated via the SPI interface. Unless calibrated, input offset voltage may exceed the limits detailed in the Electrical Characteristics table. Calibration is not required to achieve the specified Input Offset Voltage Drift, ΔV_{IOS}, and leaves this parameter unaltered.

Amplifiers are calibrated by writing a 1 to the appropriate SxC bit in the Configuration 3 register. If an SxC bit is already set to 1, it must first be cleared to 0 before writing 1, otherwise a calibration cycle will not take place. Before initiating a calibration, the relevant positive and negative amplifier input pins (CSxP and CSxM) must be held at the same potential by ensuring that no current is flowing in the associated sense resistor, and this condition must be maintained until the calibration operation is complete. Calibration starts on the STRn rising edge associated with writing 1 to the SxC bit and is completed within an Offset Calibration Time, t_{Cal}, from this point. After a calibration, the amplifier automatically reverts to normal operating mode. More than one amplifier may be calibrated simultanously by setting multiple SxC bits on a given serial interface write cycle. The calibration of one amplifier should not be initiated if the calibration of any other is in progress, as the accuracy of both operations may be reduced. During calibration, transient voltage variations may be observed on the CSxO pins

Diagnostic Monitors

Multiple diagnostic features provide three levels of fault monitoring. These include critical protection for the A4911, monitors for operational voltages and states, and detection of power bridge and load fault conditions. All diagnostics, except for POR, serial transfer error and overtemperature can be masked by setting the appropriate bit in the mask registers.

Except for the three phase state outputs, the fault status is available from two sources, (i) the DIAG output terminal and (ii) the diagnostic and status registers accessed through the serial interface.

Table 5: Diagnostic Functions

Name	Diagnostic	Level
POR	Internal logic supply undervoltage causing power-on reset	Chip
OT	Chip junction over temperature	Chip
SE	Serial transmission error	Chip
EE	EEPROM error	Chip
TW	High chip junction temperature warning	Monitor
VSO	VBB supply overvoltage (Load dump detection)	Monitor
VSU	VBB supply undervoltage	Monitor
VLO	Logic terminal overvoltage	Monitor
ETO	Enable watchdog timeout	Monitor
VRO	VREG output overvoltage	Monitor
VRU	VREG output undervoltage	Monitor
AHU	A high-side VGS undervoltage	Monitor
ALU	A low-side VGS undervoltage	Monitor
BHU	B high-side VGS undervoltage	Monitor
BLU	B Low-side VGS undervoltage	Monitor
CHU	C high-side VGS undervoltage	Monitor
CLU	C Low-side VGS undervoltage	Monitor
OC1	Overcurrent on sense amp 1	Bridge
OC2	Overcurrent on sense amp 2	Bridge
OC3	Overcurrent on sense amp 3	Bridge
OL	Open Load	Bridge
VA	Bootstrap undervoltage phase A	Bridge
VB	Bootstrap undervoltage phase B	Bridge
VC	Bootstrap undervoltage phase C	Bridge
AHO	Phase A high-side VDS overvoltage	Bridge
ALO	Phase A low-side VDS overvoltage	Bridge
BHO	Phase B high-side VDS overvoltage	Bridge
BLO	Phase B low-side VDS overvoltage	Bridge
CHO	Phase C high-side VDS overvoltage	Bridge
CLO	Phase C low-side VDS overvoltage	Bridge

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DIAG Diagnostic Output

The DIAG terminal is a single diagnostic output signal that can be programmed by setting the contents of the DG[1:0] variable through the serial interface to provide one of four dedicated diagnostic signals:

DG = 0 – a general fault flag

DG = 1 – a pulsed fault flag

DG = 2 – a voltage representing the temperature of the internal silicon

DG = 3 – a clock signal derived from the internal chip clock

At power-up, or after a power-on-reset, the DIAG terminal outputs a general logic-level fault flag which will be active-low if a fault is present. This fault flag remains low while the fault is present or if one of the latched faults has been detected and the outputs disabled. When the general fault flag is reset, the DIAG output will be high.

The pulsed fault output option provides a continuous, low-frequency, low-duty cycle pulsed output when a fault is present or if one of the latched faults has been detected and the outputs disabled. When the general fault flag is reset and no fault is present, the signal output on the DIAG terminal is continuous low-frequency, high-duty cycle pulses. The period of the DIAG signal in pulsed mode is defined by t_{FP} and is typically 100 ms. The two duty cycles are defined by D_{FP} and are typically 20% when a fault is present and 80% when no fault is present.

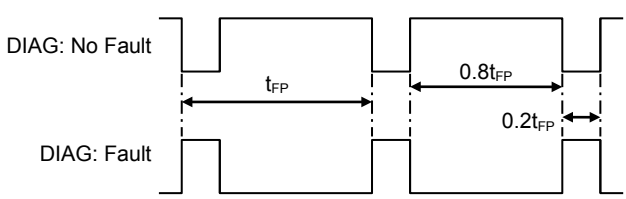

Figure 8: DIAG – Pulsed Output Mode

The temperature output option provides access to the internal voltage representing the surface temperature of the silicon. Temperature may be approximated from this voltage as

$$T_J \approx (V_{DIAG} - V_{TJD}) / A_{TJD}$$

where T_J is the approximate silicon temperature in ºC, V_{DIAG} is the analog voltage on the DIAG pin in mV, and V_{TJD} and A_{TJD} are the typical range and slope values presented in the Electrical Characteristics table.

The clock output option provides a logic-level square wave output at a ratio of the internal clock frequency to allow more precise calibration of the timing settings if required.

All digital outputs available on the DIAG pin (DG set to 0, 1, or 3) are open drain. On-state drive capability and off-state leakage current limits are defined in the Electrical Characteristics table by the V_{OL} and I_{ODI} parameters respectively and may be used to calculate a suitable pull-up resistance. In the majority of applications, a resistor in the range 10 to 20 kΩ is acceptable.

Diagnostic Registers

The serial interface allows detailed diagnostic information to be read from the diagnostic registers on the SDO output terminal at any time.

A system Status register provides a summary of all faults in a single read transaction. The Status register is always output on SDO when any register is written.

The first bit (bit 15) of the Status register contains a common fault flag, FF, which will be high if any of the fault bits in the Status register have been set. This allows fault condition to be detected using the serial interface by simply taking STRn low. As soon as STRn goes low, the first bit in the Status register can be read on SDO to determine if a fault has been detected at any time since the last fault register reset. In all cases, the fault bits in the diagnostic registers are latched and only cleared after a diagnostic register reset.

Note that FF (bit 15) does not provide the same function as the general fault flag output on the DIAG terminal when STRn is high and the DIAG output is in its default mode. The fault output on the DIAG terminal provides an indication that either a fault is present or the outputs have been disabled due to a latched fault state. FF provides an indication that a fault has occurred since the last fault reset and one or more fault bits have been set.

Chip-Level Protection

Chip-wide parameters critical for correct operation of the A4911 are monitored. These include maximum chip temperature, minimum internal logic supply voltage, and the serial interface transmission. These three monitors are necessary to ensure that the A4911 is able to respond as specified.

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Chip Fault State: Internal Logic Undervoltage

The A4911 has an independent integrated logic regulator to supply the internal logic. This is to ensure that external events, other than loss of supply, do not prevent the A4911 from operating correctly. The internal logic supply regulator will continue to operate with a low supply voltage, for example if the main supply voltage drops to a very low value during a severe cold crank event. In extreme low supply voltage circumstances, or during power-up or power-down, an undervoltage detector ensures that the A4911 operates correctly. The logic supply undervoltage lockout cannot be masked as it is essential to guarantee correct operation over the full supply range.

When power is first applied to the A4911, the internal logic is prevented from operating, and all gate drive outputs are held in the off-state until the internal regulator voltage, V_{DD}, exceeds the logic supply undervoltage lockout rising (turn-on) threshold. This threshold is derived from the sum of the VBB POR threshold, V_{BBR}, and the VBB POR Hysteresis, V_{BBRHys}. At this point, all serial control registers will be reset to their power-on state and all fault states and the general fault flag will be reset. The FF bit and the POR bit in the Status register will be set to 1 to indicate that a power-on-reset has taken place. The A4911 then goes into its fully operational state and begins operating as specified.

Once the A4911 is operational, the internal logic supply continues to be monitored. If, during the operational state, V_{DD} drops below logic supply undervoltage lockout falling (turn-off) threshold, derived from V_{BBR}, then the logical function of the A4911 cannot be guaranteed and the outputs will be immediately disabled. The A4911 will enter a power-down state and all internal activity, other than the logic regulator voltage monitor, will be suspended. If the logic supply undervoltage is a transient event, then the A4911 will follow the power-up sequence above as the voltage rises.

Chip Fault State: Overtemperature

If the chip temperature rises above the over temperature threshold, T_{JF}, the general fault flag will be active and the overtemperature bit, OT, will be set in the Status register. If ESF = 1 when an overtemperature is detected, all gate drive outputs will be disabled automatically. If ESF = 0, then no circuitry will be disabled and action must be taken by the user to limit the power dissipation in some way so as to prevent overtemperature damage to the chip and unpredictable device operation. When the temperature drops below T_{JF} by more than the hysteresis value, T_{JFHys}, the general fault flag will be reset, but the overtemperature bit remains in the Status register until reset.

Chip Fault State: Serial Error

If there are more than 16 rising edges on SCK, or if STRn goes high and there are fewer than 16 rising edges on SCK, or the parity is not odd, then the write will be cancelled without writing data to the registers. In addition, the Status register will not be reset and the SE bit will be set to indicate a data transfer error. If the transfer is a write, then the Status register will not be reset. If the transfer is a diagnostic or verification result read, then the addressed register will not be reset.

Chip Fault State: EEPROM

Configuration and calibration information is stored within internal EEPROM and loaded into working registers to configure the device at power up. As part of this process, a data integrity check is carried out. If the check returns a single bit error, automatic error correction is applied and the part starts up. If the check returns a multiple bit error, all gate drives are disabled, the general fault flag is set low, and the EEPROM error bit, EE, is set in the Status register. EEPROM faults can only be cleared by a power-on-reset (POR).

Operational Monitors

Parameters related to the safe operation of the A4911 in a system are monitored. These include parameters associated with external active and passive components, power supplies, and interaction with external controllers.

Voltages relating to driving the external power MOSFETs are monitored, specifically V_{REG}, each bootstrap capacitor voltage, and the V_{GS} of each gate drive output. The main supply voltage, V_{BB}, is monitored for overvoltage and undervoltage events.

The logic inputs are capable of being shorted to the main supply voltage without damage, but any high voltage on these pins will be detected. In addition, a watchdog timer can be applied to the ENABLE input to verify continued operation of the external controller.

Monitor: VREG Undervoltage and Overvoltage

The internal charge-pump regulator supplies the low-side gate driver and the bootstrap charge current. It is critical to ensure that the regulated voltage, V_{REG}, at the VREG terminal is sufficiently

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high before enabling any of the outputs.

If V_{REG} goes below the VREG undervoltage threshold, V_{ROFF}, the general fault flag will be active and the VREG undervoltage bit, VRU, will be set in the Diagnostic 1 register. All gate drive outputs will go low, the motor drive will be disabled, and the motor will coast. When V_{REG} rises above the rising threshold, V_{RON}, the gate drive outputs are re-enabled and the general fault flag is cleared. The fault bit remains in the Diagnostic 1 register until cleared.

The VREG undervoltage monitor circuit is active during power-up. The general fault flag will be active and all gate drives will be low until V_{REG} is greater than V_{RON}. Note that this is sufficient to turn on standard threshold external power MOSFETs at a battery voltage as low as 5.5 V, but the on-resistance of the MOSFET may be higher than its specified maximum.

The VREG undervoltage monitor can be disabled by setting the VRU bit in the Mask 1 register. Although not recommended, this can allow the A4911 to operate below its minimum specified supply voltage level with a severely impaired gate drive. The specified electrical parameters will not be valid in this condition.

The output of the VREG regulator is also monitored to detect any overvoltage applied to the VREG terminal.

If V_{REG} goes above the VREG overvoltage threshold, V_{ROV}, the general fault flag will be active and the VREG overvoltage bit, VRO, will be set in the Diagnostic 1 register. No action will be taken, as the gate drive outputs are protected from overvoltage by independent Zener clamps. When V_{REG} falls below V_{ROV} by more than the hysteresis voltage, V_{ROVHys}, the general fault flags are cleared, but the VRO bit remains in the Diagnostic 1 register until cleared.

Monitor: Temperature Warning

If the chip temperature rises above the temperature warning threshold, T_{JW}, the general fault flag will be active and the hot warning bit, TW, will be set in the Status register. No action will be taken by the A4911. When the temperature drops below T_{JW} by more than the hysteresis value, T_{JWHys}, the general fault flag is reset but the TW bit remains in the Status register until reset.

Monitor: VBB Supply Overvoltage and Undervoltage

The main supply to the A4911 on the VBB terminal, V_{BB}, is monitored to indicate if the supply voltage has exceeded its normal operating range (for example, during a load dump event). If V_{BB} rises above the VBB overvoltage warning threshold, V_{BBOV}, then the VSO bit will be set in the Diagnostic 2 register and the VS bit (which indicates the logical OR of the VSO and VSU bits) will be set in the Status register. The general fault flag will be set but all gate drive outputs will continue to function. When V_{BB} drops below the falling VBB overvoltage warning threshold, $V_{BBOV} - V_{BBOVHys}$, the general fault flag will be cleared but the VSO and VS bits will remain set until the Diagnostic 2 register is read.

If V_{BB} falls below the VBB undervoltage warning threshold, V_{BBUV}, then the VSU bit will be set in the Diagnostic 2 register and the VS bit (which indicates the logical OR of the VSO and VSU bits) will be set in the Status register. The general fault flag will be set and all gate drive outputs will be driven low, causing the motor to coast. When V_{BB} moves above the rising VBB undervoltage threshold, $V_{BBUV} + V_{BBUVHys}$, the gate drive outputs will be re-enabled, and the general fault flag will be cleared, but the VSU and VS bits will remain set until the Diagnostic 2 register is read.

Monitor: VGS Undervoltage

To ensure that the gate drive output is operating correctly, each gate drive output voltage is independently monitored, when active, to ensure the drive voltage, V_{GS}, is sufficient to fully enhance the power MOSFET in the external bridge.

If V_{GS}, on any active gate drive output, is lower than the gate drive undervoltage warning threshold, V_{GSUV}, the corresponding VGS undervoltage comparator detects a fault. On high-side comparators, the V_{GSUV} thresholds are set 1 V(typ) below the voltage on the corresponding CX pin, and on low-side gate drives, 1 V(typ) below V_{REG}.

The output from each VGS undervoltage comparator is filtered by a VGS fault qualifier circuit. This circuit uses a timer to verify that the output from the comparator is indicating a valid VGS fault. The duration of the VGS fault qualifying timer, t_{VDQ}, is determined by the contents of the TVD[5:0] variable. t_{VDQ} is approximately defined as:

$$t_{VDQ} = n \times 100 \text{ ns}$$

where n is a positive integer defined by TVD[5:0].

The qualifier can operate in one of two ways: debounce mode or blanking mode, selected by the VDQ bit.

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In debounce mode (the default setting), a timer is started each time the comparator output indicates a VGS fault detection when the corresponding MOSFET is active. This timer is reset when the comparator changes back to indicate V_{GS} is within 1 V of the voltage on the CX pin (high-side gate drives) or V_{REG} (low-side gate drives). If the debounce timer reaches the end of the timeout period, set by t_{VDQ}, then the VGS fault is considered valid. The general fault flag on the DIAG pin goes low and the appropriate VGS fault bit, AHU, ALU, BHU, BLU, CHU, or CLU, is set in the Diagnostic 0 register, but the gate drive outputs are not disabled.

In blanking mode (optional), a timer is started when any gate drive is turned on or turned off. The outputs from the VGS undervoltage comparators for all MOSFETs are ignored (blanked) for the duration of the timer's active period, set by t_{VDQ}. If any gate drive changes state while a blanking period is in progress, the timer is re-triggered, resulting in an extended overall blanking time. If any comparator output indicates a VGS fault and the blanking timer is not active, then the VGS fault is considered valid. The general fault flag on the DIAG pin goes low and the appropriate VGS fault bit, AHU, ALU, BHU, BLU, CHU, or CLU, is set in the Diagnostic 0 register, but the gate drive outputs are not disabled.

The VDQ and TVD[5:0] qualifier parameters set in the Config 2 register apply to both the VGS undervoltage and VDS overvoltage monitors.

Monitor: Logic Terminal Overvoltage

Nine of the logic terminals are capable of being shorted to the main supply voltage, up to 50 V, without damage. These terminals are HA, LA, HB, LB, HC, LC, RESETn, ENABLE, and DIAG. The voltage on these pins, V_L, is monitored to provide an indication of a terminal short-to-battery fault. If V_L on any of the terminals rises above the logic terminal overvoltage warning threshold, V_{LOV}, then the VLO bit is set in the Status register. Additionally, the general fault flag is set to active (low), except in the case of a DIAG pin overvoltage where the open-drain output maintains a high-impedance (off) state. The DIAG pin is protected and the overvoltage detect function is active regardless of the signal output selected via the DG[1:0] bits in the Control register. If the fault is on one of the input terminals and the ESF bit is set, then all gate drive outputs will be disabled. When V_L on all terminals falls below the logic terminal overvoltage warning threshold, V_{LOV}, the fault flag will be reset and the outputs will be reactivated. The VLO bit remains in the Status register until reset.

Monitor: ENABLE Watchdog Timeout

The ENABLE input provides a direct connection to all gate drive outputs and can be used as a safety override to immediately disable the outputs. The ENABLE input is programmed to operate as a direct logic control by default but can be monitored by a watchdog timer by setting the EWD bit to 1. In the direct mode, the input is not monitored other than for input overvoltage, as described in the Logic Terminal Overvoltage section above. In watchdog mode, the first change of state on the ENABLE input will activate the gate drive outputs under command from the corresponding phase control signals and a watchdog timer is started. The ENABLE input must then change state before the end of the ENABLE timeout period, t_{ETO}. If the ENABLE input does not change before the end of the timeout period, then all gate drive outputs will be driven low, the ETO bit will be set in the Status register, and the general fault flag will be active. Any following change of state on the ENABLE input will reactivate the gate drive outputs and reset the general fault flag. The ETO bit remains in the Status register until reset.

Power Bridge and Load Faults

Bridge: Overcurrent Detect

Current sense amplifiers 1, 2, and 3 are fully independent and may be allocated to any phase (A, B, or C).

The output from each of the three sense amplifiers is fed into a comparator referenced to the overcurrent threshold voltage, V_{OCT}, to provide indication of overcurrent events. V_{OCT} is generated by a 4-bit DAC with a resolution of 300 mV and defined by the contents of the OCT[3:0] variable. V_{OCT} is approximately defined as:

$$V_{OCT} = (n + 1) \times 300 \text{ mV}$$

where n is a positive integer defined by OCT[3:0].

Any offset programmed on SAO[3:0] is applied to both the current sense amplifier output and the V_{OCT} threshold and has no effect on the overcurrent threshold, I_{OCT}. In effect, V_{CSD} is compared with V_{OCT} and the relationship between the threshold voltage and threshold current is given by:

$$I_{OCT} = V_{OCT} / (R_S \times A_V)$$

where V_{OCT} is the overcurrent threshold voltage programmed by OCT[3:0], I_{OCT} is the corresponding current value, R_S is the sense resistor value in Ω, and A_V is the sense amp gain defined by SAG[2:0].

The output from each overcurrent comparator is filtered by an

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overcurrent qualifier circuit. This circuit uses a timer to verify that the output from comparator is indicating a valid overcurrent event. The qualifier can operate in one of two ways: debounce or blanking, selected by the OCQ bit.

In the default debounce mode, a timer is started each time a comparator output indicates an overcurrent detection. This timer is reset when the comparator changes back to indicate normal operation. If the debounce timer reaches the end of the timeout period, set by t_{OCQ}, then the overcurrent event is considered valid and the corresponding overcurrent bit (OC1, OC2, or OC3) will be set in the Diagnostic 2 register.

In the optional blanking mode, a timer is started when any gate drive is turned on. The output from all comparators is ignored (blanked) for the duration of the timeout period, set by t_{OCQ}. If a comparator output indicates an overcurrent event when the blanking timer is not active, then the overcurrent event is considered valid and the corresponding overcurrent bit (OC1, OC2, or OC3) will be set in the Diagnostic 2 register. If a gate drive is turned on while a timeout period is in progress, the timeout is extended to run for a period of t_{OCQ} from the new turn-on event. If all gate drives are turned off during a timeout period, the timeout period is terminated.

The duration of the overcurrent qualifying timer, t_{OCQ}, is determined by the contents of the TOC[3:0] variable. t_{OCQ} is approximately defined as:

$$t_{OCQ} = n \times 500 \text{ ns}$$

where n is a positive integer defined by TOC[3:0].

When a valid overcurrent is detected, the general fault flag is not affected. Only the OC1, OC2, or OC3 bit is set and remains in the Diagnostic 2 register until reset.

Bridge: Open-Load Detect

Two open-load fault detection methods are provided, an on-state current monitor and an off-state open-load detector. An on-state is defined by the state of the gate drive outputs as one or two high-side MOSFETs switched on and one or two low-side MOSFETs switched on. The resulting combinations are the only ones where current can be passed through the low-side sense resistor. An off-state is defined by the state of the gate drive outputs as all MOSFETs switched off. In this state, the load connections are high impedance and can be used to detect the presence of a load.

On-State Open-Load detection

On-state open-load detection is only active when AOL = 1 and one or two high-side MOSFETs are switched on and one or two low-side MOSFETs are switched on. This excludes the cases where a high-side MOSFET and a low-side MOSFET in the same phase are commanded to be on at the same time. Table 4 shows the open-load detection mode for each combination of output demand.

During the on-state, the A4911 compares the output from each sense amplifier against the open-load threshold voltage, V_{OLTH}. V_{OLTH} is generated by an internal DAC and is defined by the value in the OLT[3:0] variable. These bits provide the input to a 4-bit DAC with a least significant bit value of typically 25 mV. The output of the DAC produces V_{OLTH} approximately defined as:

$$V_{OLTH} = (n + 1) \times 25 \text{ mV}$$

where n is a positive integer defined by OLT[3:0].

Any offset programmed on SAO[3:0] is applied to both the current sense amplifier output and the V_{OLTH} threshold and has no effect on the open-load detect threshold current, I_{OLT}. V_{CSD} is compared with V_{OLTH} and the relationship between the threshold voltage and threshold current is given by:

$$I_{OLT} = V_{OLTH} / (R_S \times A_V)$$

where V_{OLTH} is the open load threshold voltage programmed by OLT[3:0], I_{OLT} is the corresponding current value, R_S is the sense resistor value in **Ω**, and A_V is the sense amp gain defined by SAG[2:0].

If the output of all sense amplifiers is less than V_{OLTH} during the on-state, then a timer is allowed to increment. If the output of any amplifier is higher than V_{OLTH} during the on-state, then the timer is reset. If the timer reaches the open-load timeout value, t_{OLTO}, typically 100 ms, then the general fault flag will be active and the open-load fault bit, OL, will be set in the Diagnostic 2 register indicating a valid open-load condition.

As soon as the output of any amplifier is higher than V_{OLTH} during the on-state, then the general fault flag will be reset but the open-load fault bit remains in the Diagnostic 2 register until reset.

If the sense amplifier is not used in an application, then the on-state open-load detection can be completely disabled by setting AOL to 0.

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Off-State Open-Load Detection

Off-state open-load detection is only active when DOO = 0 and all gate drive outputs are off. In the off-state, a current sink of magnitude I_{OLTS} is applied to the SB terminal and current sources of magnitude I_{OLTT} are applied to the SA and SC terminals.

I_{OLTS} is typically 10 mA, which is low enough to allow the A4911 to survive a short-to-VBB on the SB terminal during the off-state without damage, and high enough to discharge any output capacitance in an acceptable time.

The value of I_{OLTT} is selected by the OLI bit. When OLI = 0, I_{OLTT} = –70 µA; when OLI = 1, I_{OLTT} = –400 µA.

The sink current, I_{OLTS}, pulls the SB terminal to ground once any energy remaining in the load, when entering the off-state, has dissipated. The source current, I_{OLTT}, applies a test current to the load. As the sink current is much larger than the source current, the current through the load will be the source current. The voltage at the SB terminal, V_{SB}, should be close to zero, and the voltages at the SA and SC terminals, V_{SA} and V_{SC}, will allow the load resistance to be measured. V_{SA} and V_{SC} are compared to a fixed threshold, V_{OLTT}, of typically 1.5 V. If V_{SA} and V_{SC} are both less than V_{OLTT}, then a load is assumed to be present. If either V_{SA} or V_{SC} is greater than V_{OLTT}, then a timer is started. If the timer reaches the open-load timeout value, t_{OLTO}, typically 100 ms, then the general fault flag will be active and the open-load fault bit, OL, will be set in the Diagnostic 2 register indicating a valid open load condition.

When OLI = 0, the threshold for load resistance is 21 kΩ; when OLI = 1, the threshold is 3.8 kΩ—consequently any load resistance greater than 21 kΩ or 3.8 kΩ respectively is indicated as an open load.

If both V_{SA} and V_{SC} become less than V_{OLTT}, or the bridge exits the off-state at any time before the timeout is complete, then the timer is reset without indicating an open load.

If both V_{SA} and V_{SC} become less than V_{OLTT}, or the bridge exits the off-state after the open-load fault condition has been detected, then the general fault flag will be reset, but the OL bit remains in the Diagnostic 2 register until reset.

If DOO = 1 off-state open-load detection is completely disabled.

Motor Winding Considerations

If driving a star-connected motor, the on-state and off-state methods described above allow the detection of open-load faults in the bridge-to-motor interconnects and within the motor itself. If driving a delta-connected motor, only faults in the bridge-to-motor interconnects may be detected, as motor inter-terminal impedance will remain relatively low in the event of an internal motor single point failure (this type of motor having two internal current paths between each terminal).

Bridge: Bootstrap Capacitor Undervoltage Fault

The A4911 monitors the individual bootstrap capacitor charge voltages to ensure sufficient high-side drive. It also includes an optional bootstrap capacitor charge management system (bootstrap manager) to ensure that the bootstrap capacitor remains sufficiently charged under all conditions. The bootstrap manager is active by default, but may be disabled by setting the DBM bit to 1. This may be required in systems where the output MOSFET switching must only be allowed by the controlling processor.

If the bootstrap manager is disabled, then the user must ensure that the bootstrap capacitor does not become discharged below the bootstrap undervoltage threshold, V_{BCUV}, or a bootstrap fault will be indicated and the outputs disabled. This can happen with very high PWM duty cycles when the charge time for the bootstrap capacitor is insufficient to ensure a sufficient recharge to match the MOSFET gate charge transfer during turn on.

When the bootstrap manager is active, the bootstrap capacitor voltage must be higher than the turn-on voltage limit before a high-side drive can be turned on. If this is not the case, then the A4911 will attempt to charge the bootstrap capacitor by activating the complementary low-side drive. Under normal circumstances this will charge the capacitor above the turn-on voltage in a few microseconds and the high-side drive will then be enabled. The bootstrap voltage monitor remains active while the high-side drive is active, and if the voltage drops below the turn-off voltage, a charge cycle is also initiated.

If there is a fault that prevents the bootstrap capacitor charging during the managed recharge cycle, then the charge cycle will timeout after typically 200 µs and the bootstrap undervoltage fault is considered to be valid. If the bootstrap manager is disabled and a bootstrap undervoltage is detected when a high-side MOSFET is active or being switched on, then the bootstrap undervoltage is immediately valid.

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The action taken when a valid bootstrap undervoltage fault is detected, and the fault reset conditions, depend on the state of the ESF bit.

If ESF = 0, the fault state will be latched, the general fault flag will be active, the associated bootstrap undervoltage fault bit (VA, VB, VC) will be set in the Diagnostic 2 register, and the associated MOSFET will be disabled. The fault state and the general fault flag, but not the bootstrap undervoltage fault bit, will be reset the next time the MOSFET is commanded to switch on. If the MOSFET is being driven with a PWM signal, then this will usually mean that the MOSFET will be turned on again each PWM cycle. If this is the case, and the fault condition remains, then a valid fault will again be detected after the timeout period and the sequence will repeat. The general fault flag will only be reset for the duration of the validation timer. The bootstrap undervoltage fault bit will only be reset by a serial read of the Diagnostic 2 register or by a power-on reset.

If ESF = 1 the fault will be latched, the general fault flag will be active, the associated bootstrap undervoltage fault bit (VA, VB, VC) will be set in the Diagnostic 2 register, and all MOSFETs will be disabled. The fault state and the general fault flag will be reset by a low pulse on the RESETn input, by a serial read of the Diagnostic 2 register, or by a power-on reset. The bootstrap undervoltage fault bit will only be reset by a serial read of the Diagnostic 2 register or by a power-on reset.

The bootstrap undervoltage monitor can be disabled for all phases by setting the BSU bit in the Mask 2 register. Although not recommended, this can allow the A4911 to operate below its minimum specified supply voltage level with a severely impaired gate drive. The specified electrical parameters may not be valid in this condition.

Bridge: MOSFET VDS Overvoltage Fault

Faults on any external MOSFETs are determined by monitoring the drain-source voltage of the MOSFET and comparing it to a drain-source overvoltage threshold. There are two thresholds: V_{DSTH} for the high-side MOSFETs, and V_{DSTL} for the low-side. V_{DSTH} and V_{DSTL} are generated by internal DACs and are defined by the values in the VTH[5:0] and VTL[5:0] variables respectively. These variables provide the input to two 6-bit DACs with a least significant bit value of typically 50 mV. The output of the DAC produces the threshold voltage approximately defined as:

$$V_{DSTH} = n \times 50 \text{ mV}$$

where n is a positive integer defined by VTH[5:0], or

$$V_{DSTL} = n \times 50 \text{ mV}$$

where n is a positive integer defined by VTL[5:0].

The low-side drain-source voltage for any MOSFET is measured between the adjacent Sx terminal and the adjacent LSSx terminal. Using the LSSx terminal rather than the ground connection avoids adding any low-side current sense voltage to the real low-side drain-source voltage and avoids false VDS fault detection.

The high-side drain-source voltage for any MOSFET is measured between the adjacent Sx terminal and the VBRG terminal. Using the VBRG terminal rather than the VBB avoids adding any reverse diode voltage or high-side current sense voltage to the real high-side drain-source voltage and avoids false VDS fault detection.

The VBRG terminal is an independent low-current sense input to the top of the MOSFET bridge. It should be connected independently and directly to the common connection point for the drains of the power bridge MOSFETs at the positive supply connection point in the bridge. The input current to the VBRG terminal is proportional to the drain-source threshold voltage, V_{DSTH}, and is approximately:

$$I_{VBRG} = 72 \times V_{DSTH} + 52$$

where I_{VBRG} is the current into the VBRG terminal in µA, and V_{DSTH} is the drain-source threshold voltage described above in V.

Note that the VBRG terminal can withstand a negative voltage up to –5 V. This allows the terminal to remain connected directly to the top of the power bridge during negative transients where the body diodes of the power MOSFETs are used to clamp the negative transient. The same applies to the more extreme case where the MOSFET body diodes are used to clamp a reverse battery connection.

The output from each VDS overvoltage comparator is filtered by a VDS fault qualifier circuit. This circuit uses a timer to verify that the output from the comparator is indicating a valid VDS fault. The duration of the VDS fault qualifying timer, t_{VDQ}, is determined by the contents of the TVD[5:0] variable. t_{VDQ} is approximately defined as:

$$t_{VDQ} = n \times 100 \text{ ns}$$

where n is a positive integer defined by TVD[5:0].

The qualifier can operate in one of two ways: debounce mode or blanking mode, selected by the VDQ bit.

In debounce mode (the default setting), a timer is started each time the comparator output indicates a VDS fault detection when the corresponding MOSFET is active. This timer is reset when

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the comparator changes back to indicate normal operation. If the debounce timer reaches the end of the timeout period, set by t_{VDQ}, then the VDS fault is considered valid and the corresponding VDS fault bit, ALO, AHO, BLO, BHO, CLO, or CHO, will be set in the Diagnostic 1 register.

In blanking mode (optional), a timer is started when any gate drive is turned on or turned off. The outputs from the VDS overvoltage comparators for all MOSFETs are ignored (blanked) for the duration of the timer's active period, set by t_{VDQ}. If any gate drive changes state while a blanking period is in progress, the timer will be retriggered, resulting in an extended overall blanking time. If any comparator output indicates a VDS fault and the blanking timer is not active, then the VDS fault is considered valid and the corresponding VDS fault bit, ALO, AHO, BLO, BHO, CLO, or CHO, is set in the Diagnostic 1 register.

The VDQ and TVD[5:0] qualifier parameters set in the Config 2 register apply to both the VGS undervoltage and VDS overvoltage monitors.

The action taken when a valid VDS fault is detected, and the action then required to clear the fault state, depend upon the ESF bit value.

If ESF = 0 the fault state will be latched, the general fault flag will be active, the associated VDS fault bit will be set and the associated MOSFET will be disabled. The fault state and the general fault flag, but not the VDS fault bit, will be reset the next time the MOSFET is commanded to switch on. If the MOSFET is being driven with a PWM signal, then this will usually mean that the MOSFET will be turned on again each PWM cycle. If this is the case, and the fault condition remains, then a valid fault will again be detected after the timeout period and the sequence will repeat. The general fault flag will only be reset for the duration of the validation timer. The VDS fault bit will only be reset by a serial read of the Diagnostic 1 register or by a power-on reset.

If ESF = 1, the fault will be latched, the general fault flag will be active, the associated VDS fault bit will be set, and all MOSFETs will be disabled. The fault state and the general fault flag will be reset by a low pulse on the RESETn input, by a serial read of the Diagnostic 2 register, or by a power-on reset. The VDS fault bit will only be reset by a serial read of the Diagnostic 2 register or by a power-on reset.

If ESF = 0, care must be taken to avoid damage to the MOSFET where the VDS fault is detected. Although the MOSFET will be switched off as soon as the fault is detected, at the end of the fault validation timeout, it is possible that it could still be damaged by excessive power dissipation and heating. To limit any damage to the external MOSFETs or the motor, the MOSFET should be fully disabled by logic inputs from the external controller.

Fault Action

The action taken when one of the diagnostic functions indicates a fault is listed in Table 6.

When a fault is detected, a corresponding fault state is considered to exist. In some cases, the fault state only exists during the time the fault is detected. In other cases, when the fault is only detected for a short time, the fault state is latched (stored) until

Table 6: Fault Actions

Fault Description	Disable Outputs		Fault State Latched
	ESF = 0	ESF = 1	
No Fault	No	No	–
Power-On-Reset	Yes [1]	Yes [1]	No
VREG Undervoltage	Yes [1]	Yes [1]	No
Bootstrap Undervoltage	Yes [2]	Yes [1]	Yes
Logic Terminal Overvoltage	No	Yes [1][3]	No
ENABLE WD Timeout	Yes [1]	Yes [1]	No
Overtemperature	No	Yes [1]	No
VDS Fault	Yes [2]	Yes [1]	Yes
Serial Transmission Error	No	No	No
VREG Overvoltage	No	No	No
VBB Undervoltage	Yes [1]	Yes [1]	No
VBB Overvoltage	No	No	No
VGS Undervoltage	No	No	No
Temperature Warning	No	No	No
Overcurrent	No	No	No
Open Load	No	No	No
EEPROM	Yes [1]	Yes [1]	Yes

[1] All gate drives low, all MOSFETs off.
[2] Gate drive to the affected MOSFET low, only the affected MOSFET off.
[3] Outputs disabled on Hx, Lx, RESETn, ENABLE overvoltage but not on DIAG overvoltage.

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reset. The faults that are latched are indicated in Table 6. Latched fault states are always reset when RESETn is taken low, a power-on-reset state is present, or when the associated fault bit is read through the serial interface. Any fault bits that have been set in the diagnostic registers are only reset when a power-on-reset state is present or when the associated fault bit is read through the serial interface. Taking RESETn low for the Reset Pulse Width, t_{RST}, will not reset the fault bits in the Diagnostic and/or Status registers.

The fault conditions power-on-reset and VREG undervoltage are considered critical to the safe operation of the A4911 and the system. If these faults are detected, then the gate drive outputs are automatically driven low and all MOSFETs in the bridge held in the off state. This state will remain until the fault is removed.

If the ENABLE watchdog monitor is activated by setting EWD to 1, then this fault state is also considered critical to the safe operation of the A4911 and the system. If an ENABLE watchdog timeout is detected, then all gate drive outputs are driven low and all MOSFETs in the bridge are held in the off state. This state will remain until the watchdog timer is reset.

For the logic terminal overvoltage and overtemperature fault conditions, the action taken depends on the status of the ESF bit. If a fault is detected on either of these two diagnostics and ESF = 1, then all the gate drive outputs will be driven low and all MOSFETs in the bridge held in the off state. This state will remain until the fault is removed. If ESF = 0, then the gate drive outputs will not be affected.

If a VDS overvoltage or bootstrap undervoltage fault is detected, then the action taken depends on the status of the ESF bit, but these faults are handled as a special case. If a fault is detected on either of these diagnostics and ESF = 1, then all gate drive outputs are driven low and all MOSFETs in the bridge are held in the off state. When ESF = 1, this fault state is latched and remains until reset. If a VDS overvoltage or bootstrap undervoltage fault is detected and ESF = 0, then only the gate drive output to the MOSFET on which the fault was detected is driven low, and only that MOSFET is held in the off state. When ESF = 0, the VDS overvoltage or bootstrap undervoltage fault state is latched, but is reset the next time the MOSFET on which the fault was detected is commanded to switch on.

For all other faults the gate drive outputs will remain active.

Fault Masks

Individual diagnostics, except power-on reset, serial transmission error, and overtemperature, can be disabled by setting the corresponding bit in the mask registers. Power-on-reset cannot be disabled because the diagnostics and the output control depend on the logic regulator to operate correctly. If a bit is set to one in the mask registers, then the corresponding diagnostic will be completely disabled. No fault states for the disabled diagnostic will be generated and no fault flags or diagnostic bits will be set. See Mask Register definition for bit allocation.

Care must be taken when diagnostics are disabled to avoid potentially damaging conditions.

Diagnostic and System Verification

To comply with various aspects of safe system design, it is necessary for higher-level safety systems to verify that any diagnostics or functions used to guarantee safe operation are operating within specified tolerances.

Table 7: Verification Functions

Verification Type	Function Verified	Operation	
		Offline	Online
Connection	VBRG Connection		Y
Connection	Phase Connection	Y	
Connection	Sense Amp Connection		Y
Connection	LSS Connection		Y
Monitor	ENABLE Watchdog	Y	
Monitor	Overcurrent Detectors	Y	
Monitor	Phase State Monitor		Y
Diagnostic	Overtemperature Diagnostic	Y	
Diagnostic	Temperature Warning Monitor	Y	
Diagnostic	VBB Undervoltage Diagnostic	Y	
Diagnostic	VBB Overvoltage Diagnostic	Y	
Diagnostic	VREG Diagnostics	Y	
Diagnostic	VGS Undervoltage Diagnostic	Y	
Diagnostic	Logic Terminal Diagnostic	Y	
Diagnostic	Open-Load Detectors	Y	
Diagnostic	Bootstrap Capacitor Diagnostic	Y	
Diagnostic	VDS Overvoltage Diagnostic	Y	
Diagnostic	All Gate Drives Off	Y	

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There are four basic aspects to verification of diagnostic functions:

1. Verify connections.
2. Verify comparators.
3. Verify thresholds.
4. Verify fault propagation.

These must be completed for each diagnostic. In addition, the operation of system functions not directly covered by diagnostics should also be verified.

The A4911 includes additional verification functions to help the system design comply with any safety requirements. Many of these functions can only be completed when the diagnostics are not required and must be commanded to run by the main system controller. These functions are referred to as "offline" verification.

A few of the functions can be continuously active, but the results must be checked by the main system controller on a regular basis. These functions are referred to as "online" verification.

The frequency with which these offline verification functions are run, or online verifications results are checked, will depend on the safety requirements of the system using the A4911.

Online Verification

The following functions are permanently active and will set the appropriate bit in the verification result registers to indicate that the verification has failed. No other action will be taken by the A4911 unless described below. These verification functions verify that certain of the A4911 terminals are correctly connected to the power bridge circuit.

Bridge: VBRG Disconnected

The VBRG terminal provides the common-drain voltage reference for the high-side MOSFET VDS overvoltage detectors. If this becomes disconnected, then the high-side VDS detection will be invalid and VDS overvoltage faults may not be detected. If VBRG is disconnected, the internal current sink from the input will ensure that the voltage at the VBRG terminal will fall. A comparator is provided to monitor the voltage between the main supply connection at the VBB terminal and the voltage at VBRG, $V_{BB} - V_{BRG}$, is compared to the VBRG open threshold voltage, V_{BRO}, determined by the variable VTB[1:0] as:

$$V_{BRO} = (n + 1) \times 2 \text{ V}$$

where n is a positive integer defined by VTB[1:0] giving thresholds at 2 V, 4 V, 6 V, and 8 V.

If $V_{BB} - V_{BRG}$ exceeds the VBRG open threshold voltage, then the VBR bit will be set in the Verify Result 0 register, all high-side VDS fault bits will be set in the Diagnostic 1 register, the DSO and FF bits will be set in the Status register, and the general fault flag will be active. If ESF = 1, all six gate drive outputs will be disabled. If ESF = 0, no gate drive outputs will be disabled. When $V_{BB} - V_{BRG}$ falls below the falling VBRG open threshold voltage, $V_{BRO} - V_{BROHys}$, the fault flag will be reset and the outputs will be reactivated. The VBR bit remains in the verification result register until reset, and the VDS diagnostic bits remain in the Diagnostic 1 register until reset.

To ensure accurate VBRG disconnect detection at V_{BB} levels below 12 V, the selected threshold,V_{BRO}, should be no larger than 4 V less than V_{BB} (i.e. $V_{BROmax} = V_{BB} - 4$ V).

Bridge: Phase State Monitor

The bridge phase connections at the SA, SB, and SC terminals are connected to a variable threshold comparator. The output of the comparator is stored in the SAS, SBS, and SCS phase state bits in the Verify Result 1 register, to provide a logic-level monitor of the state of the power bridge outputs to the load (logic 1 indicating voltage on SA, SB, and SC more positive than the threshold). Additionally, the comparator outputs are made available as discrete logic signals on the SAL, SBL, and SCL pins (logic high indicating voltage on SA, SB, and SC more positive than the threshold). These comparators are not recommended for use with V_{BB} less than 8.5 V as this may result in unexpected phase comparator output transitions.

The threshold for the three comparators, V_{PT}, is generated, as a ratio of the bridge voltage, by a 6-bit DAC and determined by the contents of the VPT[5:0] variable. V_{PT} is approximately defined as:

$$V_{PT} = (n / 64) \times V_{BRG}$$

where n is a positive integer defined by VPT[5:0].

V_{PT} can be programmed between 0 and 98.4% V_{BRG}. At V_{BB} of less than 12 V, it is recommended that VPT[5:0] should only be set to 100000b (50% of V_{BRG}) to avoid unexpected phase comparator output transitions.

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Sense Amplifier Disconnect

Each sense amplifier includes continuous current sources, I_{SAD}, that will allow detection of an input open-circuit condition. If an input open-circuit occurs, the voltage rises above the sense amplifier open-load detect threshold, V_{SAD}, and the S1D, S2D, or S3D bit is set in the Verify Result 1 register, depending upon the sense amplifier affected.

Bridge: LSS Disconnected

Each LSS terminal includes a continuous current source, I_{LU}, to V_{REG} that will pull the LSS terminal up if it there is no low-impedance path from LSS to ground. If the voltage at an LSS terminal with respect to ground rises above the LSS open threshold, V_{LSO}, then the LAD, LBD, or LCD bit will be set in the Verify Result 0 register, the corresponding low-side VDS fault bit, ALO, BLO, or CLO will be set in the Diagnostic1 register, the DSO and FF bits will be set in the Status register, and the general fault flag will be active. If ESF = 1, all gate drive outputs will be disabled; if ESF = 0 they will not be disabled. When the voltage at the LSS terminal falls below the falling LSS open-threshold voltage, $V_{LSO} - V_{LSOHys}$, the fault flag will be reset and the outputs will be reactivated in the ESF = 1 case. The LAD, LBD, and LCD bits remain in the Verify Result 0 register until reset and the VDS diagnostic bits remain in the Diagnostic 1 register until reset.

Offline Verification

The following functions are only active when commanded by setting the appropriate bit in the verification command registers, in addition to any required gate drive commands. If the function only verifies a connection, then a fail will set the appropriate bit in the verification result register. No other action will be taken by the A4911. If the function is to verify one of the diagnostic circuits in the A4911, then the verification is completed by checking that the associated fault bit is set in the diagnostic registers.

Bridge: Phase Disconnected

The connections to each of the phases at the common node at the source of the high-side and the drain of the low-side MOSFET can be verified by a combination of MOSFET commands and test currents.

High-side and low-side tests must be performed to fully verify the connection for each phase. If a high impedance exists between all Sx terminals (e.g. an isolator is present between the MOSFET bridge and the motor and is in the "open" state), all

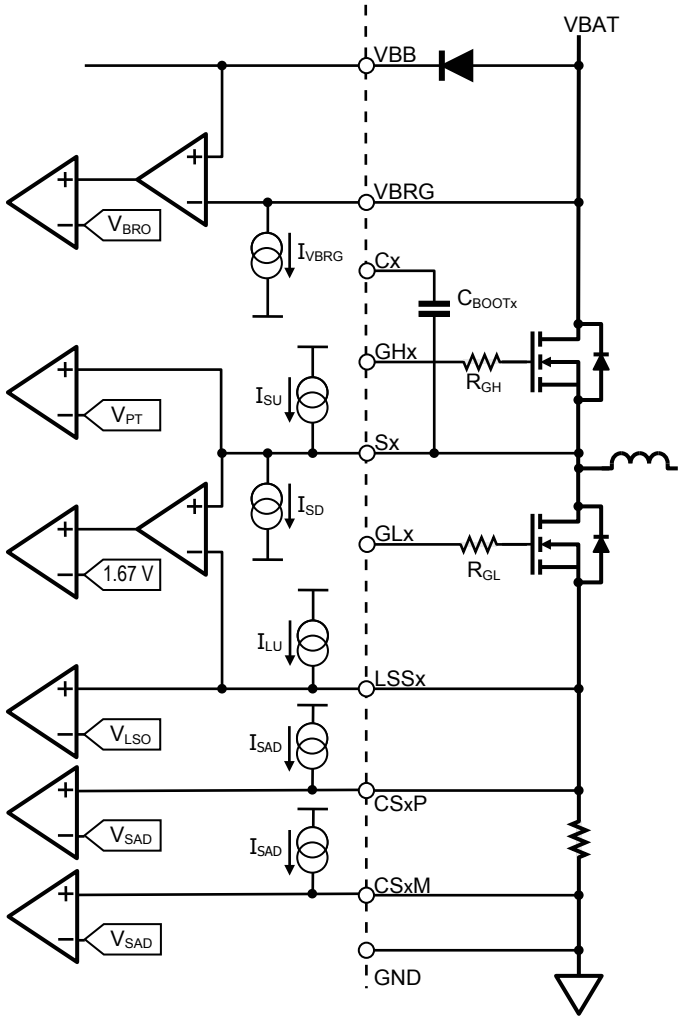

Figure 9: Bridge Terminal Connection Verification

high-side connections may be tested simultaneously, and then all low-side connections simultaneously.

For the high-side test, all high-side MOSFETs are switched on using the Control register bits or the logic input terminals. A pull-down current on each phase, I_{SD}, is then switched on by setting the YPH bit in the Verify Command 1 register to 1. The phase state monitors determine whether the resultant voltage on each Sx node is higher than the programmed V_{PT} threshold, and for every phase where this is true, the corresponding PxD bit in the Verify Result 0 register is set to 1 when YPH is reset to 0. Any PxD bit set to 1 indicates that the corresponding MOSFET source

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and Sx node are connected. Test timing is dictated by the external controller and should be set so as to ensure any capacitance associated with the bridge outputs can be discharged by the pull-down current prior to resetting YPH to 0; otherwise, fault conditions may not be detected.

For the low-side test, all low-side MOSFETs are switched on using the Control register bits or the logic input terminals. A pull-up current on each phase, I_{SU}, is then switched on by setting the YPL bit in the Verify Command 1 register to 1. The phase state monitors determine whether the resultant voltage on each Sx node is lower than a fixed threshold of 1.67 V, and for every phase where this is true, the corresponding PxD bit in the Verify Result 0 register is set to 1 when YPL is reset to 0. Any PxD bit set to 1 indicates that the corresponding MOSFET drain and Sx node are connected. Test timing is dictated by the external controller and should be set to ensure any capacitance associated with the bridge outputs can be charged by the pull-up current prior to resetting YPL to 0; otherwise, fault conditions may not be detected.

If a high impedance does not exist between all Sx terminals (e.g. no motor isolator present), phase connections can still be verified, but each high-side and each low-side connection must be tested separately (six tests in total), with the PxD bit values reported for phases not under test being ignored in each case.

Verify: VREG Undervoltage

The VREG undervoltage detector is verified by setting the YRU bit in the Verify Command 0 register to 1. This applies a voltage to the comparator that is lower than the undervoltage threshold and should cause the general fault flag to be active and a VREG undervoltage fault bit, VRU, to be latched in the Diagnostic 1 register. When YRU is reset to 0, the general fault flag will be cleared and the VRU bit will remain set in the Diagnostic 1 register until reset. If the VRU bit is not set, then the verification has failed.

Verify: VREG Overvoltage

The VREG overvoltage detector is verified by setting the YRO bit in the Verify Command 0 register to 1. This applies a voltage to the comparator that is higher than the overvoltage threshold and should cause the general fault flag to be active and the VREG overvoltage fault bit, VRO, to be latched in the Diagnostic 1 register. When YRO is reset to 0, the general fault flag will be cleared and the VRO bit will remain set in the Diagnostic 1 register until reset. If the VRO bit is not set, then the verification has failed.

Verify: Temperature Warning

The temperature warning detector is verified by setting the YTW bit in the Verify Command 2 register to 1. This applies a voltage to the comparator that is lower than the temperature warning threshold and should cause the general fault flag to be active and a temperature warning fault bit, TW, to be latched in the Status register. When YTW is reset to 0, the general fault flag will be cleared and the TW bit will remain set in the Status register until reset. If the TW bit is not set, then the verification has failed.

Verify: Overtemperature

The overtemperature detector is verified by setting the YOT bit in the Verify Command 2 register to 1. This applies a voltage to the comparator that is lower than the overtemperature threshold and should cause the general fault flag to be active and an overtemperature fault bit, OT, to be latched in the Status register. When YOT is reset to 0, the general fault flag will be cleared and the overtemperature fault will remain in the Status register until reset. If the OT bit is not set, then the verification has failed.

Verify: VBB Supply Overvoltage

The VBB overvoltage detector is verified by setting the YSO bit in the Verify Command 0 register to 1. This applies a voltage to the comparator that is higher than the VBB overvoltage threshold and should cause the general fault flag to be active and a VBB overvoltage fault bit, VSO, to be latched in the Diagnostic 2 register. When YSO is reset to 0, the general fault flag will be cleared and the VSO bit will remain set in the Diagnostic 2 register until reset. If the VSO bit is not set, then the verification has failed.

Verify: VBB Supply Undervoltage

The VBB undervoltage detector is verified by setting the YSU bit in the Verify Command 0 register to 1. This applies a voltage to the comparator that is lower than the VBB undervoltage threshold and should cause the general fault flag to be active and a VBB undervoltage fault bit, VSU, to be latched in the Diagnostic 2 register. When YSU is reset to 0 the general fault flag will be reset and the VSU bit will remain set in the Diagnostic 2 register until cleared. If the VSU bit is not set then the verification has failed.

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Verify: VGS Undervoltage

The VGS undervoltage detectors can be verified individually or in two groups, high-side and low-side. The detectors are verified by switching on the required MOSFET using the serial Control register bits or the logic input terminals and then setting the YGU bit in the Verify Command 0 register to 1. This applies a voltage that is lower than the VGS undervoltage threshold to the active comparator and should cause the general fault flag to be active and a VGS undervoltage fault to be latched in the corresponding VGS undervoltage fault bit in the Diagnostic 0 register. (For example, the CHU bit should be set after the CH bit is set in the Control register or the HC input is driven high, etc.) After a period exceeding the programmed VGS qualification time, t_{VDQ}, YGU must be returned to 0 and all gate drives must be commanded off. The general fault flag will be cleared, but the VGS undervoltage fault bits will remain in the Diagnostic 0 register until reset. This must be repeated until all MOSFETs have been switched to verify all VGS undervoltage comparators. If any VGS fault bit is not set after all MOSFETs have been switched, then the verification has failed for the corresponding comparator.

Verify: Bootstrap Capacitor Undervoltage Fault

The bootstrap capacitor undervoltage detectors are verified by setting the YBU bit in the Verify Command 0 register to 1 and switching on one or more high-side MOSFETs using the serial Control register bits or the logic input terminals. This applies a voltage that is lower than the bootstrap undervoltage threshold to any active comparator and should cause the general fault flag to be active and a bootstrap undervoltage fault to be latched in the corresponding bootstrap undervoltage fault bit (VA, VB, or VC) in the Diagnostic 2 register. This must be repeated for each high-side MOSFET to verify all bootstrap undervoltage comparators. When YBU is reset to 0 or all gate drives are commanded off, the general fault flag is cleared and the bootstrap undervoltage faults remain in the Diagnostic 2 register until reset. If any bootstrap undervoltage fault bit is not set after all MOSFETs have been switched on, then the verification has failed for the corresponding comparator.

Verify: MOSFET VDS Overvoltage Fault

The VDS overvoltage detectors can be verified individually or in two groups, high-side and low-side. The detectors are verified by switching on the required MOSFETs using the serial command register bits or the logic input terminals, and then setting the YDO bit in the Verify Command 0 register to 1. This applies a voltage that is higher than the VDS overvoltage threshold set for any active comparator by turning on the complementary MOSFET in the same phase to pull the Sx node toward VBRG (low-side verification) or LSSx (high-side verification). In response, the general fault flag should go low and a VDS overvoltage fault should be latched in the corresponding VDS overvoltage fault bit in the Diagnostic 1 register. (For example, the CHO bit should be set after the CH bit is set in the Control register or the HC input is driven high, etc.). After a period exceeding the programmed VDS qualification time, t_{VDQ}, the YDO bit must be returned to 0 to exit the verification mode. Diag 1 should then be read to inspect and clear the xLO and xHO bits, and clear the general fault flag. This must be repeated until all MOSFETs have been switched to verify all VDS overvoltage comparators. If any VDS overvoltage fault bit has not been set after all MOSFETs have been switched, then the verification has failed for the corresponding comparator.

Verify: Logic Terminal Overvoltage

The logic terminal overvoltage detector is verified by setting the YLO bit in the Verify Command 0 register to 1. This applies a voltage to the comparator associated with each logic terminal that is higher than the logic terminal overvoltage threshold and should cause the logic terminal overvoltage fault bit, VLO, to be set and latched in the Status register. When YLO is reset to 0, the VLO bit will remain set in the Status register indicating a successful verification. If the VLO bit is not set, then the verification has failed. During the period when YLO is set to 1, the general fault flag on the DIAG pin may be set to logic low and the gate drive outputs may be disabled, but neither of these conditions indicates a successful logic terminal overvoltage verification.

Verify: Overcurrent Detect and Sense Amplifier

The overcurrent detector is verified by setting the YOC bit in the Verify Command 1 register to 1. This forces the output of each sense amplifier to positive full-scale, which can then be measured. The sense amplifier outputs remain connected to the overcurrent comparators, and the full-scale output applies a voltage to the comparator that is higher than the overcurrent threshold, and should cause the overcurrent fault bits, OC1, OC2, and OC3, to be latched in the Diagnostic 2 register. When YOC is reset to 0, the sense amplifier outputs will return to normal operation and the OC1, OC2, and OC3 bits will remain set in the Diagnostic 2 register until reset. If any of the OC1, OC2, or OC3 bits are not set, then the verification has failed for the corresponding comparator.

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During verification of the overcurrent detector, the overcurrent threshold voltage, V_{OCT}, set by OCT[3:0] plus any offset, V_{OOS}, set by SAO[3:0] must not exceed the positive extreme of the sense amplifier output dynamic range of 4.8 V. If it does, then the OC1, OC2, and OC3 bits may not be set and the verification may fail.

Verify: ENABLE Watchdog Timeout

The ENABLE watchdog timeout is verified by setting the EWD bit to 1 to select the watchdog mode and then changing the state of the ENABLE input. This change of state will enable the gate drive outputs under command from the corresponding phase control signals and will start the watchdog timer. The ENABLE input must then be held in this state. At the end of the timeout period, t_{ETO}, the ETO bit should be set in the status register. If the ETO bit is not set, then the verification has failed.

Verify: All Gate Drives Off

The successful propagation of control inputs demanding all-gate-drives-off to the gate drive outputs is verified by setting up an appropriate input condition and inspecting the GDO bit in the Verify Result 1 register. If the input condition has successfully turned off all six gate drives, the GDO bit is set. The control input conditions (i.e. the combinational states of Hx, Lx, xH, xL, and ENABLE) that demand all outputs off (GHx = L, GLx = L) and hence set the GDO bit as a result of a successful verification test can be determined by inspection of Table 1, Table 2, and Table 3. If the ENABLE watchdog mode is selected (EWD = 1) and the watchdog timeout is allowed to expire, the GDO bit will similarly be set as the result of a successful test. Verification of propagation from an appropriate combination of phase logic inputs (Hx, Lx) and serial register bits (xH, xL) to the gate drive outputs does not verify propagation from the ENABLE input to the gate drive outputs and vice versa. Gate drive off events are not latched in the Verify Result 1 register and the GDO bit returns to 0 as soon as any gate drive is detected to be in the on state.

Verify: On-State Open-Load Detection and Sense Amplifier

The on-state open-load detector is verified by turning on a low-side gate drive (to select a phase for test) and at least one high-side gate drive (on a different phase), setting the AOL bit in the Config 5 register to 1, and then setting the YOL bit in the Verify Command 1 register to 1. This forces the output of the sense amplifier associated with the selected phase to its zero current output condition (equivalent to zero differential input), which then drives the open-load comparator with a voltage that is lower than the comparator's threshold. When YOL is first set to 1, any open-load faults are cleared and the open-load timer is reset. At the end of the timeout period, the YOL bit is reset by the A4911 to indicate that the timeout is complete, and the OL fault bit should be set in the Diagnostic 2 register. When YOL is reset to 0, the sense amplifier outputs return to normal operation and the OL bit remains set in the Diagnostic 2 register until reset. If the OL bit is not set, then the verification has failed. If YOL is reset to 0 before the timeout has completed, then the verification is terminated without setting any fault bits. All three phases must be tested separately to complete the verification.

Verify: Off-State Open-Load Detection

The off-state open-load detector is verified one phase at a time. For each phase, two steps are required: the first to verify the current source, I_{SU}, and the second to verify the current sink, I_{SD} (Table 8). On Phase A and Phase C the off-state open load detect comparators and timers are also verified. All gate drive outputs must be low and all MOSFETs off during verification.

Table 8: Off-State Open-Load Detection Verification

Phase	YOP [1:0]	YO1	YO2	Current	Current Strength	Verify Passed
A	00	1	0	I_{SU}	$I_{SD} < I_{SU}$	OL = 1
A	00	0	1	I_{SD}	$I_{SD} > I_{SU}$	OL = 1
B	01	1	0	I_{SU}	$I_{SD} < I_{SU}$	OL = 1
B	01	0	1	I_{SD}	$I_{SD} > I_{SU}$	OL = 1
C	10	1	0	I_{SU}	$I_{SD} < I_{SU}$	OL = 1
C	10	0	1	I_{SD}	$I_{SD} > I_{SU}$	OL = 1

Phase A: YOP[1:0] is set to 00 to select Phase A. Step 1 is initiated by setting YO1 to 1 to set the pull-down current, I_{SD}, to a value lower than the pull-up current, I_{SU}, such that the input voltage to the open-load detect comparator is greater than the open-load detection voltage. (Any open-load faults are automatically cleared and the open-load timer is reset.) After a timeout period, t_{OLTO}, the YO1 bit is reset by the A4911 and the OL bit should be set to 1 in the Diagnostic 2 register. Reading Diagnostic 2 clears the OL bit if set. If YO1 is reset to 0 before the timeout has expired, the verification will be terminated without setting the OL bit. Step 2 is initiated by setting YO2 to 1 to set the pull-down current, I_{SD}, to a value higher than the pull-up current, I_{SU}, such that the input

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voltage to the comparator is lower than the open-load detection voltage. (Any open-load faults are automatically cleared and the open-load timer is reset.) After a timeout period, t_{OLTO}, the YO2 bit is reset by the A4911 and the OL bit should be set to 1 in the Diagnostic 2 register. Reading Diagnostic 2 clears the OL bit if set. If YO2 is reset to 0 before the timeout has expired, the verification will be terminated without setting the OL bit.

Phase B: YOP[1:0] is set to 01 to select Phase B. Step 1 is initiated by setting YO1 to 1 to set the pull-down current, I_{SD}, to a value lower than the pull-up current, I_{SU}, such that the input voltage to the phase state comparator is greater than the phase comparator threshold voltage. (The open-load timer is reset.) After a timeout period, t_{OLTO}, the YO1 bit is reset by the A4911 and the OL bit should be set to 1 in the Diagnostic 2 register. If YO1 is reset to 0 before the timeout has expired, the verification will be terminated. Step 2 is initiated by setting YO2 to 1 to set the pull-down current, I_{SD}, to a value higher than the pull-up current, I_{SU}, such that the input voltage to the phase state comparator is lower than the phase comparator threshold voltage. (The open-load timer is reset.) After a timeout period, t_{OLTO}, the YO2 bit is reset by the A4911 and the OL bit should be set to 1 in the Diagnostic 2 register. If YO2 is reset to 0 before the timeout has expired, the verification will be terminated without setting the OL bit.

Phase C: YOP[1:0] is set to 10 to select Phase C. Steps 1 and 2 otherwise per Phase A above.

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SERIAL INTERFACE

Table 9: Serial Register Definition*

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0:Config 0	0	0	0	0	0	WR	DBM			DT5	DT4	DT3	DT2	DT1	DT0	P
							0	0	0	1	1	1	1	1	1	
1:Config 1	0	0	0	0	1	WR	OCQ	OCT3	OCT2	OCT1	OCT0	TOC3	TOC2	TOC1	TOC0	P
							0	0	0	1	0	1	1	1	1	
2:Config 2	0	0	0	1	0	WR	VDQ			TVD5	TVD4	TVD3	TVD2	TVD1	TVD0	P
							0	0	0	0	1	0	0	0	0	
3:Config 3	0	0	0	1	1	WR	S3C	S2C	S1C	VTL5	VTL4	VTL3	VTL2	VTL1	VTL0	P
							0	0	0	0	1	1	0	0	0	
4:Config 4	0	0	1	0	0	WR	VTB1	VTB0		VTH5	VTH4	VTH3	VTH2	VTH1	VTH0	P
							0	0	0	0	1	1	0	0	0	
5:Config 5	0	0	1	0	1	WR	AOL	OLI	DOO			OLT3	OLT2	OLT1	OLT0	P
							0	0	0	0	0	1	0	0	0	
6:Config 6	0	0	1	1	0	WR	EWD	VRG		VPT5	VPT4	VPT3	VPT2	VPT1	VPT0	P
							0	1	0	1	0	0	0	0	0	
7:Config 7	0	0	1	1	1	WR		SAO3	SAO2	SAO1	SAO0		SAG2	SAG1	SAG0	P
							0	1	1	1	1	0	0	1	0	
8:Config 8	0	1	0	0	0	WR		THR3	THR2	THR1	THR0	THF3	THF2	THF1	THF0	P
							0	0	0	0	0	0	0	0	0	
9:Config 9	0	1	0	0	1	WR		IHR13	IHR12	IHR11	IHR10	IHF13	IHF12	IHF11	IHF10	P
							0	0	0	0	0	0	0	0	0	
10:Config 10	0	1	0	1	0	WR		IHR23	IHR22	IHR21	IHR20	IHF23	IHF22	IHF21	IHF20	P
							0	0	0	0	0	0	0	0	0	
11:Config 11	0	1	0	1	1	WR		TLR3	TLR2	TLR1	TLR0	TLF3	TLF2	TLF1	TLF0	P
							0	0	0	0	0	0	0	0	0	
12:Config 12	0	1	1	0	0	WR		ILR13	ILR12	ILR11	ILR10	ILF13	ILF12	ILF11	ILF10	P
							0	0	0	0	0	0	0	0	0	
13:Config 13	0	1	1	0	1	WR		ILR23	ILR22	ILR21	ILR20	ILF23	ILF22	ILF21	ILF20	P
							0	0	0	0	0	0	0	0	0	

*Power-on reset value shown below each input register bit.

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Table 9:Serial Register Definition (continued)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
20: Verify Command 0	1	0	1	0	0	WR		YDO	YRO	YRU	YBU	YLO	YSO	YSU	YGU	P
							0	0	0	0	0	0	0	0	0	
21: Verify Command 1	1	0	1	0	1	WR	YPH	YPL	YOC		YOL	YOP1	YOP0	YO1	YO2	P
							0	0	0	0	0	1	1	0	0	
22: Verify Command 2	1	0	1	1	0	WR	YTW	YOT								P
							0	0	0	0	0	0	0	0	0	
23: Verify Result 0	1	0	1	1	1	WR			PCD	PBD	PAD	VBR	LCD	LBD	LAD	P
							0	0	0	0	0	0	0	0	0	
24: Verify Result 1	1	1	0	0	0	WR			GDO	SCS	SBS	SAS	S3D	S2D	S1D	P
							0	0	1	0	0	0	0	0	0	
25: Mask 0	1	1	0	0	1	WR				CHU	CLU	BHU	BLU	AHU	ALU	P
							0	0	0	0	0	0	0	0	0	
26: Mask 1	1	1	0	1	0	WR	VRO	VRU		CHO	CLO	BHO	BLO	AHO	ALO	P
							0	0	0	0	0	0	0	0	0	
27: Mask 2	1	1	0	1	1	WR	VS	VLO	BSU	TW						P
							0	0	0	0	0	0	0	0	0	
28: Diag 0	1	1	1	0	0	WR				CHU	CLU	BHU	BLU	AHU	ALU	P
							0	0	0	0	0	0	0	0	0	
29: Diag 1	1	1	1	0	1	WR	VRO	VRU		CHO	CLO	BHO	BLO	AHO	ALO	P
							0	0	0	0	0	0	0	0	0	
30: Diag 2	1	1	1	1	0	WR	VC	VB	VA	VSO	VSU	OC3	OC2	OC1	OL	P
							0	0	0	0	0	0	0	0	0	
31: Control	1	1	1	1	1	WR	DG1	DG0	ESF	CH	CL	BH	BL	AH	AL	P
							0	0	1	0	0	0	0	0	0	
Status	FF	POR	SE	EE	OT	TW	VS	VLO	ETO	VR		LDF	BSU	GSU	DSO	P
	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	

*Power-on reset value shown below each input register bit.

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A three-wire synchronous serial interface, compatible with SPI, is used to control the features of the A4911. The SDO terminal can be used, during a serial transfer, to provide diagnostic feedback and readback of the register contents.

The A4911 can be operated without the serial interface using the default settings and the logic control inputs; however, application specific configurations and several verification functions are only possible by setting the appropriate register bits through the serial interface. In addition to setting the configuration bits, the serial interface can also be used to control the bridge MOSFETs directly.

The serial interface timing requirements are specified in the Electrical Characteristics table, and illustrated in Figure 2. Data is received on the SDI terminal and clocked through a shift register on the rising edge of the clock signal input on the SCK terminal. STRn is normally held high, and is only brought low to initiate a serial transfer. No data is clocked through the shift register when STRn is high, allowing multiple slave units to use common SDI and SCK connections. Each slave then requires an independent STRn connection. The SDO output assumes a high-impedance state when STRn is high, allowing a common data readback connection. When driving devices running from a 5 V logic supply, it may be necessary to add a 2 kΩ pull-up resistor from SDO to that supply to ensure an adequate logic high output voltage level is achieved.

After 16 data bits have been clocked into the shift register, STRn must be taken high to latch the data into the selected register. When this occurs, the internal control circuits act on the new data and the registers are reset depending on the type of transfer.

If there are more than 16 rising edges on SCK, or if STRn goes high and there are fewer than 16 rising edges on SCK (either being described as a framing error), the write will be cancelled without latching data to the register. The Status register will not be reset.

The first five bits, D[15:11], in a serial word are the register address bits giving the possibility of 32 register addresses. The sixth bit, WR (D[10]), is the write/read bit. When WR is 1, the following 9 bits, D[9:1], clocked in from the SDI terminal, are written to the addressed register. When WR is 0, the following 9 bits, D[9:1], clocked in from the SDI terminal, are ignored; no data is written to the serial registers and the contents of the addressed register are clocked out on the SDO terminal.

The last bit in any serial transfer, D[0], is a parity bit that is set to ensure odd parity in the complete 16-bit word. Odd parity means that the total number of 1s in any transfer should always be an odd number. This ensures that there is always at least one bit set to 1 and one bit set to 0 and allows detection of stuck-at faults on the serial input and output data connections. The parity bit is not stored but generated on each transfer.

In addition to the addressable registers, a read-only Status register is output on SDO for all register addresses when WR is set to 1. For all serial transfers, the first six bits output on SDO will always be the first six bits from the Status register. Register data is output on the SDO terminal MSB first while STRn is low and changes to the next bit on each falling edge of SCK. The first bit, which is always the FF bit from the Status register, is output as soon as STRn goes low.

Registers 23, 24, 28, 29, and 30 contain verification results and diagnostic fault indicators and are read only. If the WR bit for these registers is set to 1, then the data input through SDI is ignored and the contents of the Status register is clocked out on the SDO terminal then reset as for a normal write. No other action is taken. If the WR bit for these registers is set to 0, then the data input through SDI is ignored, the contents of the addressed register is clocked out on the SDO terminal, and the addressed register is reset.

If a framing error is detected and/or the parity of any received transfer is even rather than odd, the SE bit is set in the Status register to indicate a data transfer error. This fault condition can be cleared by a subsequent valid serial write or by a power-on-reset.

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Configuration Registers

Thirteen registers are used to configure the operating parameters of the A4911.

Config 0: Bridge timing settings:

- DBM, disabled bootstrap management function.
- DT[5:0], a 6-bit integer to set the dead time, t_{DEAD}, in 50 ns increments

Config 1: Bridge monitor setting:

- OCQ, selects the overcurrent time qualifier mode, blank or debounce.
- OCT[3:0], a 4-bit integer to set the overcurrent threshold voltage, V_{OCT}, in 300 mV increments.
- TOC[3:0], a 4-bit integer to set the overcurrent verification time, t_{OCQ}, in 500 ns increments

Config 2: Bridge monitor setting:

- VDQ, selects the VDS and VGS qualifier mode, blank or debounce.
- TVD[5:0], a 6-bit integer to set the VDS and VGS fault qualification time, t_{VDQ}, in 100 ns increments.

Config 3: Bridge monitor setting:

- VTL[5:0], a 6-bit integer to set the low-side drain-source threshold voltage, V_{DSTL}, in 50 mV increments.
- S3C, S2C, S1C, initiates current sense amplifier calibration.

Config 4: Bridge monitor setting:

- VTB[1:0], a 2-bit integer to set the VBRG disconnect threshold voltage, V_{BRO}, in 2 V increments.
- VTH[5:0], a 6-bit integer to set the high-side drain-source threshold voltage, V_{DSTH}, in 50 mV increments.

Config 5: Bridge monitor setting:

- AOL, activate on-state open-load detection
- OLI, selects the open-load test current
- DOO, disables off-state open-load detect
- OLT[3:0], a 4-bit integer to set the open-load threshold voltage, V_{OLTH}, in 25 mV increments.

Config 6: Bridge monitor setting:

- EWD, activate ENABLE watchdog monitor.
- VRG, selects the regulator and gate drive voltage.
- VPT[5:0], a 6-bit integer to set the phase comparator threshold voltage, V_{PT}, as a ratio of the bridge voltage, V_{BRG}, in 1.56% increments from 0 to 98.4%.

Config 7: Sense amp gain and offset:

- SAO[3:0], a 4-bit integer to set the sense amplifier offset of between 0 and 2.5 V.
- SAG[2:0], a 3-bit integer to set the sense amplifier gain between 10 and 50 V/V.

Config 8: Gate drive control (high-side timing):

- THR[3:0], a 4-bit integer to set the high-side rising (GHx low-to-high) I1 time in 50 ns increments.
- THF[3:0], a 4-bit integer to set the high-side falling (GHx high-to-low) I1 time in 50 ns increments.

Config 9: Gate drive control (high-side I1 current):

- IHR1[3:0]], a 4-bit integer to set the high-side rising (GHx low-to-high) I1 current in 5 mA increments.
- IHF1[3:0] , a 4-bit integer to set the high-side falling (GHx high-to-low) I1 current in 5 mA increments.

Config 10: Gate drive control (high-side I2 current):

- IHR2[3:0]], a 4-bit integer to set the high-side rising (GHx low-to-high) I2 current in 5 mA increments.
- IHF2[3:0] , a 4-bit integer to set the high-side falling (GHx high-to-low) I2 current in 5 mA increments.

Config 11: Gate drive control (low-side timing):

- TLR[3:0] , a 4-bit integer to set the low-side rising (GLx low-to-high) I1 time in 50 ns increments.
- TLF[3:0], a 4-bit integer to set the low-side falling (GLx high-to-low) I1 time in 50 ns increments.

Config 12: Gate drive control (low-side I1 current):

- ILR1[3:0] , a 4-bit integer to set the low-side rising (GLx low-to-high) I1 current in 5 mA increments.

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- ILF1[3:0] , a 4-bit integer to set the low-side falling (GLx high-to-low) I1 current in 5 mA increments.

Config 13: Gate drive control (low side I2 current):

- ILR2[3:0] , a 4-bit integer to set the low-side rising (GLx low-to-high) I2 current in 5 mA increments.
- ILF2[3:0] , a 4-bit integer to set the low-side falling (GLx high-to-low) I2 current in 5mA increments.

Verification Registers

Four registers are used to manage the system and diagnostic verification features.

Verify Command 0:

Individual bits to initiate offline verification tests for VDS, VREG, bootstrap, logic overvoltage, VBB, and VGS diagnostics.

Verify Command 1:

Individual bits to initiate offline verification tests for phase disconnect, overcurrent and open-load diagnostics.

Verify Command 2:

Individual bits to initiate offline verification tests for temperature diagnostics.

Verify Result 0 (read only):

Individual bits holding the results of phase disconnect, VBRG open, and LSS open verification tests. These bits are reset on completion of a successful read of the register.

Verify Result 1 (read only):

Individual bits holding the results of phase state, sense amp, and gate drive off verification tests. These bits are reset on completion of a successful read of the register.

Diagnostic Registers

In addition to the read-only status register, three read-only diagnostic registers provide detailed diagnostic management and reporting. Three mask registers allow individual diagnostics to be disabled. If a bit is set to one in the mask registers, then the corresponding diagnostic will be completely disabled. No fault states for the disabled diagnostic will be generated and no fault flags or diagnostic bits will be set. These bits in the diagnostic registers are reset on completion of a successful read of the register.

Mask 0:

Individual bits to disable VGS diagnostic monitors.

Mask 1:

Individual bits to disable VREG and VDS diagnostic monitors.

Mask 2:

Individual bits to disable VBB, logic, bootstrap, and temperature diagnostic monitors.

Diagnostic 0 (read only):

Individual bits indicating faults detected in VGS diagnostic monitor.

Diagnostic 1 (read only):

Individual bits indicating faults detected in VREG and VDS diagnostic monitors.

Diagnostic 2 (read only):

Individual bits indicating faults detected in bootstrap, VBB, overcurrent and open-load diagnostic monitors.

Control Register

The Control register contains one control bit for each MOSFET and some system function settings:

- DG[1:0], 2 bits select the output that is to be routed to the DIAG terminal. The options are a general, active-low fault flag, a pulsed fault flag, a voltage indicating the approximate chip junction temperature, or a divided ratio of the system clock.
- ESF, defines the action taken when certain faults are detected. See Diagnostic Monitors section for further details.
- CH, CL, MOSFET Control bits for Phase C
- BH, BL, MOSFET Control bits for Phase B
- AH, AL, MOSFET Control bits for Phase A

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Status Register

There is one Status register in addition to the addressable registers. When any register transfer takes place, the first six bits output on SDO are always the most significant six bits of the Status register, irrespective of whether the addressed register is being read or written (see Figure 2: Serial Interface Timing). The content of the remaining ten bits will depend on the state of the WR bit input on SDI. When WR is 1, the addressed register will be written, and the remaining ten bits output on SDO will be the least significant nine bits of the Status register followed by a parity bit. When WR is 0, the addressed register will be read, and the remaining ten bits will be the contents of the addressed register, followed by a parity bit. If an attempt is made to write to a read-only register by setting WR to 1, no data will be written to the addressed register and all 15 bits of the Status register followed by a parity bit will be output on SDO. The read-only Status register provides a summary of the chip status by indicating if any diagnostic monitors have detected a fault. The most significant four bits of the Status register indicate critical system faults. Bits 11 through 1 provide indicators for specific individual faults and the contents of the three diagnostic registers. The contents and mapping to the diagnostic registers is listed in Table 10.

Table 10: Status Register Mapping

Status Register Bit	Diagnostic	Related Diagnostic Register Bits
FF	Status Flag	None
POR	Power-on-reset	None
SE	Serial Error	None
EE	EEPROM Error	None
OT	Over temperature	None
TW	Temperature warning	None
VS	VBB out of range	VSU, VSO
VLO	Logic OV	None
ETO	ENABLE timeout	None
VR	VREG monitor	VRU. VRO
LDF	Load monitor	OC1, OC2, OC3, OL
BSU	Bootstrap UV	VA, VB, VC
GSU	VGS UV	AHU, BHU, CHU, ALU, BLU, CLU
DSO	VDS OV	AHO, BHO, CHO ALO, BLO, CLO

UV = Undervoltage, OV = Overvoltage

The first most significant bit in the register is the diagnostic status flag, FF. This is high if any bits in the Status register are set. When STRn goes low to start a serial write, SDO outputs the diagnostic status flag. This allows the main controller to poll the A4911 through the serial interface to determine if a fault has been detected. If no faults have been detected, then the serial transfer may be terminated without generating a serial read fault by ensuring that SCK remains high while STRn is low. When STRn goes high, the transfer will be terminated and SDO will go into its high-impedance state.

The second most significant bit is the POR bit. At power-up or after a power-on-reset, the FF bit and the POR bit are set, indicating to the external controller that a power-on-reset has taken place. All other diagnostic bits are reset, and all other registers are returned to their default state. Note that a power-on-reset only occurs when the output of the internal logic regulator rises above its undervoltage threshold. Power-on-reset is not affected by the state of the VBB supply or VREG regulator output. In general, the VR and VRU bits will also be set following a power-on-reset, as the regulators will not have reached their respective rising undervoltage thresholds until after the register reset is completed. The POR bit is cleared by the first Status register read (write to an addressable device register) after power up.

The third bit in the Status register is the SE bit, which indicates that the previous serial transfer was not completed successfully.

The fourth bit in the Status register is the EE bit, which indicates that an EEPROM error was detected at device power-up.

If one or more of the OT, TW, VLO, and ETO faults are no longer present, the corresponding fault bit(s) will be reset following a successful read of the Status register. Resetting only affects latched fault bits for faults that are no longer present. For any static faults that are still present, for example overtemperature, the fault flag will remain set after the reset.

The remaining bits VS,VR, LDF, BSU, GSU, and DSO are all derived from the contents of the diagnostic registers (Table 10). These bits are only cleared when the corresponding contents of the diagnostic registers are read and reset—they cannot be reset by reading the Status register. A fault indicated on any of the related diagnostic register bits will set the corresponding status bit to 1. The related diagnostic register must then be read to determine the exact fault and clear the fault state if the fault condition has cleared.

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Serial Register Definition

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0:Config 0	0	0	0	0	0	WR	DBM			DT5	DT4	DT3	DT2	DT1	DT0	P
							0	0	0	1	1	1	1	1	1	
1:Config 1	0	0	0	0	1	WR	OCQ	OCT3	OCT2	OCT1	OCT0	TOC3	TOC2	TOC1	TOC0	P
							0	0	0	1	0	1	1	1	1	

*Power-on reset value shown below each input register bit.

Config 0

DBM Disable Bootstrap manager

DBM	Bootstrap Manager	Default
0	Active	D
1	Disabled	

DT[5:0] Dead time.

$t_{DEAD} = n \times 50$ ns

where where n is a positive integer defined by DT[5:0]. For example, for the power-on reset condition, DT[5:0] = [11 1111], t_{DEAD} = 3.15 µs.

The range of t_{DEAD} is 100 ns to 3.15 µs. Selecting a value of 1 or 2 will set the dead time to 100 ns. Setting DT[5:0]=0 disables the dead time.
If DT[5:0] = 0 and DBM = 0, a fixed value of dead time of 3.15 µs is applied on bootstrap management cycles.

P Parity bit. Ensures an odd number of 1s in any serial transfer.

Config 1

OCQ Overcurrent time qualifier mode

OCQ	Qualifier	Default
0	Debounce	D
1	Blanking	

OCT[3:0] Overcurrent threshold.

$V_{OCT} = (n + 1) \times 300$ mV

where n is a positive integer defined by OCT[3:0], e.g. for the power-on-reset condition OCT[3:0] = [0010] then V_{OCT} = 0.9 V.
The range of V_{OCT} is 0.3 to 4.8 V.

TOC[3:0] Overcurrent qualify time.

$t_{OCQ} = n \times 500$ ns

where n is a positive integer defined by TOC[3:0], e.g. for the power-on-reset condition TOC[3:0] = [1111] then t_{OCQ} = 7.5 µs.
The range of t_{OCQ} is 0 to 7.5 µs.

P Parity bit. Ensures an odd number of 1s in any serial transfer.

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	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
2:Config 2	0	0	0	1	0	WR	VDQ			TVD5	TVD4	TVD3	TVD2	TVD1	TVD0	P
							0	0	0	0	1	0	0	0	0	
3:Config 3	0	0	0	1	1	WR	S3C	S2C	S1C	VTL5	VTL4	VTL3	VTL2	VTL1	VTL0	P
							0	0	0	0	1	1	0	0	0	

*Power-on reset value shown below each input register bit.

Config 2

VDQ VDS and VGS Fault qualifier mode.

VDQ	VDS and VGS Fault Qualifier	Default
0	Debounce	D
1	Blank	

TVD[5:0] VDS and VGS qualification time.

$t_{VDQ} = n \times 100$ ns

where n is a positive integer defined by TVD[5:0].
e.g. for the power-on-reset condition
TVD[5:0] = [01 0000] then t_{VDQ} = 1.6 µs.
The range of t_{VDQ} is 0 to 6.3 µs.

P Parity bit. Ensures an odd number of 1s in any serial transfer.

Config 3

VTL[5:0] Low-side VDS overvoltage threshold.

$V_{DSTL} = n \times 50$ mV

where n is a positive integer defined by VTL[5:0],
e.g. for the power-on-reset condition
VTL[5:0] = [01 1000] then V_{DSTL} = 1.2 V.
The range of V_{DSTL} is 0 to 3.15 V.

S3C Sense amp 3 calibrate.

S2C Sense amp 2 calibrate.

S1C Sense amp 1 calibrate.

P Parity bit. Ensures an odd number of 1s in any serial transfer.

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	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
4:Config 4	0	0	1	0	0	WR	VTB1	VTB0		VTH5	VTH4	VTH3	VTH2	VTH1	VTH0	P
							0	0	0	0	1	1	0	0	0	
5:Config 5	0	0	1	0	1	WR	AOL	OLI	DOO			OLT3	OLT2	OLT1	OLT0	P
							0	0	0	0	0	1	0	0	0	

*Power-on reset value shown below each input register bit.

Config 4

VTB[1:0] VBRG open threshold.

$V_{BRO} = (n + 1) \times 2$ V

where n is a positive integer defined by VTB[1:0], e.g. for the power-on-reset condition VTB[1:0] = [00] then V_{BRO} = 2 V. The range of V_{BRO} is 2 to 8 V.

VTH[5:0] High-side VDS overvoltage threshold.

$V_{DSTH} = n \times 50$ mV

where n is a positive integer defined by VTH[5:0], e.g. for the power-on-reset condition VTH[5:0] = [01 1000] then V_{DSTH} = 1.2 V. The range of V_{DSTH} is 0 to 3.15 V.

P Parity bit. Ensures an odd number of 1s in any serial transfer.

Config 5

AOL On-state open-load detect.

AOL	On-State Open-Load Detect	Default
0	Inactive	D
1	Active	

OLI Open-load test current.

OLI	Test Current	Default
0	–70 µA	D
1	–400 µA	

DOO Disable off-state open-load detect.

DOO	Off-State Open-Load Detect	Default
0	Active	D
1	Disabled	

OLT[3:0] Open load threshold.

$V_{OLTH} = (n + 1) \times 25$ mV

where n is a positive integer defined by OLT[3:0], e.g. for the power-on-reset condition OL[3:0] = [1000] then V_{OLT} =225 mV. The range of V_{OLTH} is 25 to 400 mV.

P Parity bit. Ensures an odd number of 1s in any serial transfer.

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	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
6:Config 6	0	0	1	1	0	WR	EWD	VRG		VPT5	VPT4	VPT3	VPT2	VPT1	VPT0	P
							0	1	0	1	0	0	0	0	0	
7:Config 7	0	0	1	1	1	WR		SAO3	SAO2	SAO1	SAO0		SAG2	SAG1	SAG0	P
							0	1	1	1	1	0	0	1	0	

*Power-on reset value shown below each input register bit.

Config 6

EWD ENABLE Watchdog.

EWD	ENABLE Watchdog	Default
0	Disabled	D
1	Active	

VRG V_{REG} Voltage level.

VRG	VREG Voltage	Default
0	8 V	
1	11 V	D

VPT[5:0] Phase comparator threshold.

$V_{PT} = (n / 64) \times V_{BRG}$

where n is a positive integer defined by VPT[5:0], e.g. for the power-on-reset condition VPT[5:0] = [10 0000] then V_{PT} = 50% V_{BRG}. The range of V_{PT} is 0 to 98.4% V_{BRG}.

P Parity bit. Ensures an odd number of 1s in any serial transfer.

Config 7

SAO[3:0] Sense amp offset.

SAO	Offset	Default
0	0	
1	0	
2	100 mV	
3	100 mV	
4	200 mV	
5	300 mV	
6	400 mV	
7	500 mV	
8	750 mV	
9	1 V	
10	1.25 V	
11	1.5 V	
12	1.75 V	
13	2 V	
14	2.25 V	
15	2.5 V	D

where SAO is a positive integer defined by SAO[3:0].

SAG[2:0] Sense amp gain.

SAG	Gain	Default
0	10	
1	15	
2	20	D
3	25	
4	30	
5	35	
6	40	
7	50	

where SAG is a positive integer defined by SAG[2:0].

P Parity bit. Ensures an odd number of 1s in any serial transfer.

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	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
8:Config 8	0	1	0	0	0	WR		THR3	THR2	THR1	THR0	THF3	THF2	THF1	THF0	P
							0	0	0	0	0	0	0	0	0	
9:Config 9	0	1	0	0	1	WR		IHR13	IHR12	IHR11	IHR10	IHF13	IHF12	IHF11	IHF10	P
							0	0	0	0	0	0	0	0	0	

*Power-on reset value shown below each input register bit.

Config 8

THR[3:0] High-side rising t1 Time.

$t_1 = (n + 1) \times 50$ ns

where n is a positive integer defined by THR[3:0], e.g. if THR[3:0] = [0001] then t_1 = 100 ns. The range of t_1 is 50 to 800 ns.

THF[3:0] High-side falling t1 Time.

$t_1 = (n + 1) \times 50$ ns

where n is a positive integer defined by THF[3:0], e.g. if THF[3:0] = [0001] then t_1 = 100 ns. The range of t_1 is 50 to 800 ns.

P Parity bit. Ensures an odd number of 1s in any serial transfer.

Config 9

IHR1[3:0] High-side rising I1 Current.

$I_1 = n \times -5$ mA

where n is a positive integer defined by IHR1[3:0], e.g. if IHR1[3:0] = [1000] then I_1 = –40 mA. The range of I_1 is –5 to –75 mA. Selecting a value of 0 will set maximum gate drive to turn on the MOSFET as quickly as possible.

IHF1[3:0] High-side falling I1 Current.

$I_1 = n \times 5$ mA

where n is a positive integer defined by IHF1[3:0], e.g. if IHF1[3:0] = [1000] then I_1 = 40 mA. The range of I_1 is 5 to 75 mA. Selecting a value of 0 will set maximum gate drive to turn off the MOSFET as quickly as possible.

P Parity bit. Ensures an odd number of 1s in any serial transfer.

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	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
10:Config 10	0	1	0	1	0	WR		IHR23	IHR22	IHR21	IHR20	IHF23	IHF22	IHF21	IHF20	P
							0	0	0	0	0	0	0	0	0	
11:Config 11	0	1	0	1	1	WR		TLR3	TLR2	TLR1	TLR0	TLF3	TLF2	TLF1	TLF0	P
							0	0	0	0	0	0	0	0	0	

*Power-on reset value shown below each input register bit.

Config 10

IHR2[3:0] High-side rising I2 Current.

$I_2 = n \times -5$ mA

where n is a positive integer defined by IHR2[3:0], e.g. if IHR2[3:0] = [1000] then $I_2 = -40$ mA. The range of I_2 is –5 to –75 mA. Selecting a value of 0 will set maximum gate drive to turn on the MOSFET as quickly as possible.

IHF2[3:0] High-side falling I2 Current.

$I_2 = n \times 5$ mA

where n is a positive integer defined by IHF2[3:0], e.g. if IHF2[3:0] = [1000] then $I_2 = 40$ mA. The range of I_2 is 5 to 75 mA. Selecting a value of 0 will set maximum gate drive to turn off the MOSFET as quickly as possible.

P Parity bit. Ensures an odd number of 1s in any serial transfer.

Config 11

TLR[3:0] Low-side rising t1 Time.

$t_1 = (n + 1) \times 50$ ns

where n is a positive integer defined by TLR[3:0], e.g. if TLR[3:0] = [0001] then $t_1 = 100$ ns. The range of t_1 is 50 to 800 ns.

TLF[3:0] Low-side falling t1 Time.

$t_1 = (n + 1) \times 50$ ns

where n is a positive integer defined by TLF[3:0], e.g. if TLF[3:0] = [0001] then $t_1 = 100$ ns. The range of t_1 is 50 to 800 ns.

P Parity bit. Ensures an odd number of 1s in any serial transfer.

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	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
12:Config 12	0	1	1	0	0	WR		ILR13	ILR12	ILR11	ILR10	ILF13	ILF12	ILF11	ILF10	P
							0	0	0	0	0	0	0	0	0	
13:Config 13	0	1	1	0	1	WR		ILR23	ILR22	ILR21	ILR20	ILF23	ILF22	ILF21	ILF20	P
							0	0	0	0	0	0	0	0	0	

*Power-on reset value shown below each input register bit.

Config 12

ILR1[3:0] Low-side rising I1 Current.

$I_1 = n \times -5$ mA

where n is a positive integer defined by ILR1[3:0], e.g. if ILR1[3:0] = [1000] then $I_1 = -40$ mA. The range of I_1 is –5 to –75 mA. Selecting a value of 0 will set maximum gate drive to turn on the MOSFET as quickly as possible.

ILF1[3:0] Low-side falling I1 Current.

$I_1 = n \times 5$ mA

where n is a positive integer defined by ILF1[3:0], e.g. if ILF1[3:0] = [1000] then $I_1 = 40$ mA. The range of I_1 is 5 to 75 mA. Selecting a value of 0 will set maximum gate drive to turn off the MOSFET as quickly as possible.

P Parity bit. Ensures an odd number of 1s in any serial transfer.

Config 13

ILR2[3:0] Low-side rising I2 Current.

$I_2 = n \times -5$ mA

where n is a positive integer defined by ILR2[3:0], e.g. if ILR2[3:0] = [1000] then $I_2 = -40$ mA. The range of I_1 is –5 to –75 mA. Selecting a value of 0 will set maximum gate drive to turn on the MOSFET as quickly as possible.

ILF2[3:0] Low-side falling I2 Current.

$I_2 = n \times 5$ mA

where n is a positive integer defined by ILF2[3:0], e.g. if ILF2[3:0] = [1000] then $I_2 = 40$ mA. The range of I_2 is 5 to 75 mA. Selecting a value of 0 will set maximum gate drive to turn off the MOSFET as quickly as possible.

P Parity bit. Ensures an odd number of 1s in any serial transfer.

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	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
20: Verify Command 0	1	0	1	0	0	WR		YDO	YRO	YRU	YBU	YLO	YSO	YSU	YGU	P
							0	0	0	0	0	0	0	0	0	
21: Verify Command 1	1	0	1	0	1	WR	YPH	YPL	YOC		YOL	YOP1	YOP0	YO1	YO2	P
							0	0	0	0	0	0	0	0	0	
22: Verify Command 2	1	0	1	1	0	WR	YTW	YOT								P
							0	0	0	0	0	0	0	0	0	

*Power-on reset value shown below each input register bit.

Verify Command 0

YDO VDS overvoltage

YRO VREG overvoltage

YRU VREG undervoltage

YBU Bootstrap undervoltage

YLO Logic overvoltage

YSO VBB Supply overvoltage

YSU VBB Supply undervoltage

YGU VGS undervoltage

Yxx	Verification	Default
0	Inactive	D
1	Active and Initiate	

P Parity bit. Ensures an odd number of 1s in any serial transfer.

Verify Command 1

YPH Phase disconnect high-side

YPL Phase disconnect low-side

YOC Overcurrent

YOL On-state open load

YOP[1:0] Off-state open-load phase select.

YOP	Phase	Default
0	A	
1	B	
2	C	
3	None	D

YO1 Off-state open load 1

YO2 Off-state open load 2

Yxx	Verification	Default
0	Inactive	D
1	Active and Initiate	

P Parity bit. Ensures an odd number of 1s in any serial transfer.

Verify Command 2

YTW Temperature warning

YOT Overtemperature

Yxx	Verification	Default
0	Inactive	D
1	Active and Initiate	

P Parity bit. Ensures an odd number of 1s in any serial transfer.

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	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
23: Verify Result 0	1	0	1	1	1	WR			PCD	PBD	PAD	VBR	LCD	LBD	LAD	P
							0	0	0	0	0	0	0	0	0	
24: Verify Result 1	1	1	0	0	0	WR			GDO	SCS	SBS	SAS	S3D	S2D	S1D	P
							0	0	1	0	0	0	0	0	0	

*Power-on reset value shown below each input register bit.

Verify Result 0 (read only)

PCD Phase C disconnect

PBD Phase B disconnect

PAD Phase A disconnect

VBR VBRG open circuit

LCD LSSC disconnect

LBD LSSB disconnect

LAD LSSA disconnect

xxx	Verification Result	Default
0	Not detected	D
1	Detected	

P Parity bit. Ensures an odd number of 1s in any serial transfer.

Verify Result 1 (read only)

GDO All gate drives off

GDO	Verification Result	Default
0	Gate drives not off	
1	Gate drives off	D

SCS Phase C state

SBS Phase B state

SAS Phase A state

SxS	Verification Result	Default
0	Phase low	D
1	Phase high	

S3D Sense amp 3 disconnect

S2D Sense amp 2 disconnect

S1D Sense amp 1 disconnect

SxD	Verification Result	Default
0	Not detected	D
1	Detected	

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	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
25: Mask 0	1	1	0	0	1	WR				CHU	CLU	BHU	BLU	AHU	ALU	P
							0	0	0	0	0	0	0	0	0	
26: Mask 1	1	1	0	1	0	WR	VRO	VRU		CHO	CLO	BHO	BLO	AHO	ALO	P
							0	0	0	0	0	0	0	0	0	
27: Mask 2	1	1	0	1	1	WR	VS	VLO	BSU	TW						P
							0	0	0	0	0	0	0	0	0	

*Power-on reset value shown below each input register bit.

Mask 0

CHU Phase C high-side VGS undervoltage

CLU Phase C low-side VGS undervoltage

BHU Phase B high-side VGS undervoltage

BLU Phase B low-side VGS undervoltage

AHU Phase A high-side VGS undervoltage

ALU Phase A low-side VGS undervoltage

xxx	Fault Mask	Default
0	Fault detection permitted	D
1	Fault detection disabled	

P Parity bit. Ensures an odd number of 1s in any serial transfer.

Mask 1

VRO VREG Overvoltage

VRU VREG Undervoltage

CHO Phase C high-side VDS overvoltage

CLO Phase C low-side VDS overvoltage

BHO Phase B high-side VDS overvoltage

BLO Phase B low-side VDS overvoltage

AHO Phase A high-side VDS overvoltage

ALO Phase A low-side VDS overvoltage

xxx	Fault Mask	Default
0	Fault detection permitted	D
1	Fault detection disabled	

P Parity bit. Ensures an odd number of 1s in any serial transfer.

Mask 2

VS VBB out of range

VLO Logic overvoltage

BSU Bootstrap undervoltage

TW Temperature warning

xxx	Fault Mask	Default
0	Fault detection permitted	D
1	Fault detection disabled	

P Parity bit. Ensures an odd number of 1s in any serial transfer.

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	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
28: Diag 0	1	1	1	0	0	WR				CHU	CLU	BHU	BLU	AHU	ALU	P
							0	0	0	0	0	0	0	0	0	
29: Diag 1	1	1	1	0	1	WR	VRO	VRU		CHO	CLO	BHO	BLO	AHO	ALO	P
							0	0	0	0	0	0	0	0	0	
30: Diag 2	1	1	1	1	0	WR	VC	VB	VA	VSO	VSU	OC3	OC2	OC1	OL	P
							0	0	0	0	0	0	0	0	0	

*Power-on reset value shown below each input register bit.

Diag 0 (read only)

CHU Phase C high-side VGS undervoltage

CLU Phase C low-side VGS undervoltage

BHU Phase B high-side VGS undervoltage

BLU Phase B low-side VGS undervoltage

AHU Phase A high-side VGS undervoltage

ALU Phase A low-side VGS undervoltage

xxx	Status	Default
0	No fault detected	D
1	Fault detected	

P Parity bit. Ensures an odd number of 1s in any serial transfer.

Diag 1 (read only)

VRO VREG Overvoltage

VRU VREG Undervoltage

CHO Phase C high-side VDS overvoltage

CLO Phase C low-side VDS overvoltage

BHO Phase B high-side VDS overvoltage

BLO Phase B low-side VDS overvoltage

AHO Phase A high-side VDS overvoltage

ALO Phase A low-side VDS overvoltage

xxx	Status	Default
0	No fault detected	D
1	Fault detected	

P Parity bit. Ensures an odd number of 1s in any serial transfer.

Diag 2 (read only)

VC Phase C bootstrap undervoltage

VB Phase B bootstrap undervoltage

VA Phase A bootstrap undervoltage

VSO VBB overvoltage

VSU VBB undervoltage

OC3 Overcurrent on sense amp 3

OC2 Overcurrent on sense amp 2

OC1 Overcurrent on sense amp 1

OL Open load

xxx	Status	Default
0	No fault detected	D
1	Fault detected	

P Parity bit. Ensures an odd number of 1s in any serial transfer.

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	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
31: Control	1	1	1	1	1	WR	DG1	DG0	ESF	CH	CL	BH	BL	AH	AL	P
							0	0	1	0	0	0	0	0	0	

*Power-on reset value shown below each input register bit.

Control

DG[1:0] Selects signal routed to DIAG.

DG1	DG0	Signal on DIAG Pin	Default
0	0	Fault – low true	D
0	1	Pulse Fault	
1	0	Temperature	
1	1	Clock	

ESF Enable Stop on Fail.

ESF	Recirculation	Default
0	No stop on fail. Report fault.	
1	Stop on fail. Report fault.	D

CH Phase C, High-side gate drive

CL Phase C, Low-side gate drive

BH Phase B, High-side gate drive

BL Phase B, Low-side gate drive

AH Phase A, High-side gate drive

AL Phase A, Low-side gate drive

See Table 2 and Table 3 for control logic operation.

P Parity bit. Ensures an odd number of 1s in any serial transfer.

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	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Status	FF	POR	SE	EE	OT	TW	VS	VLO	ETO	VR		LDF	BSU	GSU	DSO	P
	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	

*Power-on reset value shown below each input register bit.

Status

FF Status register flag
POR Power-on-reset
SE Serial Error
EE EEPROM Error

OT Overtemperature
TW High temperature warning
VS VBB out of range
VLO Logic overvoltage
ETO ENABLE watchdog timeout
VR VREG out of range
LDF Load fault
BSU Bootstrap undervoltage
GSU VGS undervoltage
DSO VDS overvoltage

xxx	Status
0	No fault detected
1	Fault detected

P Parity bit. Ensures an odd number of 1s in any serial transfer.

Status Register Bit Mapping

Status Register Bit	Related Diagnostic Register Bits
FF	None
POR	None
SE	None
EE	None
OT	None
TW	None
VS	VSU, VSO
VLO	None
ETO	None
VR	VRU, VRO
LDF	OC1, OC2, OC3, OL
BSU	VA, VB, VC
GSU	AHU, ALU, BHU, BLU, CHU, CLU
DSO	AHO, ALO, BHO, BLO, CHO, CLO

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APPLICATION INFORMATION

Dead-Time Selection

The choice of power MOSFET and external series gate resistance determines the selection of the dead time. The dead time, t_{DEAD}, should be made long enough to ensure that one MOSFET has stopped conducting before the complementary MOSFET starts conducting. This should also account for the tolerance and variation of the MOSFET gate capacitance, the series gate resistance, and the on-resistance of the driver in the A4911.

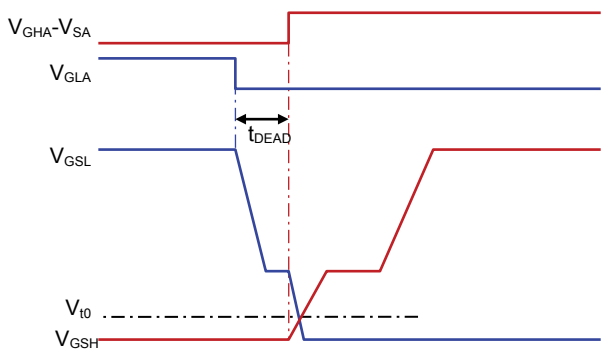

Figure 10: Minimum Dead Time

Figure 10 shows the typical switching characteristics of a pair of complementary MOSFETs. Ideally, one MOSFET should start to turn on just after the other has completely turned off. The point at which a MOSFET starts to conduct is the threshold voltage V_{t0}. The dead time should be long enough to ensure that the gate-source voltage of the MOSFET that is switching off is just below V_{t0} before the gate-source voltage of the MOSFET that is switching on rises to V_{t0}. This will be the minimum theoretical dead time, but in practice the dead time will have to be longer than this to accommodate variations in MOSFET and driver parameters for process variations and overtemperature.

Bootstrap Capacitor Selection

The A4911 requires three bootstrap capacitors: CA, CB, and CC. To simplify the description of bootstrap capacitor selection criteria, generic naming is used here. For example, C_{BOOT}, Q_{BOOT}, and V_{BOOT} refer to any of the three capacitors, and Q_{GATE} refers to any of the six associated MOSFETs. C_{BOOT} must be correctly selected to ensure proper operation of the device: too large and time will be wasted charging the capacitor, resulting in a limit on the maximum duty cycle and PWM frequency; too small and there can be a large voltage drop at the time the charge is transferred from C_{BOOT} to the MOSFET gate.

To keep the voltage drop due to charge sharing small, the charge in the bootstrap capacitor, Q_{BOOT}, should be much larger than Q_{GATE}, the charge required by the gate:

$$Q_{BOOT} \gg Q_{GATE}$$

A factor of 20 is a reasonable value, so

$$Q_{BOOT} = C_{BOOT} \times V_{BOOT} = Q_{GATE} \times 20$$

or

$$C_{BOOT} = \frac{Q_{GATE} \times 20}{V_{BOOT}}$$

where V_{BOOT} is the voltage across the bootstrap capacitor.

The voltage drop, ΔV, across the bootstrap capacitor as the MOSFET is being turned on, can be approximated by:

$$\Delta V = \frac{Q_{GATE}}{C_{BOOT}}$$

so for a factor of 20, ΔV will be 5% of V_{BOOT}.

The maximum voltage across the bootstrap capacitor under normal operating conditions is V_{REG}(max). However, in some circumstances, the voltage may transiently reach a maximum of 18 V, which is the clamp voltage of the Zener diode between the Cx terminal and the Sx terminal. In most applications with a good ceramic capacitor, the working voltage can be limited to 16 V.

Bootstrap Charging

It is good practice to ensure the high-side bootstrap capacitor is completely charged before a high-side PWM cycle is requested. The time required to charge the capacitor, t_{CHARGE}, in µs, is approximated by:

$$t_{CHARGE} = \frac{C_{BOOT} \times \Delta V}{100}$$

where C_{BOOT} is the value of the bootstrap capacitor in nF, and ΔV is the required voltage of the bootstrap capacitor. At power-up, and when the drivers have been disabled for a long time, the bootstrap capacitor can be completely discharged. In this case, ΔV can be considered to be the full high-side drive voltage, 12 V. Otherwise, ΔV is the amount of voltage dropped during the charge transfer, which should be 400 mV or less. The capacitor is charged whenever the Sx terminal is pulled low and current flows from VREG through the internal bootstrap diode circuit to C_{BOOT}.

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VREG Capacitor Selection

The internal reference, VREG, supplies current for the low-side gate-drive circuits and the charging current for the bootstrap capacitors. When a low-side MOSFET is turned on, the gate-drive circuit will provide the high transient current to the gate that is necessary to turn the MOSFET on quickly. This current, which can be several hundred milliamperes, cannot be provided directly by the limited output of the VREG regulator but must be supplied by an external capacitor, C_{REG}, connected between the VREG terminal and GND.

The turn-on current for the high-side MOSFET is similar in value but is mainly supplied by the bootstrap capacitor. However, the bootstrap capacitor must then be recharged from C_{REG} through the VREG terminal. Unfortunately, the bootstrap recharge can occur a very short time after the low-side turn-on occurs. This means that the value of C_{REG} between VREG and GND should be high enough to minimize the transient voltage drop on VREG for the combination of a low-side MOSFET turn-on and a bootstrap capacitor recharge.

For block commutation control (trapezoidal drive),where only one high side and one low side are switching during each PWM period, a minimum value of 20 × C_{BOOT} is reasonable. For sinusoidal control schemes, a minimum value of 40 × C_{BOOT} is recommended. As the maximum working voltage of C_{REG} will never exceed VREG, the capacitor voltage rating can be as low as 15 V. However, it is recommended that a capacitor rated to at least twice the maximum working voltage should be used to reduce any impact operating voltage may have on capacitance value. For best performance, C_{REG} should be ceramic rather than electrolytic. C_{REG} should be mounted as close to the VREG terminal as possible.

Braking

The A4911 can be used to perform dynamic braking by either forcing all low-side MOSFETs on and all high-side MOSFETs off or, inversely, by forcing all low-side off and all high-side on. This will effectively short-circuit the back EMF of the motor, creating a braking torque. During braking, the load current, I_{BRAKE}, can be approximated by:

$$I_{BRAKE} = \frac{V_{BEMF}}{R_L}$$

where V_{BEMF} is the voltage generated by the motor and R_L is the resistance of the phase winding. Care must be taken during braking to ensure that the power MOSFET maximum ratings are not exceeded. Dynamic braking is equivalent to slow decay with synchronous rectification and all phases enabled.

The A4911 can also be used to perform regenerative braking. This is equivalent to using fast decay with synchronous rectification. Note that the supply must be capable of managing the reverse current, for example, by connecting a resistive load or dumping the current to a battery or capacitor.

Current Sense Amplifier Configuration

Amplifier Gain, A_V, and output offset zero point voltage, V_{OOS}, may be set to a range of values by the SAG[2:0] and SAO[3:0] variables respectively as defined in the Current Sense Amplifiers section above. It is important that both values are selected to ensure the *absolute* voltage at the CSxO output, V_{CSO}, remains within the amplifier's dynamic range, V_{CSOUT}, and the input range of any downstream signal processing circuitry. Allowance must be made for both positive and negative current flows within the sense resistor.

With reference to Figure 1, the relationship between phase current I_{PH}, sense resistor value, R_S, and differential amplifier input voltage, V_{ID}, is given by:

$$V_{ID} = V_{CSP} - V_{CSM} = I_{PH} \times R_S$$

The current sense amplifier's output voltage on CSxO with respect to the programmed value of output offset on OOS is:

$$V_{CSD} = (V_{CSP} - V_{CSM}) \times A_V$$

The absolute voltage on CSxO with respect to ground is therefore:

$$V_{CSO} = [(V_{CSP} - V_{CSM}) \times A_V] + V_{OOS}$$

If, for example, the following parameter values are assumed :

R_S = 1 mΩ

I_{PH} = –20 to +40 A

A_V = 20 (SAG[2:0] = 0b010)

V_{OOS} = 1 V (SAO[3:0] = 0b1001)

V_{ID} ranges between –20 mV and 40 mV and V_{CSO} between 0.6 V and 1.8 V. V_{CSO} remains within the amplifier dynamic range, V_{CSOUT}, of 0.3 to 4.8 V. However, if A_V is increased to 50, V_{CSO}

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attempts to drive to 0 V and 3.0 V, the amplifier dynamic range limits are not complied with and the amplifier output saturates at its negative limit. This situation could be remedied by reducing A_V to 30 (0.4 V < V_{CSO} < 2.2 V) or increasing V_{OOS} to 1.5 V (0.5 V < V_{CSO} < 3.5 V).

Current Sense Amplifier Output Signals

As defined in Figure 1, the current sense amplifier output signals on the CSxO pins are internally referenced to the voltage on the OOS pin. Consequently, the signal voltages on CSxO should be measured differentially with respect to OOS (V_{CSD}). Alternatively, the voltages on both CSxO (V_{CSO}) and OOS (V_{OOS}) may be measured consecutively with respect to ground and the values subtracted to give the required output signal voltages as $V_{CSD} = V_{CSO} - V_{OOS}$.

The Input Offset Voltage, V_{IOS}, and the associated drift, ΔV_{IOS}, multiplied by the selected amplifier gain, A_V, represent the offset and offset drift limits that apply to V_{CSD}. The Output Offset Error limit, E_{VO}, and Output Offset Drift limit, V_{OOSD}, apply directly to V_{OOS}. E_{VO} and V_{OOSD} do not affect current sense output accuracy.

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INPUT/OUTPUT STRUCTURES

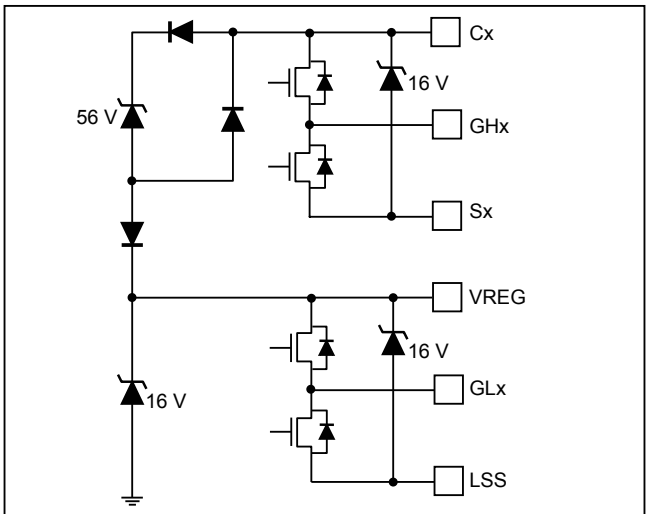

Figure 11a: Gate Drive Outputs

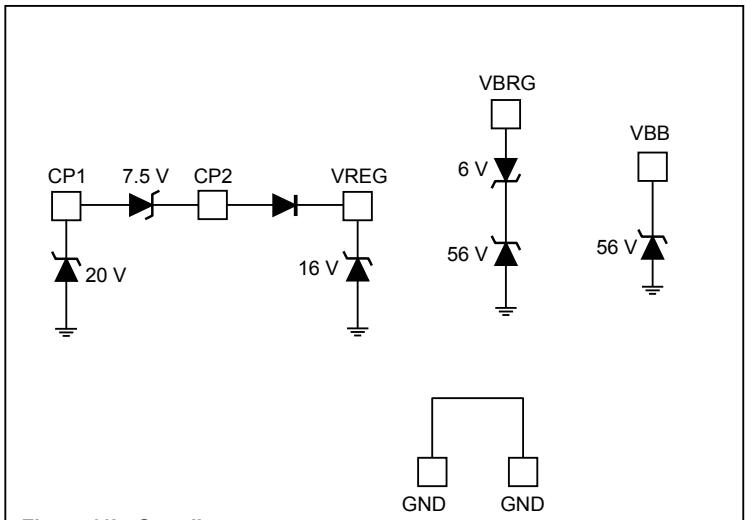

Figure 11b: Supplies

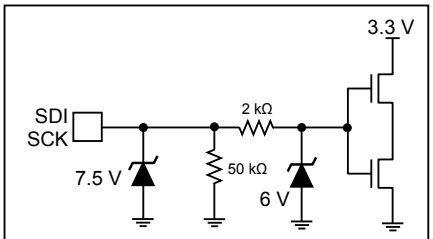

Figure 11c: SDI, SCK Inputs

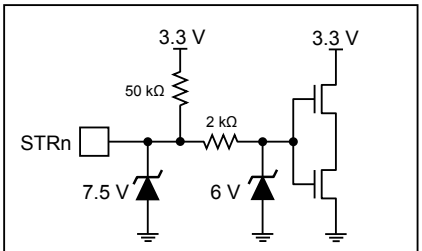

Figure 11d: STRn Input

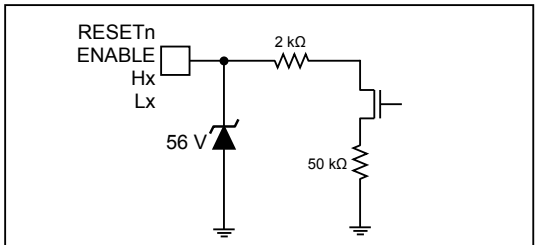

Figure 11e: RESETn, ENABLE, Hx, and Lx Inputs

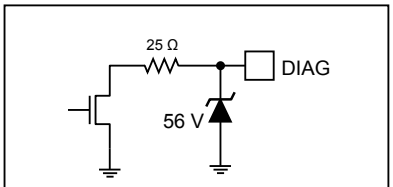

Figure 11f: DIAG Output

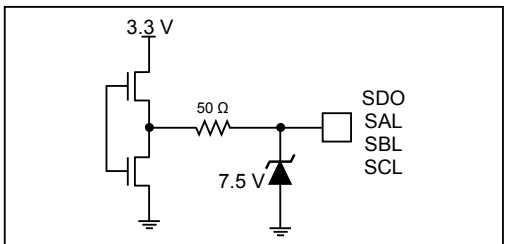

Figure 11g: SDO, SxL Outputs

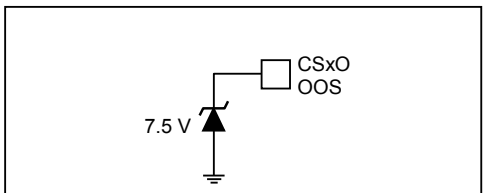

Figure 11h: CSxO, OOS Outputs

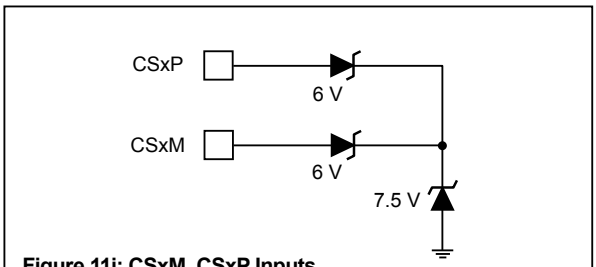

Figure 11i: CSxM, CSxP Inputs

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LAYOUT RECOMMENDATIONS

Careful consideration must be given to PCB layout when designing high-frequency, fast-switching, high-current circuits:

• The two A4911 ground terminals, both designated GND, are internally connected but must also be connected together on the PCB close to the device for correct operation. This common point should return separately to the negative side of the motor supply filtering capacitor. This will minimize the effect of switching noise on the device logic and analog reference.

• The exposed thermal pad should be connected to the common point of the two GND terminals.

• Minimize stray inductance by using short, wide copper traces at the drain and source terminals of all power MOSFETs. This includes motor lead connections, the input power bus, and the common source of the low-side power MOSFETs. This will minimize voltages induced by fast switching of large load currents.

• Consider the addition of small (100 nF) ceramic decoupling capacitors across the source and drain of the power MOSFETs to limit fast transient voltage spikes caused by PCB trace inductance.

• Keep the gate discharge return connections Sx and LSSx as short as possible. Any inductance on these traces will cause negative transitions on the corresponding A4911 terminals, which may exceed the absolute maximum ratings. If this is likely, consider the use of clamping diodes to limit the negative excursion on these terminals with respect to the GND terminals.

• Supply decoupling, typically a 100 nF ceramic capacitor, should be connected between VBB and GND as close to the A4911 terminals as possible.

• Check the peak voltage excursion of the transients on the LSSx terminals with reference to the GND terminals using a close-grounded ('tip and barrel') probe. If the voltage at any LSSx terminal exceeds the absolute maximum in the datasheet, add additional clamping and/or capacitance between the LSSx terminal and the GND terminals.

• Gate charge drive paths and gate discharge return paths may carry a large transient current pulse. Therefore the traces from GHx, GLx, Sx, and LSSx (x = A, B, or C) should be as short as possible to reduce trace inductance.

• Provide an independent connection from each LSSx terminal to the source of the corresponding low-side MOSFET in the power bridge. Connection of the LSSx terminals directly to the GND terminals is not recommended as this may inject noise into sensitive functions such as the various voltage monitors.

• The inputs to the sense amplifiers, CSxP and CSxM, should take the form of independent traces and for best results should be matched in length and route.

• A low-cost diode can be placed in the connection to VBB to provide reverse-battery protection. In reverse-battery conditions, it is possible to use the body diodes of the power MOSFETs to clamp the reverse voltage to approximately 4 V. In this case, the additional diode in the VBB connection will prevent damage to the A4911 and the VBRG input will survive the reverse voltage.

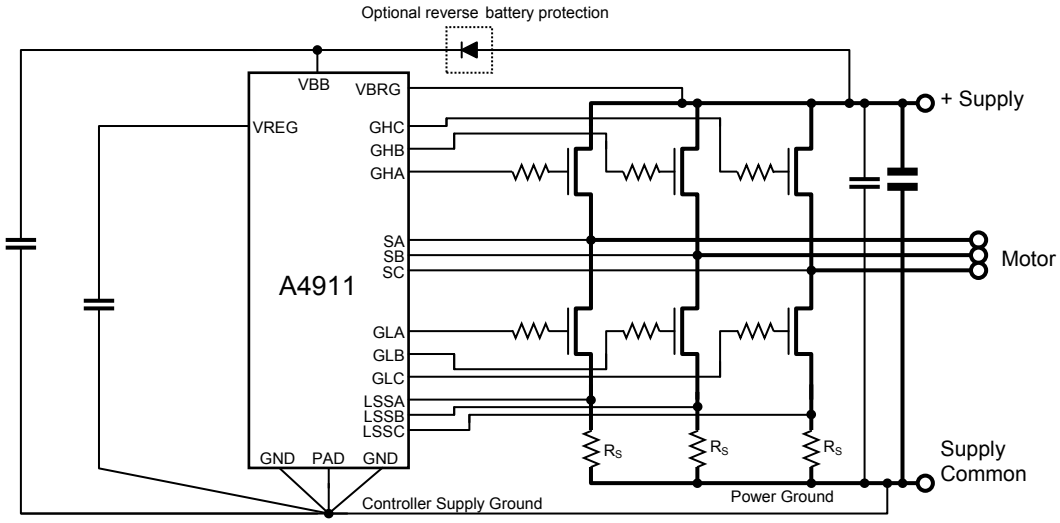

Figure 12: Supply Routing Suggestions

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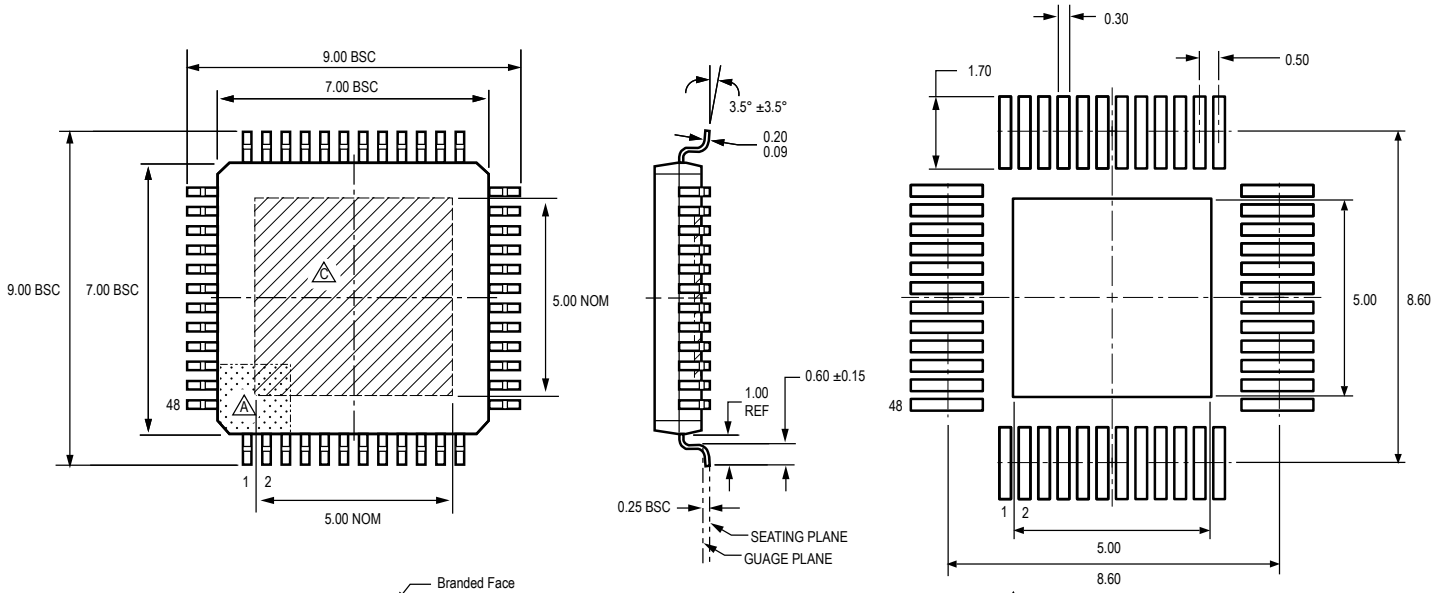
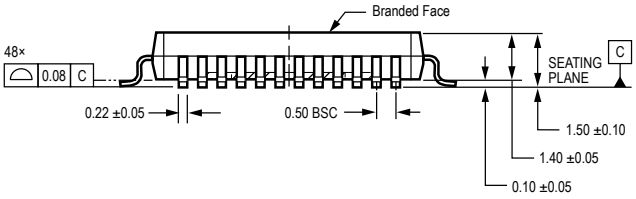
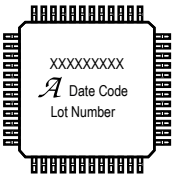
Package JP, 48-Pin LQFP
with Exposed Thermal Pad

For Reference Only – Not for Tooling Use

(Reference Allegro DWG-0000386, Rev. 5 or JEDEC MS-026 BBCHD)
NOT TO SCALE
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown







A Terminal #1 mark area

B Reference land pattern layout (reference IPC7351 QFP50P900X900X160-48M); adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

C Exposed thermal pad (bottom surface); exact dimensions may vary with device

D Branding scale and appearance at supplier discretion

D Standard Branding Reference View
Line 1, 2, 3: Maximum 9 characters per line

Line 1: Part Number
Line 2: Logo A, 4-digit Date Code
Line 3: Assembly Lot Number

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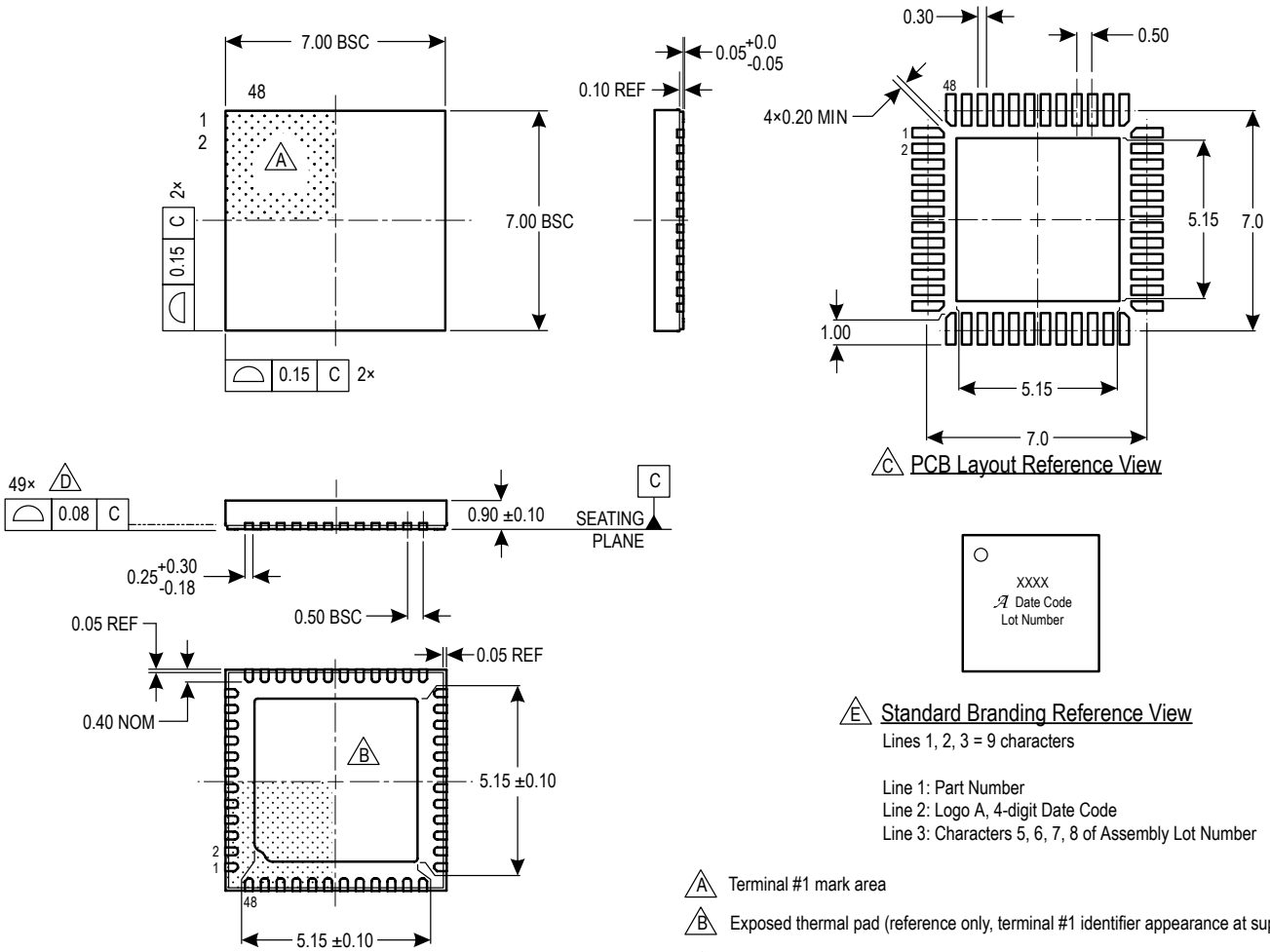
Package EV, 48-Pin QFN

with Exposed Thermal Pad and Wettable Flank

For Reference Only – Not for Tooling Use

(Reference DWG-0000378, Rev. 3)
Dimensions in millimeters
NOT TO SCALE
Exact case and lead configuration at supplier discretion within limits shown



E Standard Branding Reference View

Lines 1, 2, 3 = 9 characters

Line 1: Part Number
Line 2: Logo A, 4-digit Date Code
Line 3: Characters 5, 6, 7, 8 of Assembly Lot Number

A Terminal #1 mark area

B Exposed thermal pad (reference only, terminal #1 identifier appearance at supplier discretion)

C Reference land pattern layout (reference IPC7351 QFN50P700X700X100-49M); all pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

D Coplanarity includes exposed thermal pad and terminals

E Branding scale and appearance at supplier discretion

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Revision History

Number	Date	Description
–	June 19, 2017	Initial release
1	July 17, 2017	Updated Output Current Sink min value (p. 9), VBB POR Voltage Hysteresis min and max values (p. 10), VBRG Open Threshold max value (p. 12)
2	August 14, 2017	Updated Selection Guide (p. 2)
3	September 1, 2017	Updated Pull-Up On-Resistance (p. 7)
4	June 20, 2018	Corrected Package Drawing (p. 65)
5	July 11, 2019	Minor editorial updates
6	June 11, 2020	Updated Bridge Phase State Monitor section (p. 34)
7	June 3, 2022	Updated package drawings (pages 64-65) and minor editorial updates
8	December 1, 2022	Updated selection guide table (page 2), common-mode rejection minimum value (page 10), and high-side VDS threshold offset minimum and maximum values (page 11)
9	June 21, 2023	Updated selection guide table (page 2)
10	September 3, 2024	Updated selection guide table (page 2) and corrected web status
11	June 13, 2025	Updated ASIL logo and text (pages 1-2)

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