



#### **DUAL N CHANNEL ENHANCEMENT MODE MOSFET**

## **Product Summary**

Device	BV <sub>DSS</sub>	R <sub>DS(ON)</sub> MAX	I <sub>D MAX</sub> T <sub>A</sub> = +25°C
N-Channel	60V	17mΩ @ V <sub>GS</sub> = 10V	8.8A
in-Channel	607	26mΩ @ V <sub>GS</sub> = 4.5V	6.9A

## **Description**

This new generation MOSFET is designed to minimize the on-state resistance ( $R_{DS(ON)}$ ) and yet maintain superior switching performance, making it ideal for high efficiency power management applications.

## **Applications**

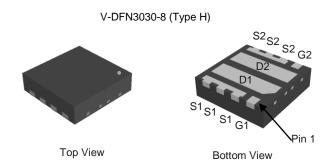
- Power Management Functions
- Analog Switch

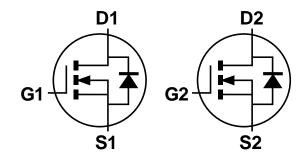
## **Features**

- Low On-Resistance
- Low Input Capacitance
- Fast Switching Speed
- Low Input/Output Leakage
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)

### **Mechanical Data**

- Case: V-DFN3030-8 (Type H)
- Case Material: Molded Plastic, "Green" Molding Compound.
   UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections: See Diagram
- Terminals: Finish NiPdAu Over Copper Leadframe. Solderable per MIL-STD-202, Method 208 @4)
- Weight: 0.02 grams (Approximate)





**Equivalent Circuit** 

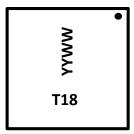
## **Ordering Information** (Note 4)

Part Number	Case	Packaging
DMT6018LDR-7	V-DFN3030-8 (Type H)	3000/Tape & Reel
DMT6018LDR-13	V-DFN3030-8 (Type H)	10000/Tape & Reel

Notes:

- 1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
- See http://www.diodes.com/quality/lead\_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
- 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
- 4. For packaging details, go to our website at http://www.diodes.com/products/packages.html.

# **Marking Information**



T18 = Product Type Marking Code YYWW = Date Code Marking YY = Last Two Digits of Year (ex: 16 for 2016) WW = Week Code (01 to 53)



## Absolute Maximum Ratings (@TA = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit		
Drain-Source Voltage	$V_{DSS}$	60	V		
Gate-Source Voltage			$V_{GSS}$	±20	V
Continuous Dusin Courset (Alata C) // 40//	Steady State	$T_A = +25^{\circ}C$ $T_A = +70^{\circ}C$	I <sub>D</sub>	8.8 7.1	А
Continuous Drain Current (Note 6) V <sub>GS</sub> = 10V	t<10s	$T_A = +25$ °C $T_A = +70$ °C	I <sub>D</sub>	11.4 9.1	А
Maximum Continuous Body Diode Forward Current (Note 6)			I <sub>S</sub>	3	Α
Pulsed Drain Current (10µs Pulse, Duty Cycle = 1%)			I <sub>DM</sub>	50	Α
Avalanche Current (Note 7) L = 1mH			I <sub>AS</sub>	8	Α
Avalanche Energy (Note 7) L = 1mH	E <sub>AS</sub>	32	mJ		

# Thermal Characteristics (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit		
Total Power Dissipation (Note 5)	$T_A = +25^{\circ}C$	٦	1.1	W	
Total Power Dissipation (Note 5)	$T_A = +70^{\circ}C$	$P_{D}$	0.7		
Thermal Resistance, Junction to Ambient (Note 5)	Steady State	$R_{\theta,JA}$	108	°C/W	
Thermal Resistance, Junction to Ambient (Note 5)	t<10s	КөЈА	65		
Total Power Dissipation (Note 6)	$T_A = +25$ °C	$P_{D}$	1.9	W	
Total Fower Dissipation (Note 6)	$T_A = +70^{\circ}C$	FD	1.2	VV	
Thermal Resistance, Junction to Ambient (Note 6)	Steady State	D	66		
Thermal Resistance, Junction to Ambient (Note o)	t<10s	$R_{\theta JA}$	40	°C/W	
Thermal Resistance, Junction to Case (Note 6)		$R_{ heta JC}$	11.4		
Operating and Storage Temperature Range	_	$T_{J}$ , $T_{STG}$	-55 to +150	°C	

# Electrical Characteristics (@T<sub>A</sub> = +25°C, unless otherwise specified.)

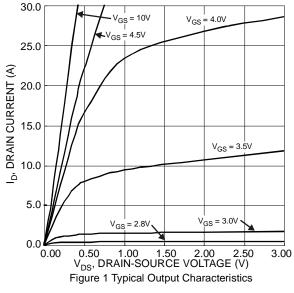
Characteristic		Min	Тур	Max	Unit	Test Condition	
OFF CHARACTERISTICS (Note 8)							
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	60	-	-	V	$V_{GS} = 0V, I_D = 250\mu A$	
Zero Gate Voltage Drain Current T <sub>J</sub> = +25°C		-	-	1.0	μΑ	$V_{DS} = 48V, V_{GS} = 0V$	
Gate-Source Leakage	I <sub>GSS</sub>	-	-	±100	nA	$V_{GS} = \pm 20V$ , $V_{DS} = 0V$	
ON CHARACTERISTICS (Note 8)							
Gate Threshold Voltage	V <sub>GS(TH)</sub>	1.0	-	3.0	V	$V_{DS} = V_{GS}, I_D = 250 \mu A$	
Static Drain-Source On-Resistance	R <sub>DS(ON)</sub>	_	13 20	17 26	mΩ	$V_{GS} = 10V, I_D = 8.2A$	
Statio Brain Course on reconstance	TOS(ON)				11122	$V_{GS} = 4.5V, I_D = 6.7A$	
Diode Forward Voltage	$V_{SD}$	-	0.75	-	V	$V_{GS} = 0V, I_{S} = 1A$	
DYNAMIC CHARACTERISTICS (Note 9)							
Input Capacitance	C <sub>iss</sub>	-	869	-	рF	V 00V V 0V	
Output Capacitance	Coss	-	226	-	pF	$V_{DS} = 30V, V_{GS} = 0V,$ f = 1.0MHz	
Reverse Transfer Capacitance	C <sub>rss</sub>	-	15	-	pF		
Gate Resistance	Rg	-	1.1	-	Ω	$V_{DS} = 0V$ , $V_{GS} = 0V$ , $f = 1MHz$	
Total Gate Charge (V <sub>GS</sub> = 4.5V)	$Q_g$	-	6.2	-	nC		
Total Gate Charge (V <sub>GS</sub> = 10V)	$Q_{g}$	-	13.9	-	nC	],, 20,, 1 0.24	
Gate-Source Charge	Q <sub>gs</sub>	-	3.0	-	nC	$V_{DS} = 30V, I_{D} = 8.2A$	
Gate-Drain Charge	$Q_{gd}$	-	1.9	-	nC		
Turn-On Delay Time	t <sub>D(ON)</sub>	-	3.5	-	ns		
Turn-On Rise Time	t <sub>R</sub>	-	4.6	-	ns	$V_{DD} = 30V, V_{GS} = 10V,$ $I_{D} = 8.2A, R_{g} = 6\Omega$	
Turn-Off Delay Time	t <sub>D(OFF)</sub>	-	10.8	-	ns		
Turn-Off Fall Time	t <sub>F</sub>	-	3.5	-	ns		
Reverse Recovery Time	t <sub>RR</sub>	-	20.3	-	ns	I <sub>F</sub> = 8.2A, di/dt = 100A/μs	
Reverse Recovery Charge	$Q_{RR}$	-	11.4	=	nC	$I_F = 8.2A$ , di/dt = 100A/ $\mu$ s	

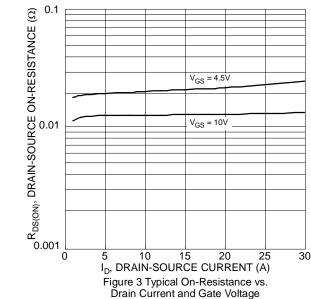
5. Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout. 6. Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate. 7.  $I_{AS}$  and  $E_{AS}$  ratings are based on low frequency and duty cycles to keep  $T_{J}$  = +25°C.

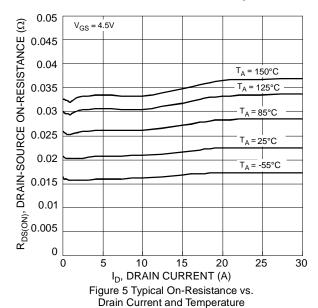
<sup>8.</sup> Short duration pulse test used to minimize self-heating effect.

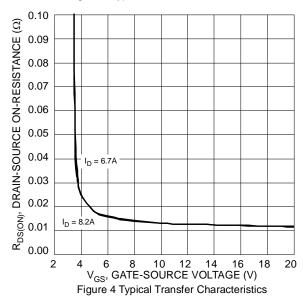
<sup>9.</sup> Guaranteed by design. Not subject to product testing.











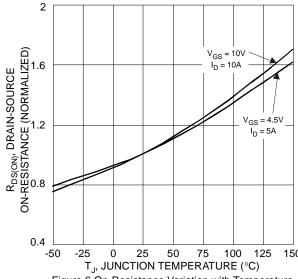
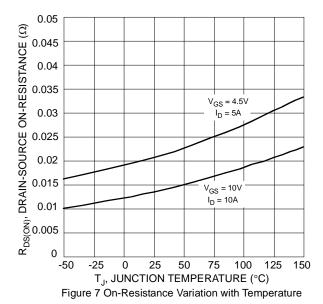
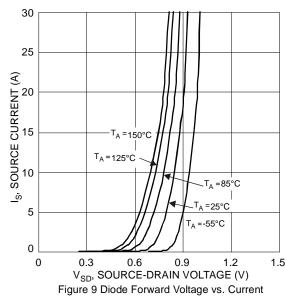
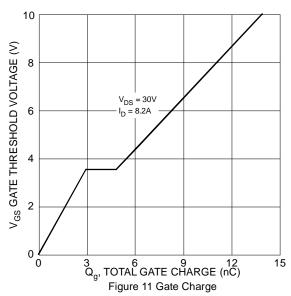


Figure 6 On-Resistance Variation with Temperature









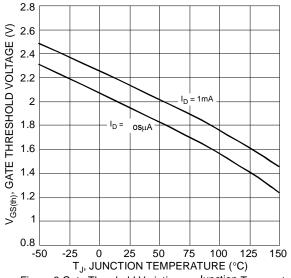
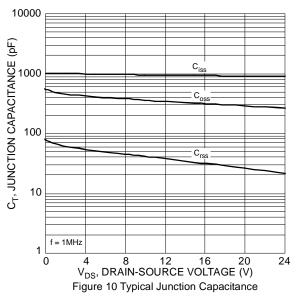
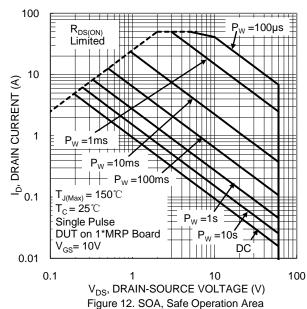
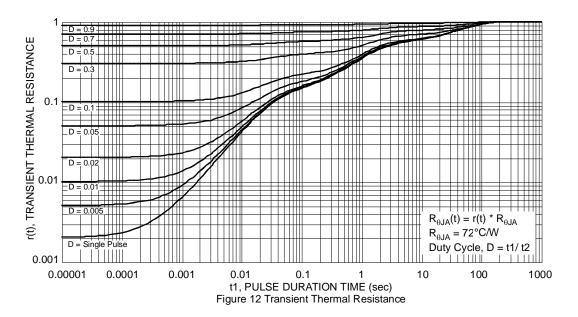


Figure 8 Gate Threshold Variation vs. Junction Temperature





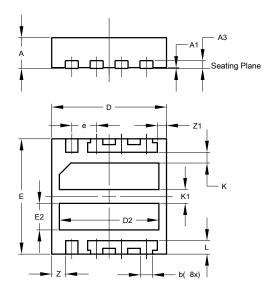




# **Package Outline Dimensions**

Please see http://www.diodes.com/package-outlines.html for the latest version.

### V-DFN3030-8 (Type H)



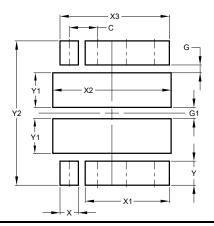
V-DFN3030-8						
(Type H)						
Dim	Min Max Ty					
Α	0.75	0.85	0.80			
A1	0	0.05	0.02			
A3	0.	203 BS	C			
b	0.27	0.37	0.32			
D	2.95	3.05	3.00			
D2	2.50	2.50 2.70 2.6				
е	0	.65 BS	С			
Е	2.95 3.05		3.00			
E2	0.59	0.79	0.69			
L	0.30 0.40 0.35					
K	K 0.28 BSC					
K1	0.36 BSC					
Z	0.365 BSC					
<b>Z</b> 1	0.24 BSC					
All Dimensions in mm						



## **Suggested Pad Layout**

Please see http://www.diodes.com/package-outlines.html for the latest version.

#### V-DFN3030-8 (Type H)



Dimensions	Value (in mm)			
С	0.650			
G	0.180			
G1	0.260			
Х	0.420			
X1	1.920			
X2	2.700			
Х3	2.495			
Y	0.550			
Y1	0.790			
Y2	3.300			

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