Off-Line PWM Controllers with Integrated Power MOSFET

STR3A100 Series

General Descriptions

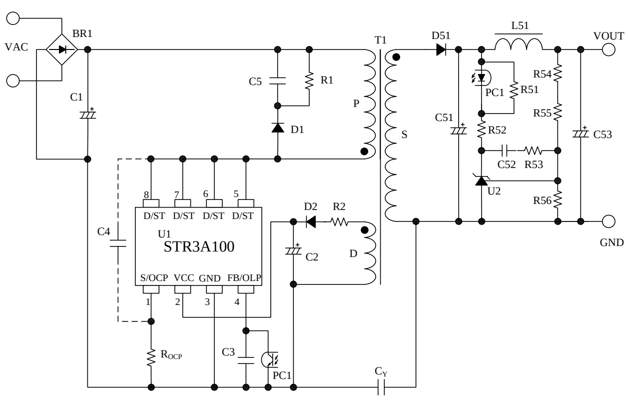
The STR3A100 series are power ICs for switching power supplies, incorporating a MOSFET and a current mode PWM controller IC.

The low standby power is accomplished by the automatic switching between the PWM operation in normal operation and the burst-oscillation under light load conditions. The product achieves high cost-performance power supply systems with few external components.

Features

- Low Thermal Resistance Package
- Current Mode Type PWM Control
- Soft Start Function
- No Load Power Consumption < 15mW
- Auto Standby Function
  Normal Operation ----------------------------- PWM Mode
  Standby---------------------------- Burst Oscillation Mode
- Random Switching Function
- Slope Compensation Function
- Leading Edge Blanking Function
- Bias Assist Function
- Protections
  ・Two Types of Overcurrent Protection (OCP); Pulse-by-Pulse, built-in compensation circuit to minimize OCP point variation on AC input voltage
  ・Overload Protection (OLP); auto-restart
  ・Overvoltage Protection (OVP); latched shutdown or auto-restart
  ・Thermal Shutdown Protection (TSD); latched shutdown or auto-restart

Typical Application Circuit



Package

DIP8

Not to Scale

Lineup

- Electrical Characteristics

Products	$f_{OSC(AVG)}$	V_{DSS} (min.)	OVP /TSD
STR3A1××	67 kHz	650 V	Latched shutdown
STR3A1××D	67 kHz	650 V	Auto restart
STR3A1××HD	100 kHz	700 V	Auto restart

- MOSFET ON Resistance and Output Power, P_{OUT}*

Products	$R_{DS(ON)}$ (max.)	P_{OUT} (Adapter)		P_{OUT} (Open frame)	
		AC230V	AC85 ~265V	AC230V	AC85 ~265V
$f_{OSC(AVG)}$ = 67 kHz					
STR3A151 / STR3A151D	4.0 Ω	29.5 W	19.5 W	37 W	23 W
STR3A152 / STR3A152D	3.0 Ω	33 W	23.5 W	45 W	29 W
STR3A153 / STR3A153D	1.9 Ω	37 W	27.5 W	53 W	35 W
STR3A154 / STR3A154D	1.4 Ω	41 W	31 W	60 W	40 W
STR3A155 / STR3A155D	1.1 Ω	45 W	35 W	65 W	44 W
$f_{OSC(AVG)}$ = 100 kHz					
STR3A161HD	4.2 Ω	25 W	20 W	36 W	24 W
STR3A162HD	3.2 Ω	28 W	23 W	40 W	28 W
STR3A163HD	2.2 Ω	32 W	25.5 W	46 W	33.5 W

* The output power is actual continues power that is measured at 50 °C ambient. The peak output power can be 120 to 140 % of the value stated here. Core size, ON Duty, and thermal design affect the output power. It may be less than the value stated here.

Applications

- Low power AC/DC adapter
- White goods
- Auxiliary power supply
- Other SMPS

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1. Absolute Maximum Ratings

- The polarity value for current specifies a sink as "+," and a source as "−," referencing the IC.
- Unless otherwise specified T_A = 25 °C, 5 pin = 6 pin = 7 pin = 8 pin

Parameter	Symbol	Test Conditions	Pins	Rating	Units	Notes
Drain Peak Current[1]	I_{DPEAK}	Single pulse	8 – 1	3.6	A	3A151 / 51D / 61HD
				4		3A152 / 52D / 62HD
				4.8		3A163HD
				5.2		3A153 / 53D
				6.4		3A154 / 54D
				7.2		3A155 / 55D
Avalanche Energy[2][3]	E_{AS}	I_{LPEAK} = 2.13 A	8 – 1	53	mJ	3A151 / 51D
		I_{LPEAK} = 2.19 A		56		3A152 / 52D
		I_{LPEAK} = 2.46 A		72		3A153 / 53D
		I_{LPEAK} = 2.66 A		83		3A154 / 54D
		I_{LPEAK} = 3.05 A		110		3A155 / 55D
		I_{LPEAK} = 1.43 A		23.8		3A161HD
		I_{LPEAK} = 1.58 A		29		3A162HD
		I_{LPEAK} = 1.88 A		41		3A163HD
S/OCP Pin Voltage	$V_{S/OCP}$		1 − 3	− 2 to 6	V	
VCC Pin Voltage	V_{CC}		2 − 3	32	V	
FB/OLP Pin Voltage	V_{FB}		4 − 3	− 0.3 to 14	V	
FB/OLP Pin Sink Current	I_{FB}		4 − 3	1.0	mA	
MOSFET Power Dissipation[4]	P_{D1}	[5]	8 – 1	1.68	W	3A151 / 51D / 52 / 52D / 61HD / 62HD
				1.76		3A153 / 53D / 54 / 54D / 63HD
				1.81		3A155 / 55D
Control Part Power Dissipation	P_{D2}		2 – 3	1.3	W	$V_{CC} \times I_{CC}$
Operating Ambient Temperature	T_{OP}		—	− 40 to 115	°C	
Storage Temperature	T_{stg}		—	− 40 to 125	°C	
Junction Temperature	T_{ch}		—	150	°C	

[1] Refer to 3.2 MOSFET Safe Operating Area Curves
[2] Refer to Figure 3-2 Avalanche Energy Derating Coefficient Curve
[3] Single pulse, V_{DD} = 99 V, L = 20 mH
[4] Refer to Section 3.3 Ta-P_{D1} Curve
[5] When embedding this hybrid IC onto the printed circuit board (cupper area in a 15 mm × 15 mm)

2. Electrical Characteristics

- The polarity value for current specifies a sink as "+," and a source as "−," referencing the IC.
- Unless otherwise specified, T_A = 25 °C, V_{CC} = 18 V, 5 pin = 6 pin = 7 pin = 8 pin

Parameter	Symbol	Test Conditions	Pins	Min.	Typ.	Max.	Units	Notes
Power Supply Startup Operation								
Operation Start Voltage	$V_{CC(ON)}$		2 − 3	13.8	15.3	16.8	V	
Operation Stop Voltage[1]	$V_{CC(OFF)}$		2 − 3	7.3	8.1	8.9	V	
Circuit Current in Operation	$I_{CC(ON)}$	V_{CC}= 12V	2 − 3	−	−	2.5	mA	
Startup Circuit Operation Voltage	$V_{ST(ON)}$		8 − 3	−	40	−	V	
Startup Current	$I_{STARTUP}$	V_{CC}= 13.5V	2 − 3	− 3.9	− 2.5	− 1.1	mA	
Startup Current Biasing Threshold Voltage	$V_{CC(BIAS)}$		2 − 3	8.5	9.5	10.5	V	
Normal Operation								
Average Switching Frequency	$f_{OSC(AVG)}$		8 − 3	60	67	74	kHz	3A15× 3A15×D
				90	100	110		3A16×HD
Switching Frequency Modulation Deviation	Δf		8 − 3	−	5	−	kHz	3A15× 3A15×D
				−	8	−		3A16×HD
Maximum ON Duty	D_{MAX}		8 − 3	65	74	83	%	3A15× 3A15×D
				77	83	89		3A16×HD
Protection Function								
Leading Edge Blanking Time	t_{BW}		−	−	350	−	ns	3A15× 3A15×D
				−	280	−		3A16×HD
OCP Compensation Coefficient	DPC		−	−	17	−	mV/μs	3A15× 3A15×D
				−	27	−		3A16×HD
OCP Compensation ON Duty	D_{DPC}		−	−	36	−	%	
OCP Threshold Voltage at Zero ON Duty	$V_{OCP(L)}$		1 − 3	0.69	0.78	0.87	V	
OCP Threshold Voltage at 36% ON Duty	$V_{OCP(H)}$		1 − 3	0.79	0.88	0.97	V	
Maximum Feedback Current	$I_{FB(MAX)}$		4 − 3	− 110	− 70	− 35	μA	
Minimum Feedback Current	$I_{FB(MIN)}$		4 − 3	− 30	− 15	− 7	μA	
FB/OLP pin Oscillation Stop Threshold Voltage	$V_{FB(OFF)}$	V_{CC}=32V	4 − 3	1.09	1.21	1.33	V	3A151 / 51D / 52 / 52D / 53 / 53D / 61HD / 62HD / 63HD
				0.85	0.98	1.09		3A154 / 54D / 55 / 55D
OLP Threshold Voltage	$V_{FB(OLP)}$	V_{CC}= 32V	4 − 3	7.3	8.1	8.9	V	
OLP Operation Current	$I_{CC(OLP)}$	V_{CC}= 12V	2 − 3	−	230	−	μA	
OLP Delay Time	t_{OLP}		−	54	70	86	ms	

[1] $V_{CC(BIAS)} > V_{CC(OFF)}$ always.

Parameter	Symbol	Test Conditions	Pins	Min.	Typ.	Max.	Units	Notes
FB/OLP Pin Clamp Voltage	$V_{FB(CLAMP)}$		4 − 3	11.0	12.8	14.0	V	
OVP Threshold Voltage	$V_{CC(OVP)}$		2 − 3	27.5	29.5	31.5	V	
Thermal Shutdown Operating Temperature	$T_{j(TSD)}$		−	135	−	−	°C	
MOSFET								
Drain-to-Source Breakdown Voltage	V_{DSS}		8 – 1	650	−	−	V	3A15× 3A15×D
				700	−	−		3A16×HD
Drain Leakage Current	I_{DSS}		8 – 1	−	−	300	μA	
On Resistance	$R_{DS(ON)}$	I_{DS} = 0.4A	8 − 1	−	−	4.2	Ω	3A161HD
				−	−	4.0		3A151 / 51D
				−	−	3.2		3A162HD
				−	−	3.0		3A152 / 52D
				−	−	2.2		3A163HD
				−	−	1.9		3A153 / 53D
				−	−	1.4		3A154 / 54D
				−	−	1.1		3A155 / 55D
Switching Time	t_f		8 – 1	−	−	250	ns	
Thermal Resistance								
Channel to Frame	θ_{ch-F}		−	−	−	16	°C/W	
Channel to Case Thermal Resistance[2]	θ_{ch-C}		−	−	−	18	°C/W	3A151 / 51D / 52 / 52D / 53 / 53D / 61HD / 62HD / 63HD
				−	−	17		3A154 / 54D / 55 / 55D

[2] θ_{ch-C} is thermal resistance between channel and case. Case temperature (T_C) is measured at the center of the case top surface.

3. Performance Curves

3.1 Derating Curves

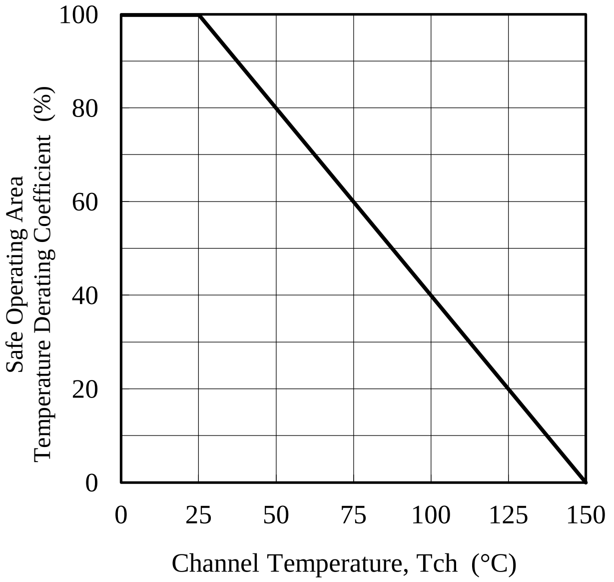


Figure 3-1 SOA Temperature Derating Coefficient Curve

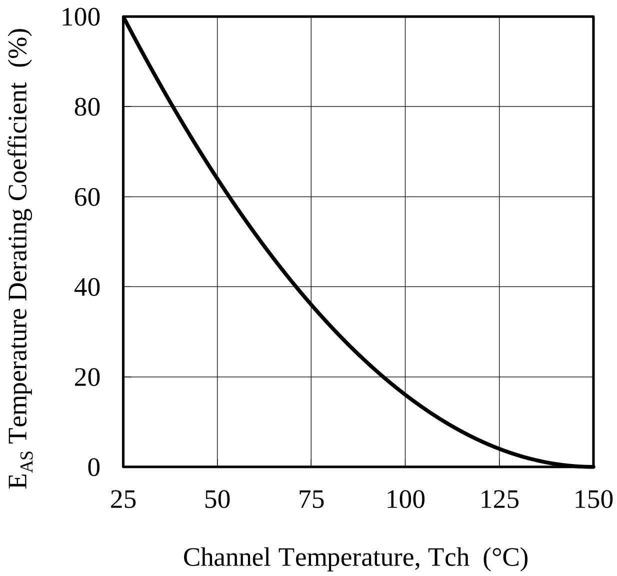
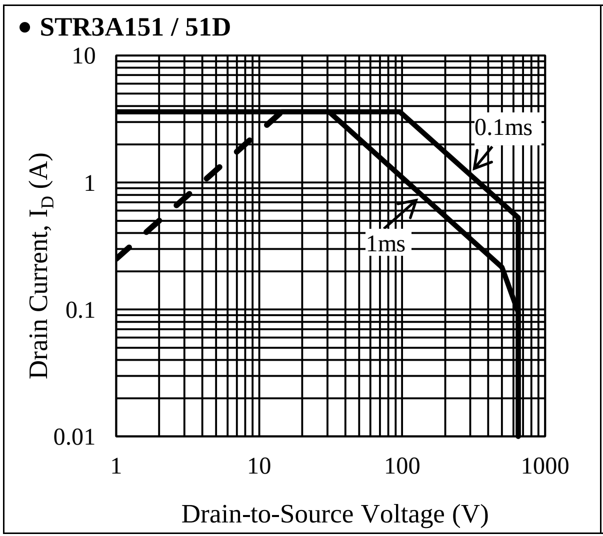
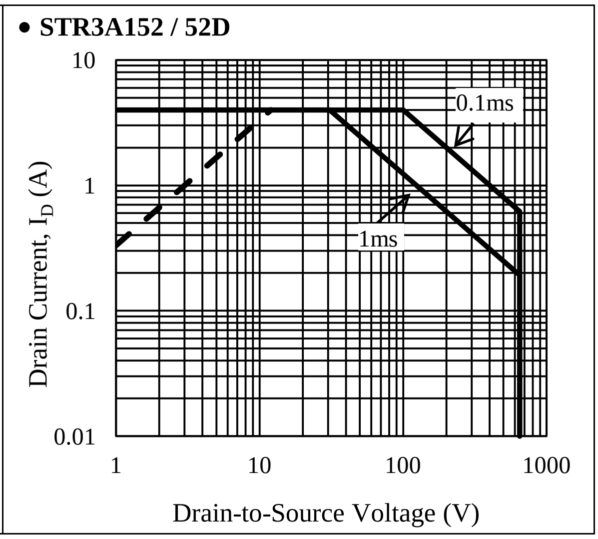


Figure 3-2 Avalanche Energy Derating Coefficient Curve

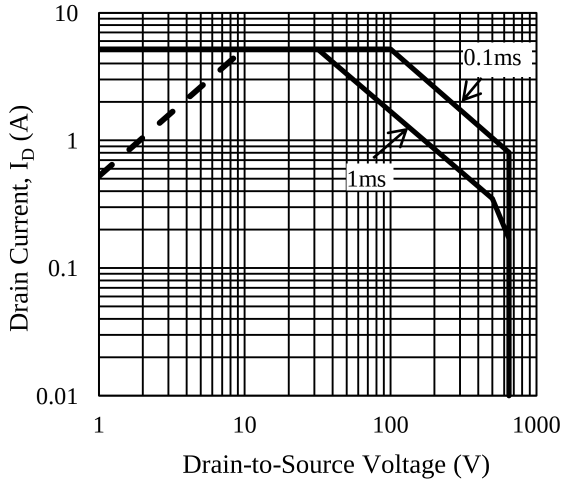
3.2 MOSFET Safe Operating Area Curves

- When the IC is used, the safe operating area curve should be multiplied by the temperature derating coefficient derived from Figure 3-1.
- The broken line in the safe operating area curve is the drain current curve limited by on-resistance.
- Unless otherwise specified, T_A = 25 °C, Single pulse

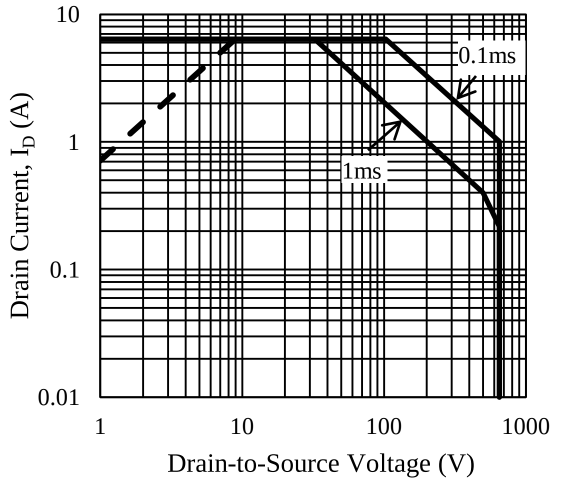




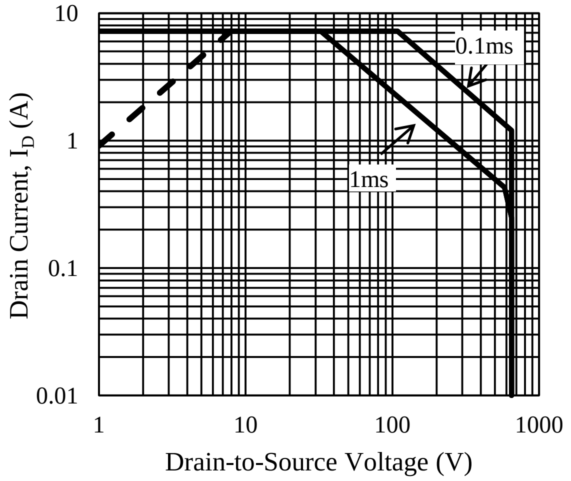
• **STR3A153 / 53D**



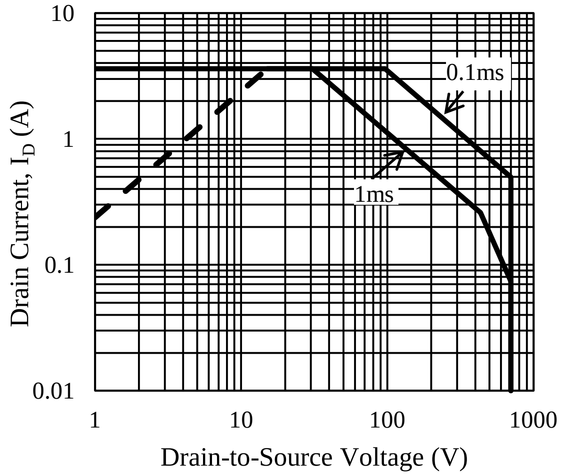
• **STR3A154 / 54D**



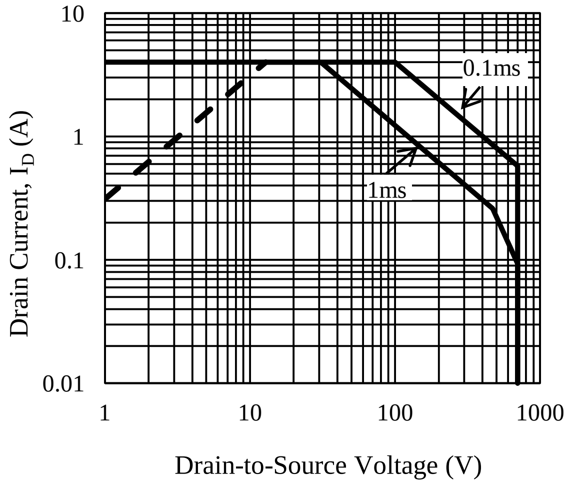
• **STR3A155 / 55D**



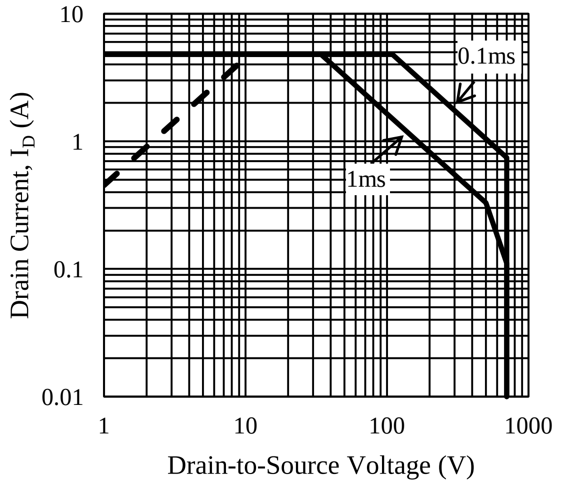
• **STR3A161HD**



• **STR3A162HD**

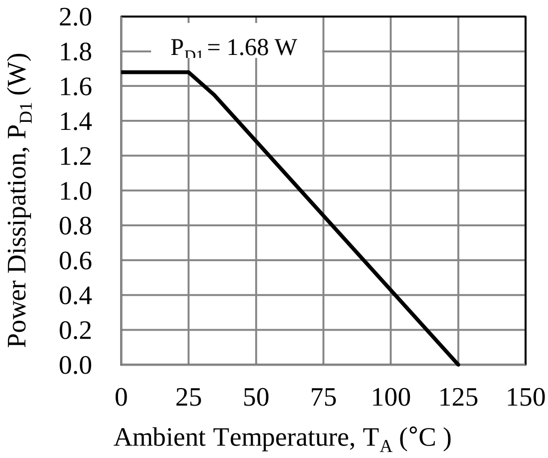


• **STR3A163HD**

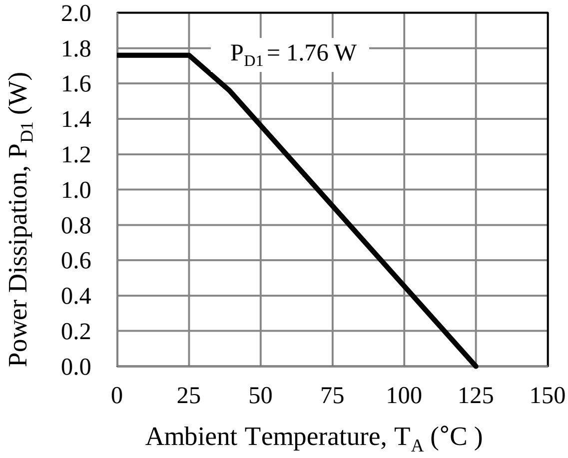


3.3 Ambient Temperature versus Power Dissipation Curves

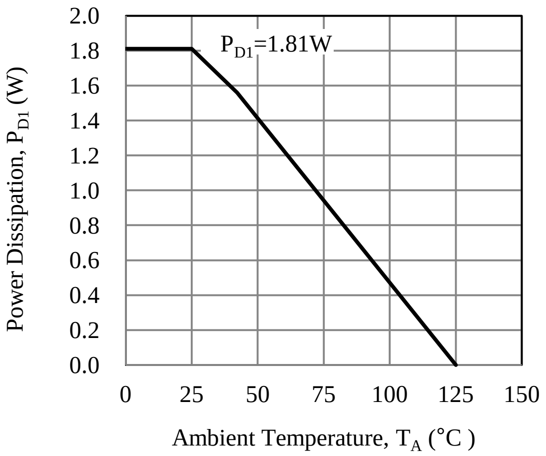
• STR3A151 / 51D / 52 / 52D / 61HD / 62HD



• STR3A153 / 53D / 54 / 54D / 63HD

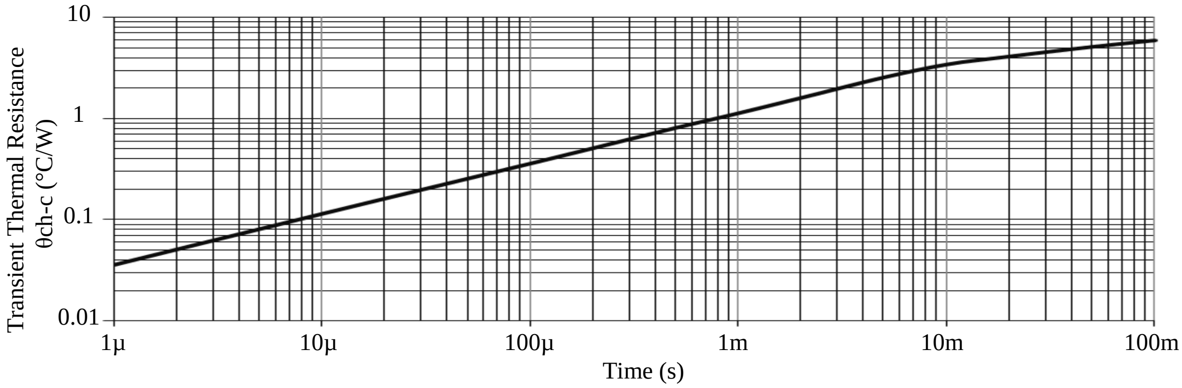


• STR3A155 / 55D

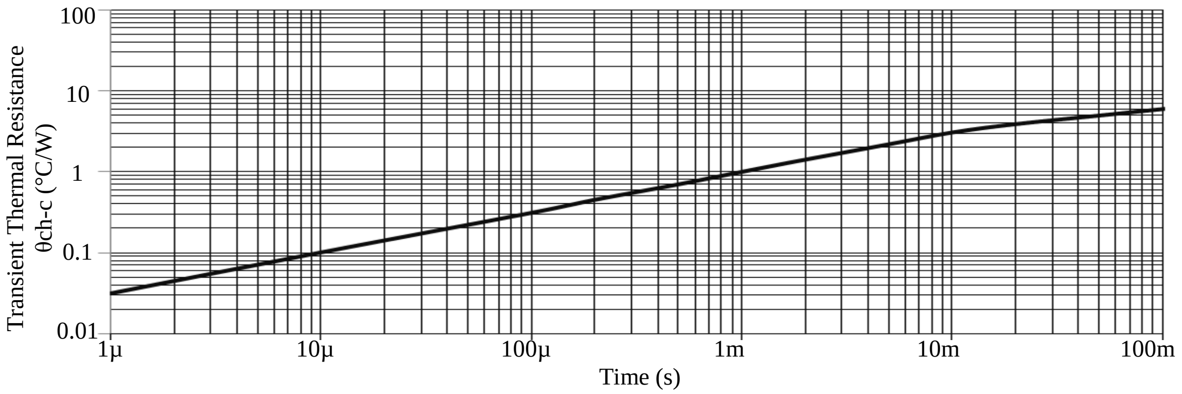


3.4 Transient Thermal Resistance Curves

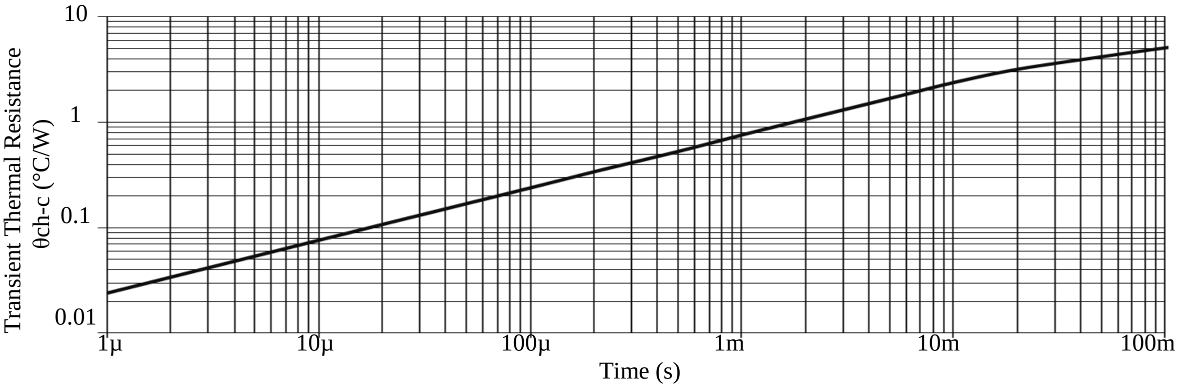
• STR3A151 / 51D / 61HD



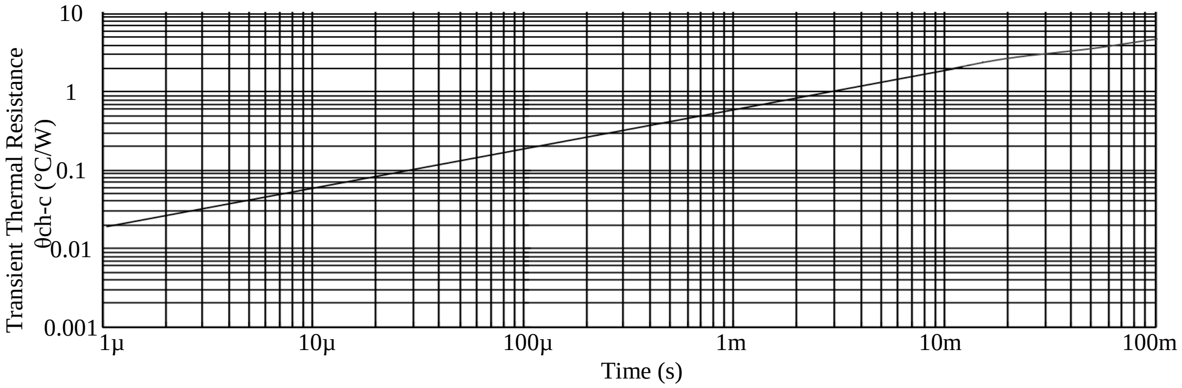
• **STR3A152 / 52D / 62HD**



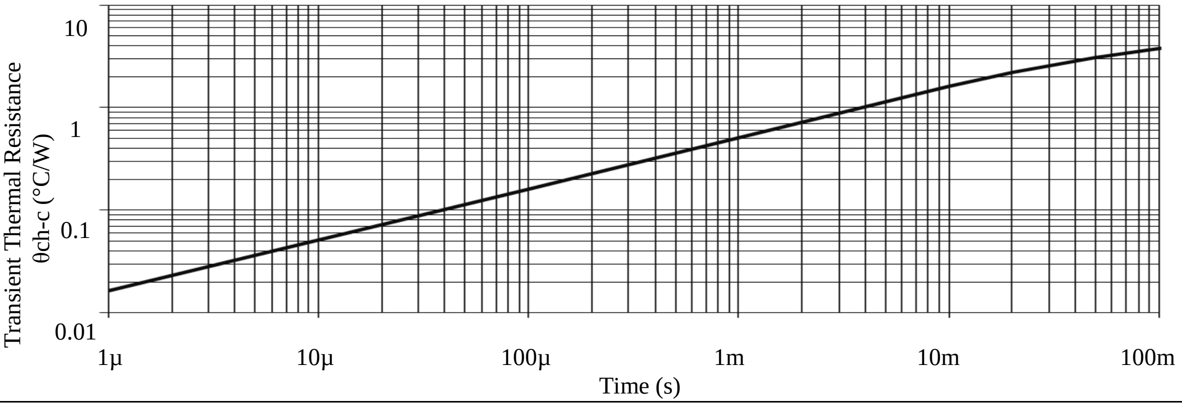
• **STR3A153 / 53D / 63HD**



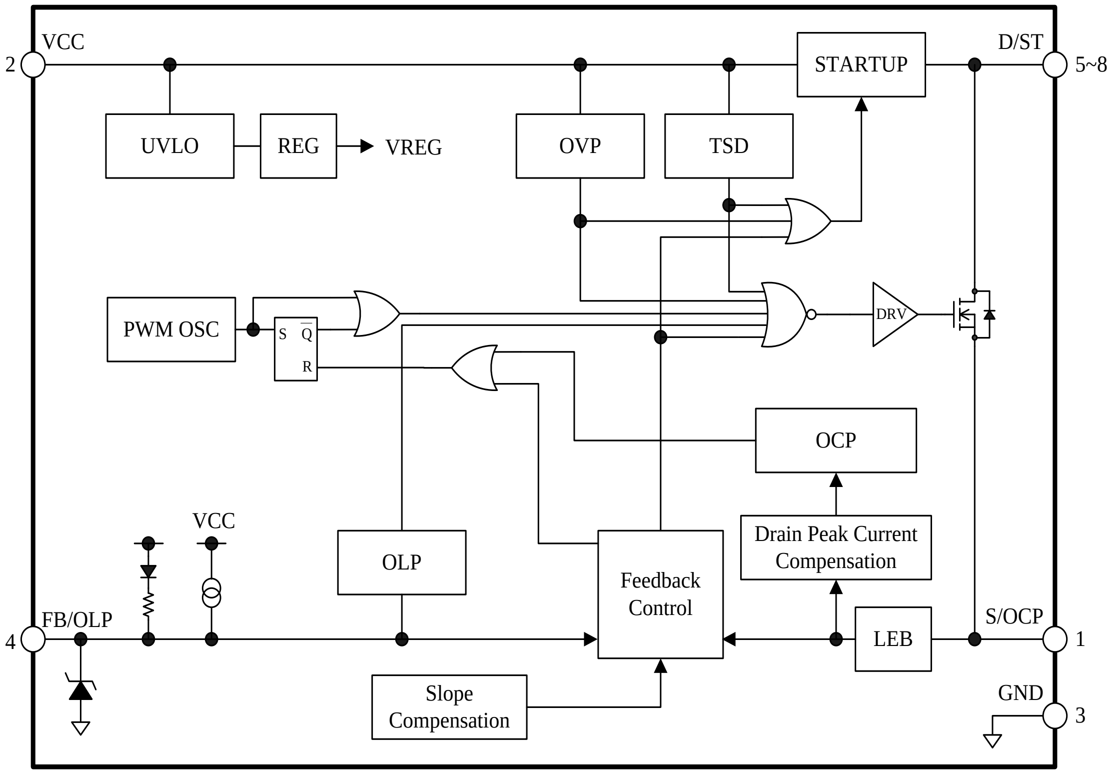
• **STR3A154 / 54D**



• **STR3A155 / 55D**

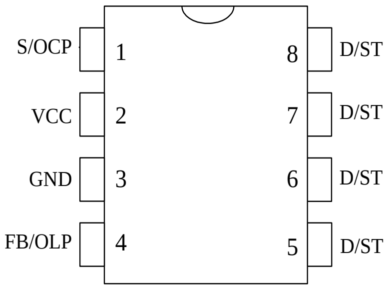


4. Functional Block Diagram



BD_STR3A100_R1

5. Pin Configuration Definitions



Pin	Name	Descriptions
1	S/OCP	MOSFET source and overcurrent protection (OCP) signal input
2	VCC	Power supply voltage input for control part and overvoltage protection (OVP) signal input
3	GND	Ground
4	FB /OLP	Constant voltage control signal input and over load protection (OLP) signal input
5	D/ST	MOSFET drain and startup current input
6		
7		
8		

6. Typical Application Circuit

- The PCB traces D/ST pins should be as wide as possible, in order to enhance thermal dissipation.
- In applications having a power supply specified such that D/ST pin has large transient surge voltages, a clamp snubber circuit of a capacitor-resistor-diode (CRD) combination should be added on the primary winding P, or a damper snubber circuit of a capacitor (C) or a resistor-capacitor (RC) combination should be added between the D/ST pin and the S/OCP pin.

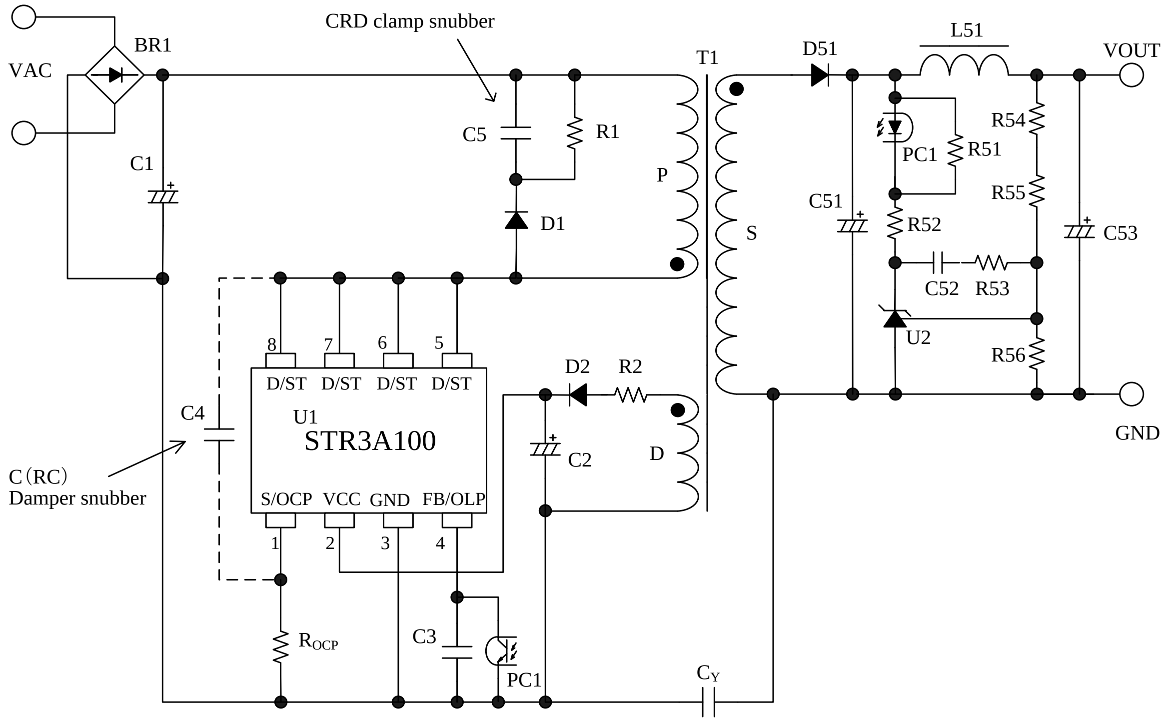
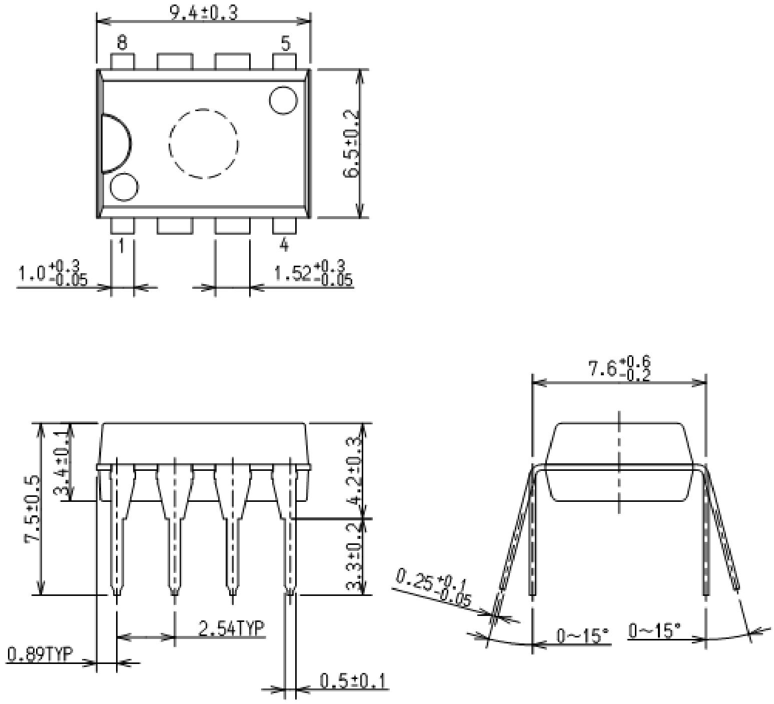


Figure 6-1 Typical application circuit

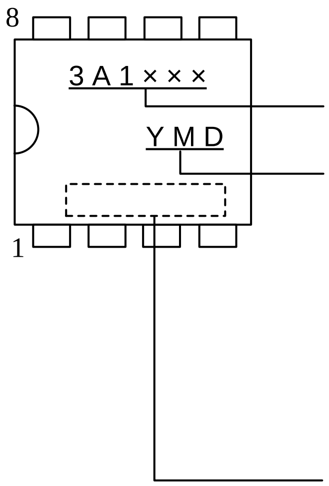
7. Package Outline

- DIP8



NOTES:
1) Dimension is in millimeters
2) Pb-free. Device composition compliant with the RoHS directive

8. Marking Diagram



Part Number (3A15× / 3A15×D / 3A16×H)

Lot Number
- Y = Last Digit of Year (0-9)
- M = Month (1-9,O,N or D)
- D =Period of days (1 to 3)
  - 1 : 1st to 10th
  - 2 : 11th to 20th
  - 3 : 21st to 31st

Sanken Control Number

9. Operational Description

- All of the parameter values used in these descriptions are typical values, unless they are specified as minimum or maximum.
- With regard to current direction, "+" indicates sink current (toward the IC) and "–" indicates source current (from the IC).

9.1 Startup Operation

Figure 9-1 shows the circuit around VCC pin.

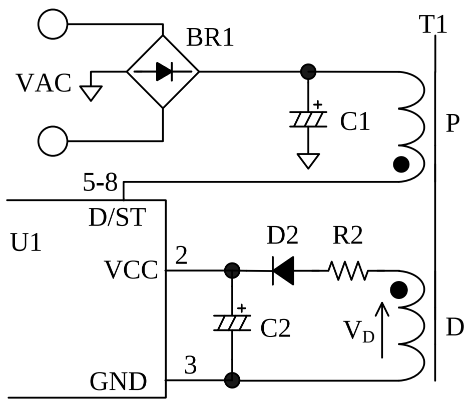


Figure 9-1 VCC pin peripheral circuit

The IC incorporates the startup circuit. The circuit is connected to D/ST pin. When D/ST pin voltage reaches to Startup Circuit Operation Voltage $V_{ST(ON)}$ = 40 V, the startup circuit starts operation.

During the startup process, the constant current, $I_{STARTUP}$ = − 2.5 mA, charges C2 at VCC pin. When VCC pin voltage increases to $V_{CC(ON)}$ = 15.3 V, the control circuit starts switching operation.

During the IC operation, the voltage rectified the auxiliary winding voltage, V_D, of Figure 9-1 becomes a power source to the VCC pin. After switching operation begins, the startup circuit turns off automatically so that its current consumption becomes zero.

The approximate value of auxiliary winding voltage is about 18V, taking account of the winding turns of D winding so that VCC pin voltage becomes Equation (1) within the specification of input and output voltage variation of power supply.

$$V_{CC(BIAS)}(\max.) < V_{CC} < V_{CC(OVP)}(\min.)$$

$$\Rightarrow 10.5\ (V) < V_{CC} < 27.5\ (V) \qquad (1)$$

The startup time of IC is determined by C2 capacitor value. The approximate startup time t_{START} is calculated as follows:

$$t_{START} = C2 \times \frac{V_{CC(ON)} - V_{CC(INT)}}{|I_{STRATUP}|} \qquad (2)$$

where,
t_{START} : Startup time of IC (s)
$V_{CC(INT)}$: Initial voltage on VCC pin (V)

9.2 Undervoltage Lockout (UVLO)

Figure 9-2 shows the relationship of VCC pin voltage and circuit current I_{CC}. When VCC pin voltage decreases to $V_{CC(OFF)}$ = 8.1 V, the control circuit stops operation by UVLO (Undervoltage Lockout) circuit, and reverts to the state before startup.

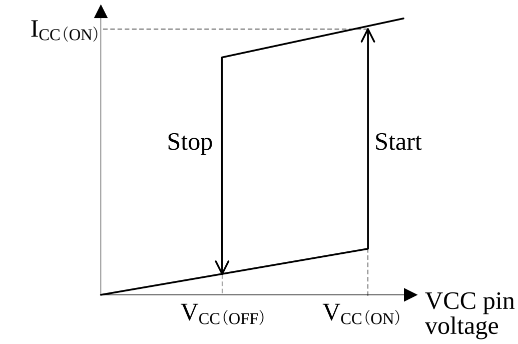


Figure 9-2 Relationship between VCC pin voltage and I_{CC}

9.3 Bias Assist Function

Figure 9-3 shows VCC pin voltage behavior during the startup period.

After VCC pin voltage increases to $V_{CC(ON)}$ = 15.3 V at startup, the IC starts the operation. Then circuit current increases and VCC pin voltage decreases. At the same time, the auxiliary winding voltage V_D increases in proportion to output voltage. These are all balanced to produce VCC pin voltage.

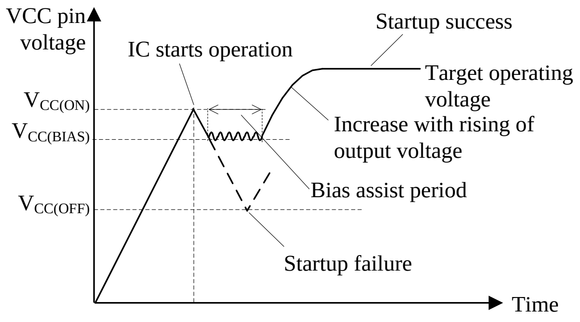


Figure 9-3 VCC pin voltage during startup period

The surge voltage is induced at output winding at turning off a power MOSFET. When the output load is light at startup, the surge voltage causes the unexpected feedback control. This results the lowering of the output power and VCC pin voltage. When the VCC pin voltage decreases to $V_{CC(OFF)}$ = 8.1 V, the IC stops switching operation and a startup failure occurs. In order to prevent this, the Bias Assist function is activated when the VCC pin voltage decreases to the startup current threshold biasing voltage, $V_{CC(BIAS)}$ = 9.5 V. While the Bias Assist function is activated, any decrease of the VCC pin voltage is counteracted by providing the startup current, $I_{STARTUP}$, from the startup circuit. Thus, the VCC pin voltage is kept almost constant.

By the Bias Assist function, the value of C2 is allowed to be small and the startup time becomes shorter. Also, because the increase of VCC pin voltage becomes faster when the output runs with excess voltage, the response time of the OVP function becomes shorter.

It is necessary to check and adjust the startup process based on actual operation in the application, so that poor starting conditions may be avoided.

9.4 Soft Start Function

Figure 9-4 shows the behavior of VCC pin voltage and drain current during the startup period.

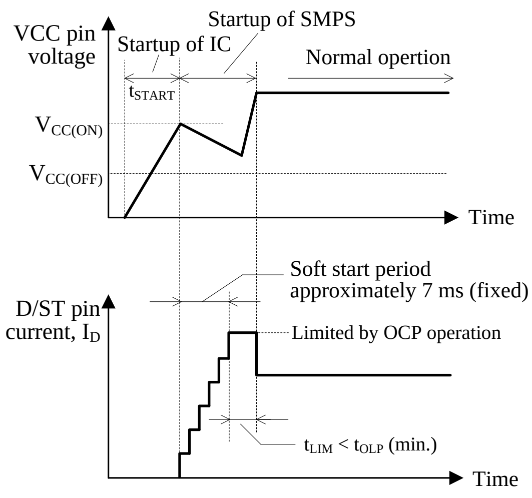


Figure 9-4 V_{CC} and I_D behavior during startup

The IC activates the soft start circuitry during the startup period. Soft start time is fixed to around 7 ms. during the soft start period, over current threshold is increased step-wisely (5 steps). This function reduces the voltage and the current stress of MOSFET and secondary side rectifier diode.

Since the Leading Edge Blanking Function (refer to Section 9.6) is deactivated during the soft start period, there is the case that ON time is less than the leading edge blanking time, t_{BW} = 350 ns.

After the soft start period, D/ST pin current, I_D, is limited by the overcurrent protection (OCP), until the output voltage increases to the target operating voltage. This period is given as t_{LIM}.

In case t_{LIM} is longer than the OLP Delay Time, t_{OLP}, the output power is limited by the OLP protection operation (OLP).

Thus, it is necessary to adjust the value of output capacitor and the turn ratio of auxiliary winding D so that the t_{LIM} is less than t_{OLP} = 54 ms (min.).

9.5 Constant Output Voltage Control

The IC achieves the constant voltage control of the power supply output by using the current-mode control method, which enhances the response speed and provides the stable operation.

The FB/OLP pin voltage is internally added the slope compensation at the feedback control (refer to Section 4.Functional Block Diagram), and the target voltage, V_{SC}, is generated. The IC compares the voltage, V_{ROCP}, of a current detection resistor with the target voltage, V_{SC}, by the internal FB comparator, and controls the peak value of V_{ROCP} so that it gets close to V_{SC}, as shown in Figure 9-5 and Figure 9-6.

- Light load conditions
  When load conditions become lighter, the output voltage, V_{OUT}, increases. Thus, the feedback current from the error amplifier on the secondary-side also increases. The feedback current is sunk at the FB/OLP pin, transferred through a photo-coupler, PC1, and the FB/OLP pin voltage decreases. Thus, V_{SC} decreases, and the peak value of V_{ROCP} is controlled to be low, and the peak drain current of I_D decreases.
  This control prevents the output voltage from increasing.

- Heavy load conditions
  When load conditions become greater, the IC performs the inverse operation to that described above. Thus, V_{SC} increases and the peak drain current of I_D increases.
  This control prevents the output voltage from decreasing.

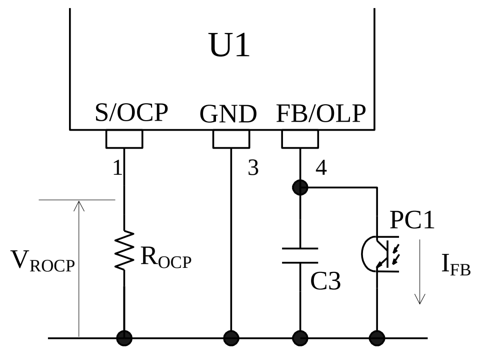


Figure 9-5 FB/OLP pin peripheral circuit

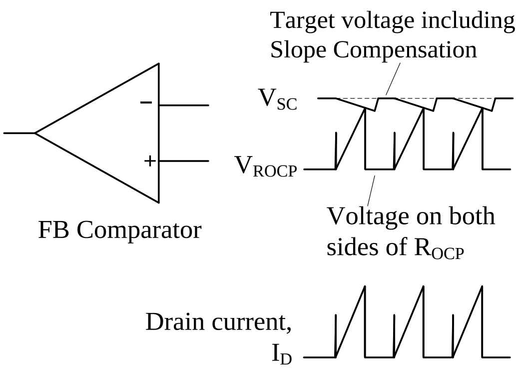


Figure 9-6 Drain current, I_D, and FB comparator operation in steady operation

In the current mode control method, when the drain current waveform becomes trapezoidal in continuous operating mode, even if the peak current level set by the target voltage is constant, the on-time fluctuates based on the initial value of the drain current.

This results in the on-time fluctuating in multiples of the fundamental operating frequency as shown in Figure 9-7. This is called the subharmonics phenomenon.

In order to avoid this, the IC incorporates the Slope Compensation function. Because the target voltage is added a down-slope compensation signal, which reduces the peak drain current as the on-duty gets wider relative to the FB/OLP pin signal to compensate V_{SC}, the subharmonics phenomenon is suppressed.

Even if subharmonic oscillations occur when the IC has some excess supply being out of feedback control, such as during startup and load shorted, this does not affect performance of normal operation.

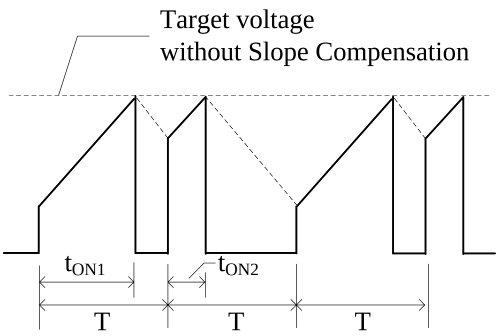


Figure 9-7 Drain current, I_D, waveform in subharmonic oscillation

9.6 Leading Edge Blanking Function

The IC uses the peak-current-mode control method for the constant voltage control of output.

In peak-current-mode control method, there is a case that the power MOSFET turns off due to unexpected response of FB comparator or overcurrent protection circuit (OCP) to the steep surge current in turning on a power MOSFET.

In order to prevent this response to the surge voltage in turning-on the power MOSFET, the Leading Edge Blanking, t_{BW} = 350 ns (STR3A16×HD for t_{BW} = 280 ns) is built-in. During t_{BW}, the OCP threshold voltage becomes about 1.7 V which is higher than the normal OCP threshold voltage (refer to Section 9.9).

9.7 Random Switching Function

The IC modulates its switching frequency randomly by superposing the modulating frequency on $f_{OSC(AVG)}$ in normal operation. This function reduces the conduction noise compared to others without this function, and simplifies noise filtering of the input lines of power supply.

9.8 Automatic Standby Mode Function

Automatic standby mode is activated automatically when the drain current, I_D, reduces under light load conditions, at which I_D is less than 20 % to 25 % (STR3A154, 54D, 55 and 55D are 15 to 20 %) of the maximum drain current (it is in the OCP state).

The operation mode becomes burst oscillation, as shown in Figure 9-8. Burst oscillation mode reduces switching losses and improves power supply efficiency because of periodic non-switching intervals.

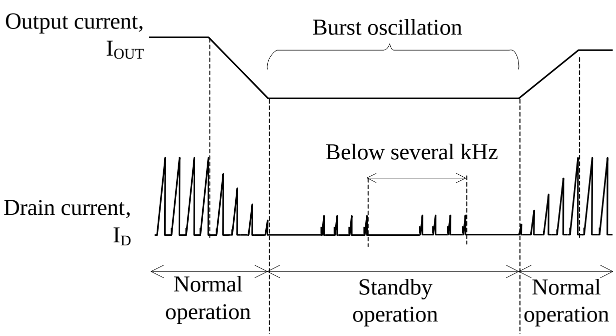


Figure 9-8 Auto Standby mode timing

Generally, to improve efficiency under light load conditions, the frequency of the burst oscillation mode becomes just a few kilohertz. Because the IC suppresses the peak drain current well during burst oscillation mode, audible noises can be reduced.

If the VCC pin voltage decreases to $V_{CC(BIAS)}$ = 9.5 V during the transition to the burst oscillation mode, the Bias Assist function is activated and stabilizes the Standby mode operation, because $I_{STARTUP}$ is provided to the VCC pin so that the VCC pin voltage does not decrease to $V_{CC(OFF)}$.

However, if the Bias Assist function is always activated during steady-state operation including standby mode, the power loss increases. Therefore, the VCC pin voltage should be more than $V_{CC(BIAS)}$, for example, by adjusting the turns ratio of the auxiliary winding and secondary winding and/or reducing the value of R2 in Figure 10-2 (refer to Section 10.1).

9.9 Overcurrent Protection Function (OCP)

Overcurrent Protection Function (OCP) detects each drain peak current level of a power MOSFET on pulse-by-pulse basis, and limits the output power when the current level reaches to OCP threshold voltage.

During Leading Edge Blanking Time, the OCP threshold voltage becomes about 1.7 V which is higher than the normal OCP threshold voltage as shown in Figure 9-9. Changing to this threshold voltage prevents the IC from responding to the surge voltage in turning-on the power MOSFET. This function operates as protection at the condition such as output windings shorted or unusual withstand voltage of secondary-side rectifier diodes.

When power MOSFET turns on, the surge voltage width of S/OCP pin should be less than t_{BW}, as shown in Figure 9-9. In order to prevent surge voltage, pay extra attention to R_{OCP} trace layout (refer to Section 0).

In addition, if a C (RC) damper snubber of Figure 9-10 is used, reduce the capacitor value of damper snubber.

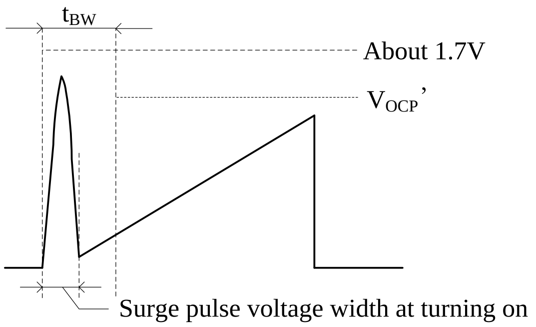


Figure 9-9 S/OCP pin voltage

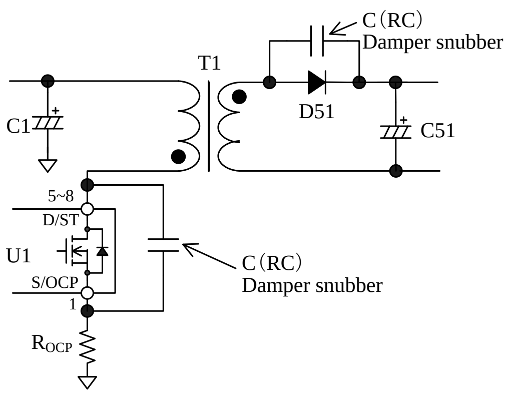


Figure 9-10 Damper snubber

< Input Compensation Function >

ICs with PWM control usually have some propagation delay time. The steeper the slope of the actual drain current at a high AC input voltage is, the larger the detection voltage of actual drain peak current is, compared to V_{OCP}. Thus, the peak current has some variation depending on the AC input voltage in OCP state.

In order to reduce the variation of peak current in OCP state, the IC incorporates a built-in Input Compensation function.

The Input Compensation Function is the function of correction of OCP threshold voltage depending with AC input voltage, as shown in Figure 9-11.

When AC input voltage is low (ON Duty is broad), the OCP threshold voltage is controlled to become high. The difference of peak drain current become small compared with the case where the AC input voltage is high (ON Duty is narrow).

The compensation signal depends on ON Duty. The relation between the ON Duty and the OCP threshold voltage after compensation V_{OCP}' is expressed as Equation (3). When ON Duty is broader than 36 %, the V_{OCP}' becomes a constant value $V_{OCP(H)} = 0.88$ V

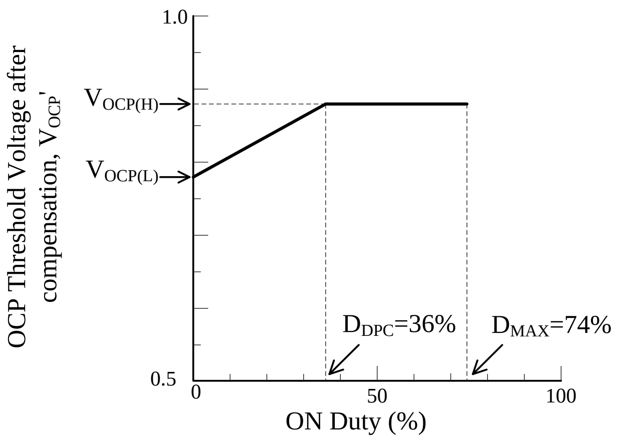


Figure 9-11 Relationship between ON Duty and Drain Current Limit after compensation

$$
\begin{aligned}
V_{OCP}' &= V_{OCP(L)} + DPC \times ONTime \\
&= V_{OCP(L)} + DPC \times \frac{ONDuty}{f_{OSC(AVG)}}
\end{aligned} \qquad (3)
$$

where,
$V_{OCP(L)}$: OCP Threshold Voltage at Zero ON Duty
DPC: OCP Compensation Coefficient
ONTime: On-time of power MOSFET
ONDuty: On duty of power MOSFET
$f_{OSC(AVG)}$: Average PWM Switching Frequency

9.10 Overload Protection Function (OLP)

Figure 9-12 shows the FB/OLP pin peripheral circuit, and Figure 9-13shows each waveform for OLP operation.

When the peak drain current of I_D is limited by OCP operation, the output voltage, V_{OUT}, decreases and the feedback current from the secondary photo-coupler becomes zero. Thus, the feedback current, I_{FB}, charges C3 connected to the FB/OLP pin and the FB/OLP pin voltage increases. When the FB/OLP pin voltage increases to $V_{FB(OLP)}$ = 8.1 V or more for the OLP delay time, t_{OLP} = 70 ms or more, the OLP function is activated, the IC stops switching operation.

During OLP operation, Bias Assist Function is disabled. Thus, VCC pin voltage decreases to $V_{CC(OFF)}$, the control circuit stops operation. After that, the IC reverts to the initial state by UVLO circuit, and the IC starts operation when VCC pin voltage increases to $V_{CC(ON)}$ by startup current. Thus the intermittent operation by UVLO is repeated in OLP state.

This intermittent operation reduces the stress of parts such as power MOSFET and secondary side rectifier diode. In addition, this operation reduces power consumption because the switching period in this intermittent operation is short compared with oscillation stop period. When the abnormal condition is removed, the IC returns to normal operation automatically.

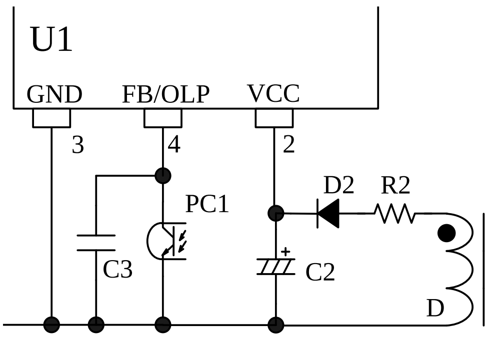


Figure 9-12 FB/OLP pin peripheral circuit

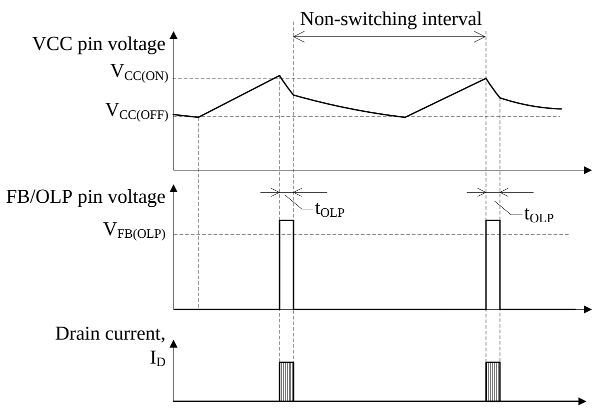


Figure 9-13 OLP operational waveforms

9.11 Overvoltage Protection (OVP)

When a voltage between VCC pin and GND terminal increases to $V_{CC(OVP)}$ = 29.5 V or more, OVP function is activated. The IC has two operation types of OVP function. One is latched shutdown. The other is auto restart.

In case the VCC pin voltage is provided by using auxiliary winding of transformer, the overvoltage conditions such as output voltage detection circuit open can be detected because the VCC pin voltage is proportional to output voltage. The approximate value of output voltage $V_{OUT(OVP)}$ in OVP condition is calculated by using Equation (4).

$$V_{OUT(OVP)} = \frac{V_{OUT(NORMAL)}}{V_{CC(NORMAL)}} \times 29.5\ (V) \qquad (4)$$

where,
$V_{OUT(NORMAL)}$: Output voltage in normal operation
$V_{CC(NORMAL)}$: VCC pin voltage in normal operation

- **Latched Shutdown type: STR3A1××**
  When the OVP function is activated, the IC stops switching operation at the latched state. In order to keep the latched state, when VCC pin voltage decreases to $V_{CC(BIAS)}$, the bias assist function is activated and VCC pin voltage is kept to over the $V_{CC(OFF)}$.
  Releasing the latched state is done by turning off the input voltage and by dropping the VCC pin voltage below $V_{CC(OFF)}$.

- **Auto Restart Type: STR3A1××D**
  When the OVP function is activated, the IC stops switching operation. During OVP operation, the Bias Assist function is disabled, the intermittent operation by UVLO is repeated (refer to Section 9.10). When the fault condition is removed, the IC returns to normal operation automatically (refer to Figure 9-14).

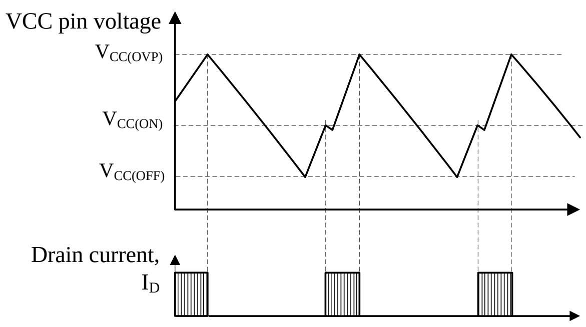


Figure 9-14 OVP operational waveforms

9.12 Thermal Shutdown Function (TSD)

When the temperature of control circuit increases to $T_{j(TSD)}$ = 135 °C (min.) or more, Thermal Shutdown function (TSD) is activated. The IC has two operation types of TSD function. One is latched shutdown, the other is auto restart.

- **Latched Shutdown type: STR3A1××**
  When the TSD function is activated, the IC stops switching operation at the latched state. In order to keep the latched state, when VCC pin voltage decreases to $V_{CC(BIAS)}$, the bias assist function is activated and VCC pin voltage is kept to over the $V_{CC(OFF)}$.
  Releasing the latched state is done by turning off the input voltage and by dropping the VCC pin voltage below $V_{CC(OFF)}$.

- **Auto Restart Type: STR3A1××D**
  When the TSD function is activated, the IC stops switching operation. During TSD operation, the Bias Assist function is disabled, the intermittent operation by UVLO is repeated (refer to Section 9.10). When the fault condition is removed and the temperature decreases to less than $T_{j(TSD)}$, the IC returns to normal operation automatically.

10. Design Notes

10.1 External Components

Take care to use properly rated, including derating as necessary and proper type of components.

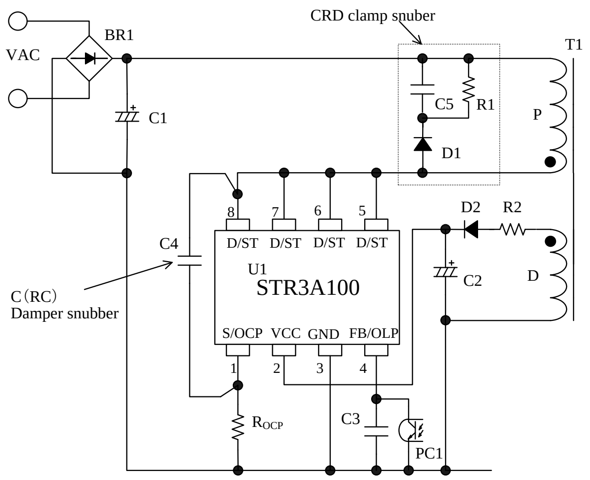


Figure 10-1 The IC peripheral circuit

- **Output Electrolytic Capacitor**
  Apply proper derating to ripple current, voltage, and temperature rise. Use of high ripple current and low impedance types, designed for switch mode power supplies, is recommended.

- **S/OCP Pin Peripheral Circuit**
  In Figure 10-1, R_{OCP} is the resistor for the current detection. A high frequency switching current flows to R_{OCP}, and may cause poor operation if a high inductance resistor is used. Choose a low inductance and high surge-tolerant type.

- **VCC Pin Peripheral Circuit**
  The value of C2 in Figure 10-1 is generally recommended to be 10 µF to 47 µF (refer to Section 9.1 Startup Operation, because the startup time is determined by the value of C2)
  In actual power supply circuits, there are cases in which the VCC pin voltage fluctuates in proportion to the output current, I_{OUT} (see Figure 10-2), and the Overvoltage Protection function (OVP) on the VCC pin may be activated. This happens because C2 is charged to a peak voltage on the auxiliary winding D, which is caused by the transient surge voltage coupled from the primary winding when the power MOSFET turns off.
  For alleviating C2 peak charging, it is effective to add some value R2, of several tenths of ohms to several ohms, in series with D2 (see Figure 10-1). The optimal value of R2 should be determined using a transformer matching what will be used in the actual application, because the variation of the auxiliary winding voltage is affected by the transformer structural design.

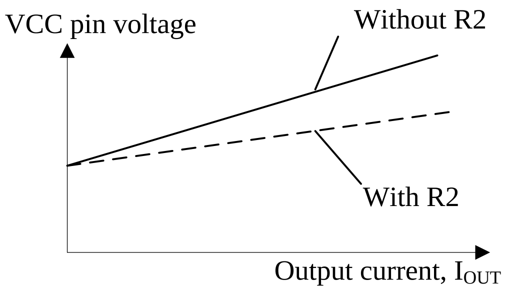


Figure 10-2 Variation of VCC pin voltage and power

- **FB/OLP Pin Peripheral Circuit**
  Figure 10-1 performs high frequency noise rejection and phase compensation, and should be connected close to these pins. The value of C3 is recommended to be about 2200 pF to 0.01 µF, and should be selected based on actual operation in the application.

- **Snubber Circuit**
  In case the serge voltage of V_{DS} is large, the circuit should be added as follows (see Figure 10-1);
  - A clamp snubber circuit of a capacitor-resistor-diode (CRD) combination should be added on the primary winding P.
  - A damper snubber circuit of a capacitor (C) or a resistor-capacitor (RC) combination should be added between the D/ST pin and the S/OCP pin.
    In case the damper snubber circuit is added, this components should be connected near D/ST pin and S/OCP pin.

- **Phase Compensation**
  Figure 10-3 shows the secondary side detection circuit with the standard shunt regulator IC (U51).
  C52 and R53 are for phase compensation. The value of C52 and R53 are recommended to be around 0.047μF to 0.47μF and 4.7 kΩ to 470 kΩ, respectively. They should be selected based on actual operation in the application.

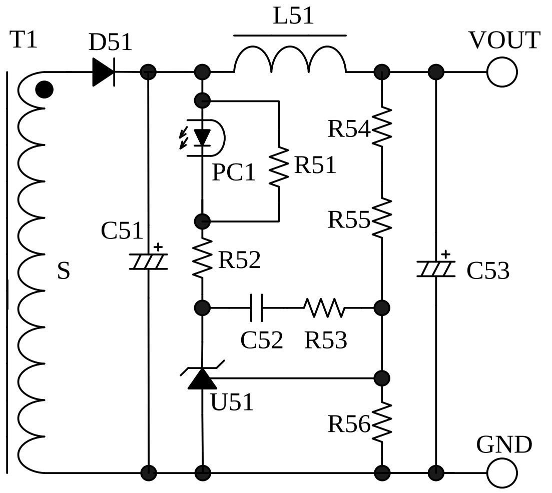


Figure 10-3 Peripheral circuit of secondary side shunt regulator (U51)

- **Transformer**
  Apply proper design margin to core temperature rise by core loss and copper loss.
  Because the switching currents contain high frequency currents, the skin effect may become a consideration.
  Choose a suitable wire gauge in consideration of the RMS current and a current density of about 3 to 4A/mm^2.
  If measures to further reduce temperature are still necessary, the following should be considered to increase the total surface area of the wiring:

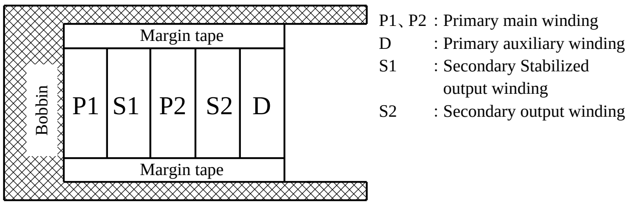
  ▫ Increase the number of wires in parallel.
  ▫ Use litz wires.
  ▫ Thicken the wire gauge.

Fluctuation of the VCC pin voltage by I_{OUT} worsens in the following cases, requiring a transformer designer to pay close attention to the placement of the auxiliary winding D:

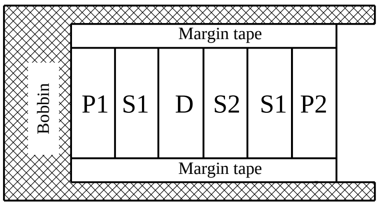
▫ Poor coupling between the primary and secondary windings (this causes high surge voltage and is seen in a design with low output voltage and high output current)
▫ Poor coupling between the auxiliary winding D and the secondary stabilized output winding where the output line voltage is controlled constant by the output voltage feedback (this is susceptible to surge voltage)

In order to reduce the influence of surge voltage on the VCC pin, Figure 10-4 shows winding structural examples that are considered the placement of the auxiliary winding D.

▫ Winding structural example (a): Separating the auxiliary winding D from the primary windings P1 and P2.
where: P1 and P2 are windings divided the primary winding into two.
▫ Winding structural example (b): Placing the auxiliary winding D within the secondary-side stabilized output winding, S1, in order to improve the coupling of those windings.
where: S1 is a stabilized output winding of secondary-side windings, controlled to constant voltage.



Winding structural example (a)



Winding structural example (b)

Figure 10-4 Winding structural examples

10.2 PCB Trace Layout and Component Placement

Since the PCB circuit trace design and the component layout significantly affects operation, EMI noise, and power dissipation, the high frequency PCB trace should be low impedance with small loop and wide trace.

In addition, the ground traces affect radiated EMI noise, and wide, short traces should be taken into account.

Figure 10-5 shows the circuit design example.

(1) Main Circuit Trace Layout:

This is the main trace containing switching currents, and thus it should be as wide trace and small loop as possible.

If C1 and the IC are distant from each other, placing a capacitor such as film capacitor (about 0.1 μF and with proper voltage rating) close to the transformer or the IC is recommended to reduce impedance of the high frequency current loop.

(2) Control Ground Trace Layout

Since the operation of IC may be affected from the large current of the main trace that flows in control ground trace, the control ground trace should be separated from main trace and connected at a single point grounding of point A in Figure 10-5 as close to the R_{OCP} pin as possible.

(3) VCC Trace Layout:

This is the trace for supplying power to the IC, and thus it should be as small loop as possible. If C2 and the IC are distant from each other, placing a capacitor such as film capacitor C_f (about 0.1 μF to 1.0 μF) close to the VCC pin and the GND pin is recommended.

(4) R_{OCP} Trace Layout

R_{OCP} should be placed as close as possible to the S/OCP pin. The connection between the power ground of the main trace and the IC ground should be at a single point ground (point A in Figure 10-5) which is close to the base of R_{OCP}.

(5) FB/OLP Trace Layout

The components connected to FB/OLP pin should be as close to FB/OLP pin as possible. The trace between the components and FB/OLP pin should be as short as possible.

(6) Secondary Rectifier Smoothing Circuit Trace Layout:

This is the trace of the rectifier smoothing loop, carrying the switching current, and thus it should be as wide trace and small loop as possible. If this trace is thin and long, inductance resulting from the loop may increase surge voltage at turning off the power MOSFET. Proper rectifier smoothing trace layout helps to increase margin against the power MOSFET breakdown voltage, and reduces stress on the clamp snubber circuit and losses in it.

(7) Thermal Considerations

Because the power MOSFET has a positive thermal coefficient of $R_{DS(ON)}$, consider it in thermal design.

Since the copper area under the IC and the D/ST pin trace act as a heatsink, its traces should be as wide as possible.

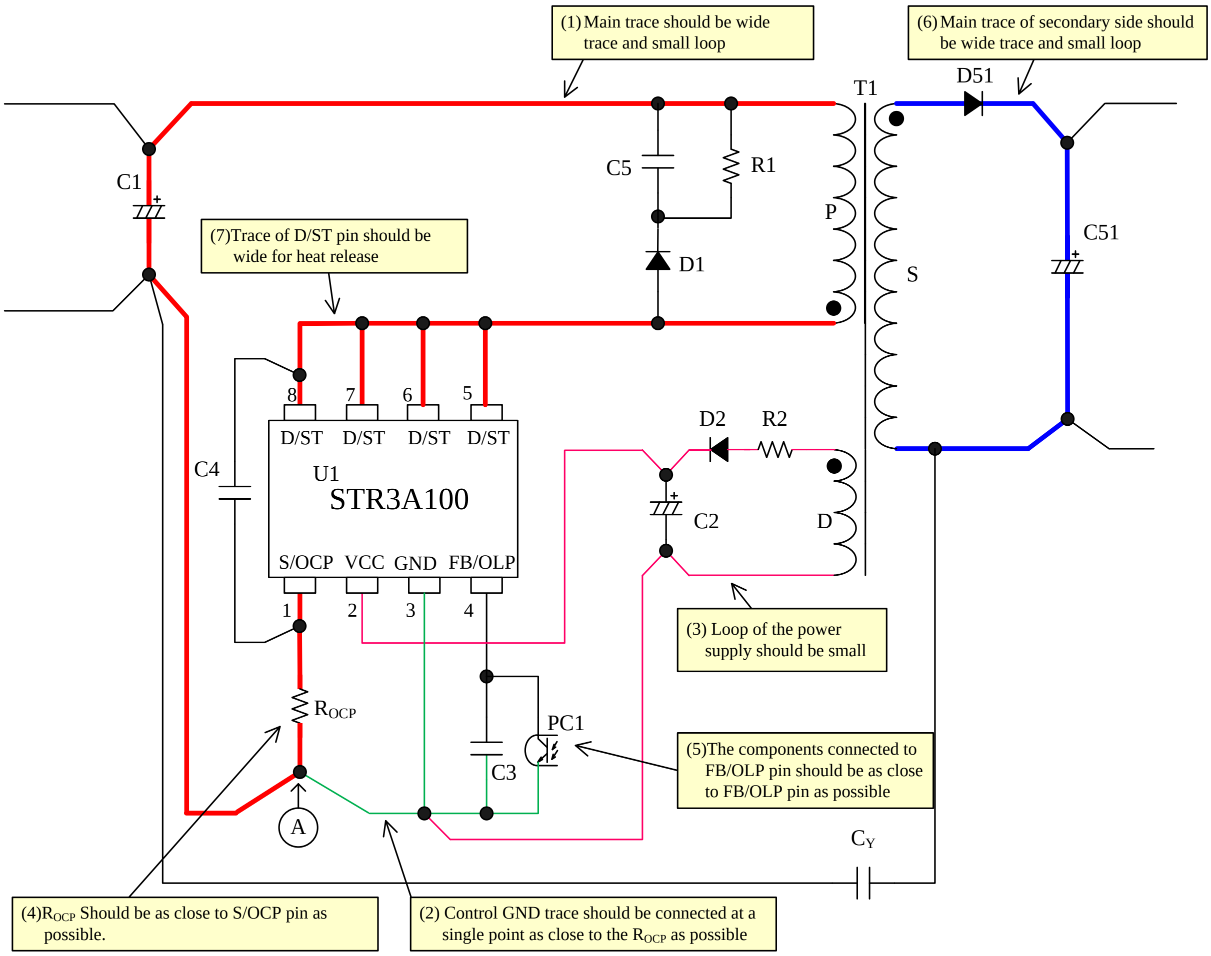


Figure 10-5 Peripheral circuit example around the IC

11. Pattern Layout Example

The following show the PCB pattern layout example and the schematic of circuit using STR3A100 series. Only the parts in the schematic are used. Other parts in PCB are leaved open.

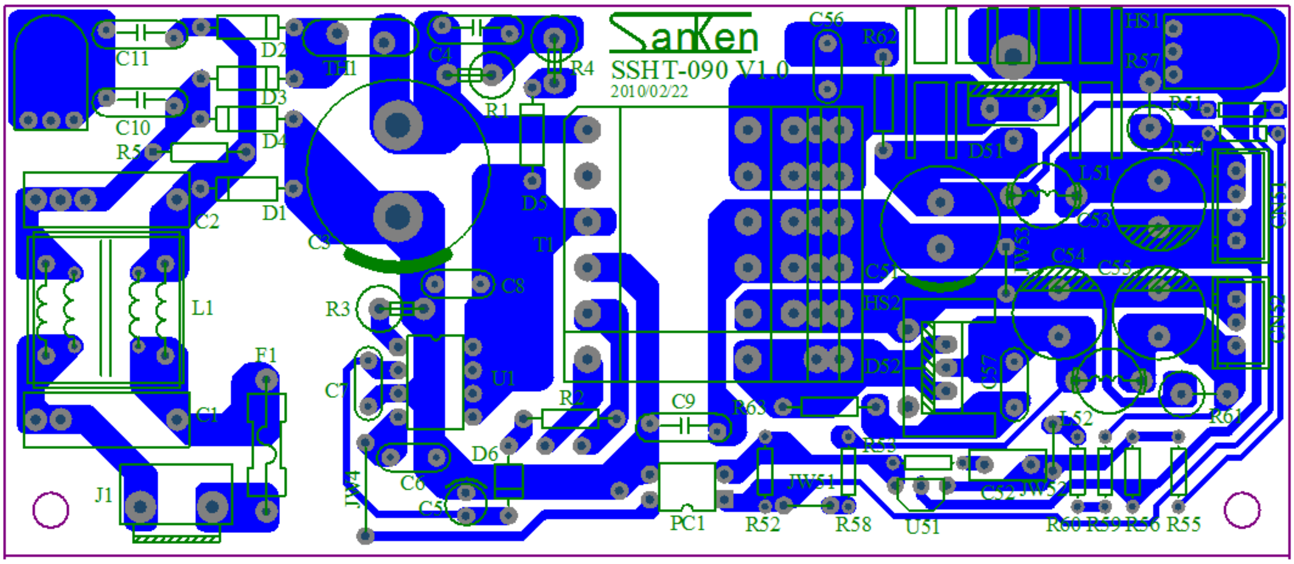


Figure 11-1 PCB circuit trace layout example

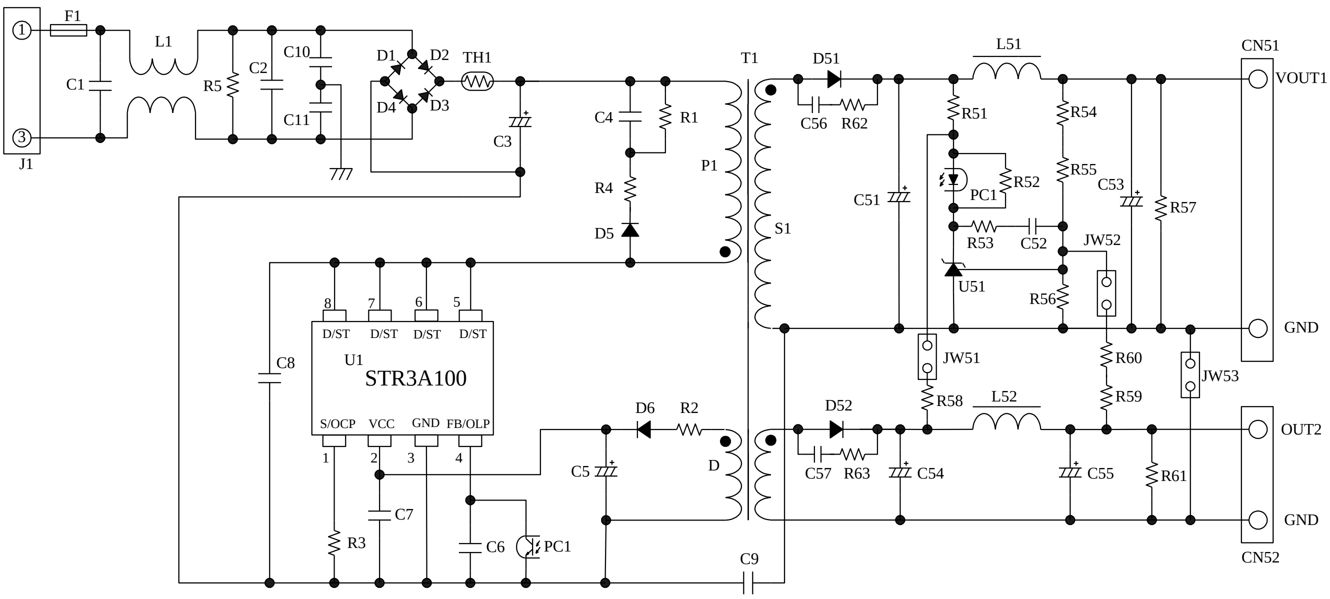


Figure 11-2 Circuit schematic for PCB circuit trace layout

The above circuit symbols correspond to these of Figure 11-1.

12. Reference Design of Power Supply

As an example, the following show the power supply specification, the circuit schematic, the bill of materials, and the transformer specification.

- Power supply specification

IC	STR3A153
Input voltage	AC85V to AC265V
Maximum output power	34.8 W (40.4 W peak)
Output 1	8 V / 0.5 A
Output 2	14 V / 2.2 A (2.6 A peak)

- Circuit schematic
  Refer to Figure 11-2

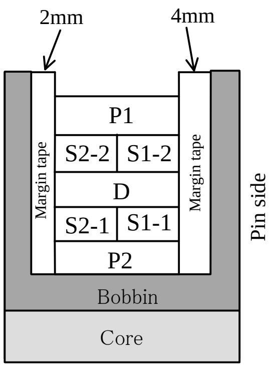
- Bill of materials

Symbol	Part type	Ratings(1)	Recommended Sanken Parts	Symbol	Part type	Ratings(1)	Recommended Sanken Parts
F1	Fuse	AC 250 V, 3 A		L51	Inductor	Short	
L1 (2)	CM inductor	3.3 mH		L52	Inductor	Short	
TH1 (2)	NTC thermistor	Short		D51	Schottky	90 V, 1.5 A	EK19
D1	General	600 V, 1 A	EM01A	D52	Schottky	150V, 10A	FMEN-210B
D2	General	600 V, 1 A	EM01A	C51 (2)	Electrolytic	470 μF, 25 V	
D3	General	600 V, 1 A	EM01A	C52 (2)	Ceramic	0.1 μF, 50 V	
D4	General	600 V, 1 A	EM01A	C53 (2)	Electrolytic	Open	
D5	Fast recovery	1000 V, 0.5 A	EG01C	C54	Electrolytic		
D6	Fast recovery	200 V, 1 A	AL01Z	C55 (2)	Electrolytic	Open	
C1 (2)	Film, X2	0.047 μF, 275 V		C56 (2)	Ceramic	Open	
C2 (2)	Electrolytic	Open		C57 (2)	Ceramic	Open	
C3	Electrolytic	10 μF, 400 V		R51	General	Open	
C4	Ceramic	1000 pF, 2 kV		R52	General	1.5 kΩ	
C5	Electrolytic	22 μF, 50 V		R53 (2)	General	100 kΩ	
C6 (2)	Ceramic	0.01 μF		R54	General, 1%	Open	
C7 (2)	Ceramic	Open		R55	General, 1%	Open	
C8 (2)	Ceramic	15 pF / 2 kV		R56	General, 1%	10 kΩ	
C9	Ceramic, Y1	2200 pF, 250 V		R57	General	Open	
C10 (2)	Ceramic	Open		R58	General	2.2 kΩ	
C11 (2)	Ceramic	Open		R59 (2)	General	6.8 kΩ	
R1 (3)	Metal oxide	150 kΩ, 2 W		R60	General, 1%	39 kΩ	
R2 (2)	General	10 Ω		R61	General	Open	
R3 (2)	General	0.47 Ω, 1/2 W		R62 (2)	General	Open	
R4 (2)	General	Short		R63 (2)	General	Open	
R5 (3)	Metal oxide	Open		JW51		Short	
PC1	Photo-coupler	PC123 or equiv		JW52		Short	
U1	IC	—	STR3A153	JW53		Short	
T1	Transformer	See the specification		U51	Shunt regulator	V_{REF} = 2.5 V TL431 or equiv	

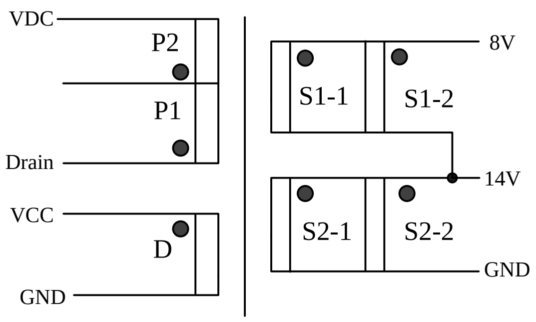
(1) Unless otherwise specified, the voltage rating of capacitor is 50 V or less and the power rating of resistor is 1/8 W or less.
(2) It is necessary to be adjusted based on actual operation in the application.
(3) Resistors applied high DC voltage and of high resistance are recommended to select resistors designed against electromigration or use combinations of resistors in series for that to reduce each applied voltage, according to the requirement of the application.

- Transformer specification
  - Primary inductance, L_P : 518 µH
  - Core size : EER-28
  - Al-value : 245 nH/N^2 (Center gap of about 0.56 mm)
  - Winding specification

Winding	Symbol	Number of turns (T)	Wire diameter (mm)	Construction
Primary winding	P1	18	φ 0.23 × 2	Single-layer, solenoid winding
Primary winding	P2	28	φ 0.30	Single-layer, solenoid winding
Auxiliary winding	D	12	φ 0.30 × 2	Solenoid winding
Output 1 winding	S1-1	6	φ 0.4 × 2	Solenoid winding
Output 1 winding	S1-2	6	φ 0.4 × 2	Solenoid winding
Output 2 winding	S2-1	4	φ 0.4 × 2	Solenoid winding
Output 2 winding	S2-2	4	φ 0.4 × 2	Solenoid winding



Cross-section view



●: Start at this pin

OPERATING PRECAUTIONS

In the case that you use Sanken products or design your products by using Sanken products, the reliability largely depends on the degree of derating to be made to the rated values. Derating may be interpreted as a case that an operation range is set by derating the load from each rated value or surge voltage or noise is considered for derating in order to assure or improve the reliability. In general, derating factors include electric stresses such as electric voltage, electric current, electric power etc., environmental stresses such as ambient temperature, humidity etc. and thermal stress caused due to self-heating of semiconductor products. For these stresses, instantaneous values, maximum values and minimum values must be taken into consideration. In addition, it should be noted that since power devices or IC's including power devices have large self-heating value, the degree of derating of junction temperature affects the reliability significantly.

Because reliability can be affected adversely by improper storage environments and handling methods, please observe the following cautions.

Cautions for Storage

- Ensure that storage conditions comply with the standard temperature (5 to 35°C) and the standard relative humidity (around 40 to 75%); avoid storage locations that experience extreme changes in temperature or humidity.
- Avoid locations where dust or harmful gases are present and avoid direct sunlight.
- Reinspect for rust on leads and solderability of the products that have been stored for a long time.

Cautions for Testing and Handling

When tests are carried out during inspection testing and other standard test periods, protect the products from power surges from the testing device, shorts between the product pins, and wrong connections. Ensure all test parameters are within the ratings specified by Sanken for the products.

Remarks About Using Silicone Grease with a Heatsink

- When silicone grease is used in mounting the products on a heatsink, it shall be applied evenly and thinly. If more silicone grease than required is applied, it may produce excess stress.
- Volatile-type silicone greases may crack after long periods of time, resulting in reduced heat radiation effect. Silicone greases with low consistency (hard grease) may cause cracks in the mold resin when screwing the products to a heatsink.
  Our recommended silicone greases for heat radiation purposes, which will not cause any adverse effect on the product life, are indicated below:

Type	Suppliers
G746	Shin-Etsu Chemical Co., Ltd.
YG6260	Momentive Performance Materials Inc.
SC102	Dow Corning Toray Co., Ltd.

Soldering

- When soldering the products, please be sure to minimize the working time, within the following limits:
  - 260 ± 5 °C   10 ± 1 s (Flow, 2 times)
  - 380 ± 10 °C   3.5 ± 0.5 s (Soldering iron, 1 time)
- Soldering should be at a distance of at least 1.5 mm from the body of the products.

Electrostatic Discharge

- When handling the products, the operator must be grounded. Grounded wrist straps worn should have at least 1MΩ of resistance from the operator to ground to prevent shock hazard, and it should be placed near the operator.
- Workbenches where the products are handled should be grounded and be provided with conductive table and floor mats.
- When using measuring equipment such as a curve tracer, the equipment should be grounded.
- When soldering the products, the head of soldering irons or the solder bath must be grounded in order to prevent leak voltages generated by them from being applied to the products.
- The products should always be stored and transported in Sanken shipping containers or conductive containers, or be wrapped in aluminum foil.

IMPORTANT NOTES

- The contents in this document are subject to changes, for improvement and other purposes, without notice. Make sure that this is the latest revision of the document before use.
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